

QS Family

QFN Style Solder-Down Computer-on-Modules

- Solder-down version
- 27mm square
- 2.3mm total height
- QFN type lead style
 - 1mm pitch
 - 100 pads
 - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- High speed design compliant
- 3.3V power supply



Key Features

- Processor RENESAS RZ/G2L
Dual 1.2GHz Arm® Cortex®-A55
200-MHz Arm® Cortex®-M33
- RAM 512MB/1GB DDR3L SDRAM
- ROM 4GB eMMC

- Grade Industrial
- Temperature -40°C to 85°C
- Display support

- Interfaces 24-bit RGB
MIPI® DSI (2-lanes)

- GPU/VPU 500-MHz Arm® Mali™-G31
H.264 Video Codec Processor

- Connectivity
 - Gb Ethernet, USB2.0, eMMC/SD
 - UART, I²C, SPI, PWM, SAI, CAN

**RZ/G2L
Dual
Cortex®-A55**

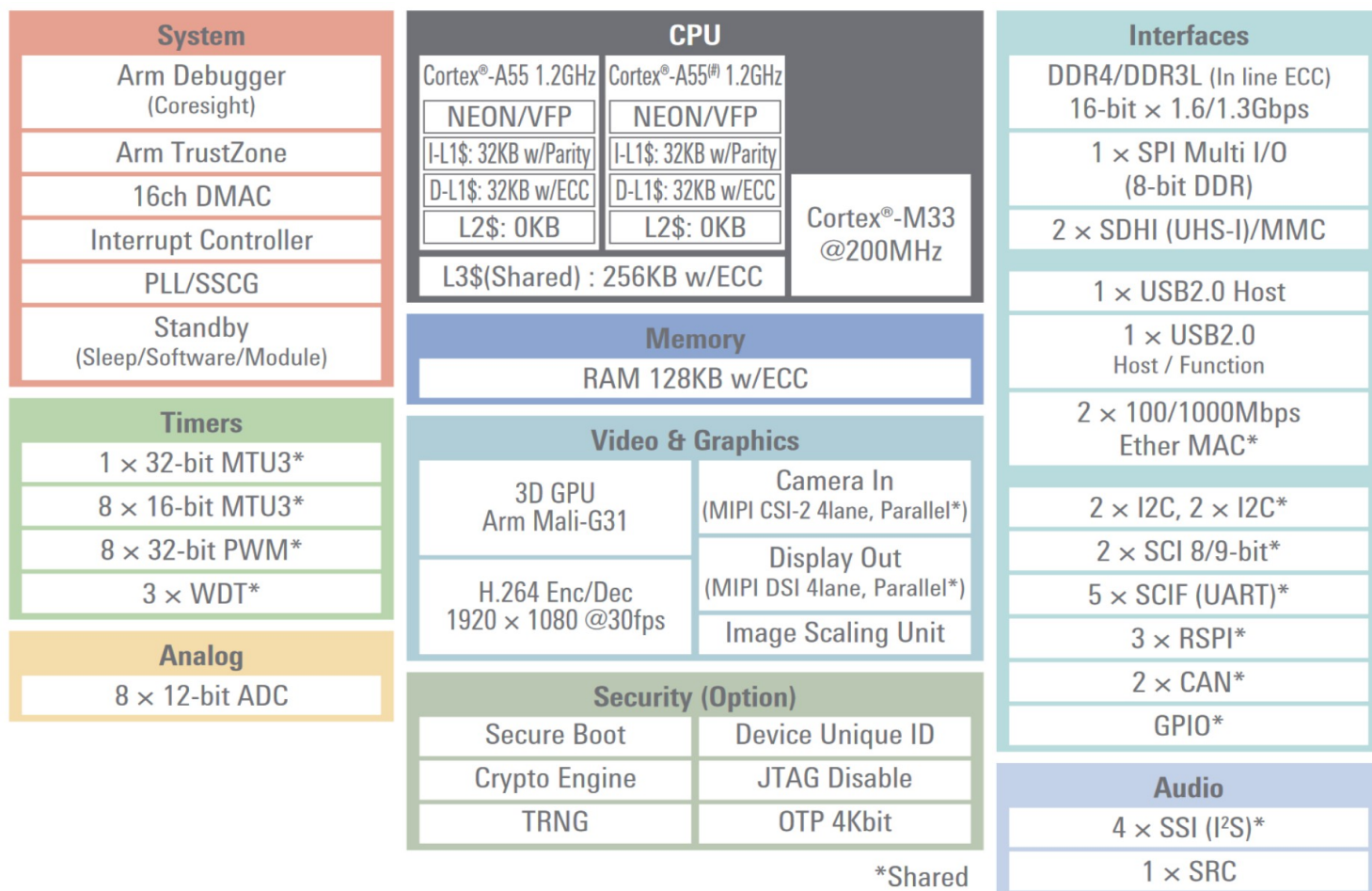
OS Support

- Linux



RENESAS

RZ/G2L Block Diagram



QSRZ – Main Feature Comparison and Ordering Information

| | QSRZ-G2L0 | QSRZ-G2L1 |
|---------------------|------------------------------|---------------------|
| Primary Arm® Core | 2x Cortex®-A55 up to 1.2 GHz | |
| Secondary Arm® Core | 1x Cortex-M33 up to 500 MHz | |
| RAM | 1 GB | 512 MB |
| ROM | 4GB eMMC | |
| Display Interface | 24-bit RGB + 2-lane MIPI-DSI | |
| GPU | yes | |
| CAN | 2x | |
| Security | Secure Boot, Cryptography | |
| Temperature | -40°C to 85°C | |
| Order Code | QSRZ/G2L/1GS/4GF/I | QSRZ/G2L/512S/4GF/I |

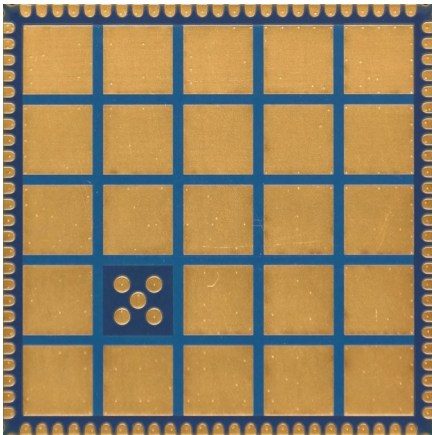
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He has also provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



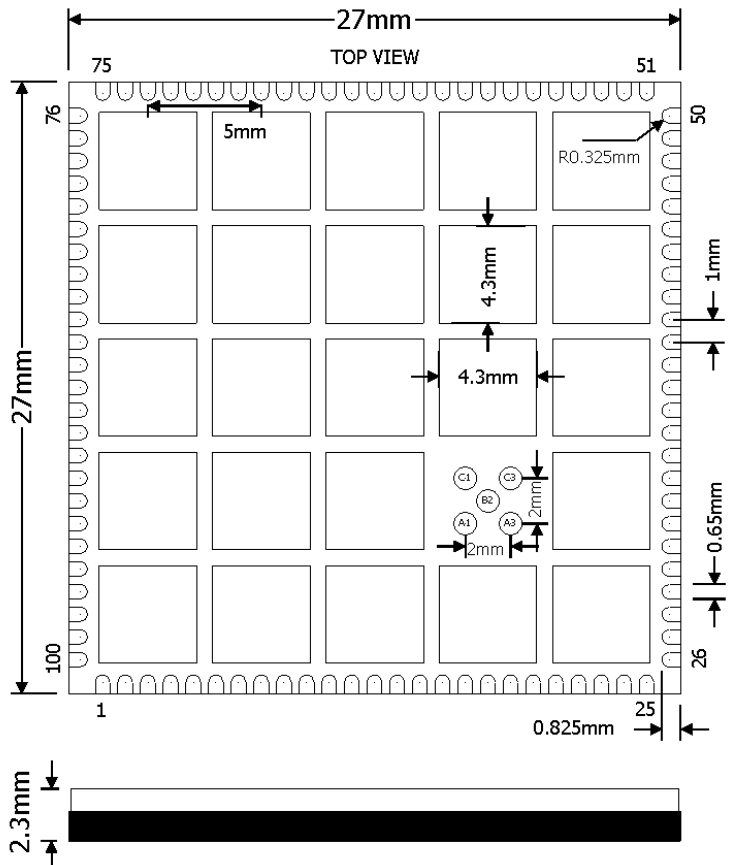
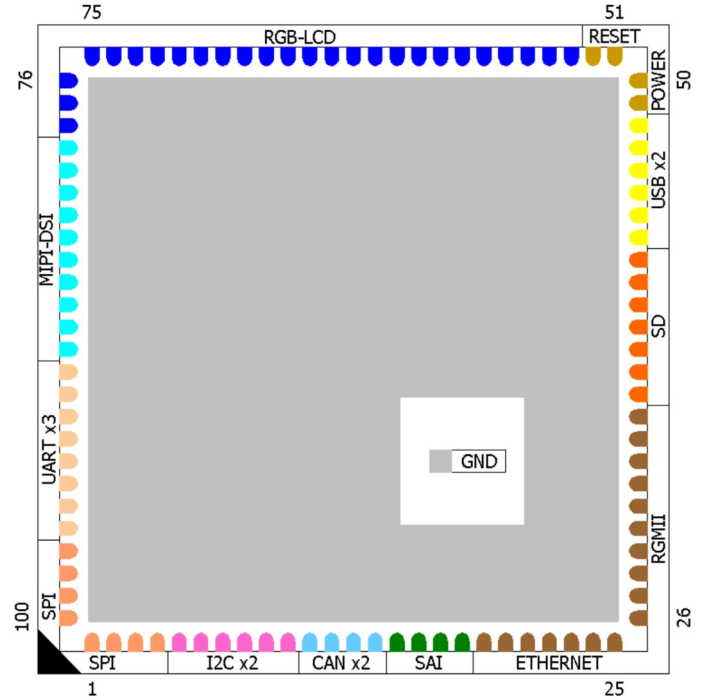
Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing the routing.

Advanced Soldering

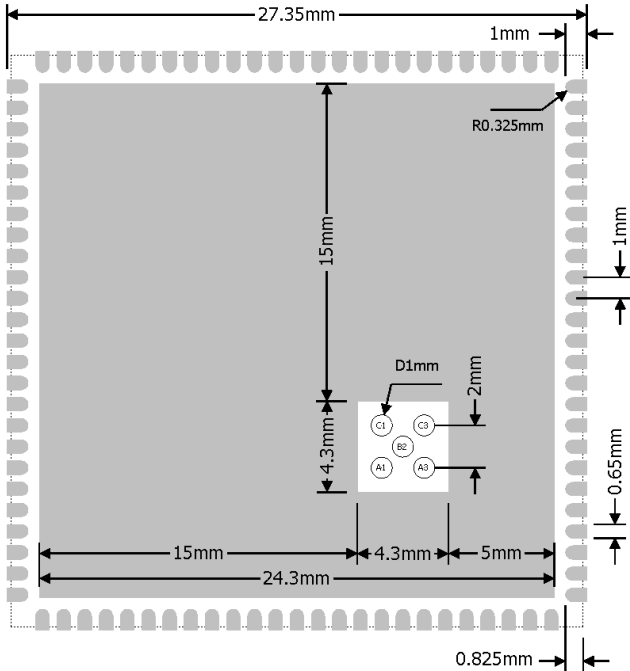
Using a large solder pad underneath the component has not only electrical and thermal advantages. This is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight, which could result in short circuits.

Standard Contact Assignments

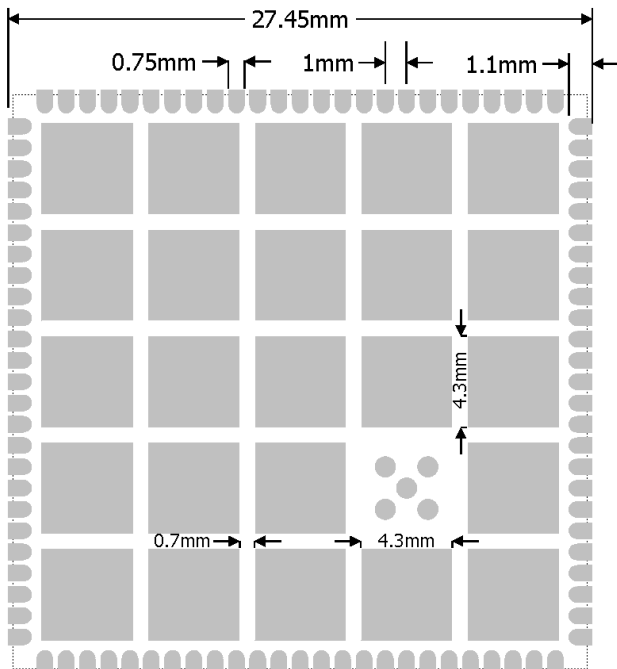


Layout Guidelines

Land pattern

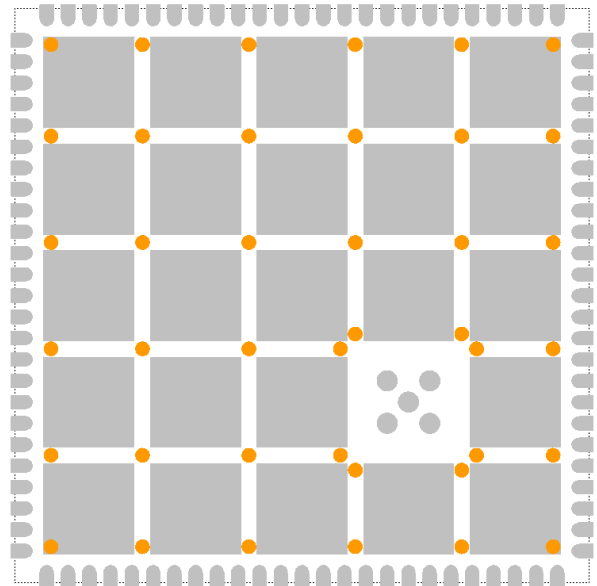


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

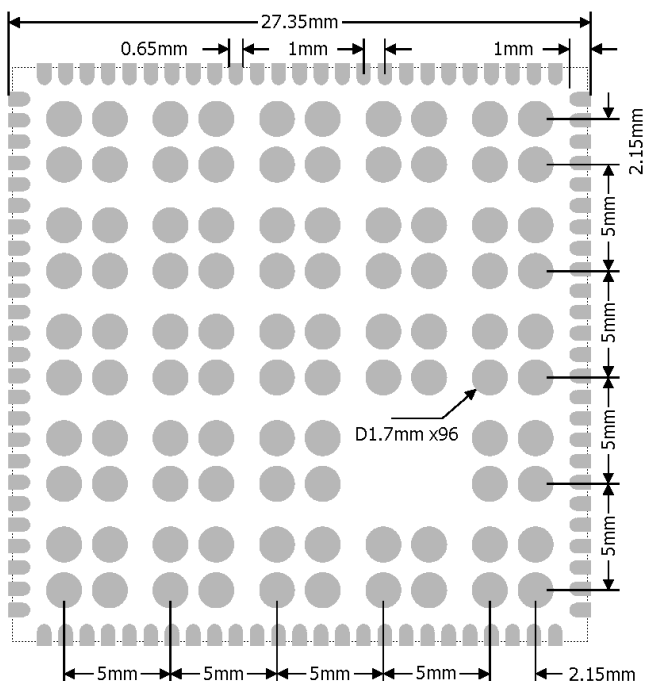


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150 μ m stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, “no clean” solder paste should be used due to low mounted height of the component.

Recommended stencil design

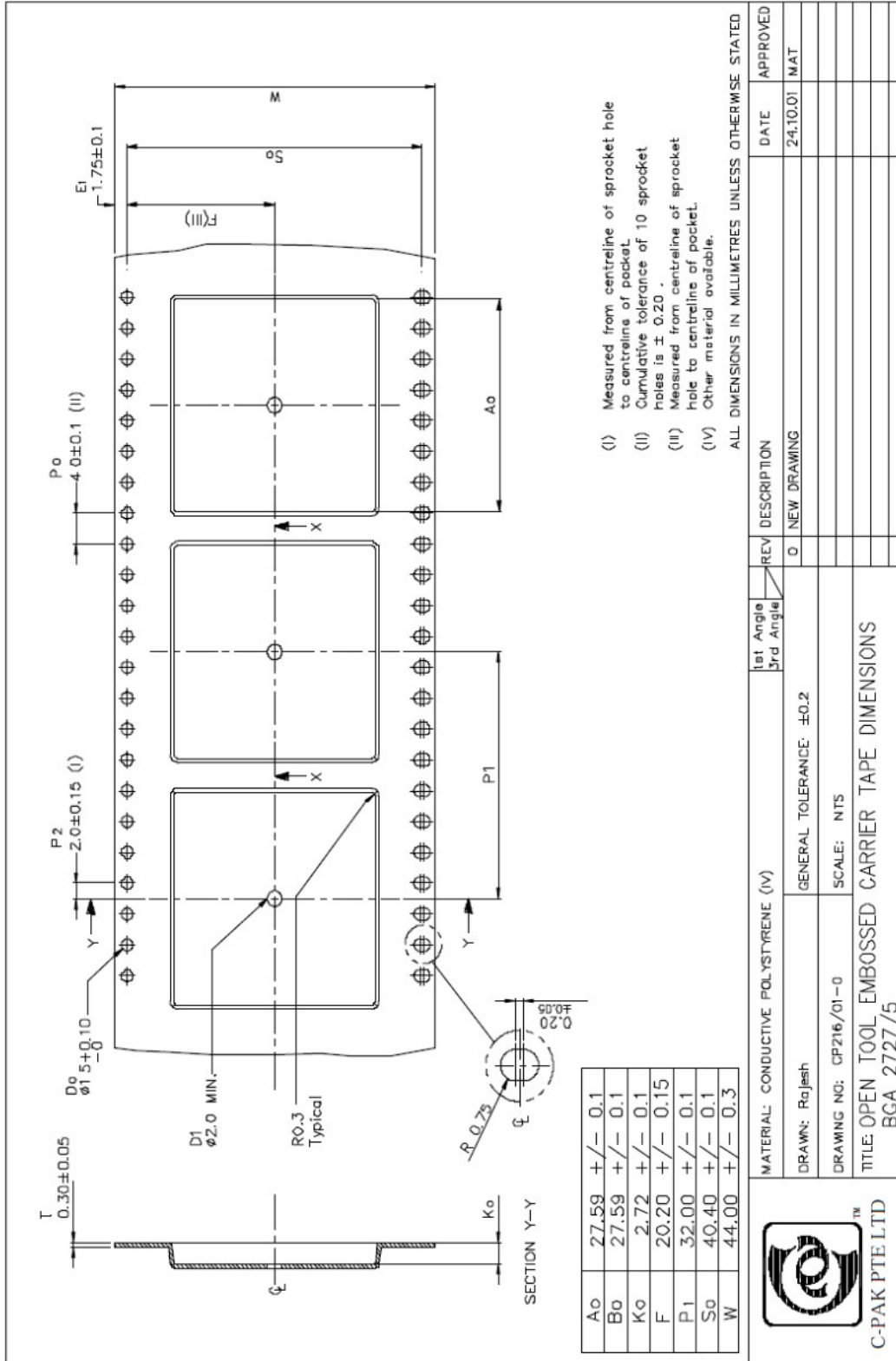


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging



- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

| | | | | | | |
|---------------------------------------------------|--|-----------|-----|-------------|----------|----------|
| MATERIAL: CONDUCTIVE POLYSTYRENE (IV) | | 1st Angle | REV | DESCRIPTION | DATE | APPROVED |
| DRAWN: Rajesh | | 3rd Angle | 0 | NEW DRAWING | 24.10.01 | MAT |
| GENERAL TOLERANCE: ± 0.2 | | | | | | |
| DRAWING NO: CP216/01-0 | | | | | | |
| SCALE: NTS | | | | | | |
| TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS | | | | | | |
| BCA 2727/5 | | | | | | |
| C-PAK PTE LTD | | | | | | |

THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.

| PINOUT | | | | | | |
|---------------------------------|------|-------------|-----------------|-----------------------------------------------------------------------------------------|--------------|------------------------------------------------------|
| PIN | Type | QS Standard | RZ/G2L Pad Name | Alternate functions | GPIO | Description (refer to RZ/G2L manuals for details) |
| POWER SUPPLY & RESET | | | | | | |
| 1st SPI | | | | | | |
| 1 | 3V3 | SPIA_NSS | P43_3 | RSPI0_SSL_B GTIOC5B_B IRQ7_D / MTIOC8D_B | P43_3 | Slave Select signal |
| 2 | 3V3 | SPIA_MISO | P43_2 | RSPI0_MISO_B GTIOC5A_B IRQ6_C / MTIOC8C_B | P43_2 | Master In/Slave Out signal |
| 3 | 3V3 | SPIA_MOSI | P43_1 | RSPI0_MOSI_B GTIOC4B_B GTIOC6B_C IRQ5_C / MTIOC8B_B | P43_1 | Master Out/Slave In signal |
| 4 | 3V3 | SPIA_SCK | P43_0 | RSPI0_CK_B GTIOC4A_B GTIOC6A_C IRQ4_C / MTIOC8A_B | P43_0 | Serial Clock signal |
| I2C | | | | | | |
| 5 | 3V3 | I2CA_SCL | RIIC1_SDA | RIIC1_SDA | N/A | I2C Data |
| 6 | 3V3 | I2CA_SDA | RIIC1_SCL | RIIC1_SCL | N/A | I2C Clock |
| 7 | 3V3 | INTA | P46_3 | SSI1_RXD_D GTETRGD_D CAN1_RX_DATARATE_EN_E RIIC3_SCL_C | P46_3 | |
| 8 | 3V3 | I2CB_SCL | P42_4 | RIIC2_SCL_C CAM_FIELD_B CAN0_RX_DATARATE_EN_D SCIF2_RTS#_D | P42_4 | |
| 9 | 3V3 | I2CB_SDA | P42_3 | RIIC2_SDA_C RSPI2_SSL_B CAN0_TX_DATARATE_EN_D SCIF2_CTS#_D MTIOC7D_B | P42_3 | |
| 10 | 3V3 | INTB | P46_2 | SSI1_TXD_D GTETRGC_D CAN1_TX_DATARATE_EN_E RIIC3_SDA_C | P46_2 | |
| CAN | | | | | | |
| 11 | 3V3 | CANA_RX | P42_2 | ADC_TRG_D RSPI2_MISO_B CAN0_RX_D SCIF2_SCK_D MTIOC7C_B | P42_2 | |
| 12 | 3V3 | CANA_TX | P42_1 | USB1_OVRCUR_D RSPI2_MOSI_B CAN0_TX_D SCIF2_RXD_D MTIOC7B_B | P42_1 | |
| 13 | 3V3 | CANB_RX | P46_1 | SSI1_RCK_D GTETRGB_D CAN1_RX_E RIIC2_SCL_D | P46_1 | |
| 14 | 3V3 | CANB_TX | P46_0 | SSI1_BCK_D GTETRGA_D CAN1_TX_E RIIC2_SDA_D | P46_0 | |
| SAI | | | | | | |
| 15 | 3V3 | SAI_TX | P45_2 | SSI0_TXD_D POE8#_C SCI1_SCK_B | P45_2 | Serial Audio Interface serial data line 0 |
| 16 | 3V3 | SAI_RX | P45_3 | SSI0_RXD_D POE10#_C SCI1_CTS# RTS#_B | P45_3 | Serial Audio Interface serial data line 1 |
| 17 | 3V3 | SAI_SCK | P45_0 | SSI0_BCK_D POE0#_C SCI1_RXD_B | P45_0 | |
| 18 | 3V3 | SAI_FS | P45_1 | SSI0_RCK_D POE4#_C SCI1_TXD_B | P45_1 | |

| PIN | Type | QS Standard | RZ/G2L Pad Name | Alternate functions | GPIO | Description (refer to RZ/G2L manuals for details) |
|-----------------|--------|-------------|-----------------|---------------------------------------------------|-------|----------------------------------------------------------------------------------|
| ETHERNET | | | | | | |
| 19 | 3V3 | ENET_RST | P28_1 | ET0_LINKSTA | P28_1 | |
| 20 | 3V3 | ENET_CK125 | AUDIO_CLK1 | AUDIO_CLK1 | N/A | |
| 21 | 3V3 | ENET_INT | P22_1 | ET0_TX_ERR SSIO_RCK_B CAN1_RX_B MTCLKB_B | P22_1 | |
| 22 | 3V3 | ENET_MDIO | P28_0 | ET0_MDIO | P28_0 | |
| 23 | 3V3 | ENET_MDC | P27_1 | ET0_MDC RSPI1_SSL_A MTIOC8D_A | P27_1 | |
| 24 | 3V3 | ENET_RXC | P24_0 | ET0_RXC RX_CLK SSI1_BCK_B POE0#_B | P24_0 | |
| 25 | 3V3 | ENET_RX_CTL | P24_1 | ET0_RX_CTL RX_DV SSI1_RCK_B POE4#_B | P24_1 | |
| 26 | 3V3 | ENET_RXD0 | P25_0 | ET0_RXD0 SSI1_TXD_B POE8#_B | P25_0 | |
| 27 | 3V3 | ENET_RXD1 | P25_1 | ET0_RXD1 SSI1_RXD_B POE10#_B | P25_1 | |
| 28 | 3V3 | ENET_RXD2 | P26_0 | ET0_RXD2 RSPI1_CK_A MTIOC8A_A | P26_0 | |
| 29 | 3V3 | ENET_RXD3 | P26_1 | ET0_RXD3 RSPI1_MOSI_A MTIOC8B_A | P26_1 | |
| 30 | 3V3 | ENET_TX_CTL | P20_1 | ET0_TX_CTL TX_EN RSPI0_MOSI_A CAN0_TX_B | P20_1 | |
| 31 | 3V3 | ENET_TXC | P20_0 | ET0_TXC TX_CLK RSPI0_CK_A CAN_CLK_B | P20_0 | |
| 32 | 3V3 | ENET_TXD3 | P22_0 | ET0_TXD3 SSIO_BCK_B CAN1_TX_B MTCLKA_B | P22_0 | |
| 33 | 3V3 | ENET_TXD2 | P21_1 | ET0_TXD2 CAN0_RX_DATARATE_EN_B | P21_1 | |
| 34 | 3V3 | ENET_TXD1 | P21_0 | ET0_TXD1 RSPI0_SSL_A CAN0_TX_DATARATE_EN_B | P21_0 | |
| 35 | 3V3 | ENET_TXD0 | P20_2 | ET0_TXD0 RSPI0_MISO_A CAN0_RX_B | P20_2 | |
| SD | | | | | | |
| 36 | 3V3 | SD_CD | P19_0 | SD1_CD_B GTIOC3A_B MTIOC1A_C RIIC2_SDA_B | P19_0 | SD Card Detect |
| 37 | 3V3 | SD_D1 | SD1_DATA1 | SD1_DATA1 | N/A | SD Data bidirectional signals, external pull up resistors must be added. |
| 38 | 3V3 | SD_D0 | SD1_DATA0 | SD1_DATA0 | N/A | |
| 39 | 3V3 | SD_CLK | SD1_CLK | SD1_CLK | N/A | SD Output Clock. |
| 40 | 3V3 | SD_CMD | SD1_CMD | SD1_CMD | N/A | SD Command bidirectional signal, external pull up resistor must be added. |
| 41 | 3V3 | SD_D3 | SD1_DATA3 | SD1_DATA3 | N/A | SD Data bidirectional signals, external pull up resistors must be added. |
| 42 | 3V3 | SD_D2 | SD1_DATA2 | SD1_DATA2 | N/A | |
| USB | | | | | | |
| 43 | analog | USBA_VBUS | Not connected | | | |
| 44 | analog | USBA_DN | USB1_DM | | | D- pin of the USB cable |
| 45 | analog | USBA_DP | USB1_DP | | | D+ pin of the USB cable |

| PIN | Type | QS Standard | RZ/G2L Pad Name | Alternate functions | GPIO | Description (refer to RZ/G2L manuals for details) |
|-----|--------|-------------|-----------------|---------------------|--------|------------------------------------------------------|
| 46 | analog | USBB_VBUS | USB0_VBUSIN | | 30K-PD | 10K/20K voltage divider |
| 47 | analog | USBB_DN | USB0_DM | | | D- pin of the USB cable |
| 48 | analog | USBB_DP | USB0_DP | | | D+ pin of the USB cable |

POWER SUPPLY & RESET

| | | | | | | |
|----|-----------|--|--|--|--|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 49 | VIN | | | | | 3.3V power supply input |
| 50 | | | | | | |
| 51 | POR | | | | | PMIC reset input pin. Pulled to LDO1 (1.8V) power rail by an onboard 10K resistor. Asserted low, PMIC performs reset. Leave unconnected, if not used. |
| 52 | BOOT_MODE | | | | | L: Boot from FLASH H: Boot from UART |

DISPLAY

| | | | | | | |
|----|-----|-----------|-------|--------------------------------------------------------------|-------|--|
| 53 | 3V3 | LCD_DE | P7_1 | DISP_DE SSI0_RXD_A USB0_OTG_ID_B MTIC5V_A | P7_1 | |
| 54 | 3V3 | LCD_VSYNC | P7_0 | DISP_VSYNC SSI0_TXD_A USB0_OVRCUR_B MTIC5U_A | P7_0 | |
| 55 | 3V3 | LCD_HSYNC | P6_1 | DISP_HSYNC SSI0_RCK_A MTIOC1B_B | P6_1 | |
| 56 | 3V3 | LCD_CLK | P6_0 | DISP_CLK SSI0_BCK_A USB0_VBUSEN_B MTIOC1A_B | P6_0 | |
| 57 | 3V3 | LCD_R1 | P8_0 | DISP_DATA1 USB1_VBUSEN_A RSPI2_CK_A RIIC3_SCL_A | P8_0 | |
| 58 | 3V3 | LCD_R2 | P8_1 | DISP_DATA2 USB1_OVRCUR_A RSPI2_MOSI_A RIIC3_SDA_A | P8_1 | |
| 59 | 3V3 | LCD_R3 | P8_2 | DISP_DATA3 RSPI2_MISO_A | P8_2 | |
| 60 | 3V3 | LCD_R4 | P9_0 | DISP_DATA4 ADC_TRG_C RSPI2_SSL_A MTIOC2A_B | P9_0 | |
| 61 | 3V3 | LCD_R5 | P9_1 | DISP_DATA5 MTIOC2B_B | P9_1 | |
| 62 | 3V3 | LCD_R6 | P10_0 | DISP_DATA6 CAN_CLK_A MTIOC6A GTETRGA_A | P10_0 | |
| 63 | 3V3 | LCD_R7 | P10_1 | DISP_DATA7 CAN0_TX_A MTIOC6B GTETRGA_A | P10_1 | |
| 64 | 3V3 | LCD_G2 | P12_0 | DISP_DATA10 CAN0_RX_DATARATE_EN_A POE0#_A GTIOC7A_A | P12_0 | |
| 65 | 3V3 | LCD_G3 | P12_1 | DISP_DATA11 CAN1_TX_A POE4#_A GTIOC7B_A | P12_1 | |
| 66 | 3V3 | LCD_G4 | P13_0 | DISP_DATA12 CAN1_RX_A POE8#_A IRQ0_B | P13_0 | |
| 67 | 3V3 | LCD_G5 | P13_1 | DISP_DATA13 CAN1_TX_DATARATE_EN_A POE10#_A IRQ1_B | P13_1 | |
| 68 | 3V3 | LCD_G6 | P13_2 | DISP_DATA14 CAN1_RX_DATARATE_EN_A IRQ7_B IRQ2_B | P13_2 | |
| 69 | 3V3 | LCD_G7 | P14_0 | DISP_DATA15 SSI1_BCK_A SD1_CD_A MTCLKA_A | P14_0 | |

| PIN | Type | QS Standard | RZ/G2L Pad Name | Alternate functions | GPIO | Description (refer to RZ/G2L manuals for details) |
|------------------------|------|-------------|-----------------|-----------------------------------------------------------------|-------|--------------------------------------------------------------|
| 70 | 3V3 | LCD_B1 | P15_0 | DISP_DATA17 SSI1_TXD_A GTIOC4A_A MTCLKC_A | P15_0 | |
| 71 | 3V3 | LCD_B2 | P15_1 | DISP_DATA18 SSI1_RXD_A GTIOC4B_A MTCLKD_A | P15_1 | |
| 72 | 3V3 | LCD_B3 | P16_0 | DISP_DATA19 SCIF2_TXD_B GTIOC5A_A IRQ3_B | P16_0 | |
| 73 | 3V3 | LCD_B4 | P16_1 | DISP_DATA20 SCIF2_RXD_B GTIOC5B_A IRQ4_B | P16_1 | |
| 74 | 3V3 | LCD_B5 | P17_0 | DISP_DATA21 SCIF2_SCK_B GTIOC6A_A IRQ5_B | P17_0 | |
| 75 | 3V3 | LCD_B6 | P17_1 | DISP_DATA22 SCIF2_CTS#_B GTIOC6B_A IRQ6_B | P17_1 | |
| 76 | 3V3 | LCD_B7 | P17_2 | DISP_DATA23 SCIF2_RTS#_B IRQ7_C | P17_2 | |
| Display Control | | | | | | |
| 77 | 3V3 | LCD_EN | | | | |
| 78 | 3V3 | LCD_BL | P19_1 | SD1_WP_B GTIOC3B_B MTIOC1B_C RIIC2_SCL_B | P19_1 | PWM Output |
| MISC | | | | | | |
| 79 | 3V3 | LCD_R0 | P7_2 | DISP_DATA0 USB0_OTG_EXICEN_B MTIC5W_A | P7_2 | |
| 80 | 3V3 | LCD_G0 | P11_0 | DISP_DATA8 CAN0_RX_A MTIOC6C GTETRGC_A | P11_0 | |
| 81 | 3V3 | LCD_G1 | P11_1 | DISP_DATA9 CAN0_TX_Datarate_EN_A MTIOC6D GTETRGD_A | P11_1 | |
| 82 | 3V3 | LCD_B0 | P14_1 | DISP_DATA16 SSI1_RCK_A SD1_WP_A MTCLKB_A | P14_1 | |
| MIPI-DSI | | | | | | |
| 83 | MIPI | DSI_DP1 | DSI_DATA1_P | DSI_DATA1_P | | |
| 84 | MIPI | DSI_DN1 | DSI_DATA1_N | DSI_DATA1_N | | |
| 85 | MIPI | DSI_DP0 | DSI_DATA0_P | DSI_DATA0_P | | |
| 86 | MIPI | DSI_DN0 | DSI_DATA0_N | DSI_DATA0_N | | |
| 87 | MIPI | DSI_CKP | DSI_CLKP | DSI_CLKP | | |
| 88 | MIPI | DSI_CKN | DSI_CLKN | DSI_CLKN | | |
| UART | | | | | | |
| 89 | 3V3 | UARTA_RXD | P38_1 | SCIF0_RXD GTETRGB_C CAN0_TX_C MTIOC4B USB1_OVRCUR_C | P38_1 | 1 st application UART Receive Data input signal |
| 90 | 3V3 | UARTA_TXD | P38_0 | SCIF0_TXD GTETRGA_C CAN_CLK_C MTIOC4A USB1_VBUSEN_C | P38_0 | 1 st application UART Transmit Data output signal |

| PIN | Type | QS Standard | RZ/G2L Pad Name | Alternate functions | GPIO | Description (refer to RZ/G2L manuals for details) |
|---------------------------|------|-------------|-----------------|-------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------|
| 91 | 3V3 | UARTB_RXD | P40_1 | SCIF1_RXD GTIOC6B_B CAN1_RX_C MTIC5V_B SCIO_TXD_B | P40_1 | 2 nd application UART Receive Data input signal |
| 92 | 3V3 | UARTB_TXD | P40_0 | SCIF1_TXD GTIOC6A_B CAN1_TX_C MTIC5U_B SCIO_RXD_B | P40_0 | 2 nd application UART Transmit Data output signal |
| 93 | 3V3 | UARTC_RXD | P48_1 | SCIF2_RXD_E RSPI1_MOSI_C RIIC2_SCL_E MTCLKB_C | P48_1 | 3 rd application UART Receive Data input signal |
| 94 | 3V3 | UARTC_TXD | P48_0 | SCIF2_TXD_E RSPI1_CK_C RIIC2_SDA_E MTCLKA_C | P48_0 | 3 rd application UART Transmit Data output signal |
| 95 | 3V3 | UARTC_CTS | P48_3 | SCIF2_CTS#_E RSPI1_SSL_C RIIC3_SCL_D MTCLKD_C | P48_3 | 3 rd application UART Clear to Send input signal |
| 96 | 3V3 | UARTC_RTS | P48_4 | SCIF2_RTS#_E ADC_TRG_E | P48_4 | 3 rd application UART Request to Send output signal |
| 2nd SPI | | | | | | |
| 97 | 3V3 | SPIB_NSS | P44_3 | RSPI1_SSL_B SSI1_RXD_C CAN1_RX_DATARATE_EN_D MTIOC3D_B GTIOC7B_C | P44_3 | |
| 98 | 3V3 | SPIB_MISO | P44_2 | RSPI1_MISO_B SSI1_TXD_C CAN1_TX_DATARATE_EN_D MTIOC3C_B GTIOC7A_C | P44_2 | |
| 99 | 3V3 | SPIB_MOSI | P44_1 | RSPI1_MOSI_B SSI1_RCK_C CAN1_RX_D MTIOC3B_B GTIOC6B_D | P44_1 | |
| 100 | 3V3 | SPIB_SCK | P44_0 | RSPI1_CK_B SSI1_BCK_C CAN1_TX_D MTIOC3A_B GTIOC6A_D | P44_0 | |

Onboard wiring

Pins used for manufacturing – leave unconnected

| PIN | (RZ/G2L PAD NAME) | PIN | (RZ/G2L PAD NAME) | PIN | (RZ/G2L PAD NAME) |
|-----|---------------------|-----|-------------------|-----|----------------------|
| C1 | JTAG_TDI (TDI) | | | C3 | JTAG_TCK (TCK/SWCLK) |
| | | B2 | JTAG_TDO (TDO) | | |
| A1 | JTAG_TRST_B (TRST#) | | | A3 | JTAG_TMS (TMS/SWDIO) |

Onboard peripherals wiring

| | RZ/G2L Pad Name | Remarks |
|------|-----------------|-------------|
| eMMC | SD0_CLK | |
| | SD0_CMD | |
| | SD0_DATA0 | |
| | SD0_DATA1 | |
| | SD0_DATA2 | |
| | SD0_DATA3 | |
| | SD0_DATA4 | |
| | SD0_DATA5 | |
| | SD0_DATA6 | |
| | SD0_DATA7 | |
| | SD0_RST# | |
| LED | P48_2 | Low: LED on |