

200/400/800 MHz, Single Arm[®] Cortex[®]-R52 on-chip FPU and NEON[™], 1.0 MB of on-chip SRAM, Ethernet MAC, EtherCAT, USB 2.0 high-speed, CAN/CANFD, various communications interfaces such as an xSPI and $\Delta\Sigma$ interface, encoder interfaces, and security functions

Features

- On-chip 32-bit Arm Cortex-R52 processor
 - High-speed realtime control with operating frequency of 200/400/800 MHz
 - On-chip Single 32-bit Arm Cortex-R52 (revision r1p2)
 - Tightly coupled memory (TCM) with ECC
 - 512 KB/64 KB
 - Instruction cache/data cache with ECC
 - 16 KB per cache
 - High-speed interrupt
 - The FPU supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single-precision and double-precision.
 - The NEON, Advanced SIMD, supports integer or single precision results.
 - Harvard architecture with 8-stage pipeline
 - Supports the memory protection unit (MPU)
 - Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces.
- Low power consumption
 - Standby mode and module stop function
- On-chip SRAM
 - 1.0 MB of the on-chip SRAM with ECC
 - 150/200 MHz
- Data transfer
 - DMAC: 16 channels × 2 units
- Event link controller
 - Module operations can be started by event signals rather than by interrupt handlers.
 - Linked operation of modules is available even while the CPU is in the standby state.
- Reset and power supply voltage control
 - Four reset sources including a pin reset
- Clock functions
 - External clock/oscillator input frequency: 25 MHz
 - CPU clock frequency: 200/400/800 MHz or 150/300/600 MHz
 - System clock frequency: 200 MHz or 150 MHz
 - Low-speed on-chip oscillator (LOCO): 240 kHz
- Safety functions
 - Register write protection, input clock oscillation stop detection and CRC
 - Master Memory Protection Unit (MPU)
- Security functions (optional)
 - Boot mode with security through encryption
 - JTAG authentication
 - Cryptologic accelerator
 - TRNG
- Encoder interfaces
 - Up to 2 channels
 - EnDat 2.2, BiSS-C, A-format, and HIPERFACE DSL-compliant interfaces
 - Frequency-divided output from an encoder
- Various communications interfaces
 - Ethernet
 - EtherCAT slave Controller: 3 ports
 - Ethernet MAC: 1 port
 - USB 2.0 high-speed host/functions: 1 channel
 - CAN/CANFD (compliant with ISO11898-1): 2 channels
 - SCI with 16-byte transmission and reception FIFOs: 6 channels
 - I2C bus interface: 3 channel for transfer at up to 400 kbps
 - SPI: 4 channels
 - xSPI: 2 channels
- External host interfaces
 - Serial host interface (SHOSTIF)
- External address space
 - Buses for high-speed data transfer at up to 100 MHz
 - Support for up to 4 CS areas
 - 8- or 16-bit bus space is selectable per area
- Up to 35 extended-function timers
 - 16-bit × 8 + 32-bit MTU3 (9 channels), 32-bit GPT (18 channels): Input capture, output compare, PWM waveform output
 - 16-bit CMT (6 channels), 32-bit CMTW (2 channels)
- $\Delta\Sigma$ interface
 - Up to 6 $\Delta\Sigma$ modulators are connectable externally.
- Trigonometric function unit
 - Simultaneous calculation of sine and cosine
 - Simultaneous calculation of arctangent and hypot_k
- 12-bit A/D converter
 - 12 bits × 2 unit (4 channels for unit 0 and 1)
- Temperature sensor for measuring temperature within the chip
- General-purpose I/O ports
 - Input pull-up/pull-down
 - The locations of input/output functions for peripheral modules are selectable from among multiple pins.
- Operating temperature range
 - Tj = -40 to +125°C

1. Overview

1.1 Outline of Specifications

The MPU is a high-performance ASSP that has Arm Cortex[®]-R52 processor with Floating-Point Unit (FPU) and NEON[™]. It incorporates integrated peripheral functions necessary for system configuration.

Table 1.1 CPU

Feature	Functional description
Arm [®] Cortex [®] -R52	<ul style="list-style-type: none"> • Single processor • Operating frequency <ul style="list-style-type: none"> – 200 MHz/400 MHz/800 MHz (in case of 200 MHz system clock) – 150 MHz/300 MHz/600 MHz (in case of 150 MHz system clock) • 32-bit CPU Cortex-R52 designed by Arm (core revision r1p2) • Address space: 4 GB • Instruction cache <ul style="list-style-type: none"> – 16 KB (with ECC) • Data cache <ul style="list-style-type: none"> – 16 KB (with ECC) • Tightly coupled memory (TCM) <ul style="list-style-type: none"> – ATCM: 512 KB (with ECC) 1 wait (0 wait selectable if less than 400 MHz) – BTCM: 64 KB (with ECC) 0 wait – CTCM: 0 KB (with ECC) • Instruction set: Arm v8-R architecture, so support includes Thumb[®] and Thumb-2 • Data arrangement <ul style="list-style-type: none"> – Instructions: Little endian – Data: Little endian • 2-stage memory protection unit (MPU)
FPU	<ul style="list-style-type: none"> • Supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single- and double-precision. • Registers <ul style="list-style-type: none"> 64-bit single-word registers: 64 bits × 32 (can be used as 16 double-word registers: 128 bits × 16)
NEON	The Advanced SIMD supporting integer or single precision results

Table 1.2 Memory

Feature	Functional description
On-chip system SRAM with ECC	<ul style="list-style-type: none"> • Capacity: Up to 1.0 MB (512 KB × 2 units) (with ECC) • Operating frequency: 150 MHz/200 MHz • SEC-DED (single error correction/double error detection) Error injection supported
One-time programmable memory	<ul style="list-style-type: none"> • Overwrite protection • Redundancy support • ECC support • Available information <ul style="list-style-type: none"> – Unique ID – Authentication settings – Trimming data – Boot mode setting – User area

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	<p>The operating mode can be selected from the following seven boot modes:</p> <ul style="list-style-type: none"> • xSPI0 boot mode (CS0 × 1 boot Serial Flash) • xSPI0 boot mode (CS0 × 8 boot Serial Flash) • 16-bit bus boot mode (CS0 NOR Flash) • xSPI1 boot mode (CS0 × 1 boot Serial Flash) • SHOSTIF boot mode • SCI boot mode • USB boot mode

Table 1.3 System (2 of 2)

Feature	Functional description
Clock generation circuit	<ul style="list-style-type: none"> The input clock can be selected from an external clock or external resonator. Detection of input clock oscillation stopping The following clocks are generated: <ul style="list-style-type: none"> CPU0 clock: System clock ×1, ×2, or ×4 System clock: 150 or 200 MHz High-speed peripheral module clock: 150 or 200 MHz Middle-speed peripheral module clock: 75 or 100 MHz Low-speed peripheral module clock: 37.5 or 50 MHz ADC clock in the 12-bit A/D converter: 18.75 or 25 MHz External bus clock: 100 MHz (max.) Low-speed on-chip oscillator: 240 kHz (fixed)
Reset	RES# pin reset, software reset, error reset, CPU0 software reset
Low-power consumption function	<ul style="list-style-type: none"> Standby mode (Cortex-R52) Module stop function
Interrupt controller (ICU)	<ul style="list-style-type: none"> Connect an interrupt to the GIC (Generic Interrupt Controller) for Cortex-R52 CPU0 Connect an activating trigger to the DMAC and ELC Peripheral function interrupts: 448 sources External interrupts: 16 sources (IRQ0 to IRQ15 pins) Software interrupts: 8 sources Non-maskable interrupts: 1 sources 16 levels specifiable for the order of priority in the GIC
Bus state controller (BSC)	<ul style="list-style-type: none"> The external address space is divided into four areas (CS0, CS2, CS3, and CS5) for management. The following features are configurable for each area independently: Bus size (8 or 16 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas). Idle wait cycle insertion (between same area access cycles or different area access cycles). Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software). Connectable memory type for each area CS0: SRAM, burst ROM CS2: SRAM CS2 + CS3: SRAM, SDRAM (CS2 only for SDRAM is not supported) CS3: SRAM, SDRAM CS5: SRAM, MPX-IO SDRAM refresh Auto refresh or self-refresh mode selectable SDRAM burst access

Table 1.4 Direct memory access

Feature	Functional description
Direct memory access controller (DMAC)	<ul style="list-style-type: none"> 2 unit (16 channels each unit) Transfer modes: Single transfer mode and block transfer mode Transfer size <ul style="list-style-type: none"> Unit 0: 1/2/4/8/16/32/64 bytes Unit 1: 1/2/4/8/16/32 bytes Activation sources: Software trigger, external DMA requests (DREQ), external interrupts, and interrupt requests from peripheral functions

Table 1.5 I/O Ports

Feature	Functional description
General-purpose I/O ports	<ul style="list-style-type: none"> 196-pin FBGA <ul style="list-style-type: none"> I/O pins: 110 Input pins: 1 Pull-up/pull-down resistors: 111 The locations of input/output functions are selectable from among multiple pins.

Table 1.6 Event link

Feature	Functional description
Event link controller (ELC)	<ul style="list-style-type: none"> Up to 213 event signals can be interlinked with the operation of modules. In particular, the operation of timer modules can be started by input event signals. Event-linked operation of signals of ports 16 and port 18 is to be possible.

Table 1.7 Timers (1 of 2)

Feature	Functional description
Multi-function timer pulse unit 3 (MTU3)	<ul style="list-style-type: none"> 9 channels (16 bits × 8 channels, 32 bits × 1 channel) Maximum of 28 pulse-input/output and 3 pulse-input possible Select from among 10, 11, 12, or 14 counter-input clock signals for each channel (with maximum operating frequency of 200 MHz) Input capture function 39 output compare/input capture registers Counter clear operation (synchronous clearing by compare match/input capture) Simultaneous writing to multiple timer counters (TCNT) Simultaneous register input/output by synchronous counter operation Buffered operation Support for cascade-connected operation Automatic transfer of register data Pulse output mode <ul style="list-style-type: none"> Toggle/PWM/complementary PWM/reset-synchronized PWM Complementary PWM output mode <ul style="list-style-type: none"> Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration Reset synchronous PWM mode <ul style="list-style-type: none"> Three phases of positive and negative PWM waveforms can be output with desired duty cycles. Phase-counting mode: 16-bit mode (channels 1 and 2), 32-bit mode (channels 1 and 2 in cascade connection) Counter functionality for dead-time compensation Generation of triggers for A/D converter conversion A/D converter start triggers can be skipped Digital noise filter function for signals on the input capture and external counter clock pins Event linking by the ELC

Table 1.7 Timers (2 of 2)

Feature	Functional description
General PWM timer (GPT)	<ul style="list-style-type: none"> • 32 bits × 18 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 400 MHz for LLPP) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of 3 counters, generation of automatic 3-phase PWM waveforms incorporating dead times • Starting, clearing, stopping, switching, up/down counters, and input capture in response to external or internal triggers • Starting, clearing, stopping, switching, up/down counters, and input capture in response to input level comparison • Internal trigger sources: software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC • Function of output duty 0% and 100% is selectable from troughs or crests/troughs. (all units)
Compare match timer (CMT)	<ul style="list-style-type: none"> • (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel
Compare match timer W (CMTW)	<ul style="list-style-type: none"> • (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.
Watchdog timer (WDT)	<ul style="list-style-type: none"> • 14 bits × 1 channel • Select from among six counter-input clock signals for each channel
Port output enable 3 (POE3)	<ul style="list-style-type: none"> • Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation anomaly detection, two types of DSMIF error detection, or software • Additional programming of output control target pins is enabled
Port output enable for GPT (POEG)	<ul style="list-style-type: none"> • Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPT • Initiation by detection of oscillation stop, two types of DSMIF error detection (unit in LLPP only), or by software
Real time clock (RTC)	<ul style="list-style-type: none"> • A 100 year calendar from 2000 to 2099 • BCD code display • Clock source is division of main oscillator. • Automatic adjustment function for leap years

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Ethernet MAC (GMAC) ^{*2}	<ul style="list-style-type: none"> ● 1 port ● IEEE802.3 ● IEEE1588-2008 ● IEEE802.3-az-2010 for EEE ● Support for 10/100/1000 Mbps data transfer ● Full duplex and half duplex are supported ● Programmable frame length to support both standard and jumbo frames up to 16 KB ● 17 MAC address registers for the address filter block ● Variety of flexible addresses filtering modes are supported ● Advanced IEEE 1588-2002 & 2008 Ethernet frame time-stamping supported ● MII/RMII/RGMII interface is supported by RMII/RGMII converter ● Timer module
EtherCAT slave controller (ESC) ^{*1 *2}	<ul style="list-style-type: none"> ● 1 channel (3 ports) ● EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented ● MII interface is supported. MII/RMII interface is supported by RGMII converter in Ethernet Subsystem.
USB 2.0 HS host/function module	<ul style="list-style-type: none"> ● 1 port ● Compliance with the USB 2.0 specification ● OTG support ● Transfer rate <ul style="list-style-type: none"> High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps, host only) ● Communications buffer <ul style="list-style-type: none"> – Incorporates 1 KB of RAM for host mode – Incorporates 8 KB of RAM for function mode ● DMAC (2 channels) incorporated
Serial communication interface (SCI)	<ul style="list-style-type: none"> ● 6 channels ● 5 communication mode <ul style="list-style-type: none"> – Asynchronous interfaces – 8-bit clock synchronous interface – Simple I2C (master-only) – Simple SPI – Smart card interface ● Clock source is select from among four internal clock signals ● Bit rate specifiable with the on-chip baud rate generator ● Full-duplex and half-duplex communication ● Data length: 7 to 9 bits (Asynchronous mode) ● Bit rate modulation ● Double speed mode (Asynchronous, Clock Synchronous, Simple SPI mode) ● RS-485 driver control function (Asynchronous mode) ● Loopback function to enable self-diagnosis (Asynchronous, Clock synchronous mode)
I ² C bus interface (IIC)	<ul style="list-style-type: none"> ● 3 channels ● Communication formats: I2C bus format or SMBus format ● Master or slave mode selectable ● Supports the multi-master ● Maximum transfer rate: 400 kbps (Standard mode and Fast mode)
CAN-FD module (CANFD) ^{*3}	<ul style="list-style-type: none"> ● 2 channels ● Comply with CAN-FD ISO 11898-1 (2015) ● Communication speed <ul style="list-style-type: none"> – Classical CAN mode: 1 Mbps – CAN FD mode: <ul style="list-style-type: none"> Nominal bit rate: max. 1 Mbps Data bit rate: max. 8 Mbps ● Total 192 message buffers (in case frame size is 76 bytes) <ul style="list-style-type: none"> – Individual buffers: 64 for TX – Shared buffers: 128 for TX and RX including FIFO ● Selectable ID type with 11-bit Standard and 18-bit Extended ● Selectable Frame type: Data Frame and Remote Frame ● Up to 256 receive rules

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Serial peripheral interface (SPI)	<ul style="list-style-type: none"> • 4 channels • SPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) capable of handling serial transfer as a master or slave • Data formats <ul style="list-style-type: none"> – Switching between MSB first and LSB first – Transfer bit length selectable to 4 - 32 bits – 32 bits × 4-stage FIFO transmit and receive buffers – Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • RSPCK can be stopped automatically with the reception buffer full for master reception
Expanded serial peripheral interface (xSPI)	<ul style="list-style-type: none"> • 2 channels • Comply with JESD251 • Multiple slave up to 2 slaves • Protocol mode: 1/4/8pin with SDR/DDR 1S-1S-1S, 4S-4D-4D, 8D-8D-8D • Support OctaFlash, OctaRAM, HyperFlash and HyperRAM • Protocol mode: 2/4pin with SDR compatible with QSPI 1S-2S-2S, 2S-2S-2S 1S-4S-4S, 4S-4S-4S • Configurable address length • Configurable initial access latency cycle • Support XiP mode • Support up to 256 MB address space • Prefetch function for burst-read with low latency • Outstanding buffer for burst-write with high throughput • Manual command configurable up to 4 commands • Output clock/input strobe port timing shift • Automatic command after released reset: up to 4 commands • 1.8 V/3.3 V selectable for xSPI0 and 3.3 V fix for xSPI1

Note 1. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany.

Note 2. The product has a device which do not support GMAC and ESC.

Note 3. The product have a device with Classical CAN mode only.

Table 1.9 Analog

Feature	Functional description
12-bit A/D converter (ADC12)	<ul style="list-style-type: none"> • 12 bits × 2 units (unit 0: 4 channels, unit 1: 4 channels) • 12-bit resolution • Conversion time 0.84 μs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in both unit 0 and unit 1) included • Sampling variable Sampling time can be set up for each channel • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, timer (MTU3, ELC) trigger, external trigger • Event linking by the ELC
Temperature sensor unit (TSU)	<ul style="list-style-type: none"> • 1 channel • Relative precision: ±1°C (typ)

Table 1.10 Hardware accelerator for industrial interfaces

Feature	Functional description
$\Delta\Sigma$ interface (DSMIF)	<ul style="list-style-type: none"> • 3 channels \times 2 units • Selectable 2 inputs (U/V) or 3 inputs (U/V/W) • Up to 6 $\Delta\Sigma$ modulators are externally connectable • Sinc filter can be selected as first, second or third order • Direct error connection to POE3 and POEG • Enhancement of current error detection
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, hypot_k ($\sqrt{x^2 + y^2}/k$) <ul style="list-style-type: none"> • Simultaneous calculation of sine and cosine • Simultaneous calculation of arctangent and hypot_k
Encoder interfaces	<ul style="list-style-type: none"> • EnDat 2.2 (2 units) • BiSS-C (2 units) • A-format (2 units) • HIPERFACE DSL (2 units) • ENCOUT (1 unit)

Table 1.11 Safety

Feature	Functional description
Memory protection unit (MPU)	<ul style="list-style-type: none"> • Cortex-R52 MPU Two stages MPUs (EL2 and EL1) 24 regions each MPU • Master MPU Memory protection for masters except Cortex-R52 (DMAC, USB, Ethernet MAC, CoreSight, SHOSTIF)
Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
CRC calculator (CRC)	<ul style="list-style-type: none"> • 2 channels • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: <ul style="list-style-type: none"> – $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet) – $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) – $X^{16} + X^{15} + X^2 + 1$ (CRC-16) – $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) – $X^8 + X^2 + X + 1$ (CRC-8)
Clock monitor circuit (CLMA)	<ul style="list-style-type: none"> • Monitors the abnormal output clock frequency from the input clock (main clock oscillator), PLL circuit, or low-speed on-chip oscillator. • Input clock oscillation stop detection: Available
Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Isolated peripherals	<ul style="list-style-type: none"> • Safety dedicated peripherals are available: <ul style="list-style-type: none"> – GPT: 4 ch – SCI: 1 ch – IIC: 1 ch – SPI: 1 ch – CRC: 1 unit – RTC: 1 unit – GPIO: Sharable with normal GPIO – On-chip system SRAM with ECC • They are mapped independently from normal peripherals so that access protection can be done by EL2 MPU.

Table 1.12 Security

Feature	Functional description
Security*1	<ul style="list-style-type: none"> ● Secure boot ● JTAG authentication ● Cryptographic accelerators <ul style="list-style-type: none"> – Symmetric Cipher: AES 128/192/256 bits with CBC/ECB/CTR/GCM/XTS – Asymmetric Cipher: ECC 256 bits, RSA 1024/2048/3072 bits, RSAES-OAEP – Hash: SHA-1, SHA-2 – Message authentication: HMAC, CMAC, GMAC – Signature algorithms: ECDSA with NIST P-256, RSASSA-PSS, RSASSA-PKCS1 ● TRNG

Note 1. For details, contact our sales representative.

Table 1.13 Debug

Feature	Functional description
Debugging interface	<ul style="list-style-type: none"> ● CoreSight architecture designed by Arm ● Debugging function by the JTAG/SWD interface, and trace function by the trace port interface

Table 1.14 External host interface

Feature	Functional description
Serial host interface (SHOSTIF)	<ul style="list-style-type: none"> ● Serial communication is possible in slave mode. ● Supported interface <ul style="list-style-type: none"> – Motorola Serial Peripheral Interface (4-wire SPI) – Enhanced SPI Modes with Dual, Quad, or Octal SPI ● Serial clock polarity switching ● Serial clock phase switching ● Single Data Transfer ● Data size is up to 32 bits × 64 burst
Mailbox and semaphore (MBXSEM)	<ul style="list-style-type: none"> ● Eight semaphores ● Four 32-bit mailboxes for both external host CPU to Cortex-R52 and Cortex-R52 to external host CPU ● Interrupts can be generated and cleared from both external host CPU and Cortex-R52

Table 1.15 Others

Feature	Functional description
Power supply voltage	VDD = 1.1 V (Core) VCC18 = 1.8 V (PLL, USB, ADC, TSU) VCC33 = 3.3 V (I/O, USB) VCC1833 = 1.8 V (RGMII, xSPI) or 3.3 V (RMII/MII, xSPI*1)
Operating temperature	Tj = -40 to +125°C
Packages	196 pin FBGA 12 × 12 mm, 0.8-mm pitch

Note 1. Maximum xSPI clock frequency is 75 MHz at 3.3 V.

1.2 Product Lineup

Table 1.16 shows a product lineup.

Table 1.16 Product lineup

Part Number	Package	CPU	System SRAM Capacity	CAN	EtherCAT	Security
R9A07G074M08GBG	PLBG0196GC-A	Single Cortex-R52	1.0 MB	CAN-FD	Available	Available
R9A07G074M05GBG	PLBG0196GC-A	Single Cortex-R52	1.0 MB	Classical CAN	Not available	Available
R9A07G074M04GBG	PLBG0196GC-A	Single Cortex-R52	1.0 MB	CAN-FD	Available	Not available
R9A07G074M01GBG	PLBG0196GC-A	Single Cortex-R52	1.0 MB	Classical CAN	Not available	Not available

1.3 Block Diagram

Figure 1.1 shows a block diagram.

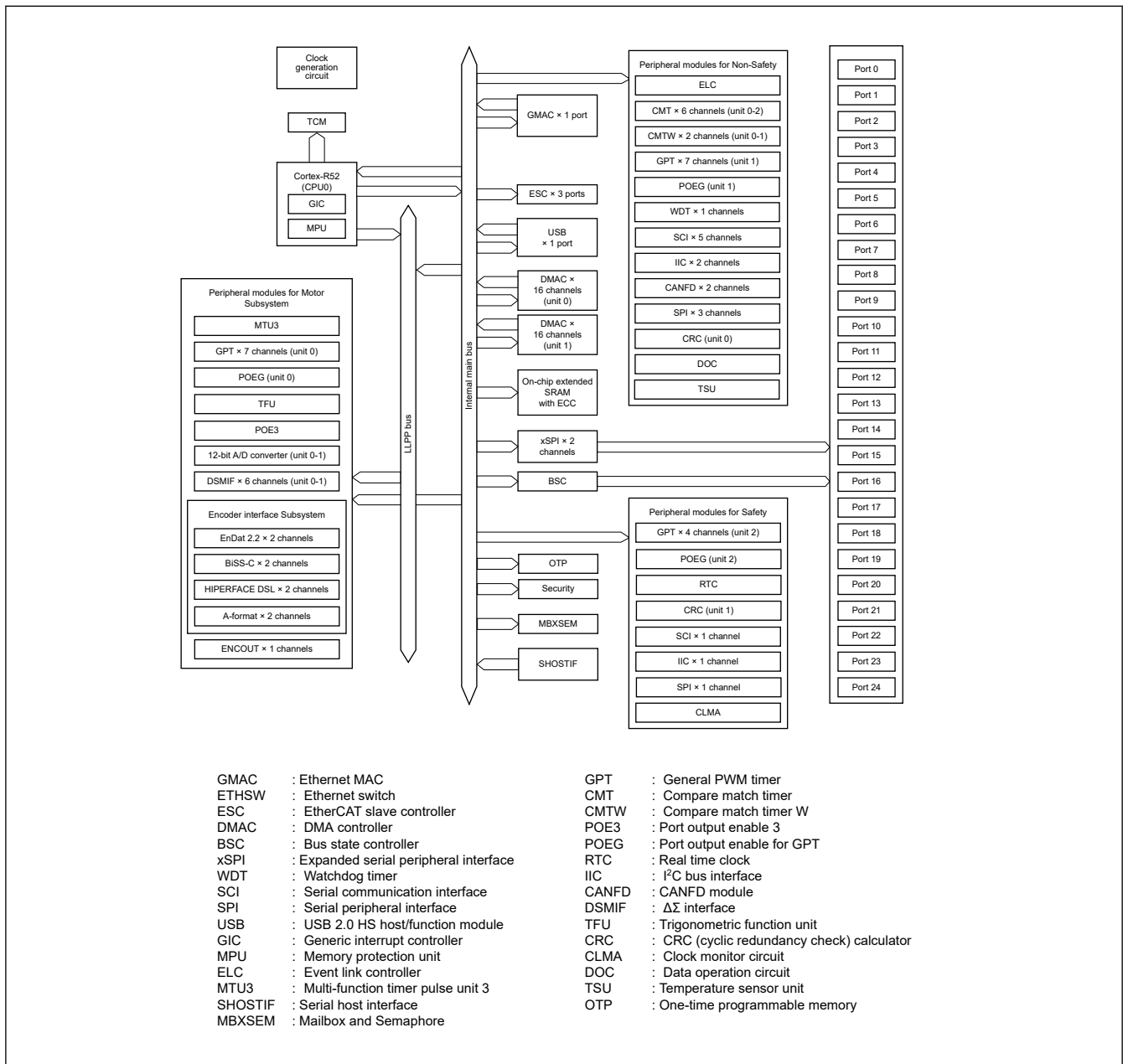


Figure 1.1 Block diagram

1.4 Pin Functions

Table 1.17 lists the pin functions.

Table 1.17 Pin functions (1 of 7)

Classification	Pin name	I/O	Description
Power supply	VDD	Input	Power supply pin. Connect this pin to the system power supply.
	VSS	Input	Ground pin. Connect this pin to the system power supply (0 V).
	VCC1833_2 VCC1833_3	Input	Power supply pin for each I/O domains. (1.8 V or 3.3 V)
	VCC33	Input	Power supply pin for I/O pins.
	VCC18_PLL0, VCC18_PLL1	Input	Power supply pins for the on-chip PLL oscillator
	AVCC18_TSU	Input	Power supply pin for the temperature sensor unit
Clock	XTAL	Output	Connected to a crystal resonator. When external clock signal is used, EXTAL pin should be driven low. XTAL pin should never be driven or loaded by anything other than crystal oscillator. The voltage level of EXTAL must not exceed core VDD (1.16 V).
	EXTAL	Input	
	EXTCLKIN	Input	Inputs the external clock. When a crystal resonator is connected, it should be driven low.
	CKIO	Output	Outputs the external bus clock for external devices.
	ETH0_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 0
	ETH1_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 1
	ETH2_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 2
	RMII0_REFCLK	Output	Outputs 50 MHz clock for RMII0
	RMII1_REFCLK	Output	Outputs 50 MHz clock for RMII1
	RMII2_REFCLK	Output	Outputs 50 MHz clock for RMII2
Operating mode control	MDX	Input	This signal should be driven low.
	MD0 to MD2	Input	Input the operating mode select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDV2, MDV3	Input	Input the operating voltage select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDW	Input	Input the ATCM wait cycle select signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDD	Input	Input the enabling JTAG authentication by hash signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES#	Input	Inputs the reset signal. This MPU enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When boundary scan is not used, this pin should be driven low.
	RSTOUT#	Output	Outputs the reset signal externally

Table 1.17 Pin functions (2 of 7)

Classification	Pin name	I/O	Description
Debugging interface	TRST#	Input	Test reset pin for the on-chip emulator
	TMS	I/O	Test mode select pin for the on-chip emulator Functions as the SWDIO pin in serial wire debug (SWD) mode
	TDI	Input	Test data input pin for the on-chip emulator
	TDO	Output	Test data output pin for the on-chip emulator
	TCK	Input	Test clock pin for the on-chip emulator Functions as the SWCLK pin in serial wire debug (SWD) mode
	TRACECLK	Output	Outputs the clock for synchronization with trace data
	TRACECTL	Output	Outputs the enable signal for trace control
	TRACEDATA0 to TRACEDATA7	Output	Output trace data
Bus state controller (BSC)	A25 to A0	Output	Output the address
	D15 to D0	I/O	Input and output the data
	CS0#, CS2#, CS3#, CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates a read is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates a read or write access
	BS#	Output	Outputs the status signal which indicates the start of the bus cycle
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O interface
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycle
	WE0#	Output	Outputs the write strobe signal to D7 to D0
	WE1#	Output	Outputs the write strobe signal to D15 to D8
	DQMLL	Output	Outputs the data mask enable signal to D7 to D0 when SDRAM is connected
	DQMLU	Output	Outputs the data mask enable signal to D15 to D8 when SDRAM is connected
	RAS#	Output	Outputs the row-address strobe signal to the SDRAM. This pin should be connected to the RAS# pin on the SDRAM.
	CAS#	Output	Outputs the column-address strobe signal to the SDRAM. This pin should be connected to the CAS# pin on the SDRAM.
	CKE	Output	Outputs the clock enable signal to the SDRAM. This pin should be connected to the CKE pin on the SDRAM.
Direct memory access controller (DMAC)	DREQ	Input	Inputs the DMA transfer request signal from the external device
	DACK	Output	Outputs the acknowledge signal which indicates acceptance of the DMA transfer request from the external device
	TEND	Output	Outputs the DMA transfer end signal
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal
	IRQ0 to IRQ15	Input	Input the external interrupt request signal

Table 1.17 Pin functions (3 of 7)

Classification	Pin name	I/O	Description
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	TGRA0 to TGRD0 input capture input, output compare output, and PWM output pins
	MTIOC1A, MTIOC1B	I/O	TGRA1 and TGRB1 input capture input, output compare output, and PWM output pins
	MTIOC2A, MTIOC2B	I/O	TGRA2 and TGRB2 input capture input, output compare output, and PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	TGRA3 to TGRD3 input capture input, output compare output, and PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	TGRA4 to TGRD4 input capture input, output compare output, and PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	TGRU5, TGRV5, and TGRW5 input capture input and dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	External clock input pins for MTU3
Port output enable 3 (POE3)	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input the request signal to place the MTU3 in the high-impedance state
General PWM timer (GPT)/ Port output enable for GPT (POEG)	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input and output-disable request input pins
	GTETRGS A, GTETRGS B	Input	External trigger input and output-disable request input pins (SAFETY)
	GTIOC0A to GTIOC17A, GTIOC0B to GTIOC17B	I/O	Input capture input/output compare output/PWM output pins
	GTADSML0, GTADSML1, GTADSMP0, GTADSMP1	Output	Output pins for monitoring A/D conversion start requests
Compare match timer W (CMTW)	CMTW0_TIC0, CMTW0_TIC1, CMTW1_TIC0, CMTW1_TIC1	Input	CMTW input capture input pins
	CMTW0_TOC0, CMTW0_TOC1, CMTW1_TOC0, CMTW1_TOC1	Output	CMTW output compare output pins
Real time clock (RTC)	RTCAT1HZ	Output	RTC 1 Hz output pin

Table 1.17 Pin functions (4 of 7)

Classification	Pin name	I/O	Description
Serial communication interface (SCI)	SCK0 to SCK5	I/O	Clock I/O pins (clock synchronous mode/simple SPI mode/smart card mode)
	RXD0 to RXD5	Input	Input the receive data (asynchronous mode/clock synchronous mode/smart card mode)
	TXD0 to TXD5	Output	Output the transmit data (asynchronous mode/clock synchronous mode/smart card mode)
	CTS0# to CTS5#	Input	Input the start of transmission (asynchronous mode/clock synchronous mode) active-low
	RTS0# to RTS5#	Output	Output the reception (asynchronous mode/clock synchronous mode) active-low
	SCL0 to SCL5	I/O	Input/output the I2C clocks (simple I2C mode)
	SDA0 to SDA5	I/O	Input/output the I2C data (simple I2C mode)
	MISO0 to MISO5	I/O	Input/output the data for slave transmission (simple SPI mode)
	MOSI0 to MOSI5	I/O	Input/output the data for master transmission (simple SPI mode)
	SS0# to SS5#	Input	Chip-select input pins (simple SPI mode) active-low
	DE0 to DE5	Output	Driver enable output pins (asynchronous mode)
I2C bus interface (IIC)	IIC_SCL0 to IIC_SCL2	I/O	Clock I/O pins
	IIC_SDA0 to IIC_SDA2	I/O	Data I/O pins
Ethernet (RGMII is supported for port-2 only.)	ETH0_TXCLK to ETH2_TXCLK	I/O	TX clock input pins (MII mode) TX clock output pins (RGMII mode)
	ETH0_TXD0 to ETH2_TXD0	Output	TX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_TXD1 to ETH2_TXD1	Output	TX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_TXD2 to ETH2_TXD2	Output	TX data 2 pins (RGMII and MII modes)
	ETH0_TXD3 to ETH2_TXD3	Output	TX data 3 pins (RGMII and MII modes)
	ETH0_TXEN to ETH2_TXEN	Output	TX data enable pins (RMII and MII modes) TX data enable/TX data error (TX_CTL) pins (RGMII mode)
	ETH2_TXER	Output	TX data error pins (MII mode)
	ETH0_RXCLK to ETH2_RXCLK	Input	RX clock pins (RGMII, RMII, and MII modes)
	ETH0_RXD0 to ETH2_RXD0	Input	RX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_RXD1 to ETH2_RXD1	Input	RX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_RXD2 to ETH2_RXD2	Input	RX data 2 pins (RGMII and MII modes)
	ETH0_RXD3 to ETH2_RXD3	Input	RX data 3 pins (RGMII and MII modes)
	ETH0_RXDV to ETH2_RXDV	Input	RX data valid pins (MII mode) Carrier sense/RX data valid (CRS_DV) pins (RMII mode) RX data valid/RX error (RX_CTL) pins (RGMII mode)
	ETH0_RXER to ETH2_RXER	Input	RX data error pins (RMII and MII modes)
	ETH2_CRS	Input	Carrier sense pins (MII mode)
	ETH2_COL	Input	Collision detection pins (MII mode)

Table 1.17 Pin functions (5 of 7)

Classification	Pin name	I/O	Description
Ethernet MAC (GMAC)	GMAC_PTPTRG0	Input	PTP timer trigger external input 0
	GMAC_PTPTRG1	Input	PTP timer trigger external input 1
	GMAC_PTPOUT0 to GMAC_PTPOUT3	Output	PTP timer pulse output
	GMAC_MDC	Output	Management data clock output pin
	GMAC_MDIO	I/O	Management data I/O pin
EtherCAT slave controller (ESC)	ESC_LED RUN	Output	Outputs the EtherCAT RUN LED signal
	ESC_IRQ	Output	Outputs the EtherCAT IRQ signal
	ESC_LED STER	Output	Outputs the EtherCAT Dual-color state LED signal
	ESC_LED ERR	Output	Outputs the EtherCAT error LED signal
	ESC_LINKACT0 to ESC_LINKACT2	Output	Output the EtherCAT link/activity LED signal
	ESC_SYNC0, ESC_SYNC1	Output	Output the EtherCAT SYNC signal
	ESC_LATCH0, ESC_LATCH1	Input	Input the EtherCAT LATCH signal
	ESC_RESETOUT#	Output	Output the EtherCAT reset signal
	ESC_I2CCLK	Output	Outputs the EtherCAT EEPROM I2C clock signal
	ESC_I2CDATA	I/O	Inputs and outputs the EtherCAT EEPROM I2C data signal
	ESC_PHYLINK0 to ESC_PHYLINK2	Input	Inputs the EtherCAT PHY link status signal.
	ESC_MDC	Output	Management data clock output pin
	ESC_MDIO	I/O	Management data I/O pin
	USB 2.0 host/function module	VCC33_USB	Input
VCC18_USB		Input	Power supply input pin for USB
VSS_USB		Input	Ground input pins for USB
AVCC18_USB		Input	Analog power supply input pin for USB
USB_RREF		Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin with 1.8 kΩ (±1%).
USB_DP		I/O	USB bus D+ data I/O pin
USB_DM		I/O	USB bus D- data I/O pin
USB_VBUSEN		Output	Outputs the VBUS power enable signal for USB
USB_OVRCUR		Input	Inputs the overcurrent signal for USB
USB_VBUSIN		Input	USB cable connection/disconnection detection input pin
USB_EXICEN		Output	OTG power supply IC control pin
USB_OTGID		Input	OTG ID pin
CANFD module (CANFD)		CANRX0, CANRX1	Input
	CANTX0, CANTX1	Output	Transmit data output pins
	CANRXDP0, CANRXDP1	Output	Receive data phase output pins
	CANTXDP0, CANTXDP1	Output	Transmit data phase output pins

Table 1.17 Pin functions (6 of 7)

Classification	Pin name	I/O	Description
Serial peripheral interface (SPI)	SPI_RSPCK0 to SPI_RSPCK3	I/O	Clock I/O pins
	SPI_MOSI0 to SPI_MOSI3	I/O	Master transmit data I/O pins
	SPI_MISO0 to SPI_MISO3	I/O	Slave transmit data I/O pins
	SPI_SSL00 to SPI_SSL30	I/O	Slave select signal I/O pins
	SPI_SSL01 to SPI_SSL31, SPI_SSL02 to SPI_SSL32, SPI_SSL03 to SPI_SSL33	Output	Slave select signal output pins
Expanded serial peripheral interface (xSPI)	XSPI0_CKP, XSPI1_CKP, XSPI0_CKN	Output	Clock output pins
	XSPI0_CS0#, XSPI0_CS1#, XSPI1_CS0#	Output	Chip select output pins
	XSPI0_DS, XSPI1_DS	I/O	Read data strobe/write data mask input/output pin
	XSPI0_IO0 to XSPI0_IO7, XSPI1_IO0 to XSPI1_IO7	I/O	Data0 to Data7 input/output pins
	XSPI0_RESET0#, XSPI0_RESET1#	Output	Master reset status output pins
	XSPI0_RSTO0#, XSPI0_RSTO1#	Input	Slave reset status input pins
	XSPI0_INT0#, XSPI0_INT1#	Input	Interrupt input pins
	XSPI0_ECS0#, XSPI0_ECS1#	Input	Error correction status input pins
	XSPI0_WP0#, XSPI0_WP1#	Output	Write protect output pins
$\Delta\Sigma$ interface (DSMIF)	MCLK0 to MCLK5	I/O	Clock I/O pins
	MDAT0 to MDAT5	Input	Data input pins
12-bit A/D converter (ADC12)	AN000 to AN003, AN100 to AN103	Input	Analog input pins for the A/D converter
	ADTRG0#, ADTRG1#	Input	External trigger input pins for the start of A/D conversion
Analog power supply	VCC18_ADC0, VCC18_ADC1	Input	Analog power supply input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
	VREFH0, VREFH1	Input	Reference voltage input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
I/O ports	P00_0 to P24_2	I/O	General-purpose input/output pins
Serial host interface (SHOSTIF)	HSPI_CK	Input	Clock input pin
	HSPI_CS#	Input	Chip select input pin
	HSPI_IO0 to HSPI_IO7	I/O	Data0 to Data7 input/output pins
	HSPI_INT#	Output	Interrupt output pin
Mailbox	MBX_HINT#	Output	Mailbox (Cortex-R52 to Host) interrupt output pin
Encoder I/F common	ENCIFCK0, ENCIFCK1	Output	Encoder I/F clock output pins
	ENCIFOE0, ENCIFOE1	Output	Encoder I/F data output enable pins
	ENCIFDO0, ENCIFDO1	Output	Encoder I/F data output pins
	ENDIFDI0, ENDIFDI1	Input	Encoder I/F data input pins
EnDat 2.2 (ENDAT)	DUEI0, DUEI1	Output	EnDat 2.2 Data transfer
	TST_OUT0, TST_OUT1	Output	EnDat 2.2 Data input after internal synchronization
	SI0#, SI1#	Output	EnDat 2.2 Start pulse

Table 1.17 Pin functions (7 of 7)

Classification	Pin name	I/O	Description
Hiperface DSL (HDSL)	HDSL0_LINK, HDSL1_LINK	Output	HDSL LINK
	HDSL0_SMPL, HDSL1_SMPL	Output	HDSL Test signal line sampler
	HDSL0_CLK1, HDSL1_CLK1	Input	HDSL SPI clock safe 1
	HDSL0_SEL1, HDSL1_SEL1	Input	HDSL SPI selection safe 1
	HDSL0_MISO1, HDSL1_MISO1	Output	HDSL SPI data output safe 1
	HDSL0_MOSI1, HDSL1_MOSI1	Input	HDSL SPI data input safe 1
	HDSL0_CLK2, HDSL1_CLK2	Input	HDSL SPI clock safe 2
	HDSL0_SEL2, HDSL1_SEL2	Input	HDSL SPI selection safe 2
	HDSL0_MISO2, HDSL1_MISO2	Output	HDSL SPI data output safe 2
	HDSL0_MOSI2, HDSL1_MOSI2	Input	HDSL SPI data input safe 2
ENCOUT	POUTA	Output	ENCOUT A-phase output pin
	POUTB	Output	ENCOUT B-phase output pin
	POUTZ	Output	ENCOUT C-phase output pin

1.5 FBGA 196 Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	P01_3	P00_3	P24_1	P22_3	P22_2	P21_6	P21_1	P20_4	VSS	AN100	AN002	AN000	VSS	A
B	P01_7	P01_5	P01_2	P00_1	P23_7	P21_7	P21_5	P21_2	VSS	AN103	AN101	AN001	VSS	P18_6	B
C	P02_1	P01_6	P01_1	P00_2	P24_2	P22_0	P21_3	P20_3	VSS	AN102	AN003	AVCC18_TSU	P18_5	P18_4	C
D	P02_3	P02_0	P01_0	P00_6	P24_0	P22_1	P21_4	VCC33	VREFH1	VREFH0	VSS	P18_2	P18_3	P18_1	D
E	P02_5	P02_2	P02_4	P01_4	P00_0	VCC1833_2	VDD	VDD	VCC18_ADC1	VCC18_ADC0	VSS	P17_4	P17_7	P18_0	E
F	P04_1	P02_7	P02_6	TRST#	VCC33	VDD	VSS	VSS	VDD	VCC33	P17_0	P17_6	P17_3	P17_5	F
G	P06_0	P05_6	P05_5	BSCANP	VDD	VSS	VSS	VSS	VDD	VDD	P16_1	P16_0	P16_2	P16_3	G
H	P06_4	P06_2	P06_1	P05_7	VDD	VSS	VSS	VSS	VDD	VDD	P15_6	P15_5	P15_4	P15_7	H
J	P06_7	P06_5	P06_6	P06_3	VCC33	VDD	VSS	VSS	VDD	VCC1833_3	P15_3	P15_0	P15_1	P15_2	J
K	P07_0	P07_2	P07_3	P07_1	P09_0	VDD	VDD	VDD	VCC33	VCC1833_3	P14_2	P14_7	P14_4	P14_6	K
L	VSS	P08_5	P08_4	P09_4	P10_1	VCC33	P07_4	VDD	P13_2	P13_3	P13_7	P13_5	P14_3	P14_5	L
M	P08_7	P08_6	P09_1	P09_7	P10_2	VSS	MDX	VCC18_PLL1	VSS	VCC33_USB	VSS_USB	P13_4	P13_6	P14_1	M
N	P09_2	P09_3	P09_5	P10_0	RES#	EXT_CLKIN	VSS	VCC18_PLL0	VSS_USB	VSS_USB	AVCC18_USB	VSS_USB	VSS_USB	P14_0	N
P	VSS	P09_6	P10_3	P10_4	VSS	EXTAL	XTAL	VSS	USB_DM	USB_DP	VCC18_USB	USB_RREF	VSS_USB	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 1.2 Pin arrangement (196-pin FBGA) (top view)

Table 1.18 List of pins and pin functions (196-pin FBGA) (1 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
A1	—	VSS	—	—	—	—	—	—	—	—	—
A2	VCC1833_2	—	P01_3	AH#	MTIOC4D / GTIOC3B	ETH2_TXD2	—	IRQ2	—	—	POUTZ

Table 1.18 List of pins and pin functions (196-pin FBGA) (2 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
A3	VCC1833_2	—	P00_3	RD/WR#	MTIC5W	SS2# / CTS2# / RTS2# / ETH2_REFCLK / RMII2_REFCLK	—	IRQ1	—	—	SH1# / HDL1_CLK1
A4	VCC1833_2	—	P24_1	D13 / CAS#	MTIOC0C / POE8# / GTETRG	ETH2_RXCLK	MCLK5	—	—	—	—
A5	—	—	P22_3	D10	MTIOC8D / GTETRGSB	RXD5 / SCL5 / MISO5 / USB_VBUSEN / SPI_SSL00	—	—	—	—	ENCIFDI1
A6	—	TRACECLK	P22_2	D9	MTIOC8C / GTETRGSB	SPI_SSL12	MCLK1	IRQ4	—	—	ENCIFDO1
A7	—	TRACEDATA5	P21_6	D5 / TEND	MTIOC7B / GTIOC16B	CTS0# / ESC_LINKACT0	MDAT2	IRQ9	—	HSPI_IO4	—
A8	—	TRACEDATA0	P21_1	D0	MTIOC6A / GTIOC14A / CMTW0_TIC0	SCK5 / IIC_SCL1 / ESC_SYNC0 / ESC_SYNC1 / SPI_SSL20	MCLK0	—	—	HSPI_INT#	—
A9	—	MDV3	P20_4	—	—	GMAC_PTPOUT0 / ESC_LINKACT1	—	—	—	—	—
A10	—	VSS	—	—	—	—	—	—	—	—	—
A11	—	—	—	—	—	—	—	—	AN100	—	—
A12	—	—	—	—	—	—	—	—	AN002	—	—
A13	—	—	—	—	—	—	—	—	AN000	—	—
A14	—	VSS	—	—	—	—	—	—	—	—	—
B1	—	TRACEDATA1	P01_7	A19	MTIOC1B / GTIOC9B	SCK1 / ETH2_TXER / CANRX0 / SPI_RSPCK3	—	—	ADTRG0#	—	ENCIFOE0
B2	VCC1833_2	—	P01_5	WE0# / DQMLL / CS0#	MTIOC4A / GTIOC2A	ETH2_TXD0 / SPI_RSPCK1	—	—	—	—	TST_OUT0 / HDL0_SMPL
B3	VCC1833_2	—	P01_2	CS2#	MTIOC4B / GTIOC2B	ETH2_TXD3	—	IRQ2	—	—	POUTB
B4	VCC1833_2	—	P00_1	A13	MTIC5U	RXD2 / SCL2 / MISO2 / ETH2_RXDV	MCLK0	IRQ0	—	—	—
B5	VCC1833_2	—	P23_7	D11 / BS	MTIOC0A / GTETRGA	SCK1 / ETH2_RXD0	MCLK4	—	—	—	—
B6	—	TRACEDATA6	P21_7	D6 / DREQ	MTIOC7C / GTIOC17A	DE0	MCLK3	IRQ10	—	HSPI_IO5	—
B7	—	TRACEDATA4	P21_5	D4	MTIOC7A / GTIOC16A / CMTW1_TOC1	CTS5# / SPI_MISO0	MCLK2	IRQ6	ADTRG1#	HSPI_IO3	ENCIFDI0
B8	—	TRACEDATA1	P21_2	D1	MTIOC6B / GTIOC14B / GTIOC15A / CMTW0_TIC1	RXD5 / SCL5 / MISO5 / IIC_SDA1 / ESC_SYNC0 / ESC_SYNC1 / SPI_MISO2	MDAT0	—	—	HSPI_CS#	—
B9	—	VSS	—	—	—	—	—	—	—	—	—
B10	—	—	—	—	—	—	—	—	AN103	—	—
B11	—	—	—	—	—	—	—	—	AN101	—	—
B12	—	—	—	—	—	—	—	—	AN001	—	—
B13	—	VSS	—	—	—	—	—	—	—	—	—
B14	—	TRACECLK	P18_6	A15	MTIC5W	SCK4 / DE4 / IIC_SCL2 / GMAC_PTPOUT2 / SPI_MISO2 / XSPI1_IO7	—	IRQ11	ADTRG0#	HSPI_CK	SI0# / HDL0_CLK1
C1	—	MDW	P02_1	A17	—	DE1 / GMAC_PTPOUT1 / ESC_SYNC0 / ESC_SYNC1	—	—	—	—	HDL0_MISO1

Table 1.18 List of pins and pin functions (196-pin FBGA) (3 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
C2	—	TRACEDATA0	P01_6	A20	MTIOC1A / MTIOC3A / GTIOC0A / GTIOC9A	CTS1# / GMAC_PTPTRG1 / ESC_LATCH1 / ESC_LATCH0 / ESC_PHYLINK0 / CANTXDP1	—	—	—	—	SI0# / HDLSL0_CLK1
C3	VCC1833_2	—	P01_1	CKE	MTIOC3D / GTIOC1B / GTETRGC	DE2 / GMAC_MDC / ESC_MDC / ESC_PHYLINK2	MDAT1	—	—	—	POUTA
C4	VCC1833_2	—	P00_2	RD#	MTIC5V	TXD2 / SDA2 / MOSI2 / ETH2_TXEN / USB_OVRCUR	—	—	—	—	TST_OUT1 / HDLSL0_MOSI2
C5	VCC1833_2	—	P24_2	D14 / RAS#	MTIOC0D / GTETRGD	TXD1 / SDA1 / MOSI1 / ETH2_RXD2	MDAT5	—	—	—	—
C6	—	TRACEDATA7	P22_0	D7	MTIOC7D / GTIOC17B	DE5	MDAT3	IRQ15	—	—	HSPI_IO6
C7	—	TRACEDATA2	P21_3	D2	MTIOC6C / GTIOC14B / GTIOC15A	TXD5 / SDA5 / MOSI5 / ESC_LED RUN / ESC_LED STER / SPI_SSL33	MCLK1	NMI	—	—	HSPI_IO2
C8	—	MDV2	P20_3	—	—	GMAC_PTPOUT1 / ESC_LEDERR / CANTX1	—	—	—	—	—
C9	—	VSS	—	—	—	—	—	—	—	—	—
C10	—	—	—	—	—	—	—	—	AN102	—	—
C11	—	—	—	—	—	—	—	—	AN003	—	—
C12	—	AVCC18_TSU	—	—	—	—	—	—	—	—	—
C13	—	TRACECTL	P18_5	RAS#	MTIC5V	RXD4 / SCL4 / MISO4 / ETH2_COL / CANRX0 / SPI_MOSI2 / XSPI1_IO6	—	—	—	—	HSPI_IO0
C14	—	—	P18_4	CAS#	MTIC5U	TXD4 / SDA4 / MOSI4 / ETH2_RXER / CANTX0 / SPI_RSPCK2 / XSPI1_IO5	—	IRQ1	—	—	HSPI_IO1
D1	—	—	P02_3	A15 / AH#	MTIOC2B / POE11# / GTIOC10B	SS1# / CTS1# / RTS1# / ETH2_COL / CANRX1 / SPI_SSL30	—	IRQ15	—	—	ENCIFD00
D2	—	TRACEDATA2	P02_0	A18	MTIOC3C / GTIOC0B / GTADSMLO	RXD1 / SCL1 / MISO1 / ETH2_CRS / USB_OTGID / CANTX1 / SPI_MISO3	—	IRQ4	—	—	ENCIFCK0
D3	VCC1833_2	—	P01_0	CAS#	MTIOC3C / MTIOC4C / GTIOC0B / GTIOC3A	CTS2# / GMAC_MDIO / ESC_MDIO	MCLK1	IRQ13	—	—	—
D4	VCC1833_2	—	P00_6	CS5#	MTIOC3A / MTIOC3B / GTIOC0A / GTIOC1A	ETH2_TXCLK	MDAT0	—	—	—	—
D5	VCC1833_2	—	P24_0	D12 / CKE / DREQ	MTIOC0B / GTETRGB	RXD1 / SCL1 / MISO1 / ETH2_RXD1	MDAT4	—	—	—	—
D6	—	TRACECTL	P22_1	D8	POE4# / GTETRGB	SS4# / CTS4# / RTS4# / ESC_LINKACT2 / SPI_MOSI0	—	IRQ13	—	—	HSPI_IO7
D7	—	TRACEDATA3	P21_4	D3	MTIOC6D / GTIOC15B	SS5# / CTS5# / RTS5# / GMAC_PTPOUT1 / ESC_SYNC0 / ESC_SYNC1 / SPI_SSL02	MDAT1 / MBX_HINT#	—	—	—	ENCIFD00
D8	—	VCC33	—	—	—	—	—	—	—	—	—

Table 1.18 List of pins and pin functions (196-pin FBGA) (4 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
D9	—	VREFH1	—	—	—	—	—	—	—	—	—
D10	—	VREFH0	—	—	—	—	—	—	—	—	—
D11	—	VSS	—	—	—	—	—	—	—	—	—
D12	—	—	P18_2	BS	MTIOC4B / MTIOC4D / GTIOC2B / GTIOC3B	SCK0 / IIC_SDA2 / GMAC_PTPOUT3 / XSPI1_CS0#	—	—	—	—	—
D13	—	—	P18_3	CKE	MTIOC4B / MTIOC4D / GTIOC2B / GTIOC3B / CMTW1_TIC1	DE3 / ETH2_CRS / CANRXDP1 / XSPI1_IO4	—	IRQ0	—	—	—
D14	—	—	P18_1	WE1# / DQMLU	MTIOC3D / GTIOC1B	SS3# / CTS3# / RTS3#	—	IRQ10	ADTRG1#	—	—
E1	—	TDI	P02_5	WE1# / DQMLU	—	SCK5 / SPI_SSL31	—	—	—	—	—
E2	—	—	P02_2	A16	MTIOC2A / POE10# / GTIOC10A / RTCAT1HZ	TXD1 / SDA1 / MOSI1 / CANTX0 / SPI_MOSI3	—	IRQ14	—	—	ENCIFDI0
E3	—	TDO	P02_4	WE0# / DQMLL	—	DE1 / SPI_SSL33	—	—	—	—	—
E4	VCC1833_2	—	P01_4	WE1# / DQMLU	POE0#	ETH2_TXD1	—	IRQ3	—	—	DUEI0 / HDSL0_LINK
E5	VCC1833_2	—	P00_0	D15	—	SCK2 / DE2 / ETH2_RXD3	—	—	—	—	DUEI1 / HDSL0_SEL1
E6	—	VCC1833_2	—	—	—	—	—	—	—	—	—
E7	—	VDD	—	—	—	—	—	—	—	—	—
E8	—	VDD	—	—	—	—	—	—	—	—	—
E9	—	VCC18_ADC1	—	—	—	—	—	—	—	—	—
E10	—	VCC18_ADC0	—	—	—	—	—	—	—	—	—
E11	—	VSS	—	—	—	—	—	—	—	—	—
E12	—	TRACECLK	P17_4	DACK	MTIOC3C / GTIOC0A / GTETRGB	CTS3# / ETH2_TXER / ESC_PHYLINK2 / SPI_SSL32 / SPI_RSPCK0 / XSPI1_IO3	—	—	—	—	HDSL1_CLK2
E13	—	—	P17_7	RD# / DACK	MTIOC4A / MTIOC4C / GTIOC2A / GTIOC3A	RXD3 / SCL3 / MISO3 / XSPI1_CKP	—	—	—	—	—
E14	—	—	P18_0	WE0# / DQMLL	MTIOC4A / MTIOC4C / GTIOC2A / GTIOC3A	TXD3 / SDA3 / MOSI3 / XSPI1_IO0	—	—	—	—	—
F1	—	—	P04_1	CKIO	—	TXD3 / SDA3 / MOSI3 / IIC_SDA2 / SPI_MOSI0	—	—	—	—	—
F2	—	TCK	P02_7	—	—	TXD5 / SDA5 / MOSI	—	—	—	—	—
F3	—	TMS	P02_6	—	—	RXD5 / SCL5 / MISO5	—	—	—	—	—
F4	—	TRST#	—	—	—	—	—	—	—	—	—
F5	—	VCC33	—	—	—	—	—	—	—	—	—
F6	—	VDD	—	—	—	—	—	—	—	—	—
F7	—	VSS	—	—	—	—	—	—	—	—	—
F8	—	VSS	—	—	—	—	—	—	—	—	—
F9	—	VDD	—	—	—	—	—	—	—	—	—
F10	—	VCC33	—	—	—	—	—	—	—	—	—
F11	—	MDD	P17_0	—	—	SS0# / CTS0# / RTS0# / ESC_IRQ / SPI_SSL01 / XSPI1_IO1	—	—	—	—	HDSL1_MISO2

Table 1.18 List of pins and pin functions (196-pin FBGA) (5 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / PORG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
F12	—	—	P17_6	RD/WR#	MTIOC3B / GTIOC1A	SCK3 / XSPI1_DS	—	—	—	—	—
F13	—	TRACECTL	P17_3	DREQ	POE0# / GTETRGA	CANRX1 / SPI_SSL31 / XSPI1_IO2	—	—	ADTRG1#	—	—
F14	—	RSTOUT#	P17_5	TEND	MTIOC3A / GTIOC0B / GTETRGC	USB_OVRCUR	—	—	—	—	—
G1	—	—	P06_0	A12	GTIOC16A / CMTW1_TOC0	SS4# / CTS4# / RTS4# / ETH1_TXD3 / CANRX1 / SPI_SSL23	—	—	—	—	HDSL0_MOS11
G2	—	—	P05_6	A13	GTIOC14A / CMTW1_TIC0	ETH1_RXER / SPI_SSL22	—	IRQ12	—	—	HDSL1_MOSI2
G3	—	—	P05_5	A14	GTIOC14B / CMTW0_TOC1	ESC_PHYLINK1 / SPI_RSPCK2	—	—	—	—	HDSL1_LINK
G4	—	BSCANP	—	—	—	—	—	—	—	—	—
G5	—	VDD	—	—	—	—	—	—	—	—	—
G6	—	VSS	—	—	—	—	—	—	—	—	—
G7	—	VSS	—	—	—	—	—	—	—	—	—
G8	—	VSS	—	—	—	—	—	—	—	—	—
G9	—	VSS	—	—	—	—	—	—	—	—	—
G10	—	VDD	—	—	—	—	—	—	—	—	—
G11	VCC1833_3	—	P16_1	CS2#	CMTW0_TOC1	RXD0 / SCL0 / MISO0 / SPI_MISO3 / XSPI0_RESET0#	MDAT3	—	ADTRG0#	—	ENCIFOE0 / HDSL1_SEL1
G12	VCC1833_3	—	P16_0	—	—	TXD0 / SDA0 / MOSI0 / ETH2_REFCLK / SPI_MOSI3 / XSPI0_CS1#	MCLK3	—	—	—	ENCIFCK0 / HDSL0_MOSI2
G13	VCC1833_3	—	P16_2	—	—	CTS0# / USB_EXICEN / SPI_RSPCK3 / SPI_SSL03 / XSPI0_RESET1#	—	NMI	—	—	ENCIFCK1 / HDSL1_MISO1
G14	VCC1833_3	—	P16_3	CS3#	GTADSM1	SCK0 / ETH2_RXER / SPI_SSL30 / XSPI0_RSTO0#	—	IRQ7	—	—	ENCIFOE1 / HDSL1_MOSI1
H1	—	—	P06_4	A7	GTIOC11A	ETH1_TXCLK / SPI_MOSI1	—	—	—	—	HDSL0_SEL2
H2	—	MD1	P06_2	A9	—	ETH1_TXD1 / CANRXDP1	—	—	—	—	—
H3	—	—	P06_1	A10	GTIOC16B	CTS4# / ETH1_REFCLK / RMII1_REFCLK / CANTX1 / SPI_SSL22	—	—	—	—	HDSL0_CLK2
H4	—	MD2	P05_7	A11	CMTW1_TOC1	ETH1_TXD2 / SPI_SSL23	—	—	—	—	—
H5	—	VDD	—	—	—	—	—	—	—	—	—
H6	—	VSS	—	—	—	—	—	—	—	—	—
H7	—	VSS	—	—	—	—	—	—	—	—	—
H8	—	VSS	—	—	—	—	—	—	—	—	—
H9	—	VSS	—	—	—	—	—	—	—	—	—
H10	—	VDD	—	—	—	—	—	—	—	—	—
H11	VCC1833_3	—	P15_6	D14	—	SPI_SSL12 / XSPI0_IO7	MDAT2	—	—	—	—
H12	VCC1833_3	—	P15_5	D13	—	XSPI0_IO6	MCLK2	IRQ7	—	—	—
H13	VCC1833_3	—	P15_4	D12	MTIOC8D	XSPI0_IO5	MDAT1	IRQ3	—	—	—
H14	VCC1833_3	—	P15_7	TEND	—	CTS5# / SPI_SSL13 / XSPI0_CS0#	—	—	—	—	—

Table 1.18 List of pins and pin functions (196-pin FBGA) (6 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
J1	—	—	P06_7	A4	GTIOC12B	ETH1_RXD1 / SPI_SSL11	—	—	—	—	DUEI1 / HDL1_LINK
J2	—	—	P06_5	A6	GTIOC11B	ETH1_TXEN / SPI_MISO1	—	—	—	—	HDSL0_MISO2
J3	—	—	P06_6	A5	GTIOC12A	ETH1_RXD0 / SPI_SSL10	—	—	—	—	HDSL1_SMPL
J4	—	MD0	P06_3	A8	—	DE4 / ETH1_TXD0 / CANTXDP1	—	—	—	—	—
J5	—	VCC33	—	—	—	—	—	—	—	—	—
J6	—	VDD	—	—	—	—	—	—	—	—	—
J7	—	VSS	—	—	—	—	—	—	—	—	—
J8	—	VSS	—	—	—	—	—	—	—	—	—
J9	—	VDD	—	—	—	—	—	—	—	—	—
J10	—	VCC1833_3	—	—	—	—	—	—	—	—	—
J11	VCC1833_3	—	P15_3	D11	MTIOC8C	XSPI0_IO4	MCLK1	NMI	—	—	—
J12	VCC1833_3	—	P15_0	A23 / CKE	—	RXD5 / SCL5 / MISO5 / SPI_MOSI1 / XSPI0_IO1	—	—	—	—	—
J13	VCC1833_3	—	P15_1	A24 / CAS#	MTIOC0C	TXD5 / SDA5 / MOSI5 / SPI_SSL10 / XSPI0_IO2	—	—	—	—	—
J14	VCC1833_3	—	P15_2	A25 / RAS#	MTIOC0D	SS5# / CTS5# / RTS5# / SPI_SSL11 / XSPI0_IO3	—	—	—	—	—
K1	—	—	P07_0	A3	GTIOC13A	ETH1_RXD2	—	—	—	—	TST_OUT1 / HDL1_SMPL
K2	—	—	P07_2	A1	GTIOC17A	ETH1_RXDV	—	—	—	—	HDSL1_SEL1
K3	—	—	P07_3	A0	GTIOC17B	ETH1_RXCLK / SPI_SSL00	—	—	—	—	HDSL1_MISO1
K4	—	—	P07_1	A2	GTIOC13B	ETH1_RXD3	—	—	—	—	SI1# / HDL1_CLK1
K5	—	—	P09_0	CS0#	MTIOC4A / MTIOC7A / GTIOC6A	RXD3 / SCL3 / MISO3 / GMAC_MDIO / ESC_MDIO	—	—	—	—	—
K6	—	VDD	—	—	—	—	—	—	—	—	—
K7	—	VDD	—	—	—	—	—	—	—	—	—
K8	—	VDD	—	—	—	—	—	—	—	—	—
K9	—	VCC33	—	—	—	—	—	—	—	—	—
K10	—	VCC1833_3	—	—	—	—	—	—	—	—	—
K11	VCC1833_3	—	P14_2	—	MTIOC8B / GTIOC8B	ETH2_CRS / SPI_SSL10 / XSPI0_ECS0#	—	IRQ6	—	—	POUTA / HDL0_CLK2
K12	VCC1833_3	—	P14_7	A22 / BS	—	SCK5 / SPI_MISO1 / XSPI0_IO0	—	—	—	—	—
K13	VCC1833_3	—	P14_4	BS	MTIOC0B	ESC_IRQ / SPI_SSL13 / XSPI0_DS	—	—	—	—	POUTZ / HDL0_MISO2
K14	VCC1833_3	—	P14_6	A21	—	XSPI0_CKP	—	—	—	—	—
L1	—	VSS	—	—	—	—	—	—	—	—	—
L2	—	—	P08_5	—	MTIOC3C / MTIOC6B / GTIOC5A	RXD2 / SCL2 / MISO2 / ETH0_RXDV	MCLK2	IRQ5	—	—	—
L3	—	—	P08_4	CS5#	MTIOC3A / MTIOC6A / GTIOC4A	SCK2 / ETH0_RXD3 / CANTXDP1 / SPI_SSL32	—	IRQ14	—	—	HDSL1_MOSI1
L4	—	—	P09_4	—	GTADSP0	TXD4 / SDA4 / MOSI4 / ETH0_TXD2 / SPI_SSL21	—	—	—	—	HDSL1_MISO2

Table 1.18 List of pins and pin functions (196-pin FBGA) (7 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
L5	—	—	P10_1	—	POE10#	CTS3# / ETH0_RXD0 / SPI_RSPCK1	—	IRQ10	—	—	ENCIFD1
L6	—	VCC33	—	—	—	—	—	—	—	—	—
L7	—	—	P07_4	—	—	USB_VBUSIN	—	IRQ1	ADTRG0#	—	HDSL1_SEL2
L8	—	VDD	—	—	—	—	—	—	—	—	—
L9	—	TRACEDATA6	P13_2	D9	MTIOC0A / GTIOC10A / POE8#	SS1# / CTS1# / RTS1# / IIC_SCL0 / GMAC_PTPOUT2 / ESC_I2CCLK / SPI_MISO0	MCLK4	IRQ5	—	—	—
L10	—	TRACEDATA7	P13_3	D8 / RD#	MTIOC0B / MTIOC0C / GTIOC10B / CMTW1_TOC0	CTS1# / IIC_SDA0 / GMAC_PTPOUT3 / ESC_I2CDATA / SPI_RSPCK0	MDAT4	—	—	—	—
L11	VCC1833_3	—	P13_7	—	MTCLKC	GMAC_PTPTRG1 / ESC_LATCH0 / ESC_LATCH1 / SPI_MOSI1 / XSPI0_ECS1#	MBX_HINT#	—	—	—	HDSL0_SEL1
L12	VCC1833_3	—	P13_5	—	MTCLKA	IIC_SCL2 / GMAC_PTPTRG0 / ESC_LATCH0 / ESC_LATCH1 / SPI_RSPCK1 / XSPI0_WP1#	—	—	—	—	—
L13	VCC1833_3	—	P14_3	—	MTIOC0A	ETH2_COL / SPI_SSL11 / XSPI0_RSTO1#	—	—	—	—	POUTB / HDSL0_SEL2
L14	VCC1833_3	—	P14_5	CS3#	POE8#	XSPI0_CKN	—	IRQ15	—	HSPI_INT#	—
M1	—	—	P08_7	WAIT#	MTIOC3D / MTIOC6D / GTIOC5B	TXD2 / SDA2 / MOSI2 / GMAC_MDC / ESC_MDC / SPI_SSL13	MDAT2	IRQ8	—	—	—
M2	—	—	P08_6	—	MTIOC3B / MTIOC6C / GTIOC4B / CMTW1_TIC1	SCK3 / ETH0_RXCLK	—	IRQ9	—	—	—
M3	—	—	P09_1	—	MTIOC4C / MTIOC7B / GTIOC7A / GTETRGSA	DE3 / ETH0_REFCLK / RMII0_REFCLK / GMAC_PTPOUT0 / ESC_SYNC0 / ESC_SYNC1 / SPI_SSL10	—	—	—	—	—
M4	—	—	P09_7	DACK	GTIOC15B	RXD4 / SCL4 / MISO4 / ETH0_TXCLK / USB_OVRCUR / CANTXDPO / SPI_SSL00	—	IRQ12	—	—	ENCIFOE1
M5	—	—	P10_2	—	MTIC5U	TXD0 / SDA0 / MOSI0 / ETH0_RXD1	—	—	—	—	—
M6	—	VSS	—	—	—	—	—	—	—	—	—
M7	—	MDX	—	—	—	—	—	—	—	—	—
M8	—	VCC18_PLL1	—	—	—	—	—	—	—	—	—
M9	—	VSS	—	—	—	—	—	—	—	—	—
M10	—	VCC33_USB	—	—	—	—	—	—	—	—	—
M11	—	VSS_USB	—	—	—	—	—	—	—	—	—
M12	—	—	P13_4	A0 / WAIT#	MTIOC0D / GTIOC8B	ESC_RESETOUT# / SPI_SSL12	—	—	—	—	—
M13	VCC1833_3	—	P13_6	—	MTCLKB	GMAC_PTPOUT0 / ESC_SYNC0 / ESC_SYNC1 / XSPI0_WP0#	—	—	—	—	—

Table 1.18 List of pins and pin functions (196-pin FBGA) (8 of 8)

Pin number	I/O power domain	Power supply clock system control	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ESC, USB, CANFD, SPI, xSPI)	DSMIF, Mailbox	Interrupt	ADC12	Host interface (SHOST)	Encoder I/F
M14	VCC1833_3	—	P14_1	—	MTIOC8A / GTIOC8A	GMAC_PTPTRG1 / ESC_LATCH0 / ESC_LATCH1 / SPI_MISO1 / XSPI0_INT1#	—	—	—	—	HDSL0_MOS1
N1	—	—	P09_2	RAS# / DACK	MTIOC4B / MTIOC7C / GTIOC6B / RTCAT1HZ	ETH0_RXER	—	IRQ0	—	—	HDSL1_CLK2
N2	—	—	P09_3	CS3#	MTIOC4D / MTIOC7D / GTIOC7B / GTETRGSB / CMTW0_TOC0	SS5# / CTS5# / RTS5# / ETH0_TXD3 / USB_VBUSEN / CANTXDP0	MCLK3	IRQ12	—	—	HDSL1_SEL2
N3	—	—	P09_5	DREQ	GTADSML1 / CMTW0_TOC0	DE5 / IIC_SCL1 / ETH0_TXD1 / USB_VBUSEN / CANRX0	—	IRQ14	—	—	HDSL1_MOS2
N4	—	—	P10_0	—	POE11# / CMTW0_TIC0	SCK4 / IIC_SDA1 / ETH0_TXEN / USB_EXICEN / CANTX0	—	IRQ15	—	—	ENCIFD01
N5	—	RES#	—	—	—	—	—	—	—	—	—
N6	—	EXTCLKIN	—	—	—	—	—	—	—	—	—
N7	—	VSS	—	—	—	—	—	—	—	—	—
N8	—	VCC18_PLL0	—	—	—	—	—	—	—	—	—
N9	—	VSS_USB	—	—	—	—	—	—	—	—	—
N10	—	VSS_USB	—	—	—	—	—	—	—	—	—
N11	—	AVCC18_USB	—	—	—	—	—	—	—	—	—
N12	—	VSS_USB	—	—	—	—	—	—	—	—	—
N13	—	VSS_USB	—	—	—	—	—	—	—	—	—
N14	VCC1833_3	—	P14_0	—	MTCLKD	GMAC_PTPOUT1 / ESC_SYNC0 / ESC_SYNC1 / XSPI0_INT0#	—	—	—	—	HDSL0_MISO1
P1	—	VSS	—	—	—	—	—	—	—	—	—
P2	—	—	P09_6	—	GTIOC15A / CMTW0_TIC1	CTS5# / ETH0_TXD0 / USB_EXICEN / CANRXDP0	MDAT3	IRQ13	—	—	ENCIFCK1
P3	—	—	P10_3	—	MTIC5V / RTCAT1HZ	RXD0 / SCL0 / MISO0 / ETH0_RXD2	—	IRQ8	—	—	—
P4	—	—	P10_4	D15	MTIC5W	SCK0 / ESC_PHYLINK0 / SPI_SSL01	MBX_HINT#	IRQ11	—	—	—
P5	—	VSS	—	—	—	—	—	—	—	—	—
P6	—	EXTAL	—	—	—	—	—	—	—	—	—
P7	—	XTAL	—	—	—	—	—	—	—	—	—
P8	—	VSS	—	—	—	—	—	—	—	—	—
P9	—	USB_DM	—	—	—	—	—	—	—	—	—
P10	—	USB_DP	—	—	—	—	—	—	—	—	—
P11	—	VCC18_USB	—	—	—	—	—	—	—	—	—
P12	—	USB_RREF	—	—	—	—	—	—	—	—	—
P13	—	VSS_USB	—	—	—	—	—	—	—	—	—
P14	—	VSS	—	—	—	—	—	—	—	—	—

2. Electrical Characteristics

Electrical characteristics of this LSI is defined with the following conditions unless otherwise described.

Conditions:

VDD = 1.05 to 1.15 V

VCC18 = VCC1833_n (1.8-V mode) = VCC18_PLL0 = VCC18_PLL1 = VCC18_USB = AVCC18_USB = VCC18_ADC0 = VCC18_ADC1 = AVCC18_TSU = VREFH0 = VREFH1 = 1.70 to 1.95 V

VCC33 = VCC1833_n (3.3-V mode) = VCC33_USB = 3.135 to 3.465 V

VSS = VSS_USB = 0 V

T_j = -40 to 125°C

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage (3.3-V mode)	VCC33, VCC1833_2, VCC1833_3	-0.3 to +3.8	V
Power supply voltage (1.8-V mode)	(VCC18) VCC1833_2, VCC1833_3	-0.3 to +2.5	V
Power supply voltage	VDD	-0.3 to +1.5	V
Input voltage	V _{in} (3.3-V logic)	-0.3 to VCC33 + 0.3	V
Input voltage	V _{in} (1.8-V logic)	-0.3 to VCC18 + 0.3	V
Analog power supply voltage	VCC18_PLL0, VCC18_PLL1, VCC18_USB, AVCC18_USB, VCC18_ADC0, VCC18_ADC1, AVCC18_TSU*1	-0.3 to smaller value of VCC18*2 + 0.3 or 2.5	V
	VCC33_USB	-0.3 to smaller value of VCC33 + 0.3 or 3.8	V
Voltage difference between power supply pins	VCC33-VCC18	-2.5 to + 2.1	V
Analog input voltage	VAN	-0.3 to smaller value of VCC18_ADC0/1 + 0.3 or 2.5	V
Reference voltage	VREFH0, VREFH1	-0.3 to smaller value of VCC18_ADC0/1 + 0.3 or 2.5	V
Crystal oscillator pins input voltage	XTAL, EXTAL	-0.3 to +1.5	V
Operating temperature (Junction temperature)	T _j	-40 to +125	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note 1. Connect Analog power supply pins to VCC18 when Analog block(s) are not used. Do not leave these pins open.

Note 2. For convention, "VCC18" virtually represents any 1.8-V power supplies of the chip such as VCC1833_n in 1.8-V mode.

Caution: Permanent damage to the LSI might result if absolute maximum ratings are exceeded.

2.2 Power Supply

Table 2.2 Power supply

Parameter	Symbol	Value	Min.	Typ.	Max.	Unit
Power supply voltages	VCC33		3.135	—	3.465	V
	VDD		1.05	1.1	1.15	V
	VSS		—	0	—	V
Power supply voltages supporting multi voltage mode	VCC1833_2, VCC1833_3	3.3-V mode	3.135	3.3	3.465	V
		1.8-V mode (VCC18)	1.70	1.8	1.95	V
Analog power supply voltages	VCC18_PLL0		—	VCC18	—	V
	VCC18_PLL1		—	VCC18	—	V
	VCC33_USB		—	VCC33	—	V
	VCC18_USB		—	VCC18	—	V
	AVCC18_USB		—	VCC18	—	V
	VCC18_ADC0		—	VCC18	—	V
	VCC18_ADC1		—	VCC18	—	V
	AVCC18_TSU		—	VCC18	—	V
	VSS_USB		—	0	—	V

2.3 Power On/Off Sequence

Power on/off sequence and timing are shown in the figure and table below.

For power-up, 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC) must be supplied first, then 3.3-V power (i.e. VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to Low level during the power-up.

For Power-down, 3.3-V power (i.e. VCC33) must go down first and then 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 μ s.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e. RES#) is driven high.

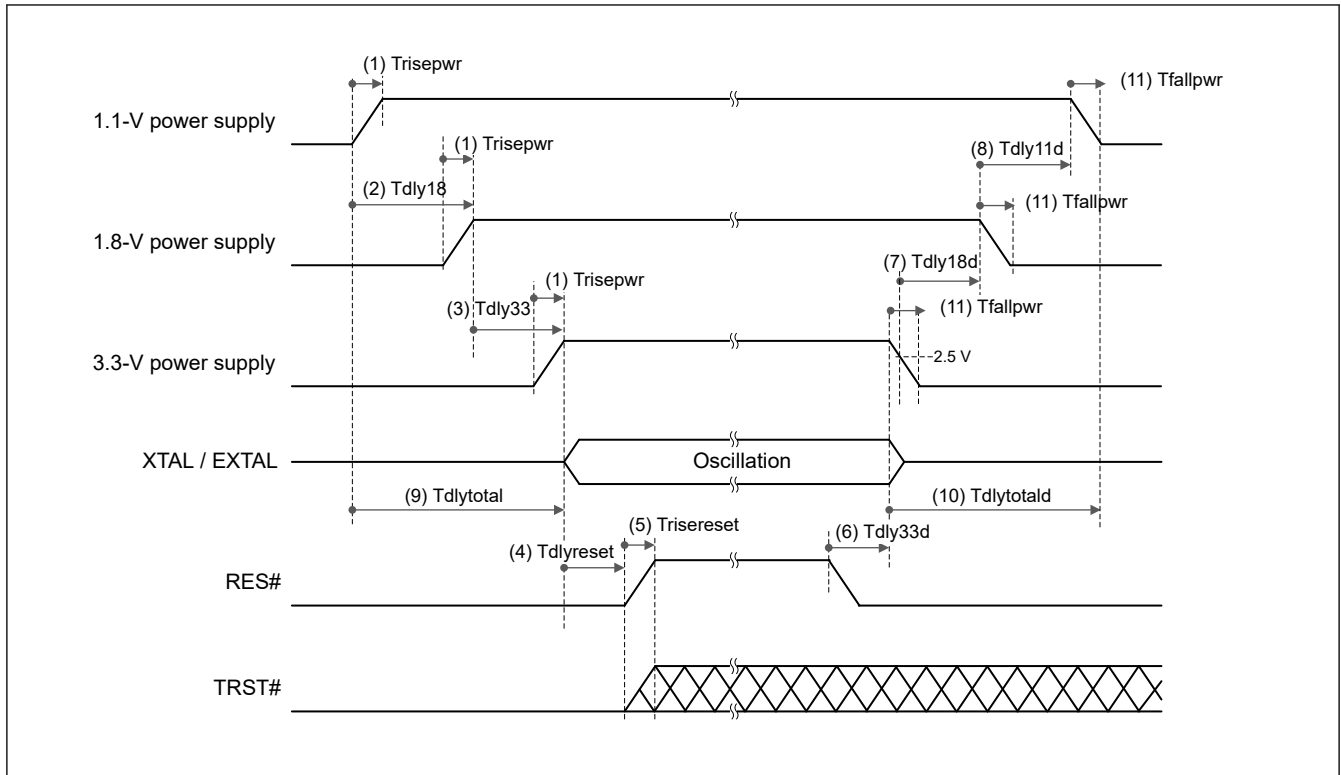


Figure 2.1 Power on/off sequence

Table 2.3 Power on/off sequence timing

No.	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepw	Rising time of the power supply voltage	10 μ s	—	30 ms
(2)	Tdly18	Delay time from start of rising of the 1.1-V power supply voltage to completion of rising of the 1.8-V power supply voltage	0	—	100 ms
(3)	Tdly33	Delay time from completion of rising of the 1.8-V power supply voltage to completion of rising of the 3.3-V power supply voltage	0	—	100 ms
(4)	Tdlyreset	Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES# when XTAL/EXTAL is used.	10 ms	—	—
		Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES# when EXTCLKIN is used.	1 ms	—	—
(5)	Trisereset	Rising time of RES#	—	—	150 μ s
(6)	Tdly33d	Delay time from start of falling of RES# to start of falling of the 3.3-V power supply voltage	10 μ s	—	—
(7)	Tdly18d	Delay time from start of falling time of the 3.3-V power supply voltage to start of falling of the 1.8-V power supply voltage	0	—	100 ms
(8)	Tdly11d	Delay time from start of falling of the 1.8-V power supply voltage to start of falling of the 1.1-V power supply voltage	0	—	100 ms
(9)	Tdlytotal	Startup time of all power supply voltage	—	—	100 ms
(10)	Tdlytotald	Shut down time of all power supply voltage	—	—	100 ms
(11)	Tfallpw	Falling time of the power supply voltage	10 μ s	—	30 ms

2.4 DC Characteristics

Table 2.4 DC Characteristics (3.3-V mode)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH33}	3.3-V mode, Schmitt Trigger Control Disabled, Except P07_4 pin	2.0	—	$V_{CC33} + 0.3$	V
Input Low-level voltage	V_{IL33}		-0.3	—	0.8	V
Positive trigger voltage	V_{T33+}	3.3-V mode, Schmitt Trigger Control Enabled, Except P07_4 pin	0.9	—	2.1	V
Negative trigger voltage	V_{T33-}		0.7	—	1.9	V
Hysteresis voltage	ΔV_{T33}		0.2	—	—	V
Input High-level voltage 2	V_{IH33_2}	3.3-V mode, Schmitt Trigger Control Disabled, P07_4 pin ONLY	$V_{CC33} \times 0.7$	—	$V_{CC33} + 0.3$	V
Input Low-level voltage 2	V_{IL33_2}		-0.3	—	$V_{CC33} \times 0.3$	V
Positive trigger voltage 2	V_{T33+_2}	3.3-V mode, Schmitt Trigger Control Enabled, P07_4 pin ONLY	—	—	$V_{CC33} \times 0.72$	V
Negative trigger voltage 2	V_{T33-_2}		$V_{CC33} \times 0.3$	—	—	V
Hysteresis voltage 2	ΔV_{T33_2}		$V_{CC33} \times 0.1$	—	—	V
Output High-level voltage	V_{OH33}	Low, IOH = -2 mA	$V_{CC33} - 0.4$	—	—	V
	V_{OH33}	Middle, IOH = -4 mA	$V_{CC33} - 0.4$	—	—	V
	V_{OH33}	High, IOH = -8 mA	$V_{CC33} - 0.4$	—	—	V
	V_{OH33}	Ultra High, IOH = -12 mA	$V_{CC33} - 0.4$	—	—	V
Output Low-level voltage	V_{OL33}	Low, IOL = 2 mA	—	—	0.4	V
	V_{OL33}	Middle, IOL = 4 mA	—	—	0.4	V
	V_{OL33}	High, IOL = 8 mA	—	—	0.4	V
	V_{OL33}	Ultra High, IOL = 12 mA	—	—	0.4	V
Input leakage current	$ I_{in} $	$V_{in} = 0\text{ V}, V_{in} = V_{CC33}$	—	—	10	μA
Three-State leakage current (off state)	$ I_{TS} $	$V_{in} = 0\text{ V}, V_{in} = V_{CC33}$	—	—	10	μA
Input Pull-up resistors resistance	R_{pu}	$V_{in} = 0\text{ V}$	15	—	300	k Ω
Input Pull-up resistors current	I_{pu}	$V_{in} = 0\text{ V}$	-220	—	-11	μA
Input Pull-down resistors resistance	R_{pd}	$V_{in} = V_{CC33}$	15	—	300	k Ω
Input Pull-down resistors current	I_{pd}	$V_{in} = V_{CC33}$	11	—	220	μA
Input Capacitance	C_{in}	All input/output and input pins	—	—	10	pF

Table 2.5 DC Characteristics (1.8-V mode) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH18}	1.8-V mode, Schmitt Trigger Control Disabled	$V_{CC18} \times 0.65$	—	$V_{CC18} + 0.3$	V
Input Low-level voltage	V_{IL18}		-0.3	—	$V_{CC18} \times 0.35$	V
Positive trigger voltage	V_{T18+}	1.8-V mode, Schmitt Trigger Control Enabled	$V_{CC18} \times 0.4$	—	$V_{CC18} \times 0.7$	V
Negative trigger voltage	V_{T18-}		$V_{CC18} \times 0.3$	—	$V_{CC18} \times 0.6$	V
Hysteresis voltage	ΔV_{T18}		$V_{CC18} \times 0.1$	—	—	V
Output High-level voltage	V_{OH18}	Low, IOH = -2 mA	$V_{CC18} - 0.45$	—	—	V
	V_{OH18}	Middle, IOH = -4 mA	$V_{CC18} - 0.45$	—	—	V
	V_{OH18}	High, IOH = -8 mA	$V_{CC18} - 0.45$	—	—	V
	V_{OH18}	Ultra High, IOH = -12 mA	$V_{CC18} - 0.45$	—	—	V

Table 2.5 DC Characteristics (1.8-V mode) (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Low-level voltage	V_{OL18}	Low, IOL = 2 mA	—	—	0.45	V
	V_{OL18}	Middle, IOL = 4 mA	—	—	0.45	V
	V_{OL18}	High, IOL = 8 mA	—	—	0.45	V
	V_{OL18}	Ultra High, IOL = 12 mA	—	—	0.45	V
Input leakage current	$ I_{in} $	$V_{in} = 0\text{ V}$, $V_{in} = V_{CC18}$	—	—	10	μA
Three-State leakage current (off state)	$ I_{TSI} $	$V_{in} = 0\text{ V}$, $V_{in} = V_{CC18}$	—	—	10	μA
Input Pull-up resistors resistance	R_{pu}	$V_{in} = 0\text{ V}$	15	—	300	$\text{k}\Omega$
Input Pull-up resistors current	I_{pu}	$V_{in} = 0\text{ V}$	-120	—	-6	μA
Input Pull-down resistors resistance	R_{pd}	$V_{in} = V_{CC18}$	15	—	300	$\text{k}\Omega$
Input Pull-down resistors current	I_{pd}	$V_{in} = V_{CC18}$	6	—	120	μA
Input Capacitance	C_{in}	All input/output and input pins	—	—	10	pF

Table 2.6 USB2.0 USB_RREF Pin

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference resistor*1	R_{REF}	—	—	1.8 ($\pm 1\%$)	—	$\text{k}\Omega$

Note 1. The reference resistor connected to the USB_RREF pin is for external connection to this LSI.

Table 2.7 USB2.0 Pull-Up/Pull-Down Resistors

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
USB_DP pull-up resistor (when the function controller is selected)	R_{PU}	Idle	0.900	—	1.575	$\text{k}\Omega$
		Transmission/reception	1.425	—	3.090	$\text{k}\Omega$
USB_DP/USB_DM pull-down resistors (when the host controller is selected)	R_{PD}	—	14.25	—	24.80	$\text{k}\Omega$

Table 2.8 USB2.0 Host/Function-Related Pins (Low/Full Speed)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high level voltage	V_{FSIH}	—	2.0	—	—	V
Input low level voltage	V_{FSIL}	—	—	—	0.8	V
Differential input sensitivity	V_{FSDI}	$ (USB_DP) - (USB_DM) $	0.2	—	—	V
Differential common mode range	V_{FSCM}	—	0.8	—	2.5	V
Output low level voltage	V_{FSOL}	IFSOL = 2 mA	0.0	—	0.3	V
Output high level voltage	V_{FSOH}	IFSOH = -200 μA	2.8	—	3.6	V
Output signal crossover voltage	V_{FSCRS}	—	1.3	—	2.0	V

Table 2.9 USB2.0 Host/Function-Related Pins (High Speed) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	—	100	—	150	mV
Disconnection detection threshold voltage (differential voltage)	V_{HSDSC}	—	525	—	625	mV
Common mode voltage range	V_{HSCM}	—	-50	—	500	mV
Idle state	V_{HSOI}	—	-10.0	—	10.0	mV
Output high level voltage	V_{HSOH}	—	360	—	440	mV

Table 2.9 USB2.0 Host/Function-Related Pins (High Speed) (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output low level voltage	V_{HSOL}	—	-10.0	—	10.0	mV
Chirp J output voltage (differential)	V_{CHIRPJ}	—	700	—	1100	mV
Chirp K output voltage (differential)	V_{CHIRPK}	—	-900	—	-500	mV

Table 2.10 Supply Current

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Normal operation	I_{vdd}	ICLK = 200 MHz, CPU0CLK = 800 MHz, $T_j \leq 110^\circ\text{C}$	—	—	400	mA
	I_{VCC33}	*1	—	60	—	mA
	$I_{VCC1833_2}$	*1	—	9	—	mA
	$I_{VCC1833_3}$	*1	—	9	—	mA
	I_{VCC18_PLL0}	—	—	—	6	mA
	I_{VCC18_PLL1}	—	—	—	6	mA
	I_{VCC18_USB}	—	—	—	39	mA
	I_{VCC18_ADC0}	—	—	—	3	mA
	I_{VCC18_ADC1}	—	—	—	3	mA
	I_{VCC18_TSU}	—	—	—	2	mA
	I_{VCC33_USB}	—	—	—	6	mA
Low power consumption mode*2	I_{vdd}	All modules inactive	—	12	—	mA
	I_{VCC33}	—	—	9	—	mA
	$I_{VCC1833_2}$	—	—	2	—	mA
	$I_{VCC1833_3}$	—	—	2	—	mA
	I_{VCC18_PLL0}	—	—	3.5	—	mA
	I_{VCC18_PLL1}	—	—	0.1	—	mA
	I_{VCC18_USB}	—	—	0.5	—	mA
	I_{VCC18_ADC0}	—	—	0.2	—	mA
	I_{VCC18_ADC1}	—	—	0.2	—	mA
	I_{VCC18_TSU}	—	—	0.1	—	mA
	I_{VCC33_USB}	—	—	0.3	—	mA

Note: These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.

Note 1. IO supply current (I_{VCC33} , $I_{VCC1833_n}$ (n = 0 to 4)) should be 80 mA or less. (ΣI_{OH} in Table 2.11)

Note 2. All applicable modules are stopped or standby mode with the lowest clock frequency setting, no pull-up/down or operation for all I/O ports, and room temperature.

Table 2.11 Permissible Output Currents

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Permissible output low current (max. value per pin)	IOL	All output pins	—	—	12	mA
Permissible output low current (total)	ΣI_{OL}	Sum of all output pins	—	—	80	mA
Permissible output high current (max. value per pin)	IOH	All output pins	—	—	-12	mA
Permissible output high current (total)	ΣI_{OH}	Sum of all output pins	—	—	-80	mA

Note: All output current values shall be within the values in this table to ensure the reliability of this LSI.

Table 2.12 Thermal Resistance value (Reference)

Item	Symbol	Package	Max.	Unit
Thermal Resistance	Θ_{ja}	196 pin, FBGA 12 × 12 mm, 0.8-mm pitch	25.4	°C/W
	Ψ_{jt}	196 pin, FBGA 12 × 12 mm, 0.8-mm pitch	0.38	°C/W

Note: Package thermal resistance values above are based on EIA/JESD51-9 (2s2p) condition and reference only.

2.5 AC Characteristics

Table 2.13 Operating frequency

Parameter	Symbol	Min.	Max.	Unit	
Operating frequency	CPU clock (CPU0CLK)	f	150 200	600 800	MHz
	System clock (ICLK)		150	200	
	Peripheral module clock H (PCLKH)		150	200	
	Peripheral module clock M (PCLKM)		75	100	
	Peripheral module clock L (PCLKL)		37.5	50	
	Peripheral module clock for ADC (PCLKADC)		18.75	25	
	Peripheral module clock for SCIn (PCLKSCIn, n = 0 to 5)		75	100	
	Peripheral module clock for SPIn (PCLKSPIn, n = 0 to 3)		75	100	
	External bus clock output (CKIO)		18.75	100	
	Ethernet PHY reference clock (ETHn_REFCLK, n = 0 to 2)			25	
	Ethernet PHY reference clock (RMIn_REFCLK, n = 0 to 2)			50	

AC Characteristics are defined in condition of the IO setting (DRCTLm register setting) show in [Table 2.14](#).

Table 2.14 IO setting (DRCTLm register setting) condition (1 of 2)

Module	Signal		IO type	Voltage	DRCTLm register		
					DRVn	SRn	SMTn
Bus	CKIO	SDRAM and High drive	—	3.3 V	High	Fast	—
		Other than the above	—	3.3 V	Middle	Fast	—
	Other than the above		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
DMAC, MTU3, IIC, CANFD, DSMIF	All signals		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
GPT (n = 0 to 17) (m = 0, 1)	GTIOCnA, GTIOCnB		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
	GTADSMLm, GTADSMPm		—	3.3 V	Low	Slow	Disable
SCI, SPI	All signals		—	3.3 V	High	Fast	Disable
xSPI (n = 0, 1; m = 0, 1)	XSPIIn_CKP, XSPI0_CKN, XSPIIn_IO[7:0], XSPIIn_CSm#, XSPIIn_DS		—	1.8 V*1	High	Fast	Disable
			—	3.3 V	High	Fast	Enable
	Other than the above		—	—	Low	Slow	Disable

Table 2.14 IO setting (DRCTLm register setting) condition (2 of 2)

Module	Signal	IO type	Voltage	DRCTLm register		
				DRVn	SRn	SMTn
Ethernet Interface (n = 0 to 2)	ETHn_TXCLK, ETHn_TXD[3:0]	—	1.8 V ¹ /3.3 V	High	Fast	Disable
	ETH2_TXER	—	3.3 V	Middle	Fast	—
	ETHn_RXCLK, ETHn_RXD[3:0]	—	1.8 V ¹ /3.3 V	—	—	Disable
	ETHn_RXER, ETH2_COL, ETH2_CRS	—	3.3 V	—	—	Disable
	ETHn_REFCLK, RMIIn_REFCLK	—	3.3 V	High	Fast	—
	Other than the above	—	—	Low	Slow	Disable
SHOSTIF	HSPI_CK, HSPI_CS#, HSPI_IO[7:0]	—	3.3 V	High	Fast	Disable
	HSPI_INT#	—	3.3 V	Low	Slow	Disable
Debug Interface	TRACECLK, TRACECTL, TRACEDATA[7:0], TDO, TMS	—	3.3 V	High	Fast	Disable
	Other than the above	—	—	Low	Slow	Disable
Other than the above	—	—	—	Low	Slow	Disable

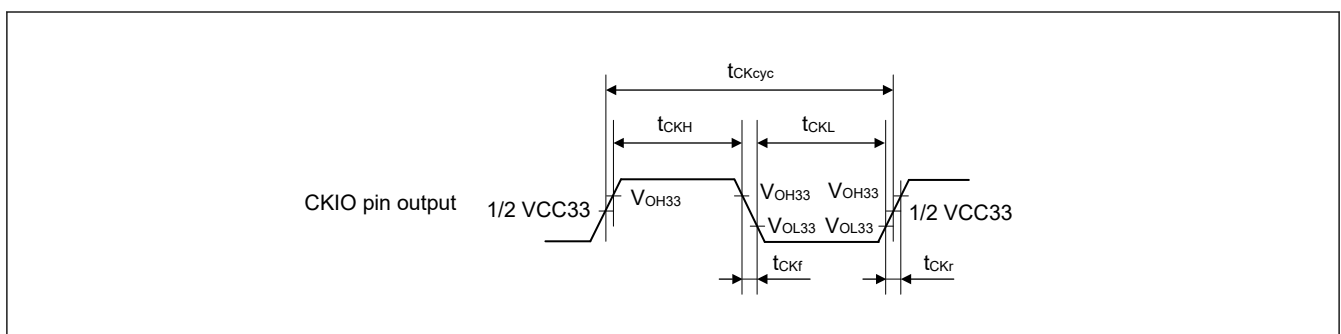
Note 1. 1.8 V is only supported for xSPI0 and Ethernet port 2 (ETH2_).

2.5.1 Clock Timing

2.5.1.1 CKIO Pin Output Timing

Table 2.15 CKIO pin output timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CKIO pin output cycle time	t_{CKcyc}	Figure 2.2	10	—	53.4	ns
CKIO pin output high level pulse width	t_{CKH}		$t_{CKcyc} / 2 - t_{CKr}$	—	—	ns
CKIO pin output low level pulse width	t_{CKL}		$t_{CKcyc} / 2 - t_{CKf}$	—	—	ns
CKIO pin output rising time 1	t_{CKr}	CKIO: High drive output Setting	—	—	3.8	ns
CKIO pin output falling time 1	t_{CKf}	CKIO: High drive output Setting	—	—	3.8	ns
CKIO pin output rising time 2	t_{CKr}	CKIO: Normal output setting	—	—	9	ns
CKIO pin output falling time 2	t_{CKf}	CKIO: Normal output setting	—	—	9	ns

**Figure 2.2 CKIO pin output timing**

2.5.1.2 Ethernet PHY Reference Clock Output Timing

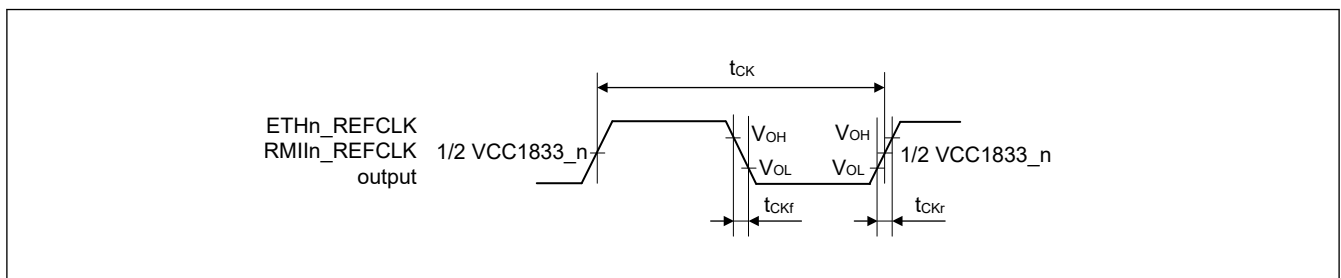
Conditions:

C = 30 pF (ETHn_REFCLK)

C = 20 pF (RMIIn_REFCLK)

Table 2.16 Ethernet PHY reference clock output timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ETHn_REFCLK cycle time	t_{CK}	Figure 2.3	40	—	—	ns
ETHn_REFCLK frequency	—		25.00 ± 50 ppm			MHz
ETHn_REFCLK duty	—		45	—	55	%
ETHn_REFCLK rising/falling time	t_{CKr} / t_{CKf}		0.5	—	4.0	ns
RMIIIn_REFCLK cycle time	t_{CK}		20	—	—	ns
RMIIIn_REFCLK frequency	—		50.00 ± 50 ppm			MHz
RMIIIn_REFCLK duty	—		45	—	55	%
RMIIIn_REFCLK rising/falling time	t_{CKr} / t_{CKf}		0.5	—	3.5	ns

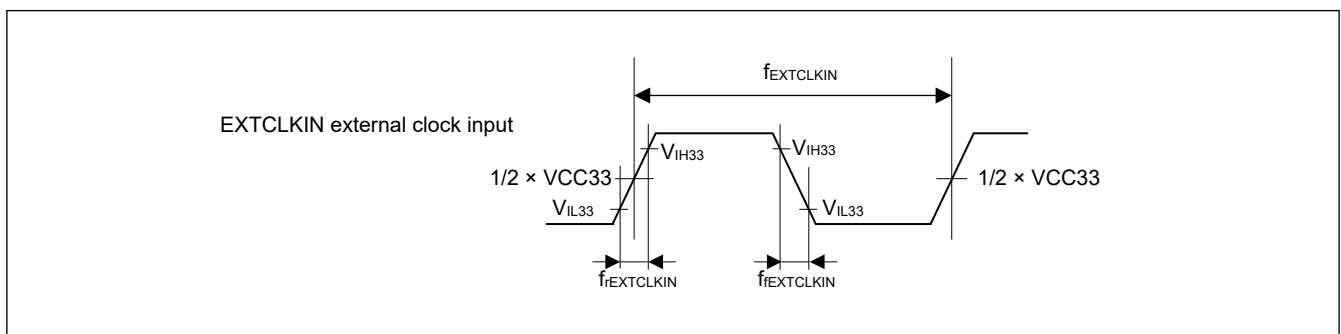
**Figure 2.3 Ethernet PHY reference clock output timing**

2.5.1.3 EXTCLKIN External Clock Input

Table 2.17 EXTCLKIN clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTCLKIN external clock frequency	$f_{EXTCLKIN}$	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
EXTCLKIN duty	$r_{EXTCLKIN}$	—	±5%			—
EXTCLKIN rising time	$t_{EXTCLKIN}$	—	0	—	5	ns
EXTCLKIN falling time	$t_{EXTCLKIN}$	—	0	—	5	ns

Note: When using crystal resonator (i.e. EXTA/XTAL clock is used), EXTCLKIN should be driven low.

**Figure 2.4 EXTCLKIN external clock input timing**

2.5.1.4 EXTAL/XTAL Clock Timing

Table 2.18 EXTAL/XTAL clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTAL/XTAL clock frequency*1	f_{XTAL}	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz

Note: When using an external oscillator, be sure to leave XTAL open-circuit and make sure that EXTAL is driven low.

Note 1. When using the EXTAL/XTAL clock (i.e. crystal resonator), ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.

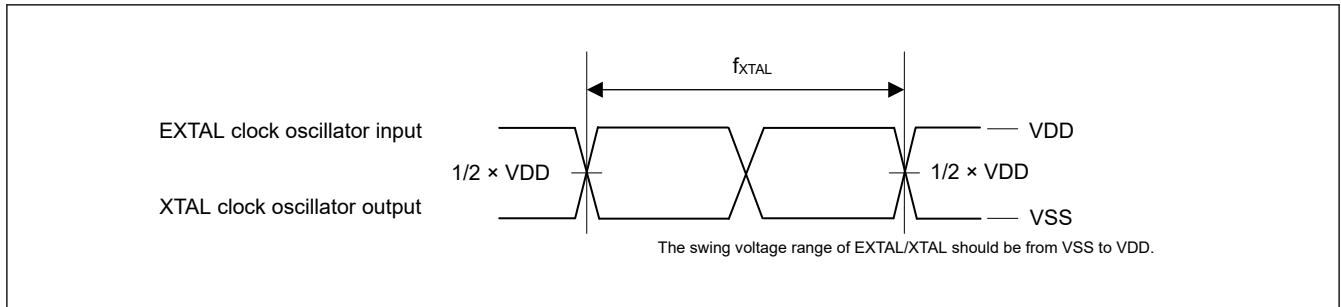


Figure 2.5 EXTAL clock oscillator input and XTAL clock oscillator output timing

2.5.1.5 LOCO Clock Timing

Table 2.19 LOCO clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOCO clock cycle time	t_{Lcyc}	—	4.62	4.17	3.79	μ s
LOCO clock oscillation frequency	t_{LOCO}	—	216	240	264	kHz
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	—	40	μ s

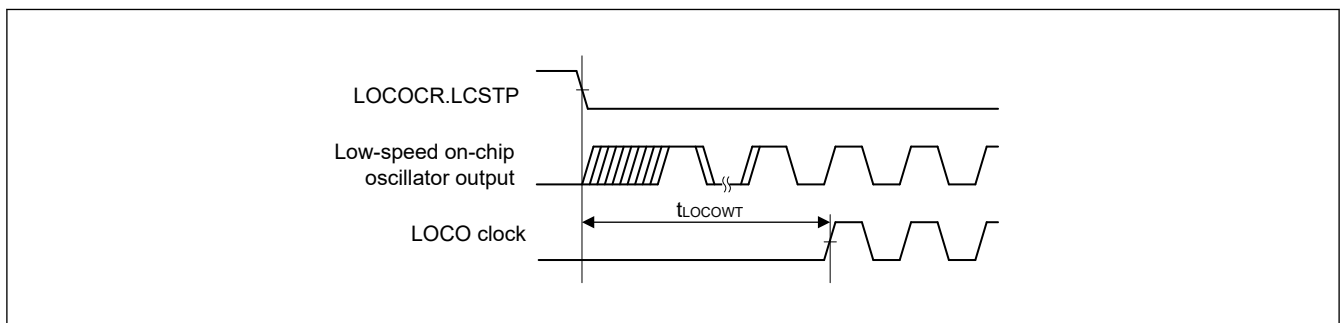


Figure 2.6 LOCO clock oscillation start timing

2.5.2 Reset, Interrupt, and Mode Timing

Table 2.20 Reset, interrupt, and mode timing (1 of 2)

Parameter	Symbol	Conditions	Min.*1	Typ.	Max.	Unit
RES# pulse width	At power on	$t_{dlyreset}$	10	—	—	ms
	Other than above	$t_{dlyreset2}$	1	—	—	ms
RES# rising time	$t_{risereset}$	Figure 2.7	—	—	150	μ s
TRST# pulse width	At power on	$t_{dlyreset}$	10	—	—	ms
	Other than above	$t_{dlyreset2}$	1	—	—	ms
TRST# rising time	$t_{risereset}$	Figure 2.7	—	—	150	μ s

Table 2.20 Reset, interrupt, and mode timing (2 of 2)

Parameter	Symbol	Conditions	Min.*1	Typ.	Max.	Unit
NMI pulse width	t_{NMIW}	Figure 2.8	$t_{cyc} \times 2$	—	—	ns
IRQ pulse width	t_{IRQW}	Figure 2.9	$t_{cyc} \times 2$	—	—	ns
Mode hold time (to RES#)	At power on t_{MDH}	Figure 2.10	250	—	—	ns

Note 1. t_{cyc} : ICLK cycle

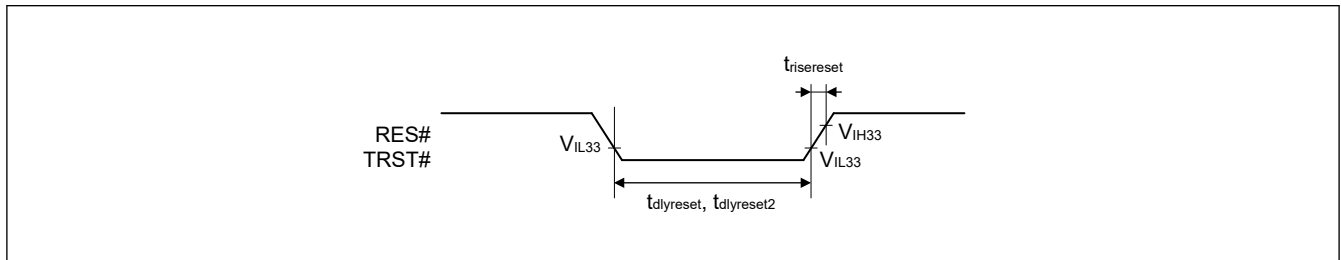


Figure 2.7 Reset input timing

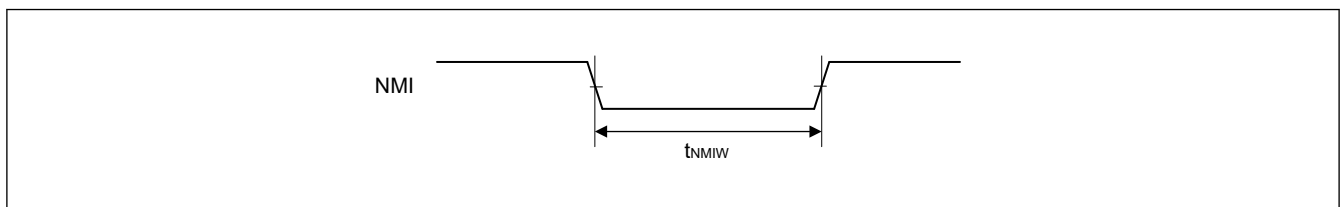


Figure 2.8 NMI interrupt input timing

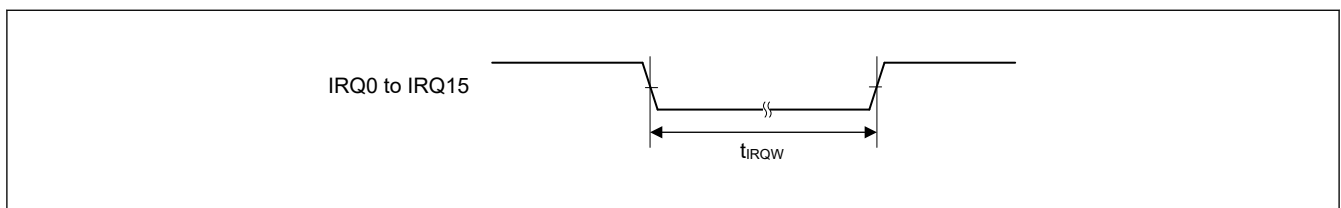


Figure 2.9 IRQ interrupt input timing

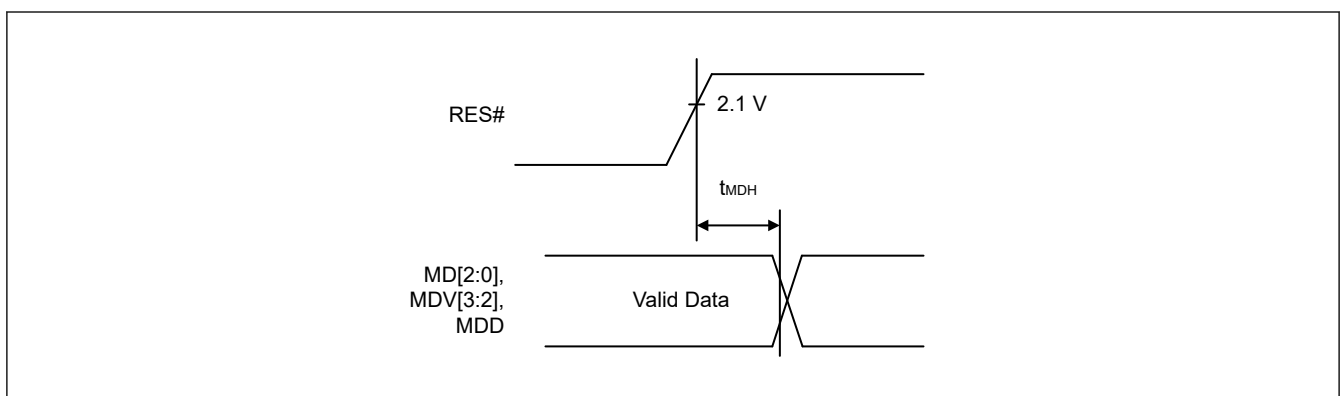


Figure 2.10 Mode input timing

2.5.3 Bus Timing

Table 2.21 Bus timing (1 of 2)Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 15$ pF (CKIO), 30 pF (others), $T_{jmin} = -40^{\circ}\text{C}$

Parameter	Symbol	CKIO = $1/t_{CKcyc}^{*1}$ (Max 66 MHz)		Unit	Reference Figure	
		Min.	Max.			
Address delay time 1	SDRAM*2	t_{AD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 10$	ns	Figure 2.18
Address setup time		t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time		t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Address hold time		t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time		t_{BSD}	—	11	ns	Figure 2.11 to Figure 2.32
CSn# delay time 1	SDRAM*2	t_{CSD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Read/write delay time 1	SDRAM*2	t_{RWD1}	2	11	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	10	ns	
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 10$	ns	Figure 2.11 to Figure 2.18
Read data setup time 1*3	High-drive output	t_{RDS1}	$1/2t_{CKcyc} + 4$	—	ns	Figure 2.11 to Figure 2.17
	Normal output		$1/2t_{CKcyc} + 7$	—	ns	
Read data setup time 2*3	High-drive output	t_{RDS2}	6.6	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data setup time 3*3	High-drive output	t_{RDS3}	$1/2t_{CKcyc} + 4$	—	ns	Figure 2.18
	Normal output		$1/2t_{CKcyc} + 7$	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 2		t_{RDH2}	2.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 10$	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2		t_{WED2}	—	11	ns	Figure 2.17
Write data delay time 1		t_{WDD1}	—	11	ns	Figure 2.11 to Figure 2.17
Write data delay time 2		t_{WDD2}	—	11	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 2		t_{WDH2}	2	—	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time*3	High-drive output	t_{WTS}	$1/2t_{CKcyc} + 4.5$	—	ns	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc} + 8$	—	ns	
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc} + 3.5$	—	ns	Figure 2.12 to Figure 2.18
RAS# delay time 1		t_{RASD1}	2	11	ns	Figure 2.19 to Figure 2.35
CAS# delay time 1		t_{CASD1}	2	11	ns	Figure 2.19 to Figure 2.35

Table 2.21 Bus timing (2 of 2)Conditions: $V_{OH} = VCC33 \times 0.5$, $V_{OL} = VCC33 \times 0.5$, $C = 15$ pF (CKIO), 30 pF (others), $T_{jmin} = -40^{\circ}C$

Parameter	Symbol	CKIO = $1/t_{CKcyc}^{*1}$ (Max 66 MHz)		Unit	Reference Figure
		Min.	Max.		
DQM delay time 1	t_{DQMD1}	2	11	ns	Figure 2.19 to Figure 2.32
CKE delay time 1	t_{CKED1}	2	11	ns	Figure 2.34
AH# delay time	t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 10$	ns	Figure 2.15
Multiplex address delay time	t_{MAD}	—	10	ns	Figure 2.15
Multiplex address hold time	t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#	t_{AVVH}	$1/2t_{CKcyc} - 2$	—	ns	Figure 2.15
DACK/TEND delay time	t_{DADC}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.32

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

Note 2. These are values when SDRAM (CSnBCR.TYPE[2:0] = 100b) is selected in the CSn space bus control register (CSnBCR) and high-drive output is selected for CKIO.

Note 3. These are values when high-drive output and normal output are respectively selected for CKIO.

Table 2.22 Bus timing (1 of 2)Conditions: $V_{OH} = VCC33 \times 0.5$, $V_{OL} = VCC33 \times 0.5$, $C = 12$ pF (CKIO), 12 pF (others), $T_{jmin} = -20^{\circ}C$

Parameter	Symbol	CKIO = $1/t_{CKcyc}^{*1}$ (Max 100 MHz)		Unit	Reference Figure	
		Min.	Max.			
Address delay time 1	SDRAM*2	t_{AD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Address delay time 2	t_{AD2}	$1/2t_{CKcyc} - 0.5$	$1/2t_{CKcyc} + 8$	ns	Figure 2.18	
Address setup time	t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18	
Chip enable setup time	t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18	
Address hold time	t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14	
BS delay time	t_{BSD}	—	8	ns	Figure 2.11 to Figure 2.32	
CSn# delay time 1	SDRAM*2	t_{CSD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Read/write delay time 1	SDRAM*2	t_{RWD1}	1.3	8	ns	Figure 2.11 to Figure 2.35
	Other than the above		0	8	ns	
Read strobe delay time	t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 8$	ns	Figure 2.11 to Figure 2.18	
Read data setup time 1*3	High-drive output	t_{RDS1}	$1/2t_{CKcyc} + 4.5$	—	ns	Figure 2.11 to Figure 2.17
	Normal output		$1/2t_{CKcyc} + 7$	—	ns	
Read data setup time 2*3	High-drive output	t_{RDS2}	3.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data setup time 3*3	High-drive output	t_{RDS3}	$1/2t_{CKcyc} + 4.5$	—	ns	Figure 2.18
	Normal output		$1/2t_{CKcyc} + 7$	—	ns	
Read data hold time 1	t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17	

Table 2.22 Bus timing (2 of 2)Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 12$ pF (CKIO), 12 pF (others), $T_{jmin} = -20^{\circ}\text{C}$

Parameter	Symbol	CKIO = $1/t_{CKcyc}^{*1}$ (Max 100 MHz)		Unit	Reference Figure
		Min.	Max.		
Read data hold time 2	t_{RDH2}	2.5	—	ns	Figure 2.19 to Figure 2.22, Figure 2.27 to Figure 2.29
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1	t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 8$	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2	t_{WED2}	—	9	ns	Figure 2.17
Write data delay time 1	t_{WDD1}	—	8	ns	Figure 2.11 to Figure 2.17
Write data delay time 2	t_{WDD2}	—	8	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 1	t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 2	t_{WDH2}	1.3	—	ns	Figure 2.23 to Figure 2.26, Figure 2.30 to Figure 2.32
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time ^{*3}	High-drive output	t_{WTS}	$1/2t_{CKcyc} + 4.5$	—	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc} + 8$	—	
WAIT# hold time	t_{WTH}	$1/2t_{CKcyc} + 3.5$	—	ns	Figure 2.12 to Figure 2.18
RAS# delay time 1	t_{RASD1}	1.3	8	ns	Figure 2.19 to Figure 2.35
CAS# delay time 1	t_{CASD1}	1.3	8	ns	Figure 2.19 to Figure 2.35
DQM delay time 1	t_{DQMD1}	1.3	8	ns	Figure 2.19 to Figure 2.32
CKE delay time 1	t_{CKED1}	1.3	8	ns	Figure 2.34
AH# delay time	t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc} + 8$	ns	Figure 2.15
Multiplex address delay time	t_{MAD}	—	8	ns	Figure 2.15
Multiplex address hold time	t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#	t_{AVVH}	$1/2t_{CKcyc} - 2$	—	ns	Figure 2.15
DACK/TEND delay time	t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.32

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the f_{max} value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

Note 2. These are values when SDRAM (CSnBCR.TYPE[2:0] = 100b) is selected in the CSn space bus control register (CSnBCR) and high-drive output is selected for CKIO.

Note 3. These are values when high-drive output and normal output are respectively selected for CKIO.

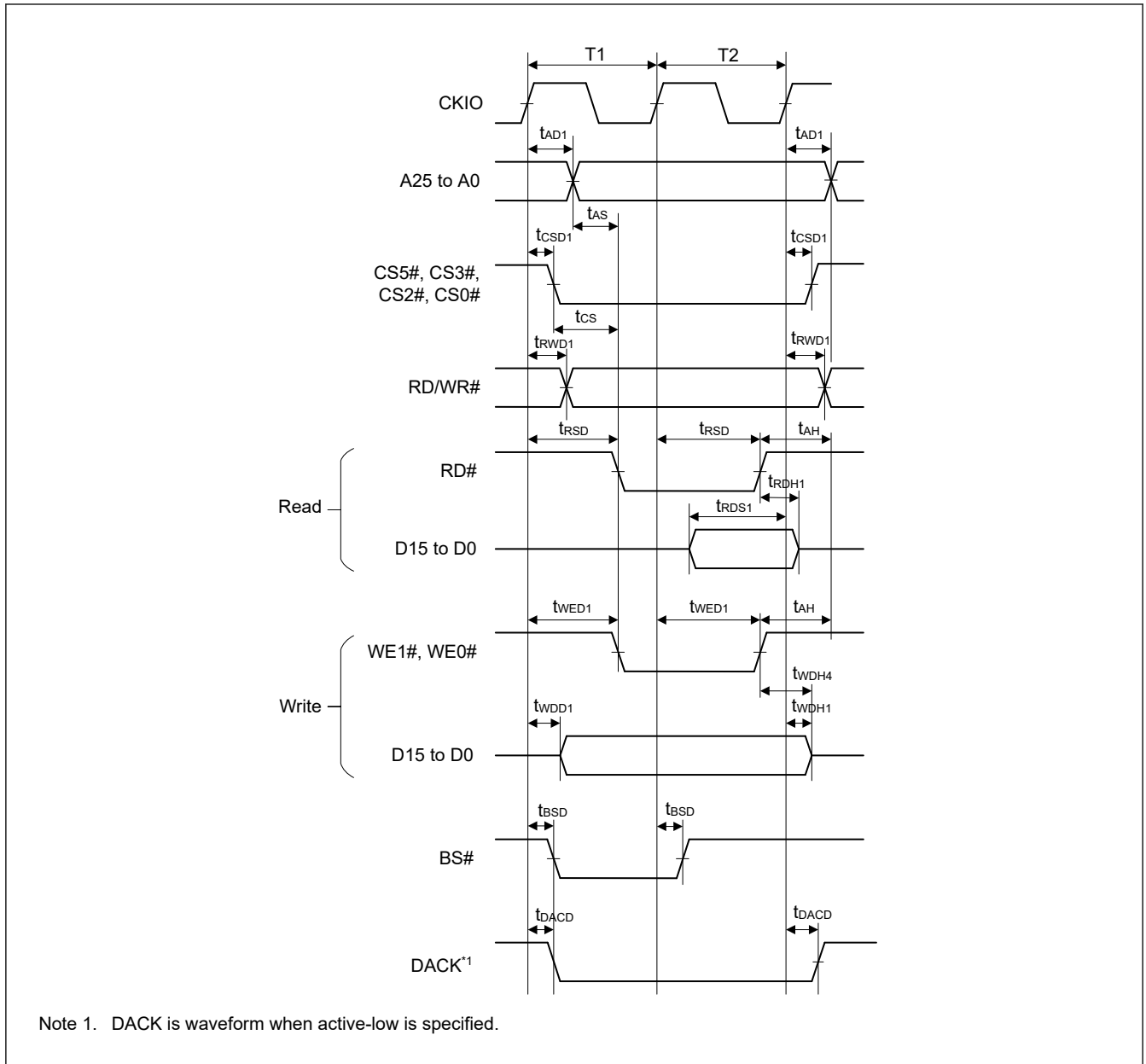


Figure 2.11 SRAM interface basic bus cycle (no wait)

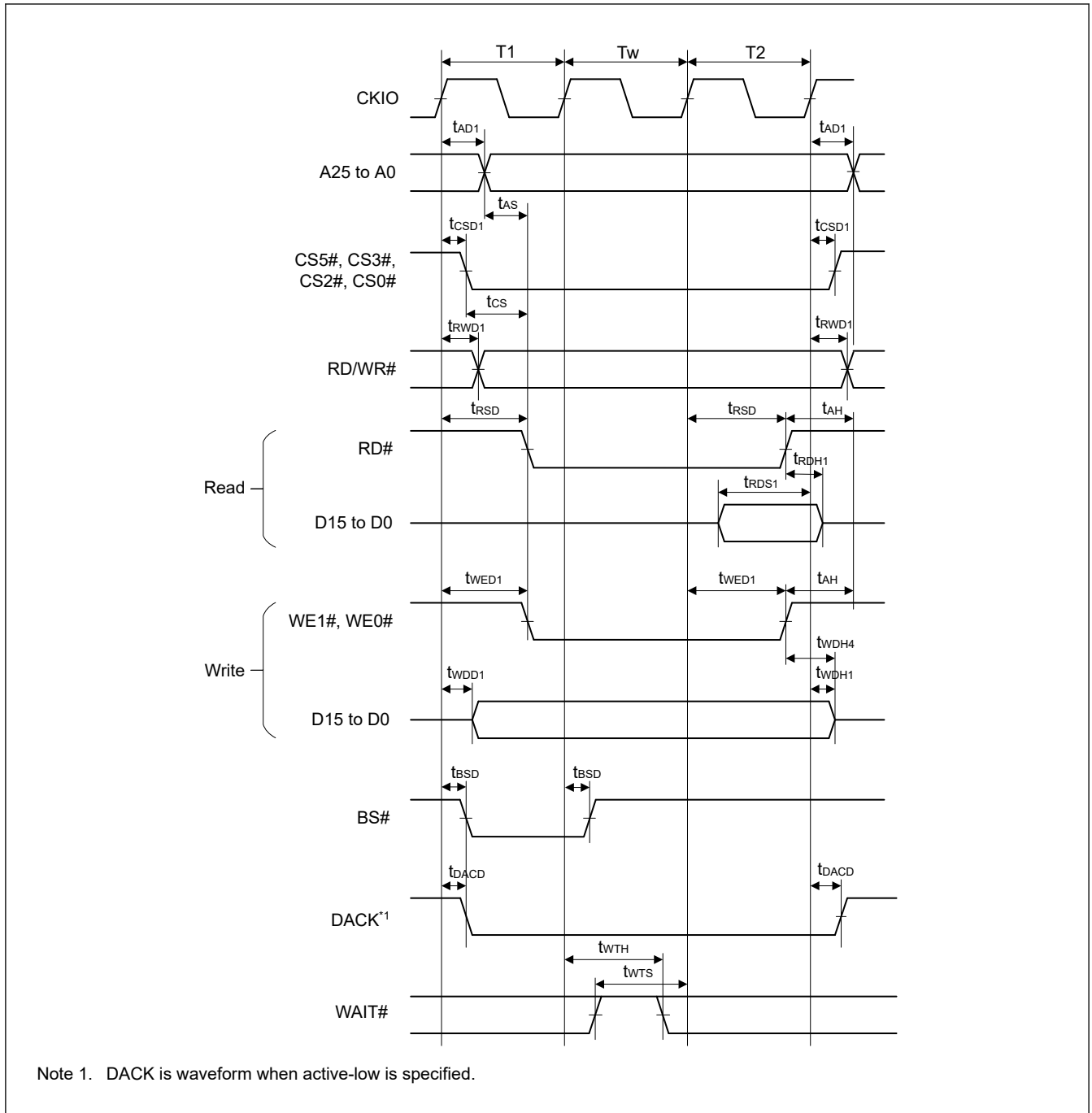


Figure 2.12 SRAM interface basic bus cycle (software wait 1)

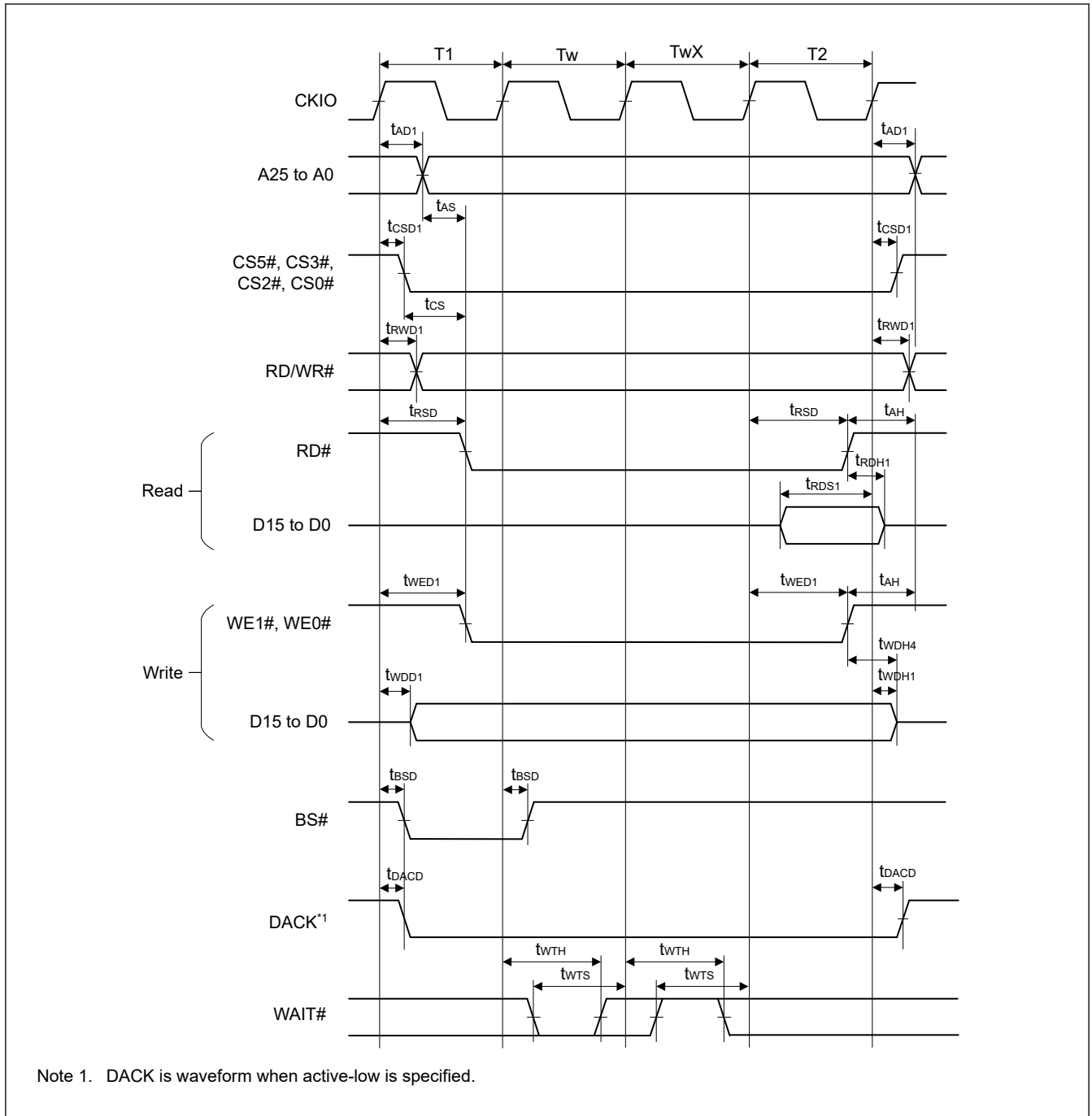


Figure 2.13 SRAM interface basic bus cycle (software wait 1, external wait 1 inserted)

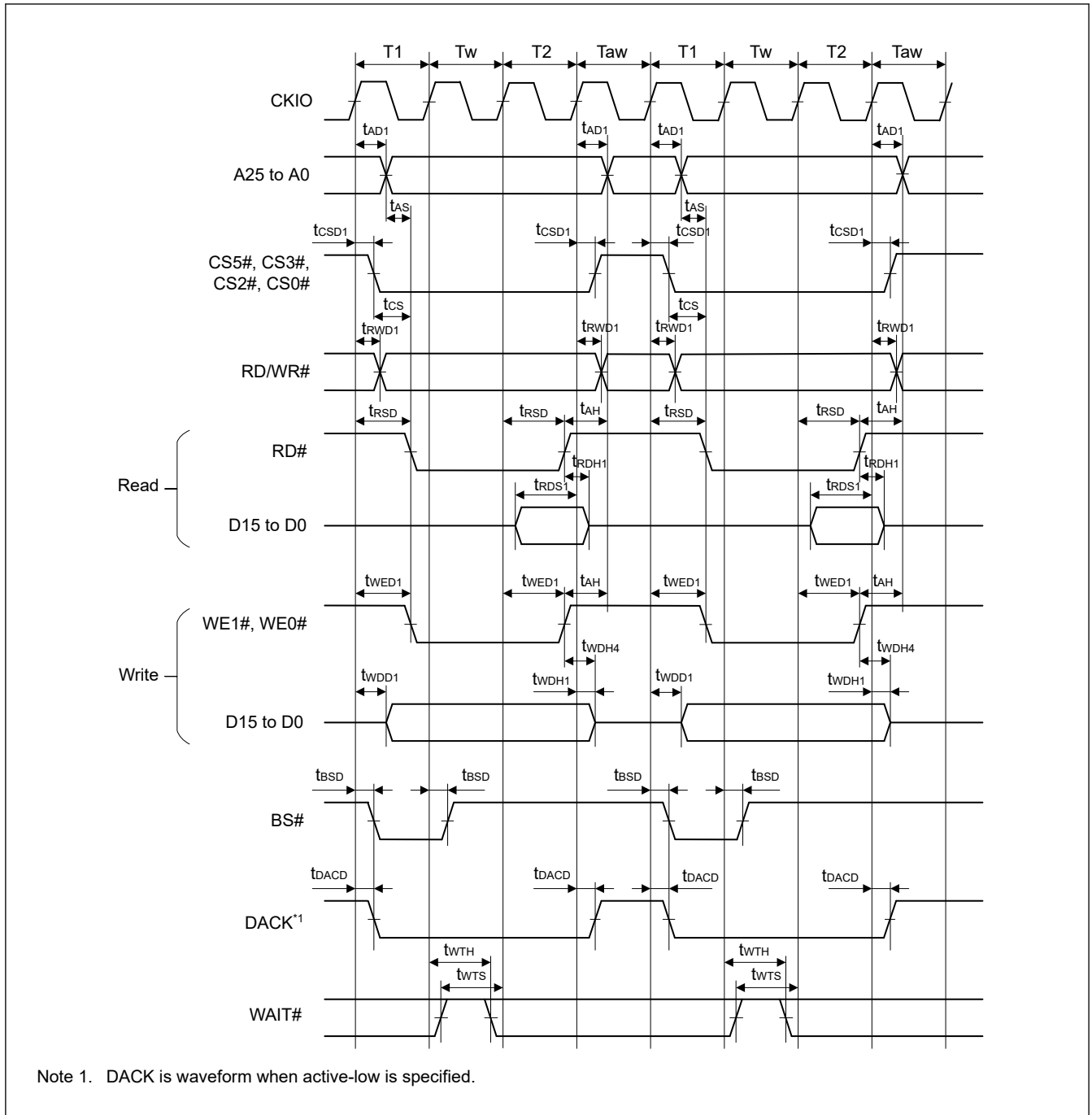
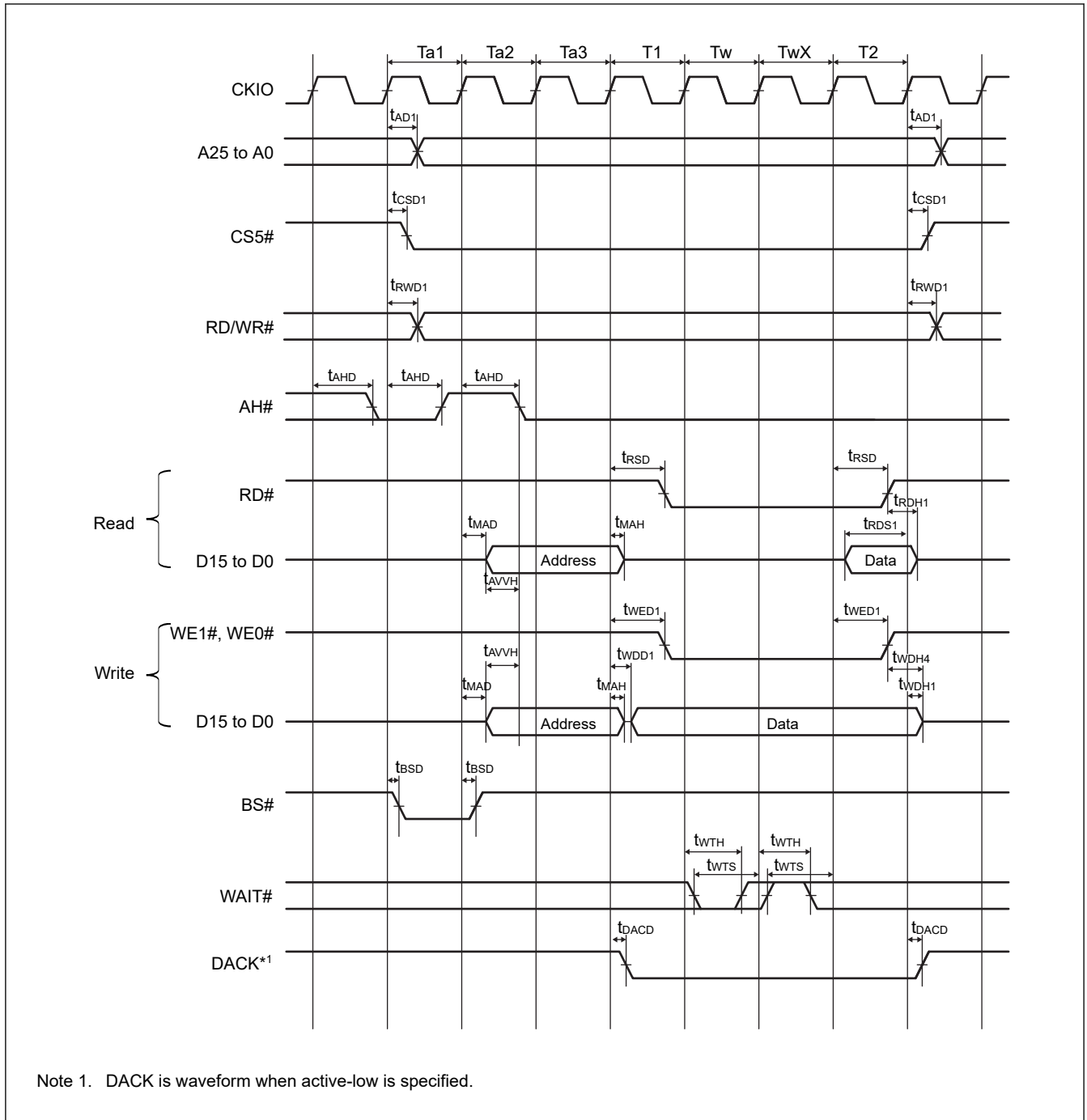


Figure 2.14 SRAM interface basic bus cycle (software wait 1, external wait enabled (WM = 0), no idle cycle)



Note 1. DACK is waveform when active-low is specified.

Figure 2.15 MPX-I/O interface bus cycle (address cycle 3, software wait 1, external wait 1 inserted)

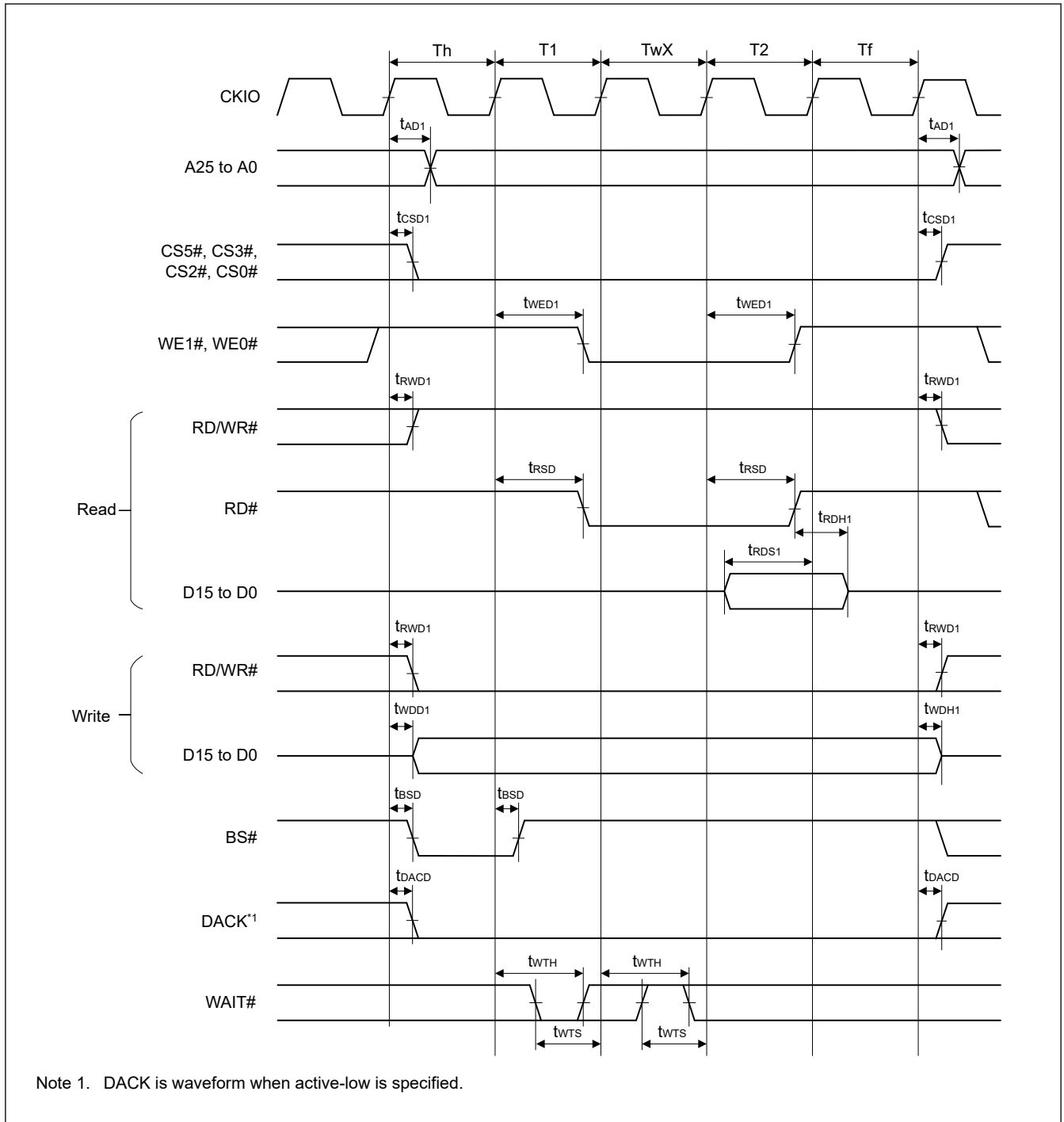


Figure 2.16 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 0 (write cycle UB/LB control))

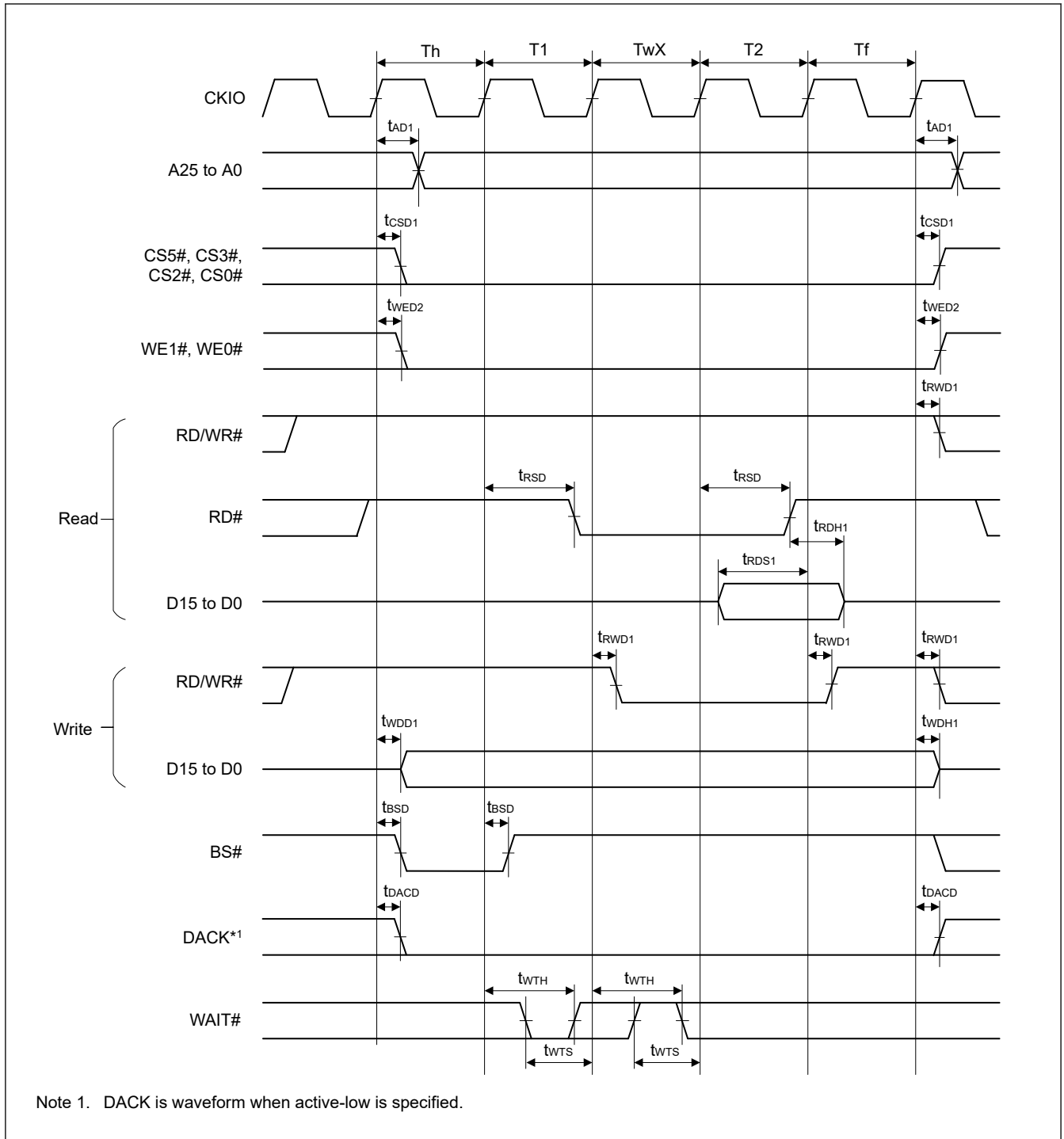


Figure 2.17 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 1 (write cycle WE control))

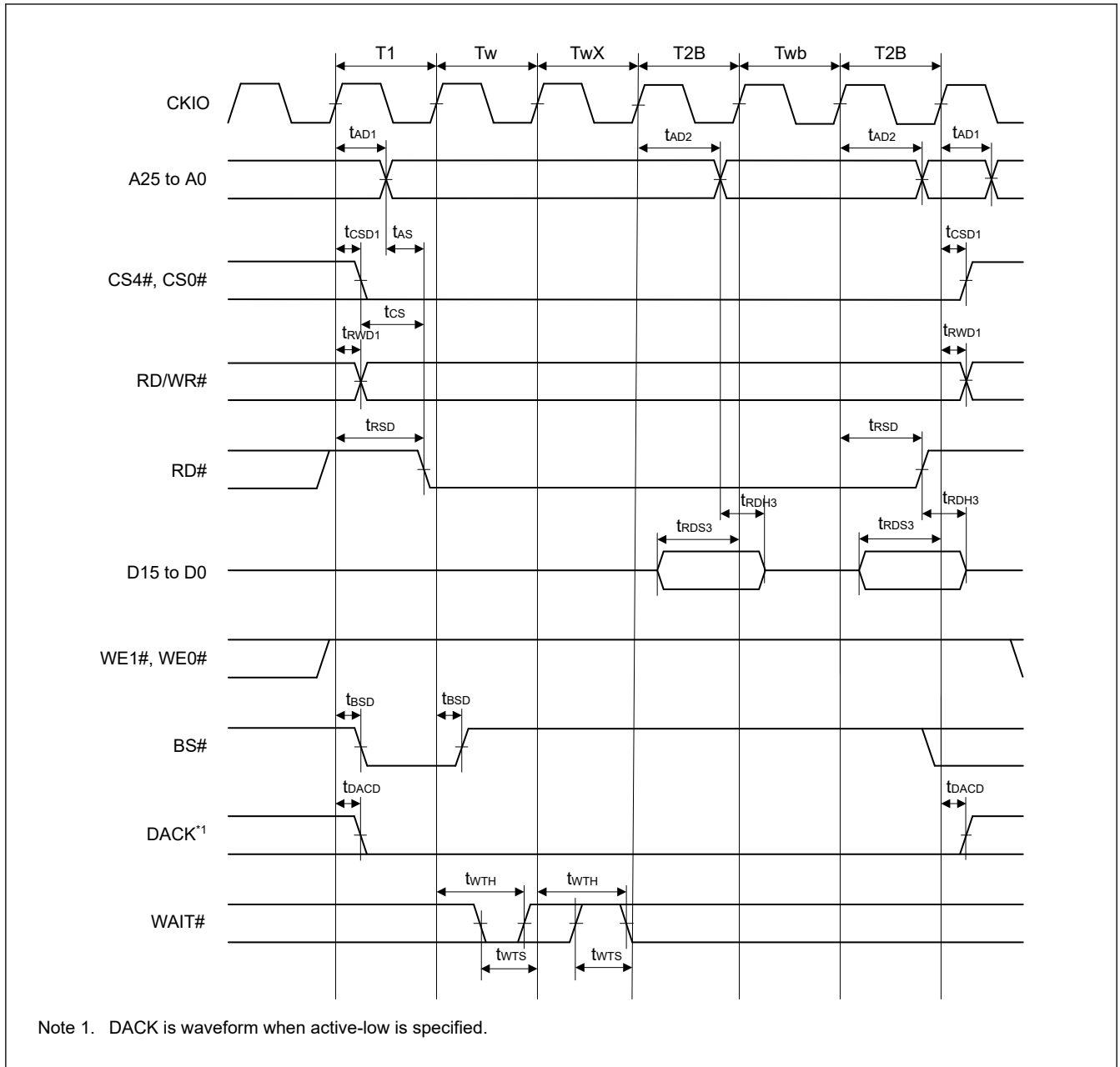


Figure 2.18 Burst ROM read cycle (software wait 1, asynchronous external wait 1 inserted, burst wait 1, 2)

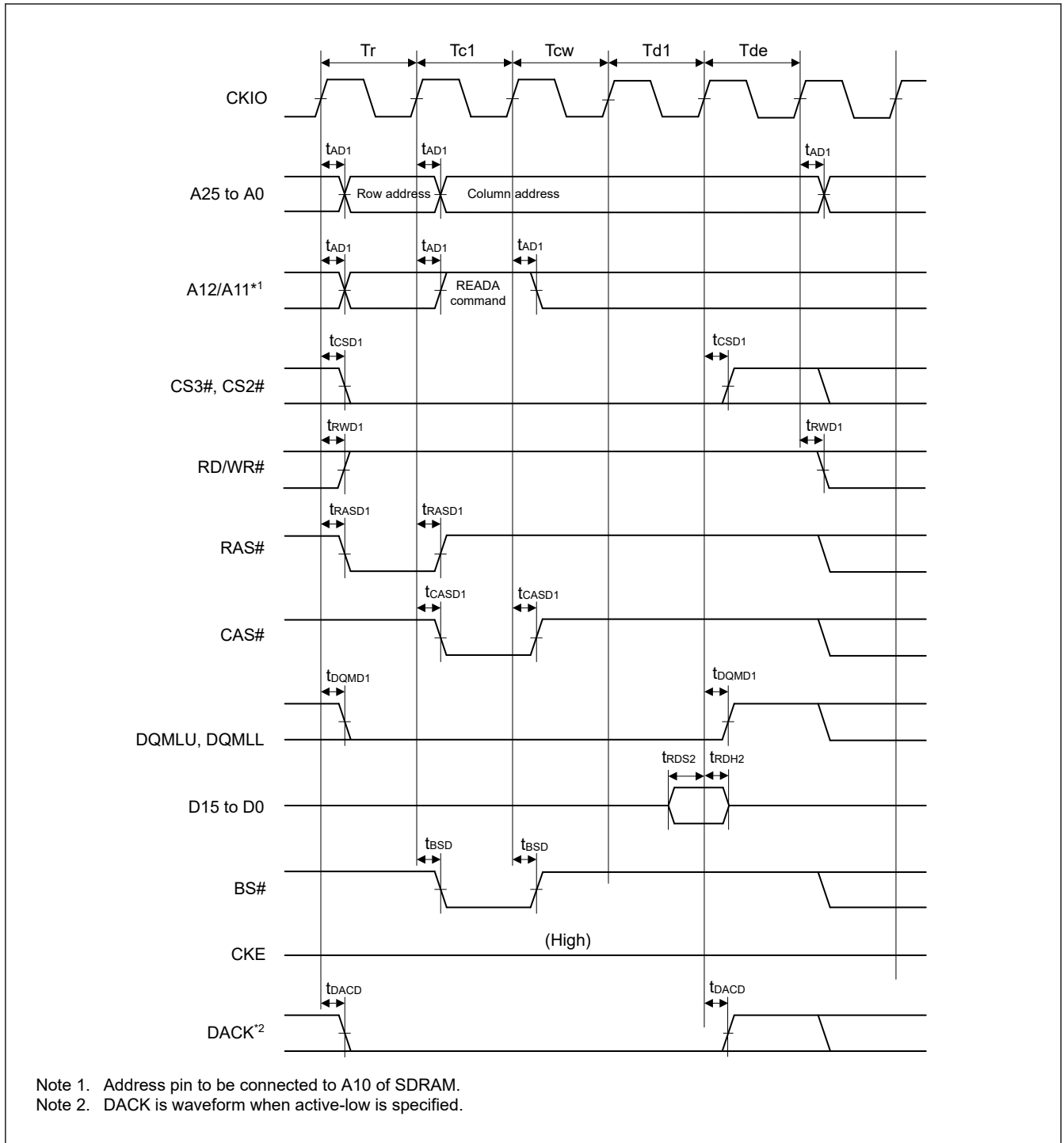


Figure 2.19 Synchronous DRAM single-read bus cycle (with auto precharge, CAS latency 2, WTRCD = 0 cycles, WTRP = 0 cycles)

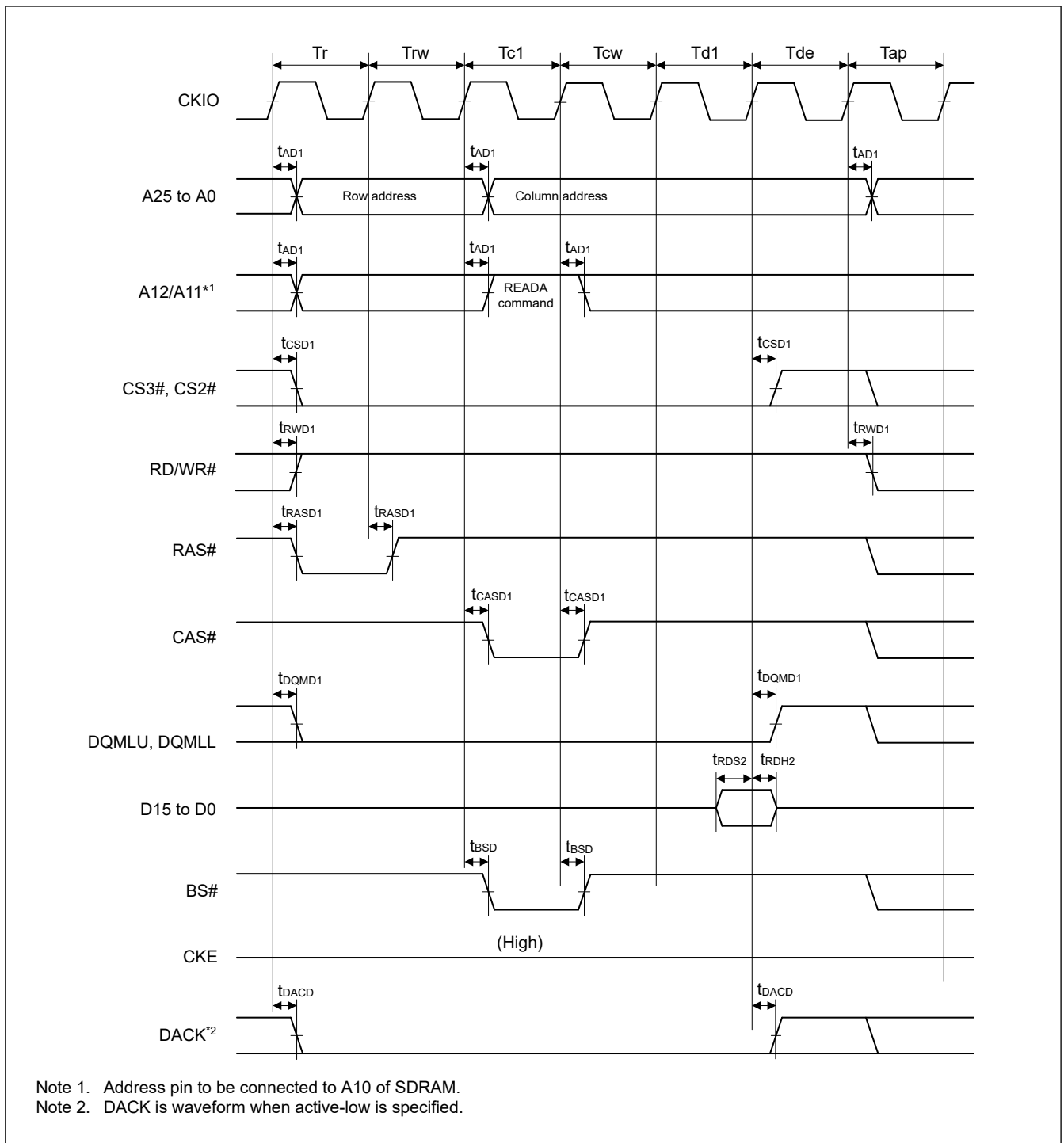


Figure 2.20 Synchronous DRAM single-read bus cycle (with auto precharge, CAS latency 2, WTRCD = 1 cycle, WTRP = 1 cycle)

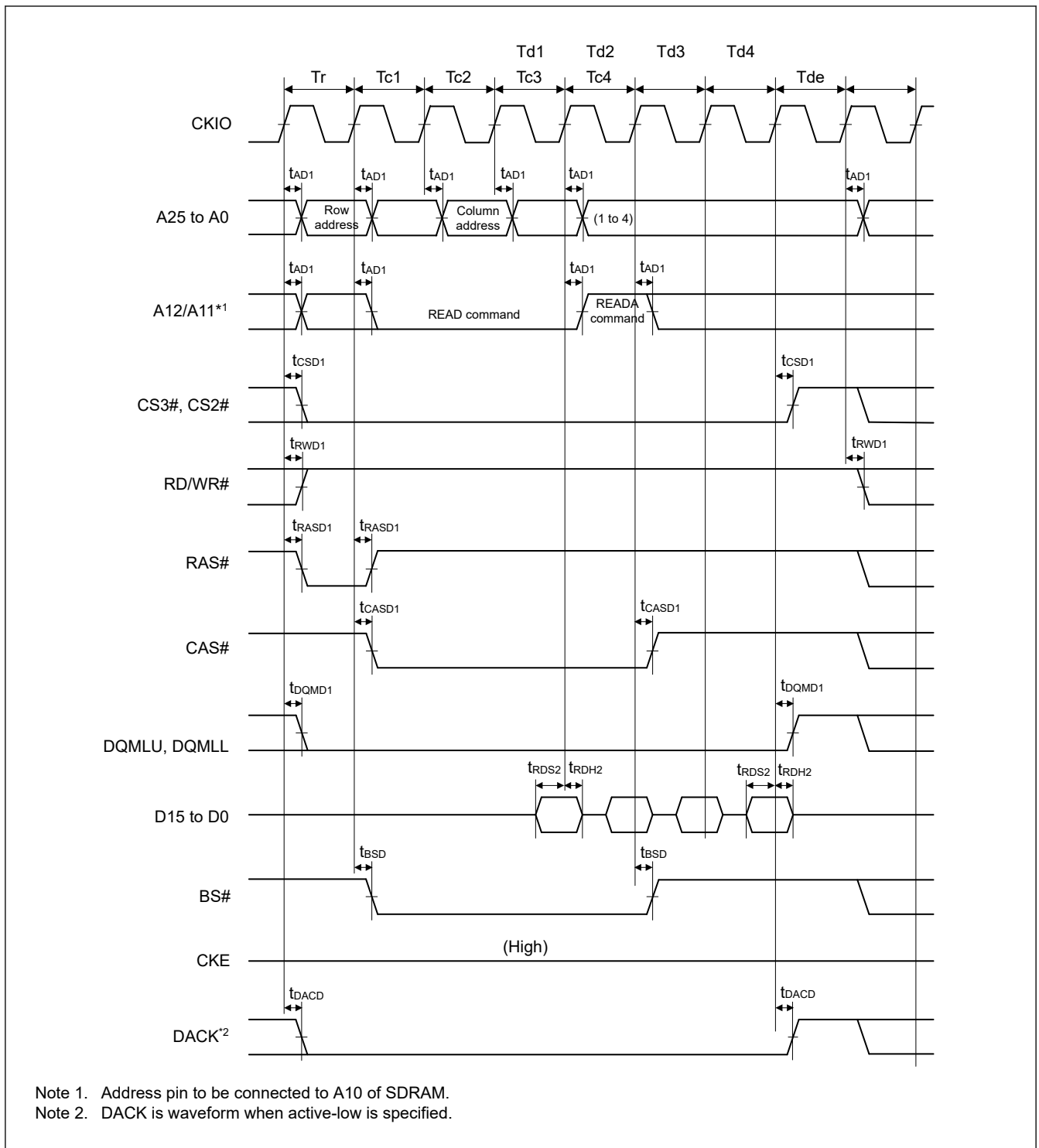


Figure 2.21 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (with auto precharge, CAS latency 2, WTRCD = 0 cycles, WTRP = 1 cycle)

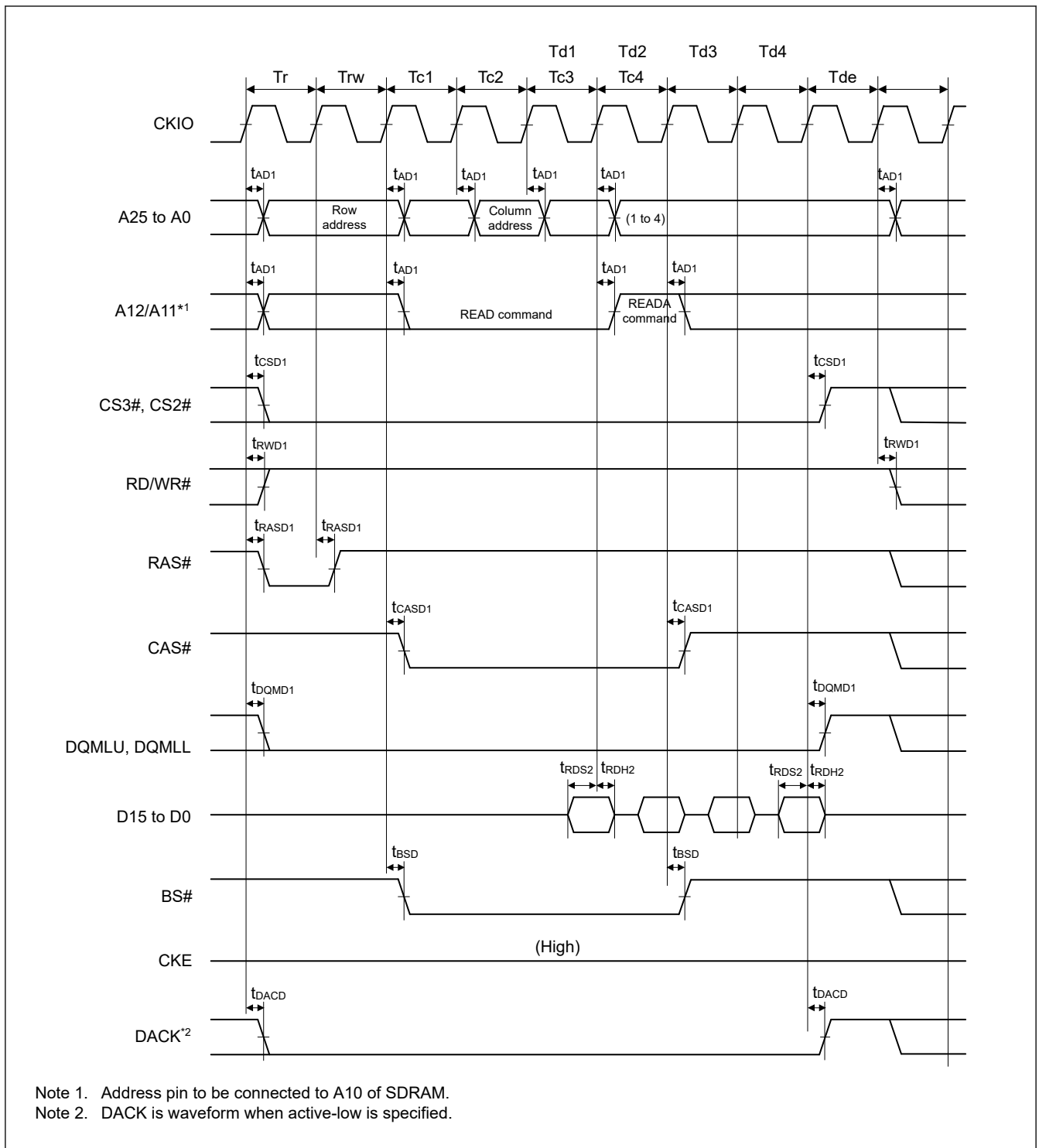


Figure 2.22 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (with auto precharge, CAS latency 2, WTRCD = 1 cycle, WTRP = 0 cycles)

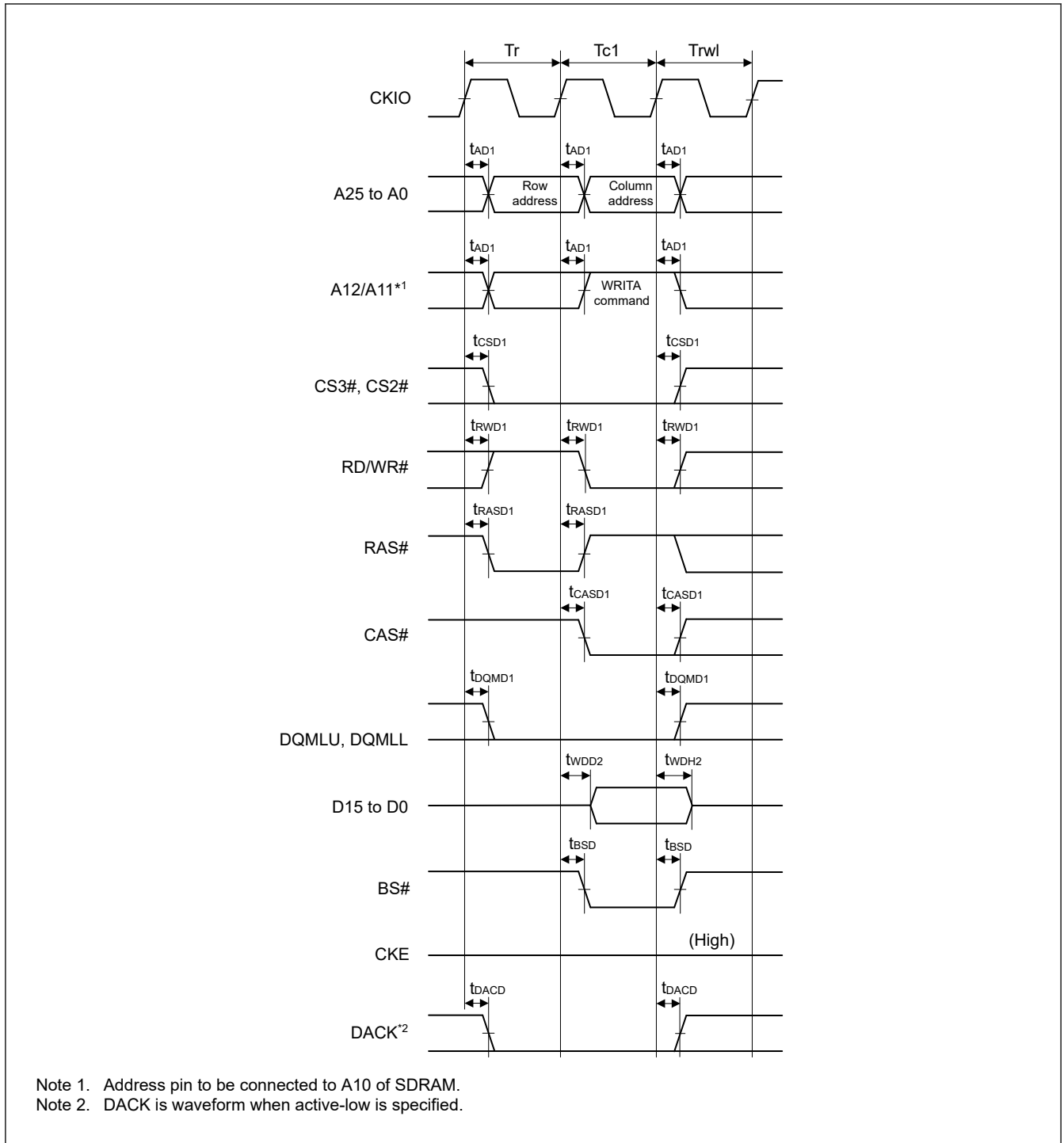


Figure 2.23 Synchronous DRAM single-write bus cycle (with auto precharge, TRWL = 1 cycle)

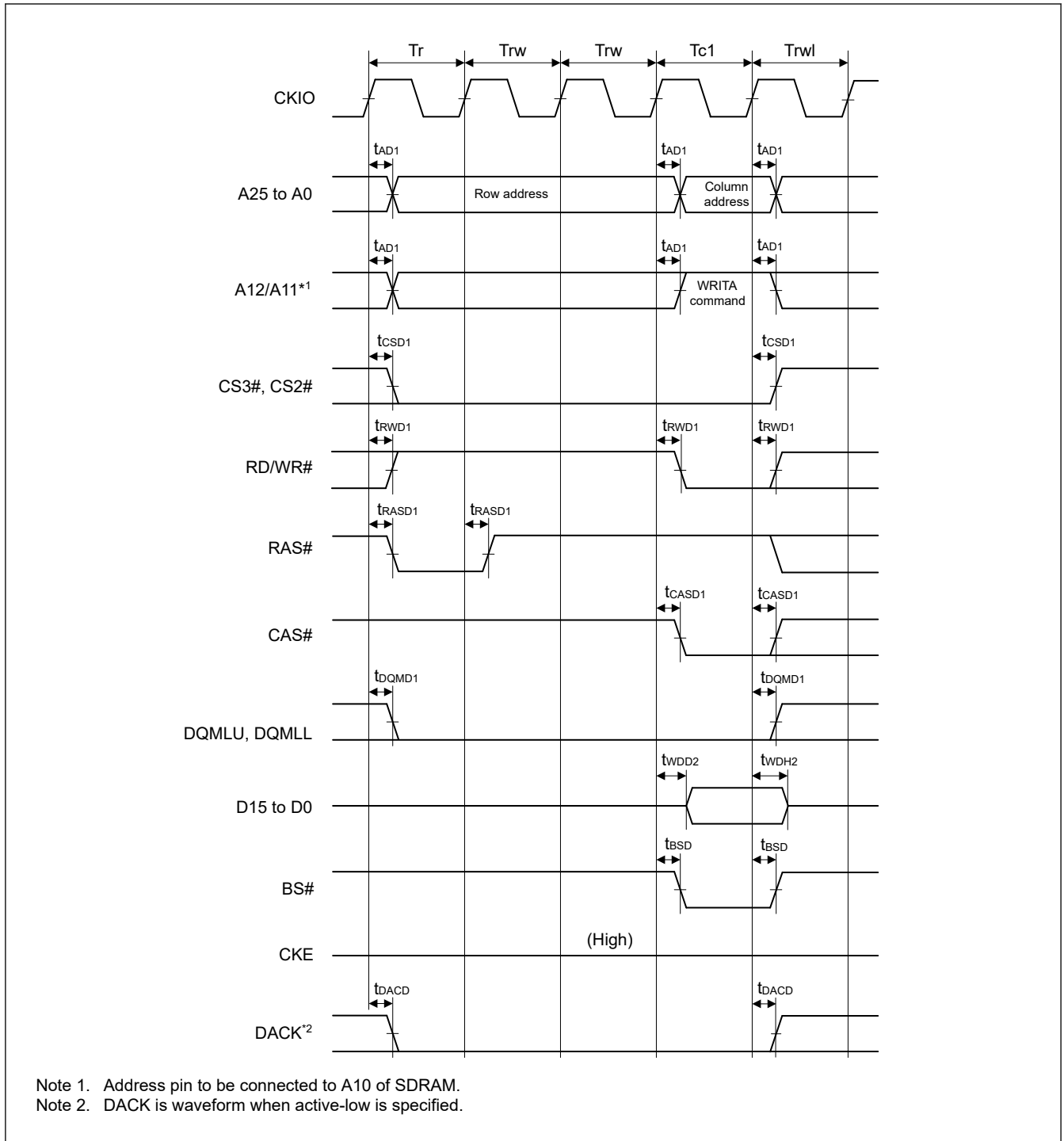
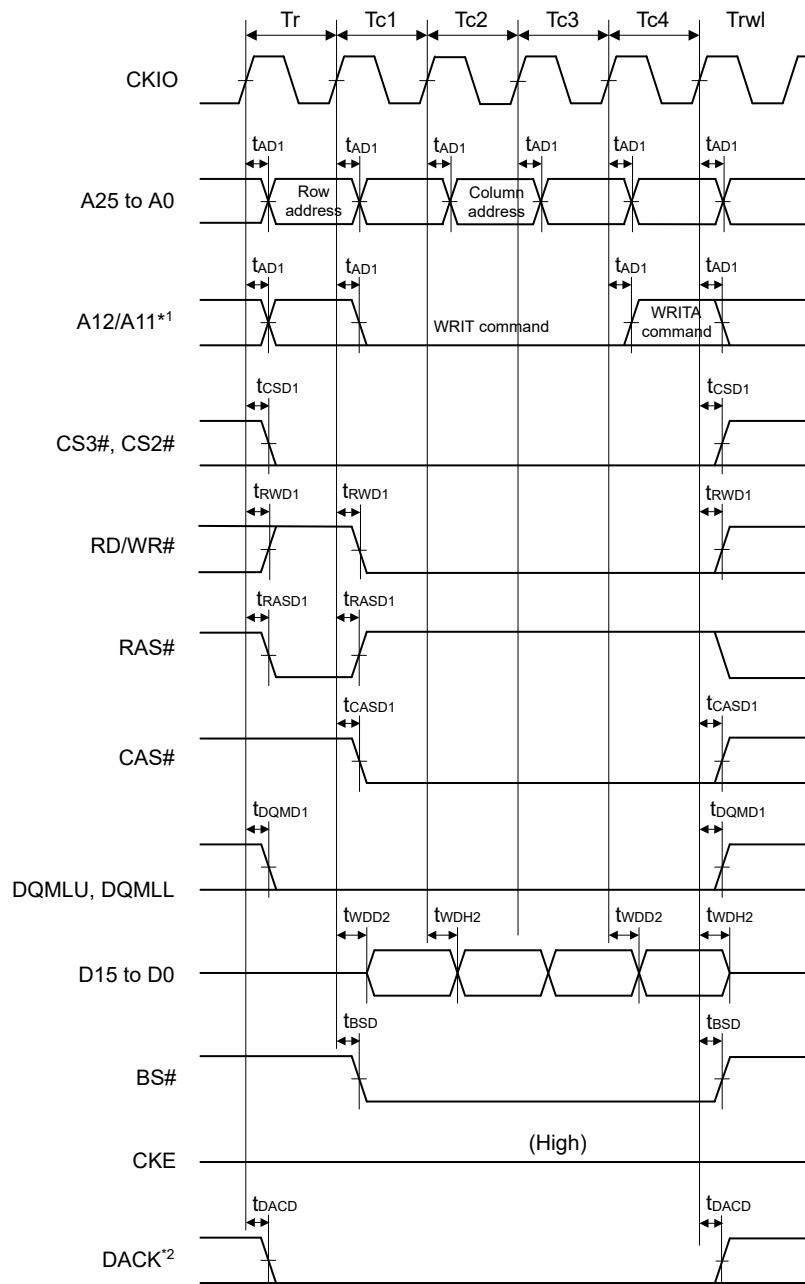
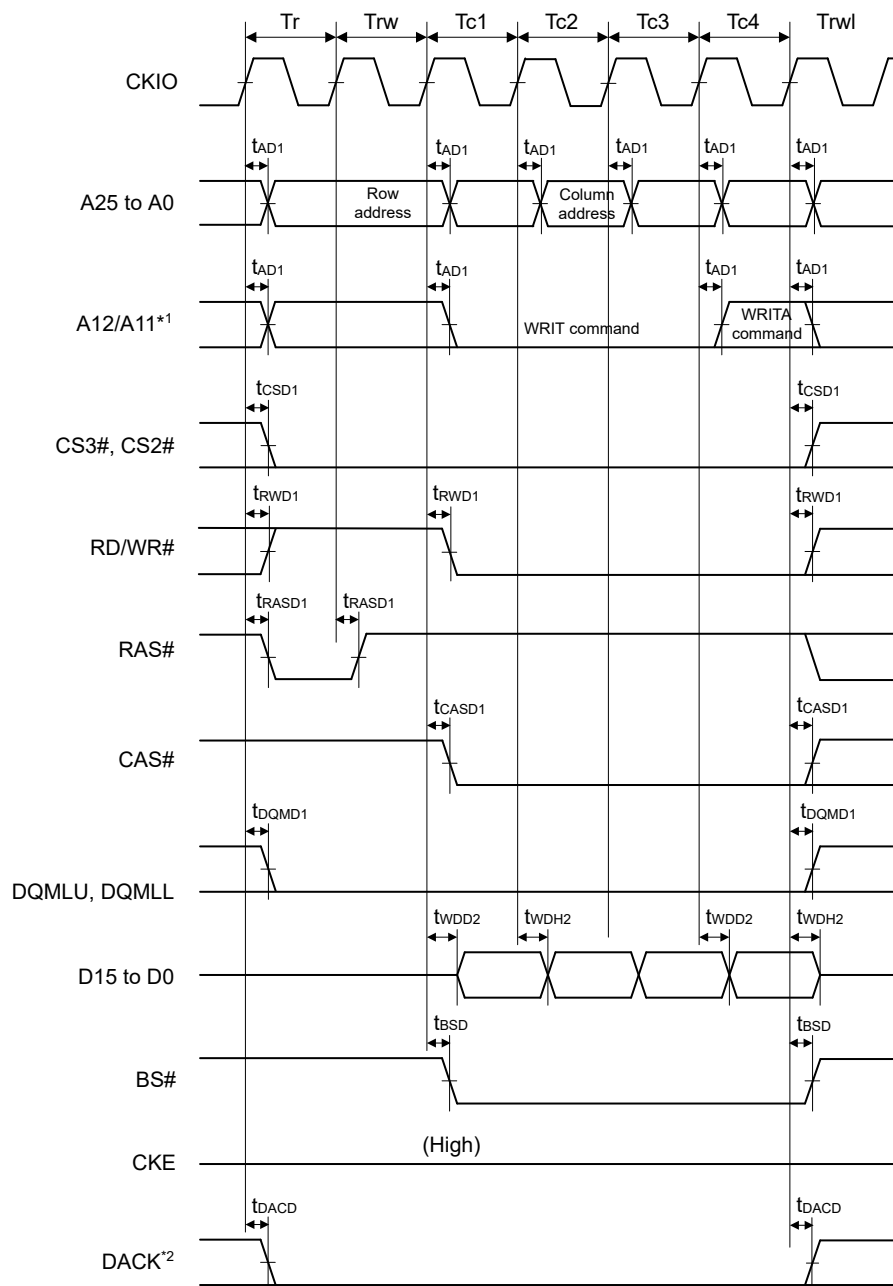


Figure 2.24 Synchronous DRAM single-write bus cycle (with auto precharge, WTRCD = 2 cycles, TRWL = 1 cycle)



Note 1. Address pin to be connected to A10 of SDRAM.
 Note 2. DACK is waveform when active-low is specified.

Figure 2.25 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (with auto precharge, WTRCD = 0 cycles, TRWL = 1 cycle)



Note 1. Address pin to be connected to A10 of SDRAM.
 Note 2. DACK is waveform when active-low is specified.

Figure 2.26 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (with auto precharge, WTRCD = 1 cycle, TRWL = 1 cycle)

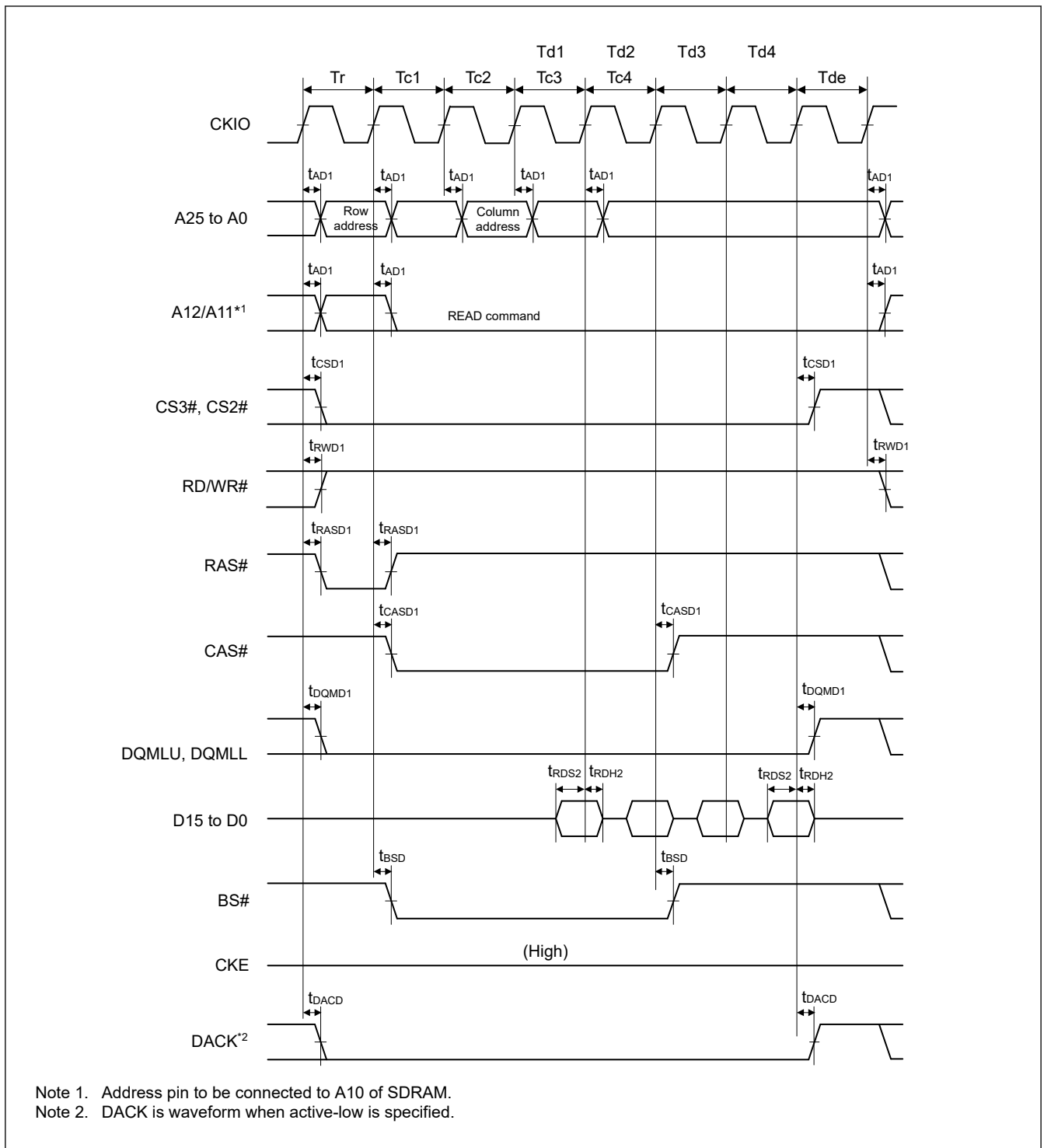


Figure 2.27 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (bank active mode: ACT + READ command, CAS latency 2, WTRCD = 0 cycles)

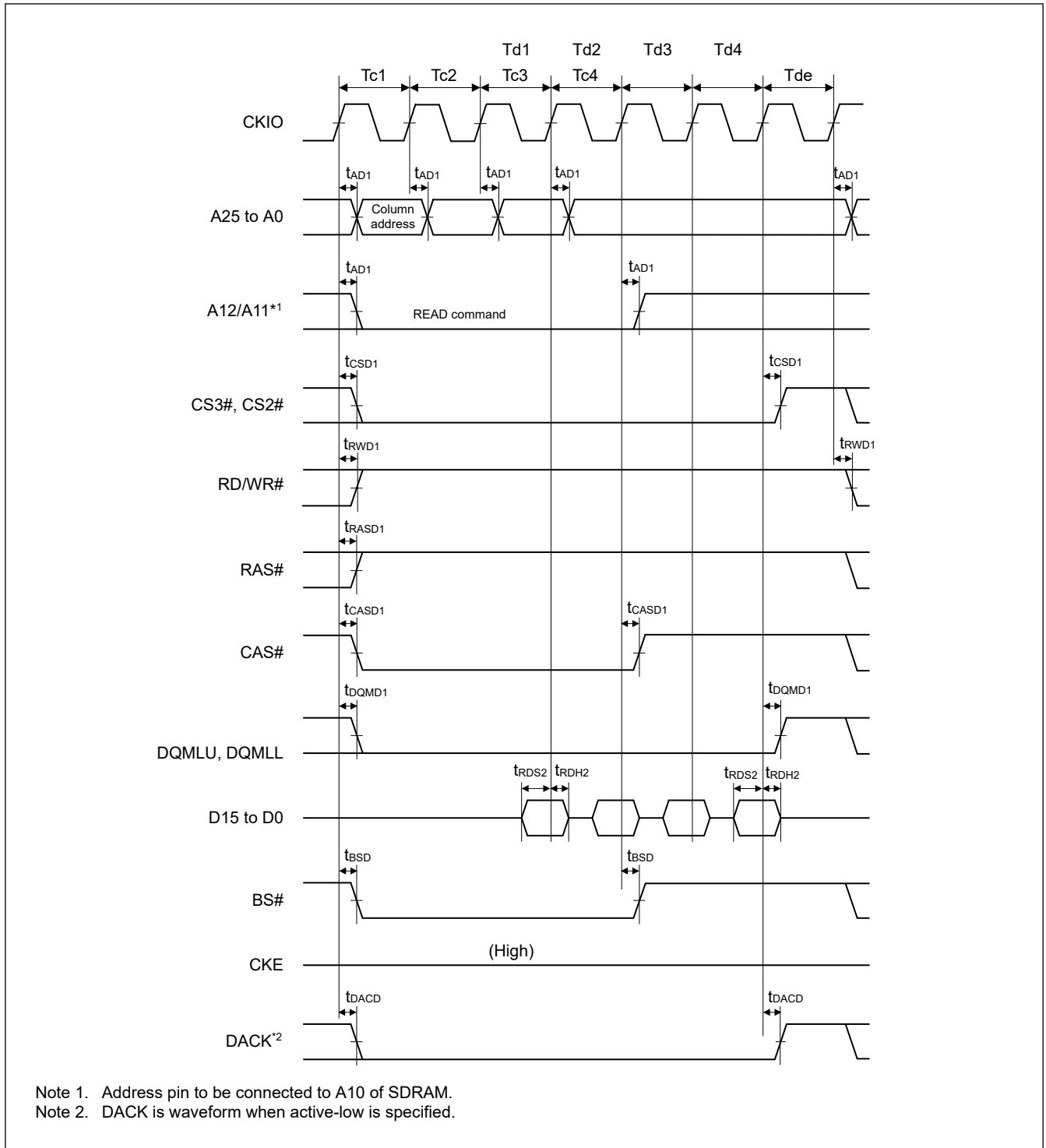


Figure 2.28 Synchronous DRAM burst-read bus cycle (read for 4 cycles) (bank active mode: READ command, same row address, CAS latency 2, WTRCD = 0 cycles)

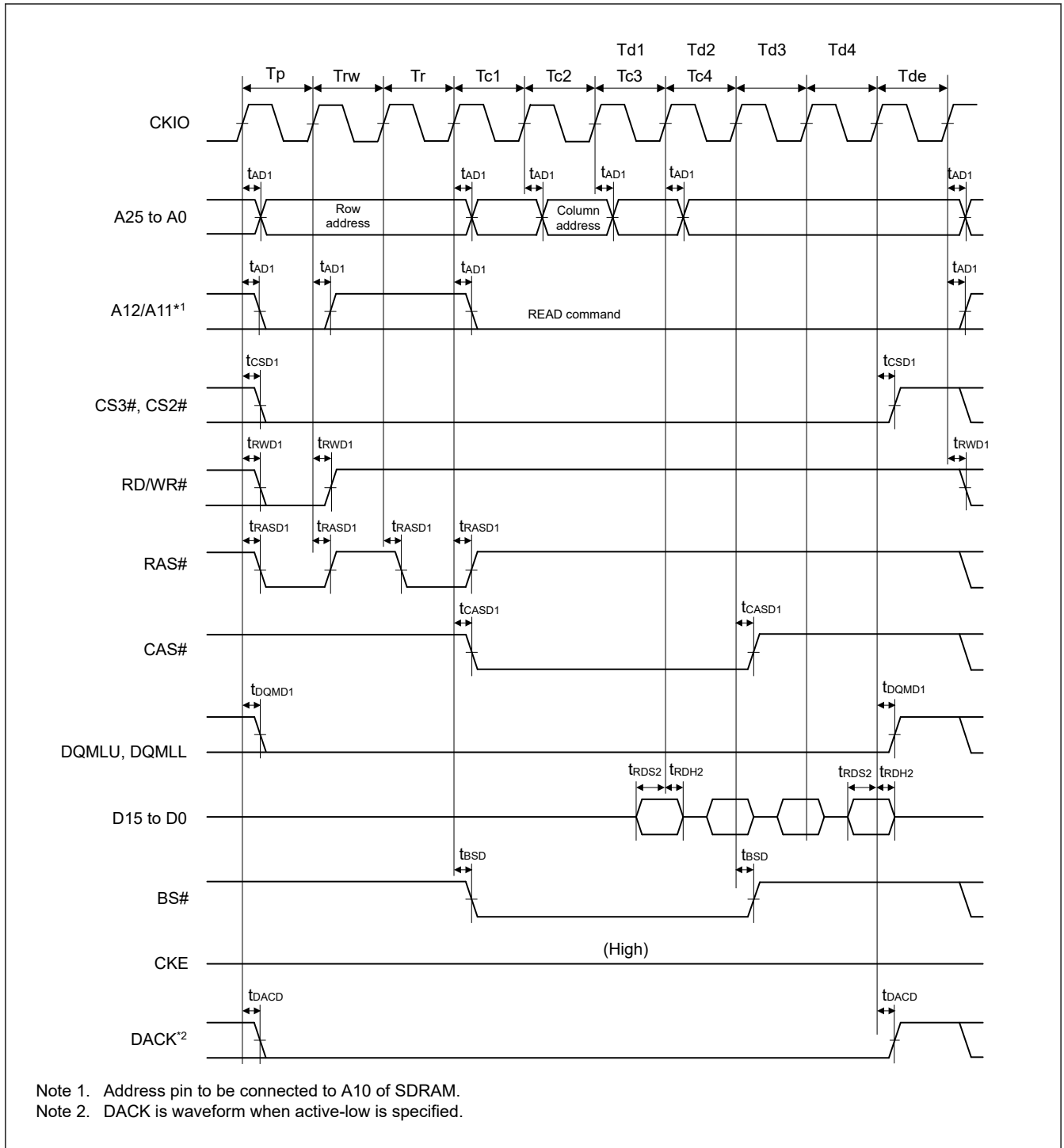


Figure 2.29 Synchronous DRAM burst-read bus Cycle (read for 4 cycles) (bank active mode: PRE + ACT + READ command, different row address, CAS latency 2, WTRCD = 0 cycles)

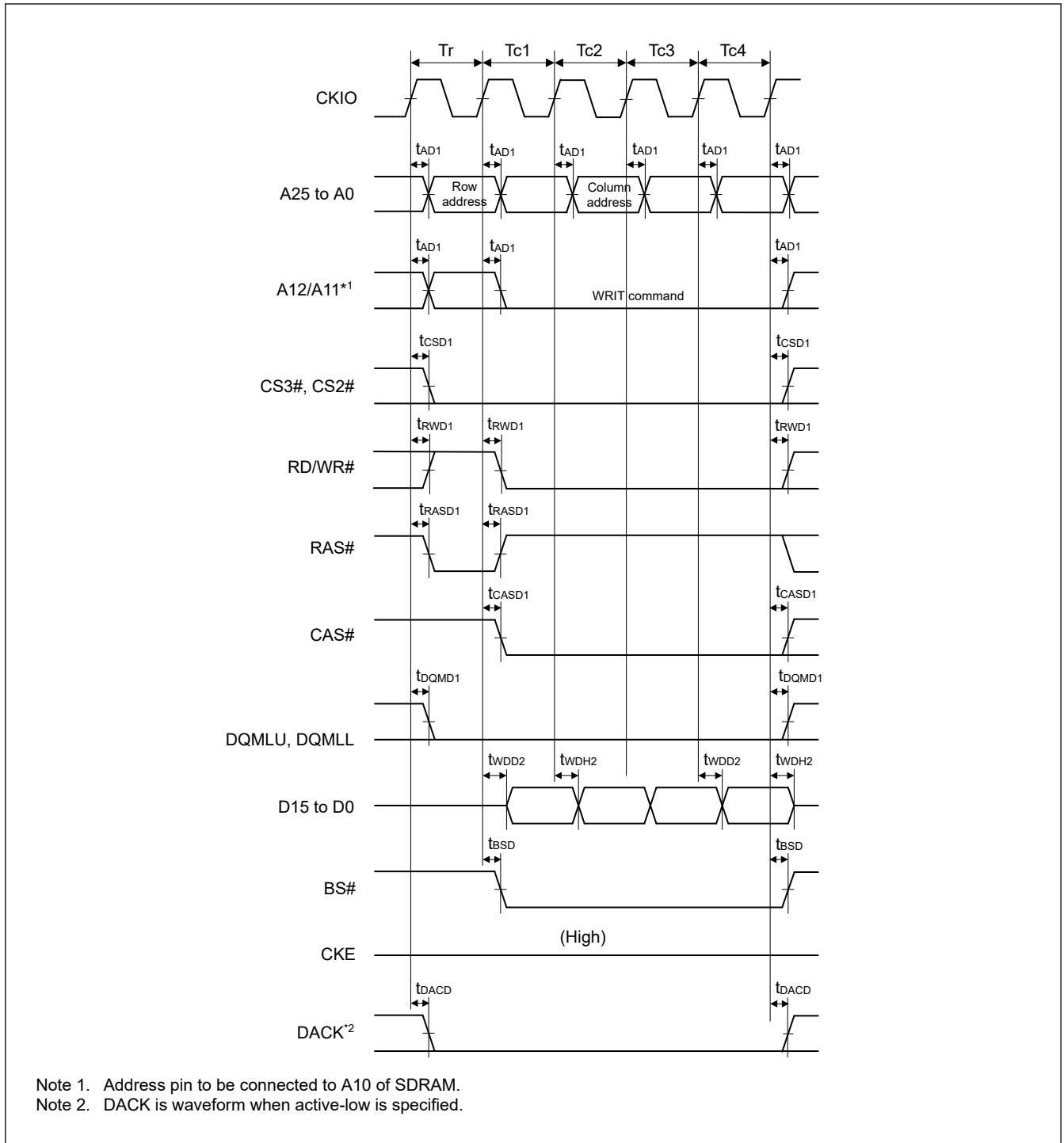


Figure 2.30 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: ACT + WRITE command, WTRCD = 0 cycles, TRWL = 0 cycles)

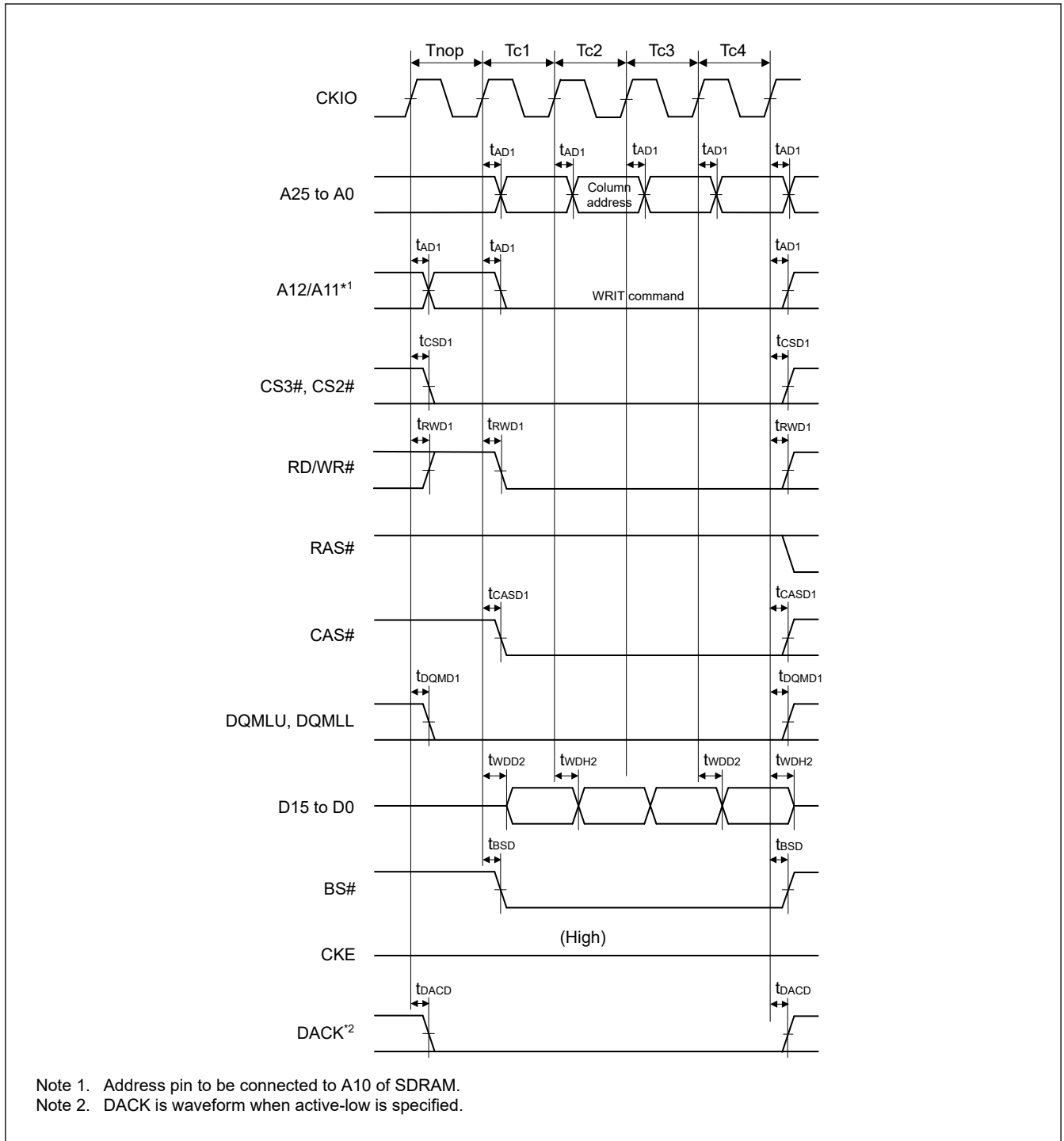


Figure 2.31 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: WRITE command, same row address, WTRCD = 0 cycles, TRWL = 0 cycles)

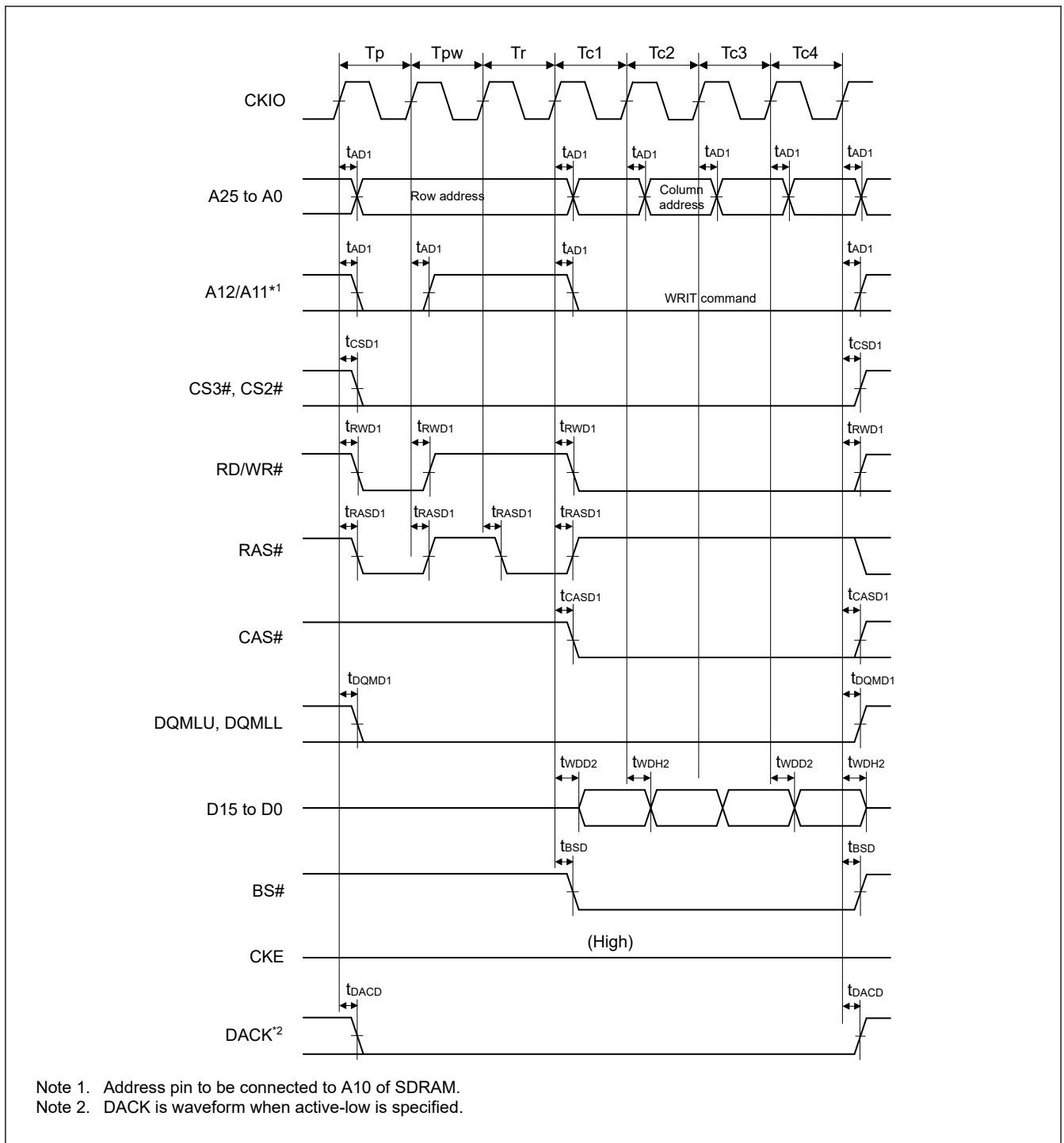


Figure 2.32 Synchronous DRAM burst-write bus cycle (write for 4 cycles) (bank active mode: PRE + ACT + WRITE command, different row address, WTRCD = 0 cycles, TRWL = 0 cycles)

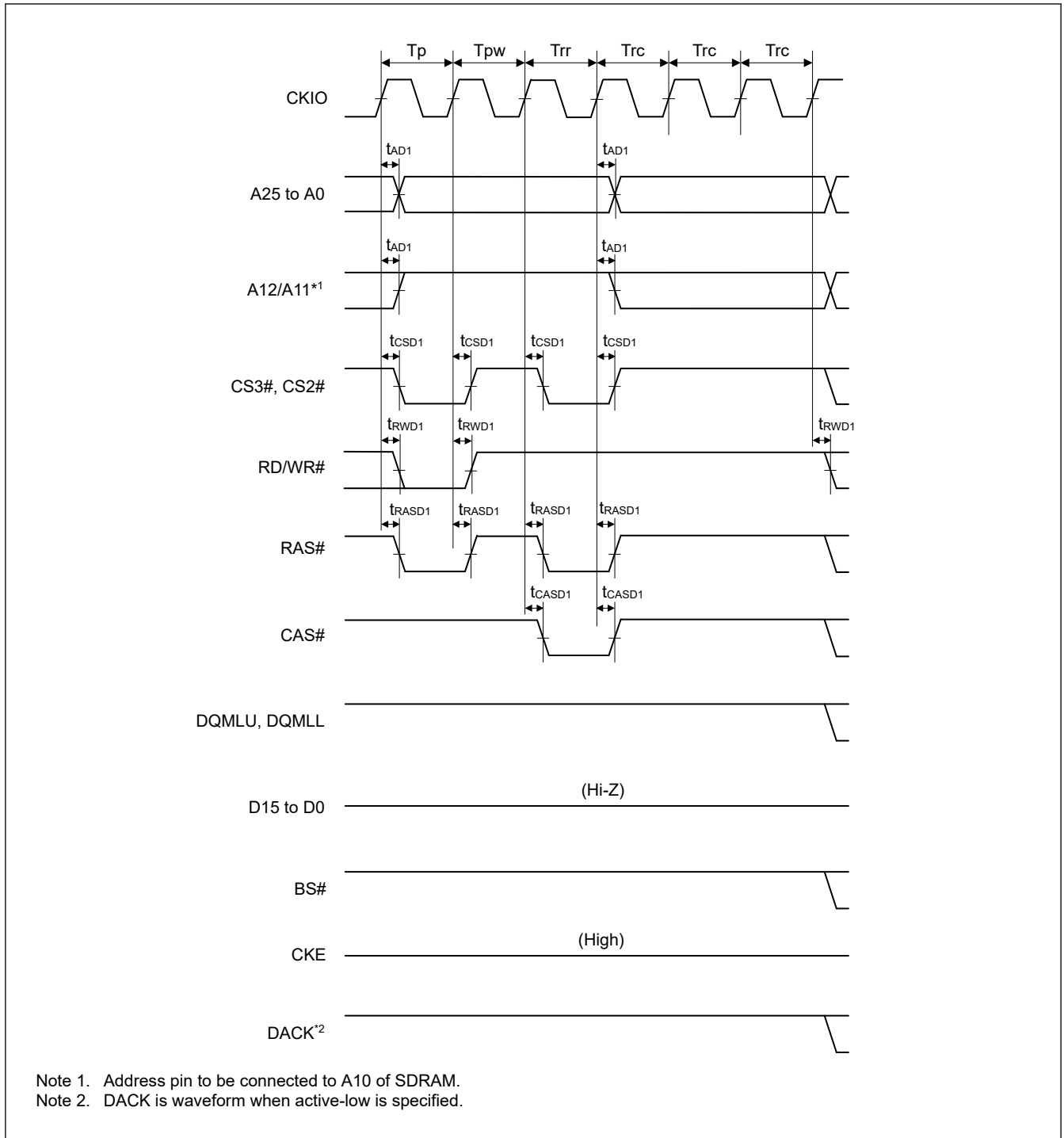


Figure 2.33 Synchronous DRAM auto-refresh timing (WTRP = 1 cycle, WTRC = 3 cycles)

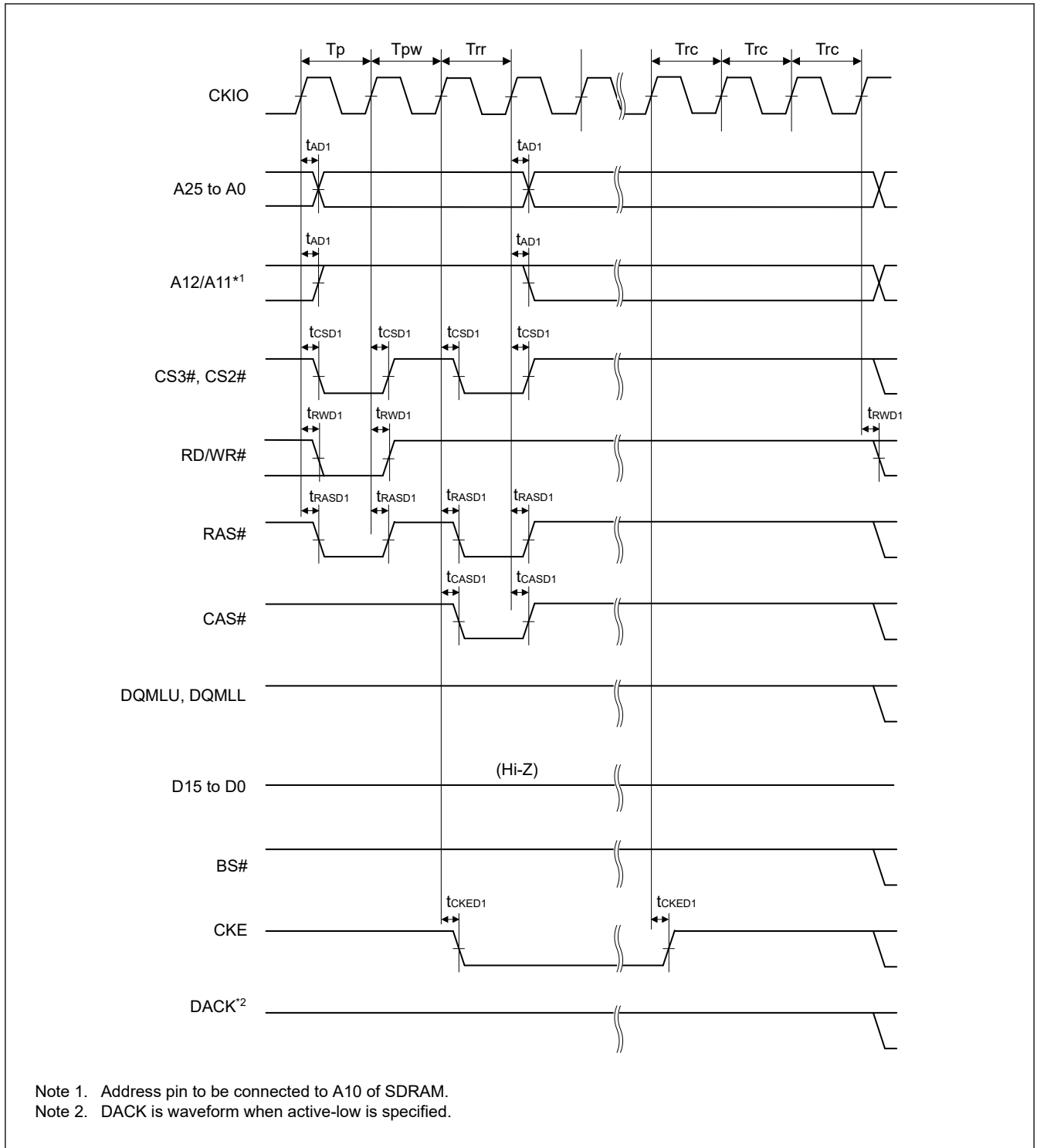


Figure 2.34 Synchronous DRAM self-refresh timing (WTRP = 1 cycle)

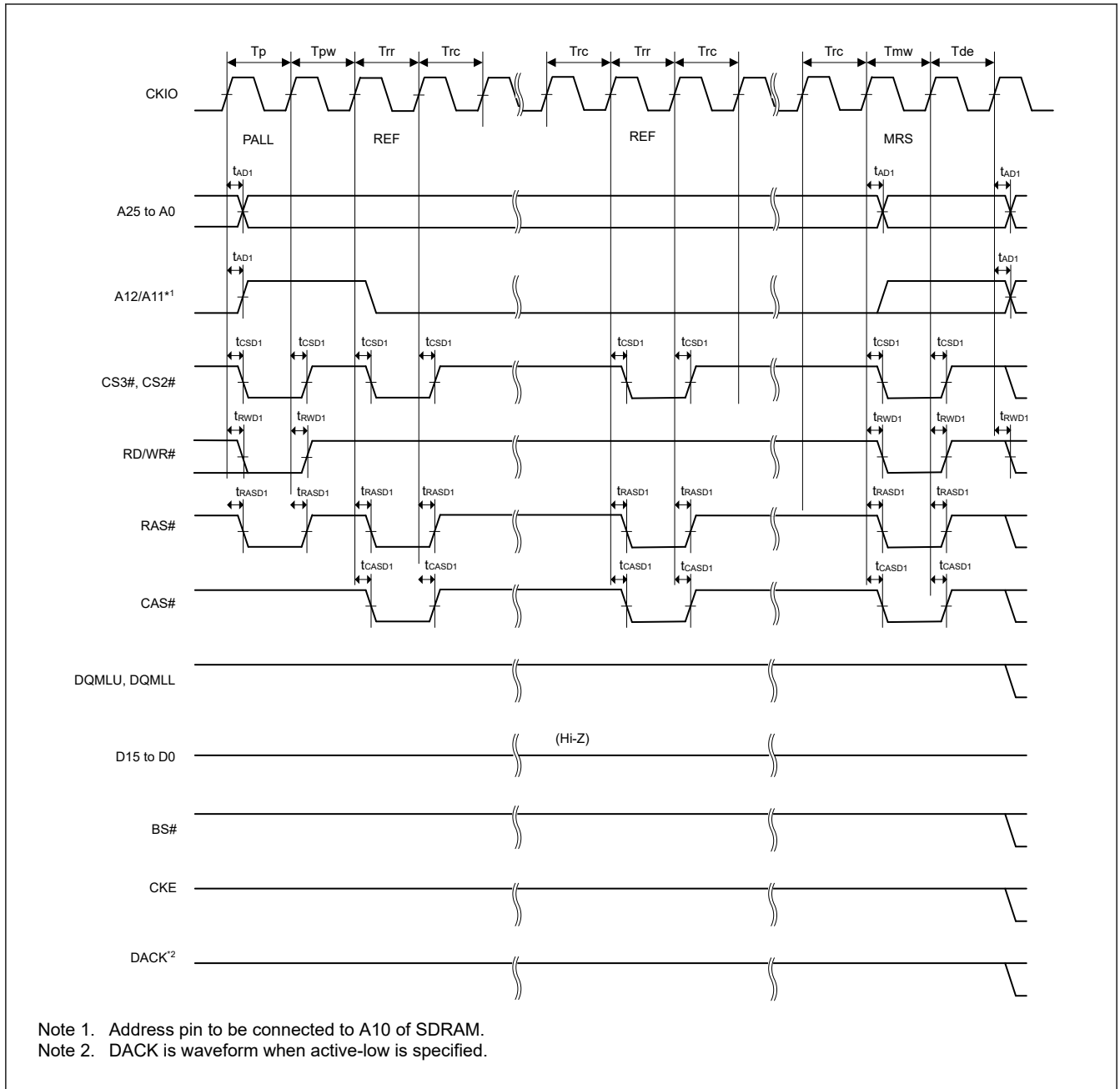


Figure 2.35 Synchronous DRAM mode register set timing (WTRP = 1 cycle)

2.5.4 DMAC Timing

Table 2.23 DMAC timing

Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 15 \text{ pF}$ (CKIO), 30 pF (others), $T_{jmin} = -40^\circ\text{C}$

Parameter	Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	$t_{PLCyc} \times 2$	ns	Figure 2.36
	DACK and TEND delay time	t_{DACD}	10	ns	Figure 2.37

Note 1. t_{PLCyc} : PCLKL cycle

Table 2.24 DMAC timing

Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 12 \text{ pF}$ (CKIO), 12 pF (others), $T_{jmin} = -20^\circ\text{C}$

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	$t_{PLcyc} \times 2$	—	ns	Figure 2.36
	DACK and TEND delay time	t_{DACD}	-0.5	8	ns	Figure 2.37

Note 1. t_{PLcyc} : PCLKL cycle

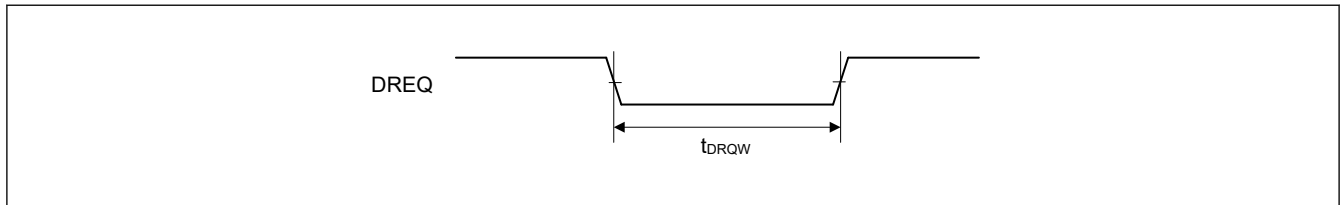


Figure 2.36 DREQ input timing

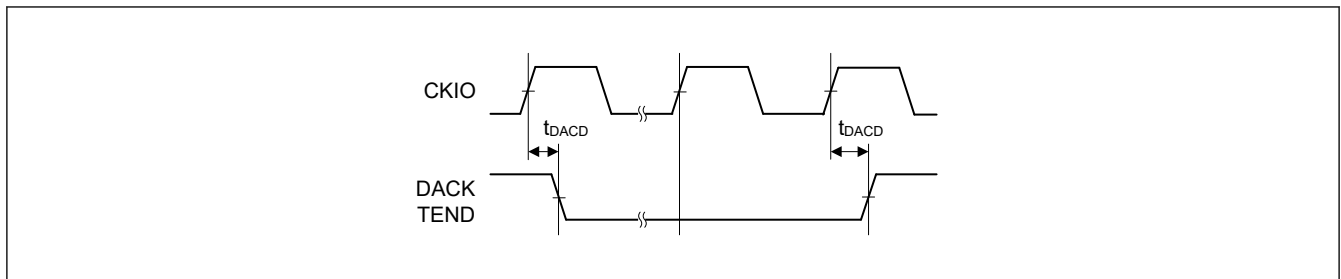


Figure 2.37 DACK and TEND output timing

2.5.5 On-Chip Peripheral Module Timing

2.5.5.1 I/O Port Timing

Table 2.25 I/O port timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PLcyc}	Figure 2.38

Note 1. t_{PLcyc} : PCLKL cycle

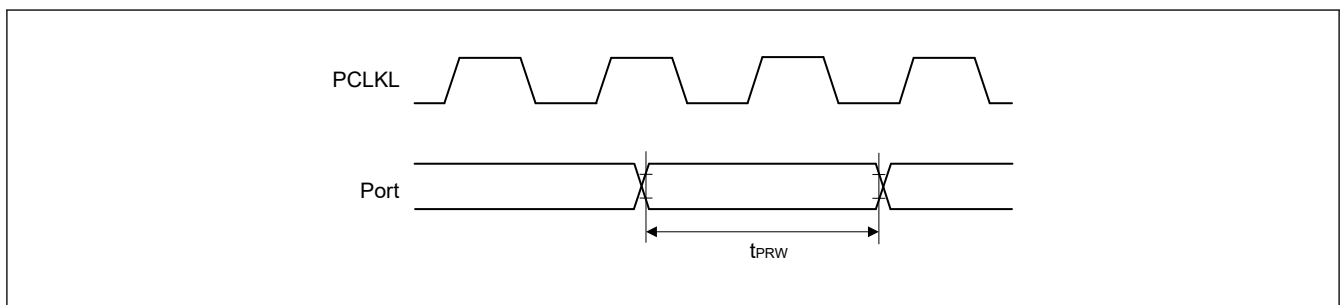


Figure 2.38 I/O port input timing

2.5.5.2 CMTW Timing

Table 2.26 CMTW timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
CMTW	Input capture input pulse width	Single-edge setting	1.5	—	t_{PLcyc}	Figure 2.39
		Both-edge setting	2.5	—		

Note 1. t_{PLcyc} : PCLKL cycle

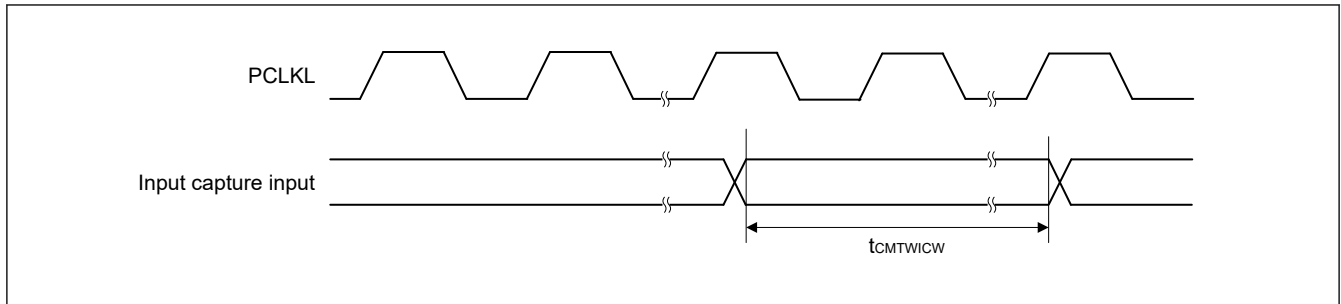


Figure 2.39 CMTW input capture input timing

2.5.5.3 MTU3 Timing

Table 2.27 MTU3 timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure	
MTU3	Input capture input pulse width	Single-edge setting	t _{MTICW}	2.5	—	t _{PHcyc}	Figure 2.40
		Both-edge setting		3.5	—		
	Timer clock pulse width	Single-edge setting	t _{MTCKWH} , t _{MTCKWL}	2.5	—	t _{PHcyc}	Figure 2.41
		Both-edge setting		3.5	—		
Phase counting mode		3.5	—				

Note 1. t_{PHcyc}: PCLKH cycle

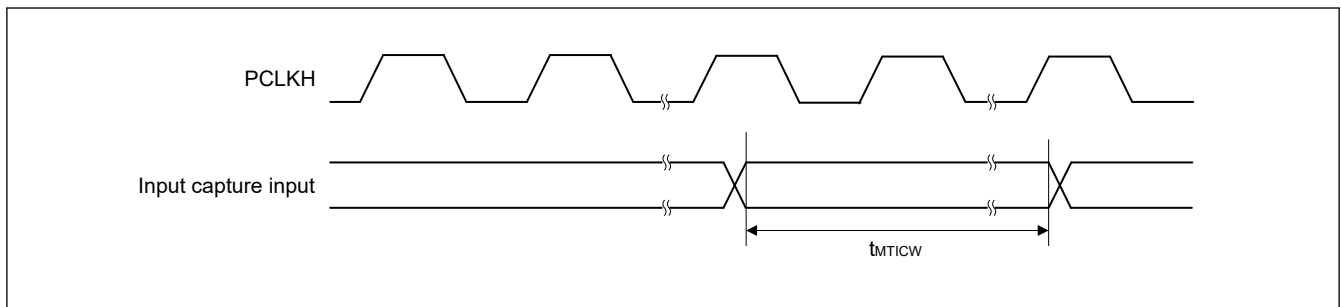


Figure 2.40 MTU3 input capture input timing

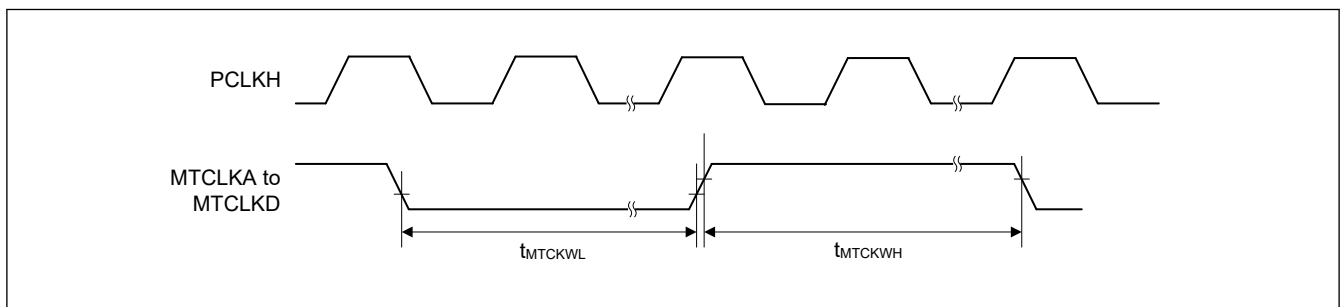


Figure 2.41 MTU3 clock input timing

2.5.5.4 POE3 Timing

Table 2.28 POE3 timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure	
POE3	POEn# input pulse width	t_{POEW}	2.5	—	t_{PHcyc}	Figure 2.42	
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	$5 \times PCLKH + 0.1$	μs	Figure 2.43
		Simultaneous conduction of output pins	t_{POEDO}	—	$3 \times PCLKH + 0.1$	μs	Figure 2.44
		Register setting	t_{POEDS}	—	$PCLKH + 0.1$	μs	Figure 2.45
		Oscillation stop detection	t_{POEDOS}	—	74	μs	Figure 2.46

Note 1. t_{PHcyc} : PCLKH cycle

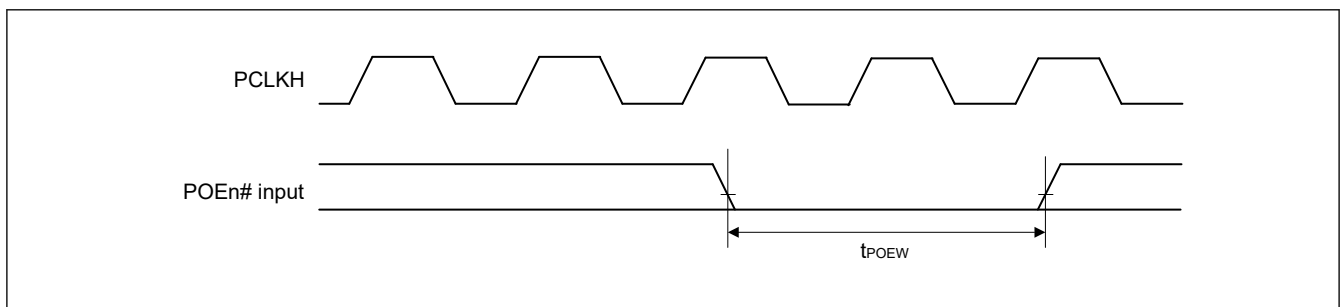


Figure 2.42 POEn# input pulse timing

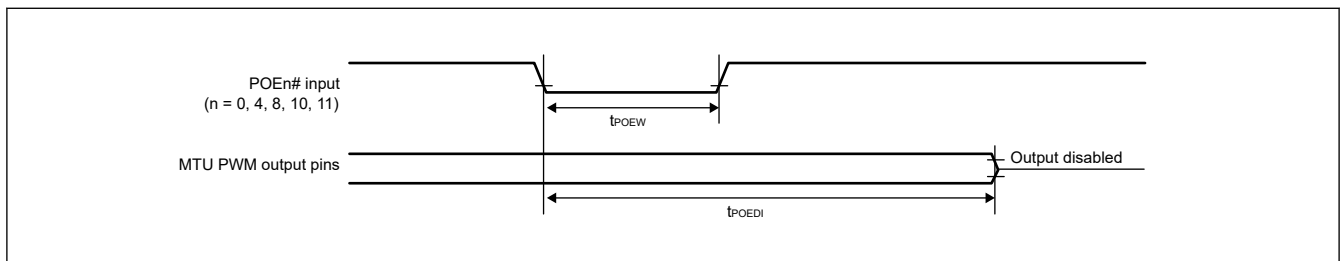
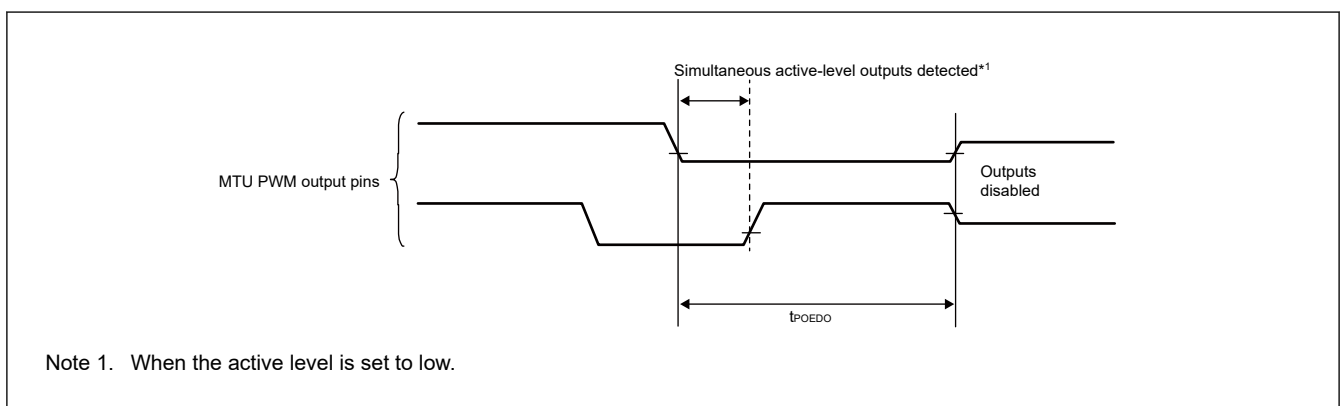


Figure 2.43 Output disable time for POE in response to transition of the POEn# signal level



Note 1. When the active level is set to low.

Figure 2.44 Output disable time for POE in response to the simultaneous conduction of output pins

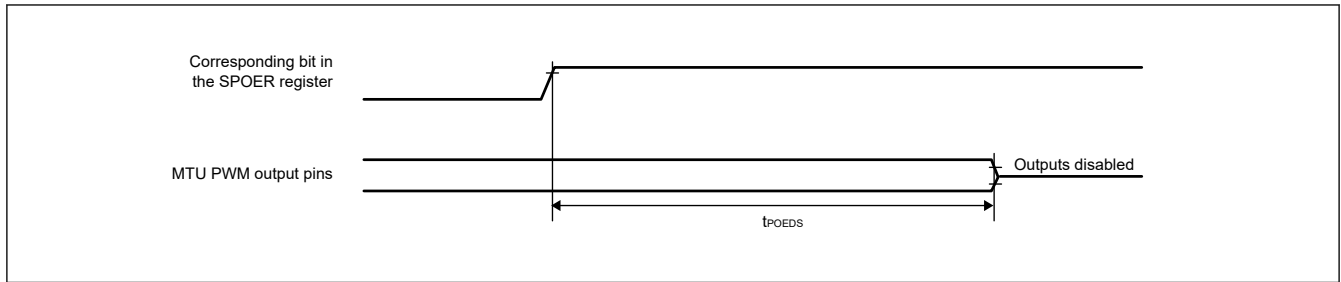


Figure 2.45 Output disable time for POE in response to the register setting

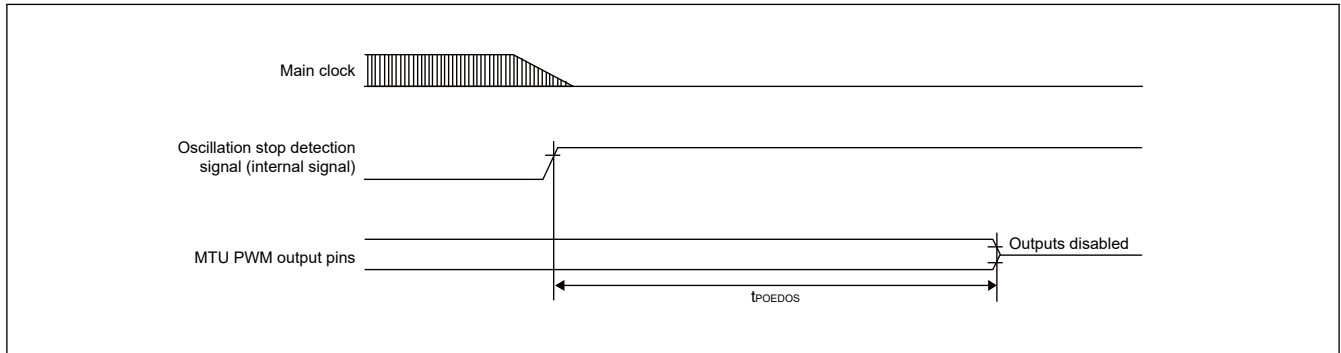


Figure 2.46 Output disable time for POE in response to the oscillation stop detection

2.5.5.5 GPT Timing

Table 2.29 GPT timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure	
GPT	Input capture input pulse width	Single-edge setting	t _{GTICW}	2.5	—	t _{PHcyc}	Figure 2.47
		Both-edge setting		3.5	—		
GPT	External trigger input pulse width	Single-edge setting	t _{GTEW}	2.5	—	t _{PHcyc}	Figure 2.48
		Both-edge setting		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKM cycle (Other channels)

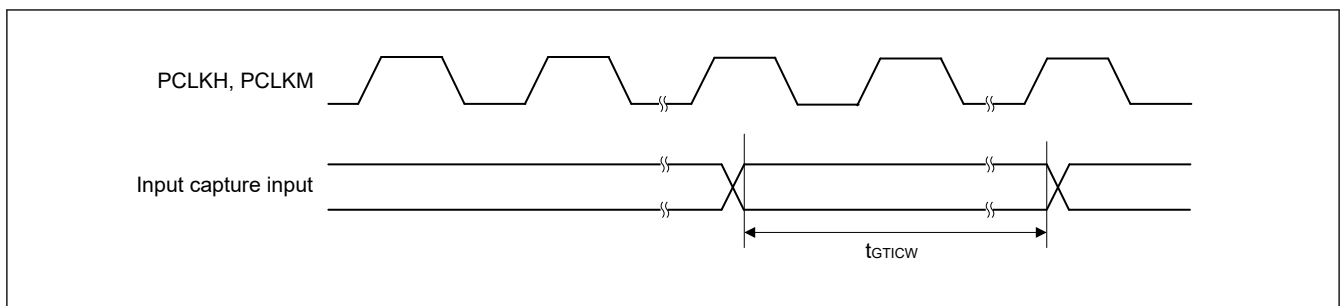


Figure 2.47 GPT input capture input timing

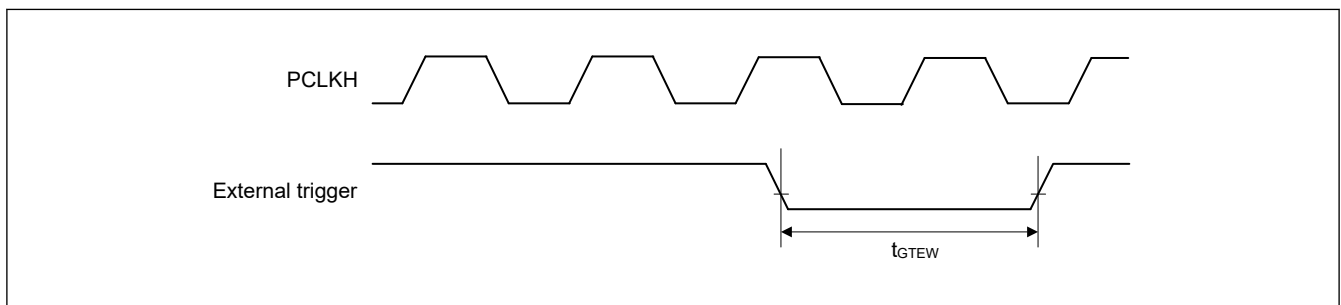


Figure 2.48 GPT external trigger input timing

2.5.5.6 POEG Timing

Table 2.30 POEG timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure	
POEG	GTETRn input pulse width (n = A to D)	t_{POEGW}	2.5	—	t_{PHcyc}	Figure 2.49	
	Output disable time	Input level detection of the GTETRn pin (via flag)	t_{POEGDI}	—	$3 \times PCLKH + 0.1$	μs	Figure 2.50
		Detection of the output stopping signal from GPT (dead time error, simultaneous high output, or simultaneous low output)	t_{POEGDO}	—	0.1	μs	Figure 2.51
	Register setting	t_{POEGDS}	—	$PCLKH + 0.1$	μs	Figure 2.52	
	Oscillation stop detection	$t_{POEGDOS}$	—	74	μs	Figure 2.53	

Note 1. t_{PHcyc} : PCLKH cycle (LLPP channels), PCLKL cycle (Other channels)

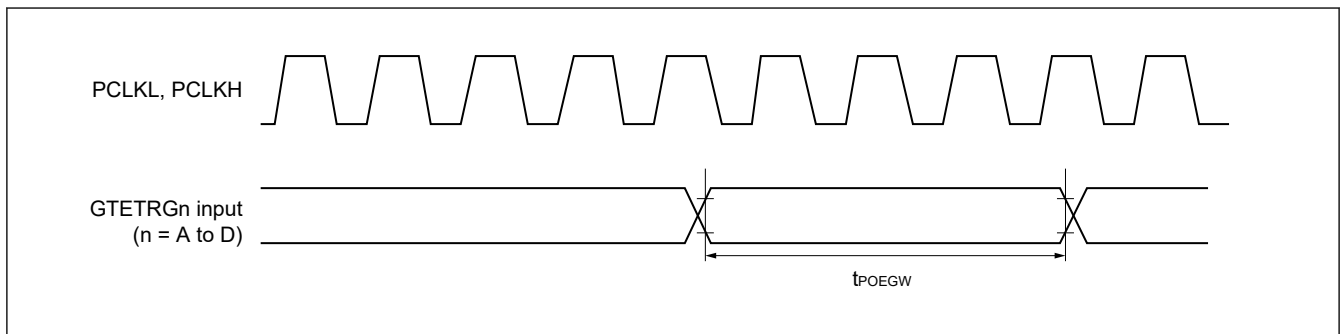


Figure 2.49 POEG input timing

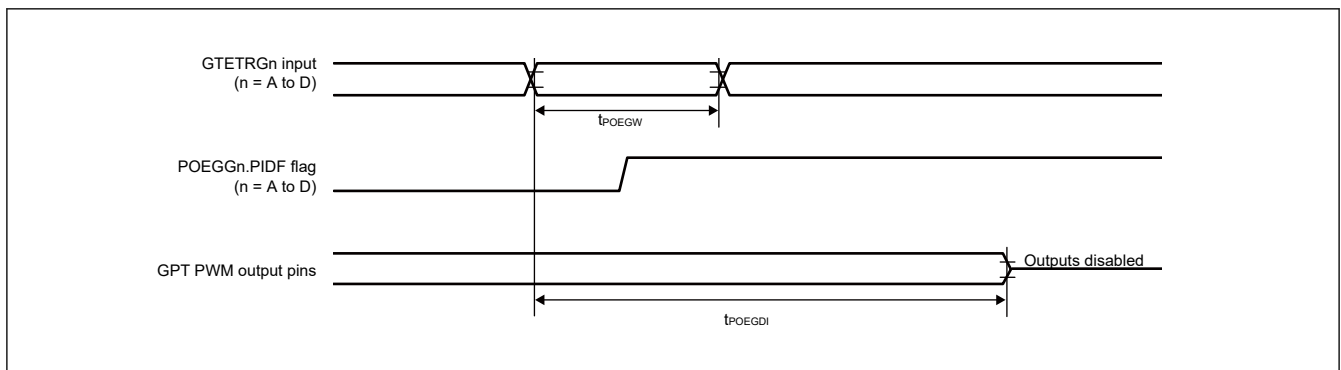


Figure 2.50 Output disable time for POEG via detection flag in response to the input level detection of the GTETRn pin

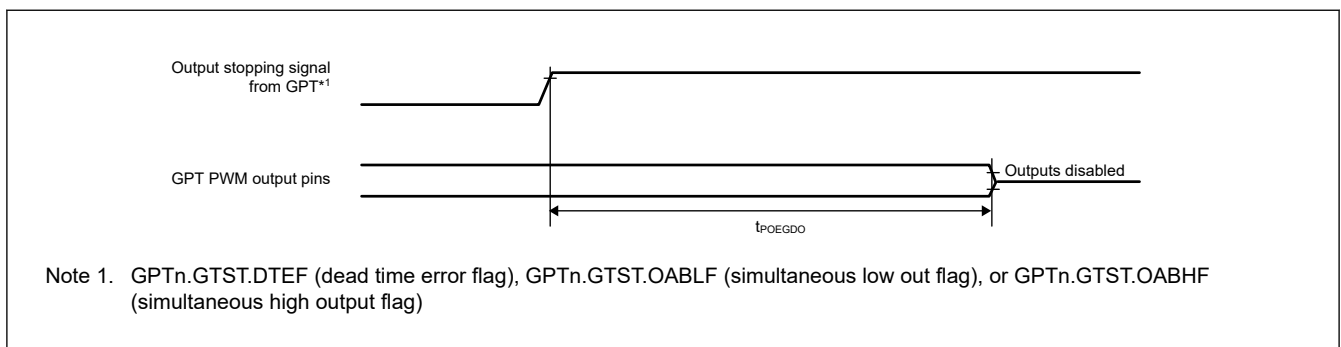


Figure 2.51 Output disable time for POEG in response to detection of the output stopping signal from GPT

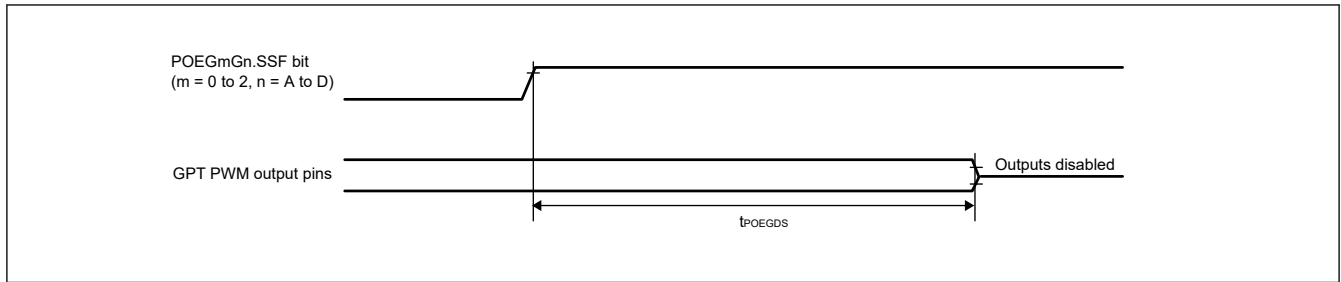


Figure 2.52 Output disable time for POEG in response to the register setting

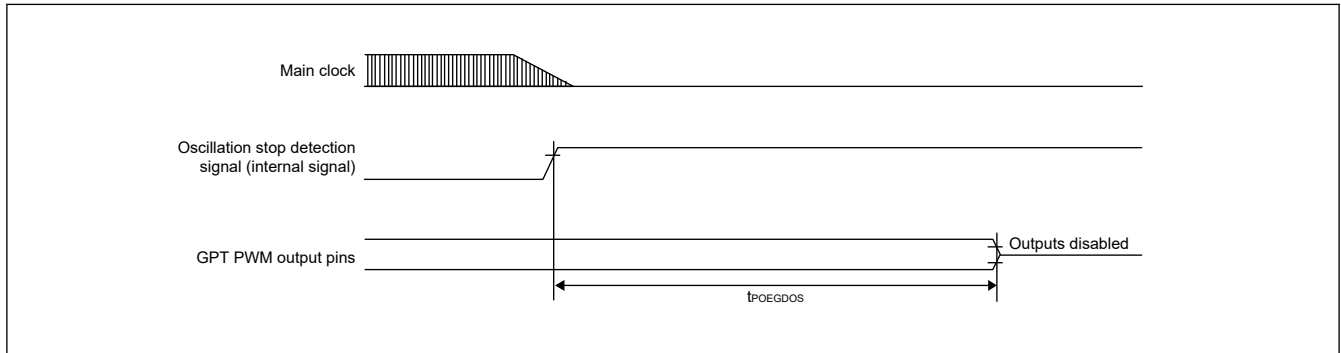


Figure 2.53 Output disable time for POEG in response to the oscillation stop detection

2.5.5.7 A/D Converter Trigger Timing

Table 2.31 A/D converter trigger timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
A/D converter	A/D converter trigger input pulse width	ADTRG0#, ADTRG1# t _{TRGW}	1.5	—	t _{PADCcyc}	Figure 2.54

Note 1. t_{PADCcyc}: PCLKADC cycle

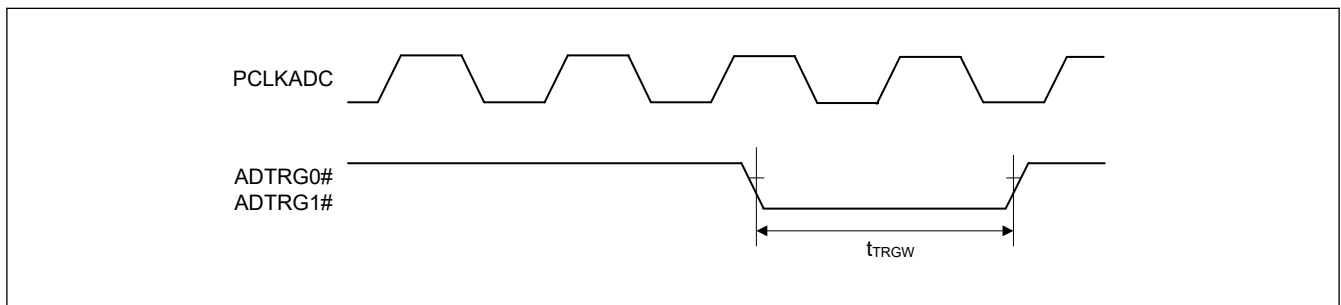


Figure 2.54 A/D converter trigger input timing (ADTRG0#, ADTRG1#)

2.5.5.8 SCI Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (except Simple I2C)

Table 2.32 SCI timing (1 of 2)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SCI (Asynchronous)	Input clock cycle	t_{Scyc}	4	—	$t_{PSClCyc}$	Figure 2.55
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	3	ns	
	Input clock fall time	t_{SCKf}	—	3	ns	
	Output clock cycle	t_{Scyc}	6	—	$t_{PSClCyc}$	
	Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	t_{SCKr}	—	3	ns	
	Output clock fall time	t_{SCKf}	—	3	ns	
SCI (Simple I2C, Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.56
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}^{*1}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
SCI (Simple I2C, Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.56
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$2 \times NF_{cyc}^{*1}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 2.32 SCI timing (2 of 2)

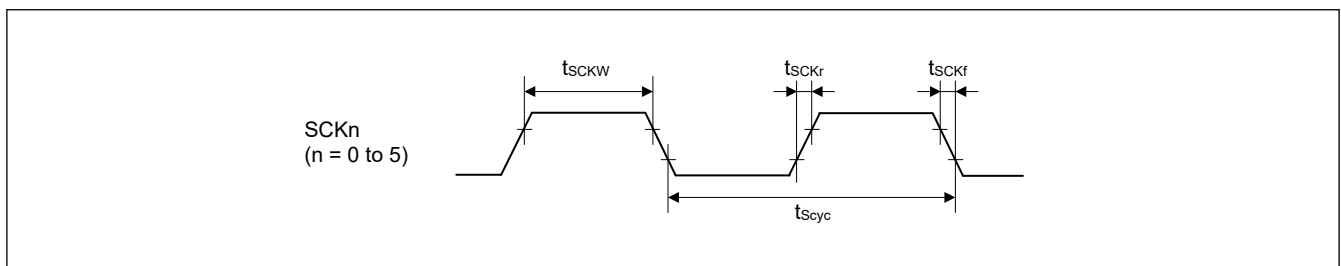
Parameter		Symbol	Min.	Max.	Unit	Reference figure	
SCI (Clock sync, Simple SPI)	SCK output clock cycle (master)	t_{SPCyc}	2	65536	$t_{PSClCyc}$	Figure 2.57 to Figure 2.62	
	SCK input clock cycle (slave)		2	65536			
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPCyc}		
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPCyc}		
	SCK clock rise/fall time	t_{SPCKR} , t_{SPCKF}	—	3	ns		
	Data input setup time	Internal clock	t_{SU}	7	—		ns
		External clock		3	—		
	Data input hold time	Internal clock	t_H	3	—		ns
		External clock		3	—		
	Data output delay time	Internal clock	t_{OD}	—	3		ns
		External clock		—	12		
	Data output hold time	Internal clock	t_{OH}	0	—		ns
		External clock		0	—		
Data rise/fall time		t_{DR} , t_{DF}	—	3	ns		
Slave access time	Internal clock	t_{SA}	—	$3 \times t_{PSClCyc} + 12$	ns		
	External clock		—	$3 \times t_{PSClCyc} + 12$			
Slave output release time	Internal clock	t_{REL}	—	$3 \times t_{PSClCyc} + 12$	ns		
	External clock		—	$3 \times t_{PSClCyc} + 12$			
SCI (Simple SPI)	SS input setup time	t_{LEAD}	1	—	t_{SPCyc}		
	SS input hold time	t_{LAG}	1	—	t_{SPCyc}		
	SS input rise/fall time	t_{SSR} , t_{SSF}	—	3	ns		

Note: $t_{PSClCyc}$: PCLKSCIn cycle

Note 1. $N_{FcyC} = 4^n \times 2^{m-1} \times t_{PSClCyc}$

n: CCR2.CKS[1:0] (n = 0, 1, 2, 3)

m: CCR1.NFCS[2:0] (m = 1, 2, 3, 4)

**Figure 2.55 SCK clock input/output timing**

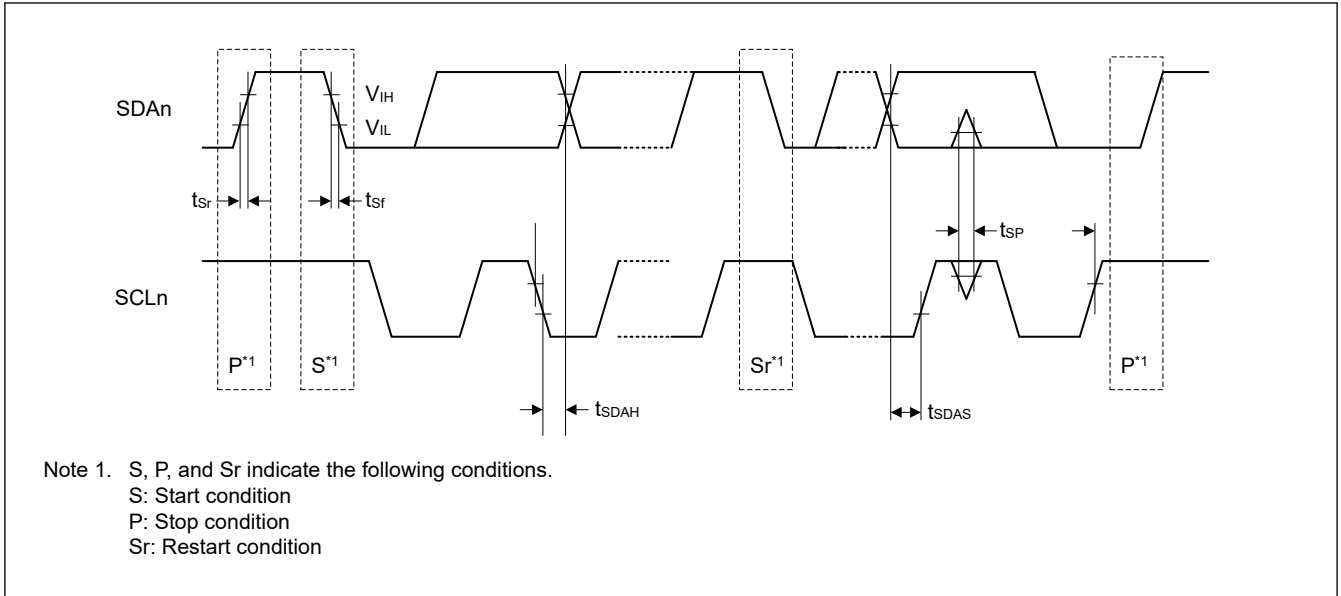


Figure 2.56 SCI simple I2C mode timing

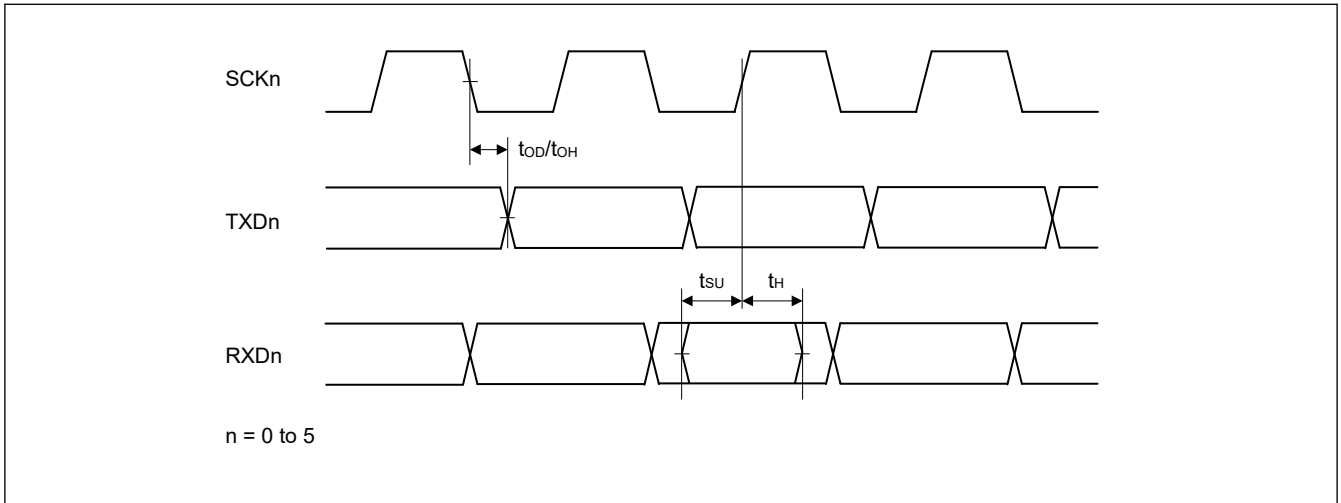


Figure 2.57 SCI input/output timing in clock synchronous mode

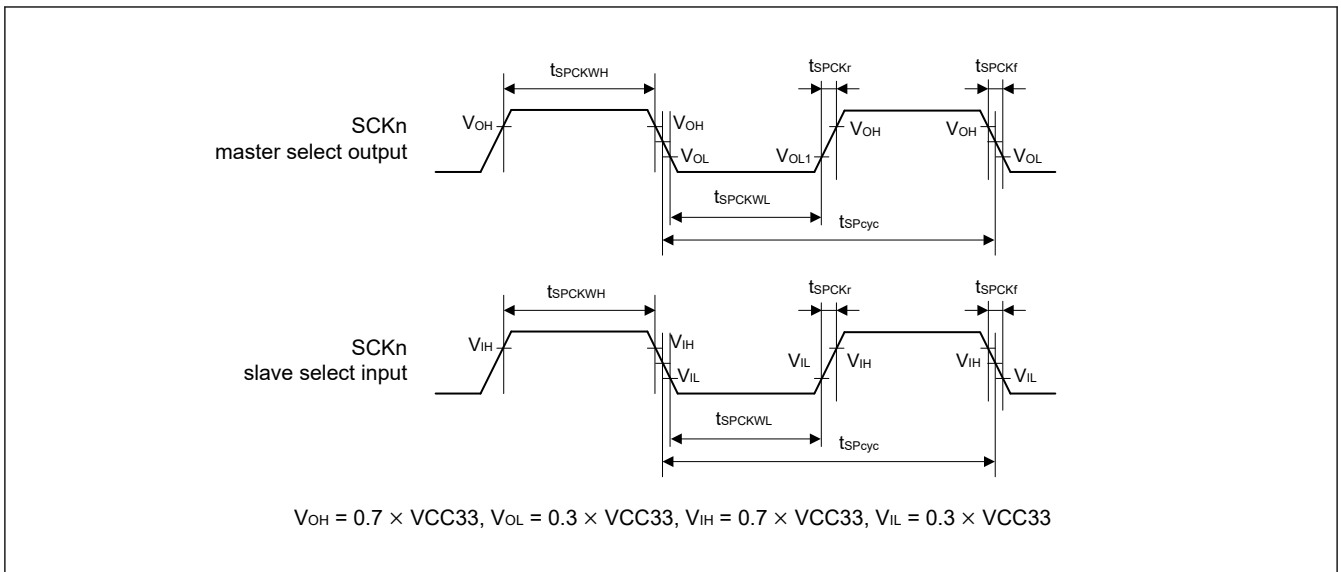


Figure 2.58 SCI simple SPI mode clock timing

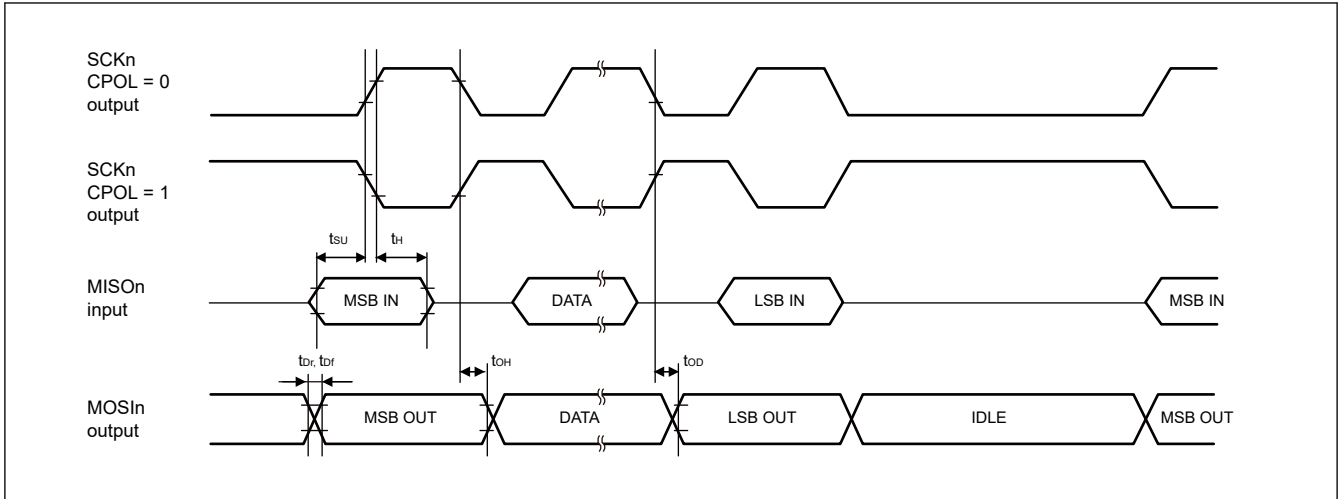


Figure 2.59 SCI simple SPI mode timing for master when CPHA = 0

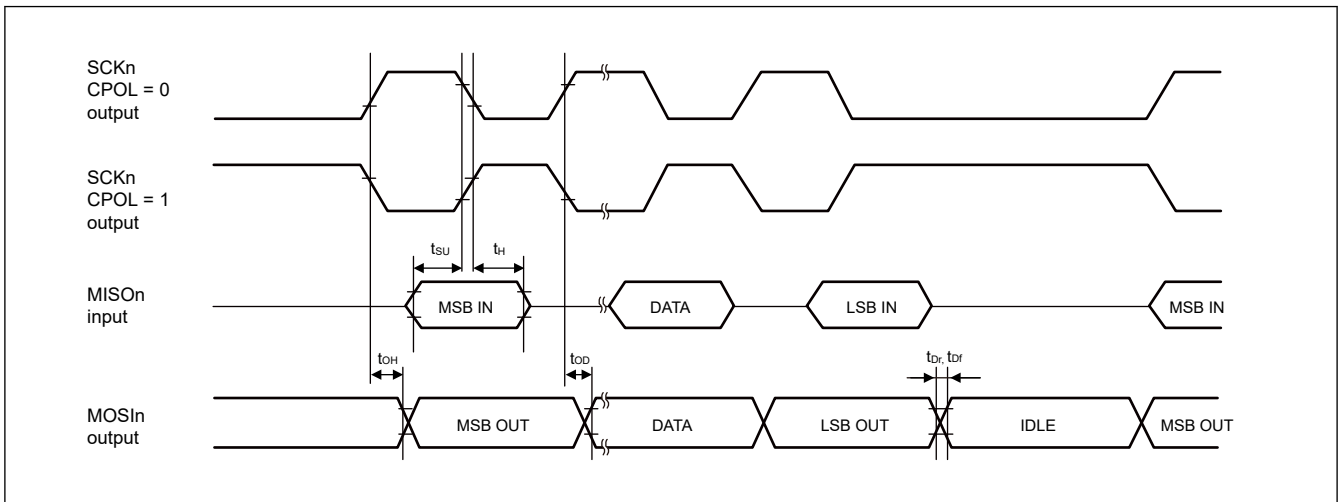


Figure 2.60 SCI simple SPI mode timing for master when CPHA = 1

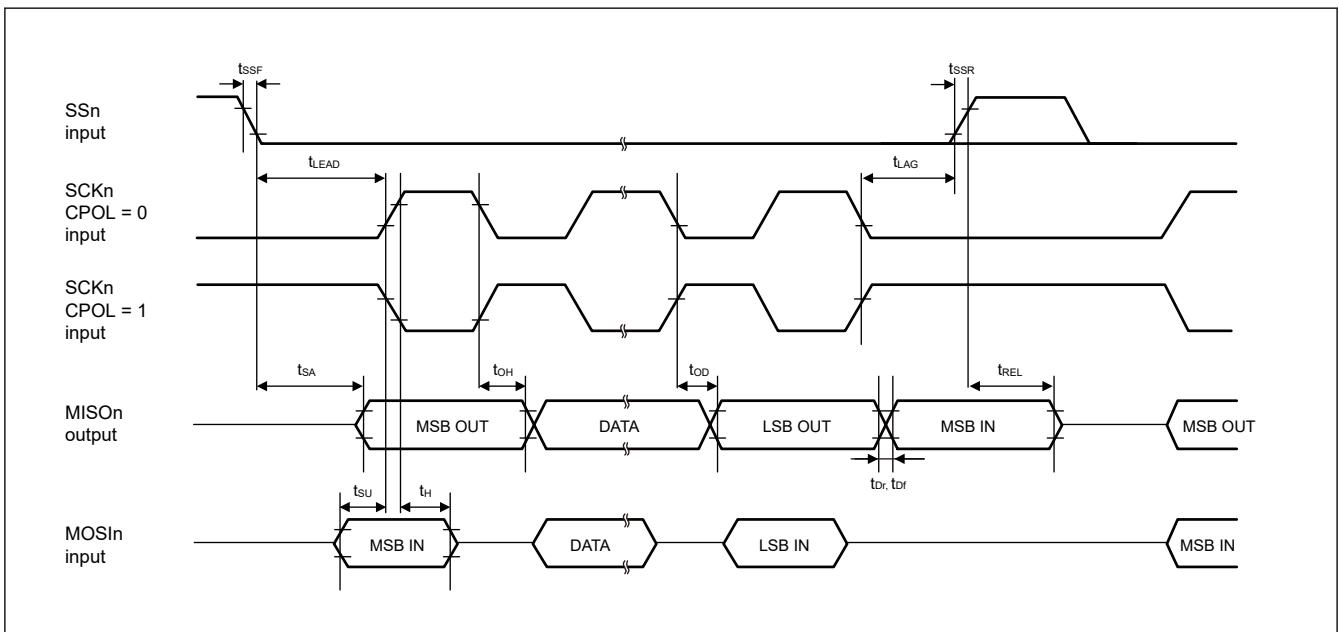


Figure 2.61 SCI simple SPI mode timing for slave when CPHA = 0

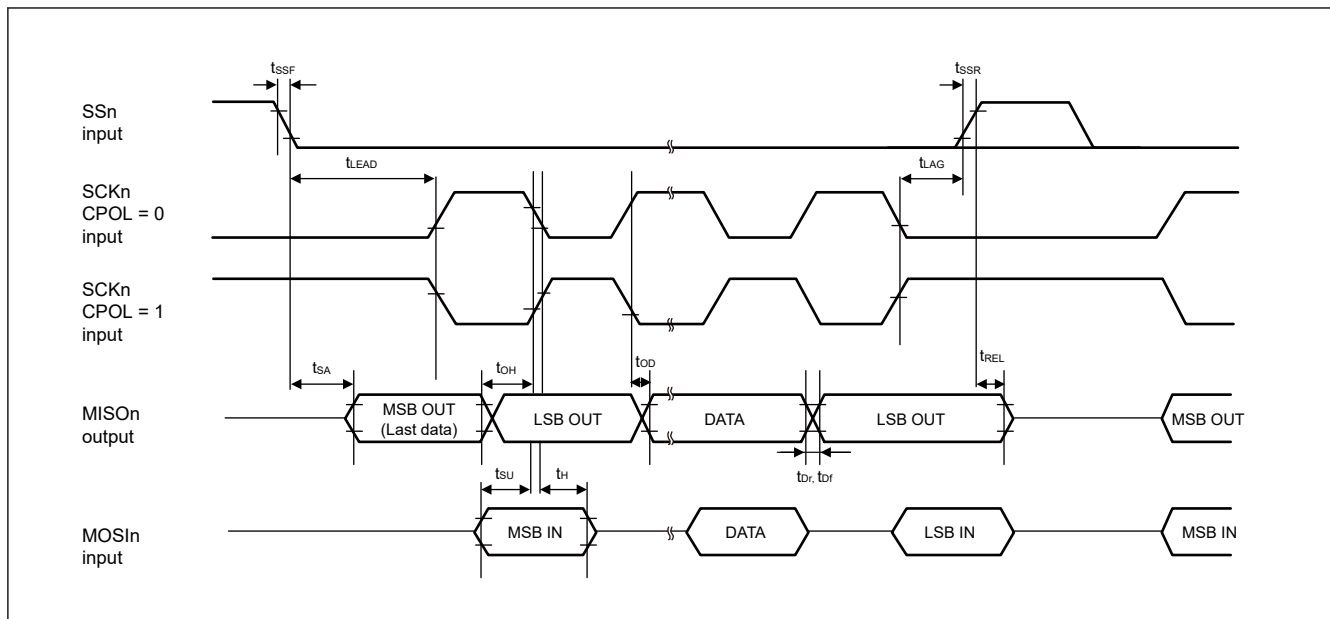


Figure 2.62 SCI simple SPI mode timing for slave when CPHA = 1

2.5.5.9 IIC Timing

Conditions: $V_{OL} = 0.4\text{ V}$, $I_{OL} = 4\text{ mA}$

Table 2.33 IIC timing

Parameter		Symbol	Min.*1 *2	Max.*1 *2	Unit	Reference figure
IIC (Standard-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 2.63
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc} : IIC internal reference clock (IIC Φ) cycle

Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.

Note 3. C_b is the total capacitance of the bus lines.

Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode.

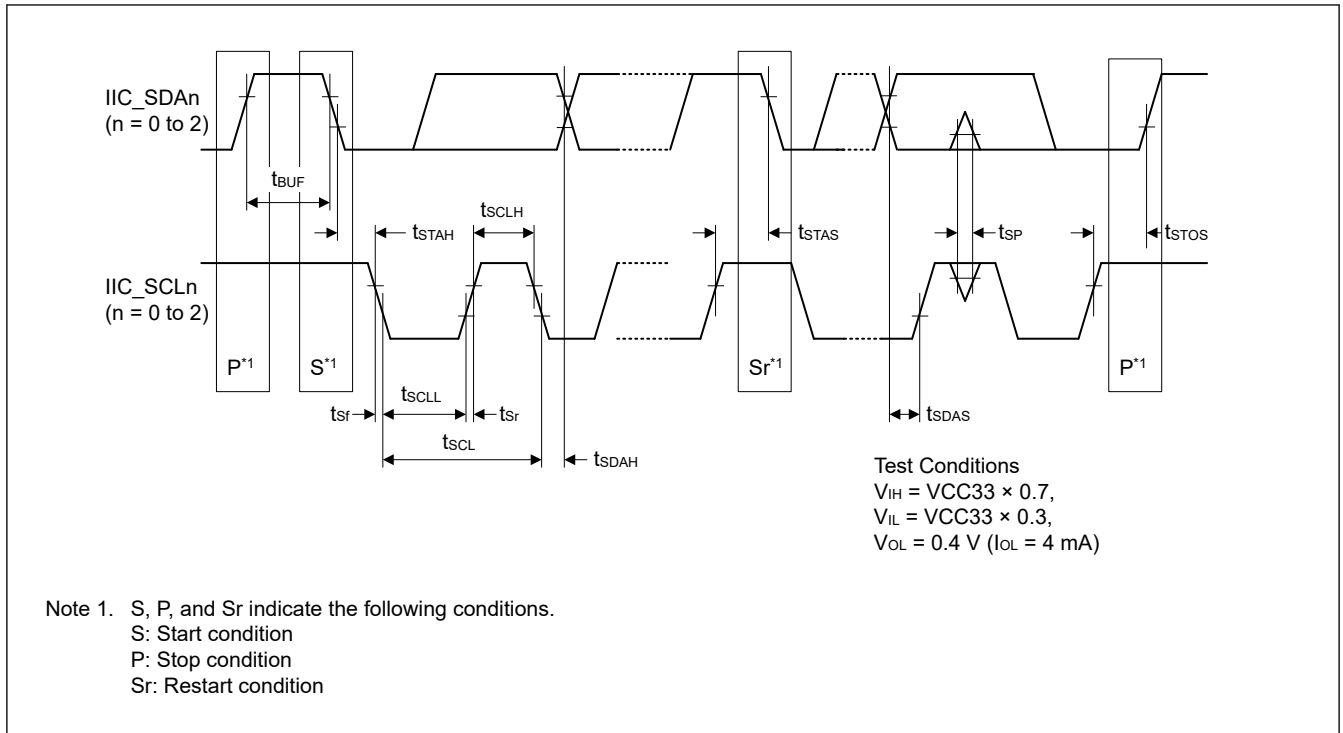


Figure 2.63 IIC bus interface input/output timing

2.5.5.10 CANFD Timing

Table 2.34 CANFD timing

Parameter	Symbol	CAN		CANFD		Unit	Reference figure
		Min.	Max.	Min.	Max.		
CANFD Internal delay time	t_{node}	—	100	—	50	ns	Figure 2.64
Transmission rate	—	—	1	—	8	Mbps	

Note: Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

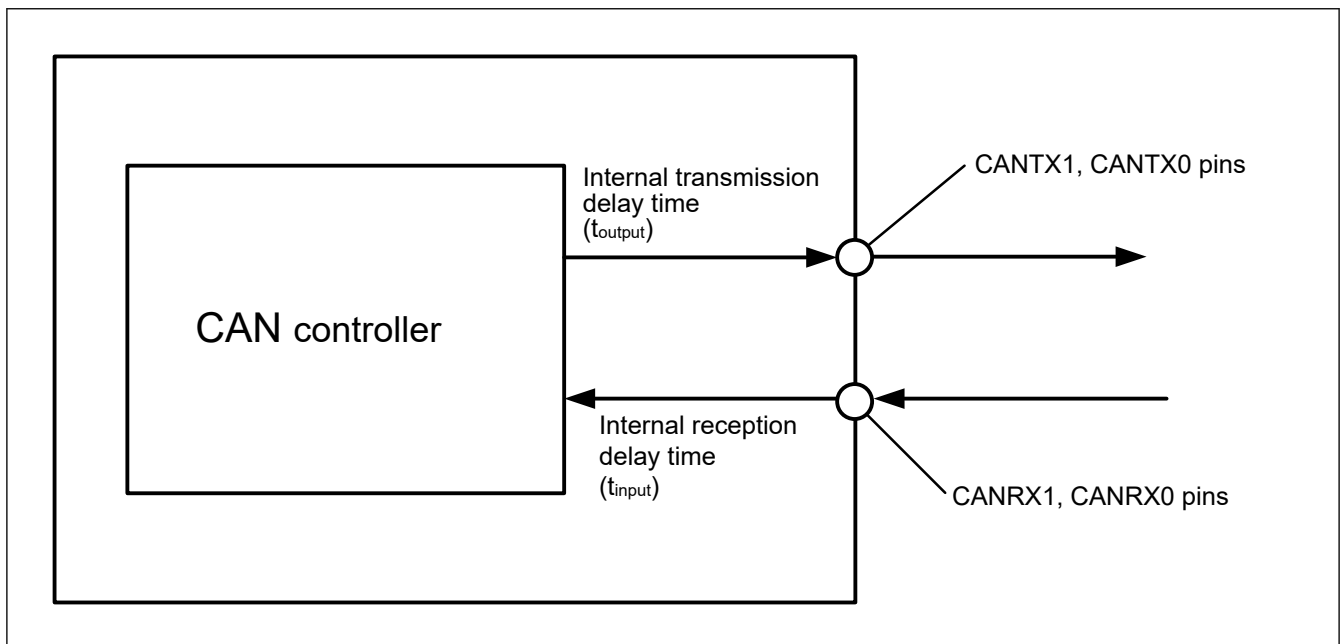


Figure 2.64 CAN interface condition

2.5.5.11 SPI Timing

Table 2.35 SPI timing (1 of 2)Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 30$ pF

Parameter		Symbol	Min.*1	Max.*1	Unit*1	Reference figure	
RSPCK clock cycle	Master	t_{SPCyc}	2	4096	t_{SPICyc}	Figure 2.65	
	Slave		2	4096			
RSPCK clock high level pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 2.5$	—	ns		
	Slave		1	—	t_{SPICyc}		
RSPCK clock low level pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 2.5$	—	ns		
	Slave		1	—	t_{SPICyc}		
RSPCK clock rising/falling time	Output	t_{SPCKr}	—	3	ns		
	Input	t_{SPCKf}	—	1	ns		
Data input setup time	Master	t_{SU}	5	—	ns		Figure 2.66 to Figure 2.72
	Slave		3	—			
Data input hold time	Master	t_H	3	—	ns		
	Slave		3	—			
SSL setup time	Master	t_{LEAD}	$N \times t_{SPCyc} - 3^{*2}$	$N \times t_{SPCyc} + 3^{*2}$	ns		Figure 2.66 to Figure 2.69
	Slave		4	—	t_{SPICyc}		
SSL hold time	Master	t_{LAG}	$N \times t_{SPCyc} - 3^{*3}$	$N \times t_{SPCyc} + 3^{*3}$	ns		
	Slave		4	—	t_{SPICyc}		
Continuous transmission delay	Master	t_{TD}	$t_{SPCyc} + 2 \times t_{SPICyc}$	$8 \times t_{SPCyc} + 2 \times t_{SPICyc}$	ns		
	Slave		$t_{SPCyc} + 5 \times t_{SPICyc}$	—			
TI-SSP SS input setup time		t_{TISS}	3	—	ns	Figure 2.70 to Figure 2.72	
TI-SSP SS input hold time		t_{TISH}	3	—	ns		
TI-SSP next access time		t_{TIND}	M^{*4}	—	t_{SPICyc}		
TI-SSP Master SS output delay		t_{TISSOD}	-3	3	ns		
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns		
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns		
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	12	ns		
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	8	ns		
Data output delay time	Master	t_{OD}	—	3	ns		Figure 2.66 to Figure 2.72
	Slave		—	12	ns		
Data output hold time	Master	t_{OH}	-3	—	ns		
	Slave		3	—			
MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	3	ns		
	Input		—	1	μs		
SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	3	ns	Figure 2.66, Figure 2.67	
	Input		—	1	μs		

Table 2.35 SPI timing (2 of 2)

Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 30$ pF

Parameter	Symbol	Min.*1	Max.*1	Unit*1	Reference figure
Slave access time	t_{SA}	—	12	ns	Figure 2.68, Figure 2.69
Slave output release time	t_{REL}	—	12	ns	

- Note 1. t_{SP1cyc} : PCLKSPI_n cycle
- Note 2. SPCKD set value + 1 (1 to 8)
- Note 3. SSLND set value + 1 (1 to 8)
- Note 4. SSLND set value + 2 (2 to 9)

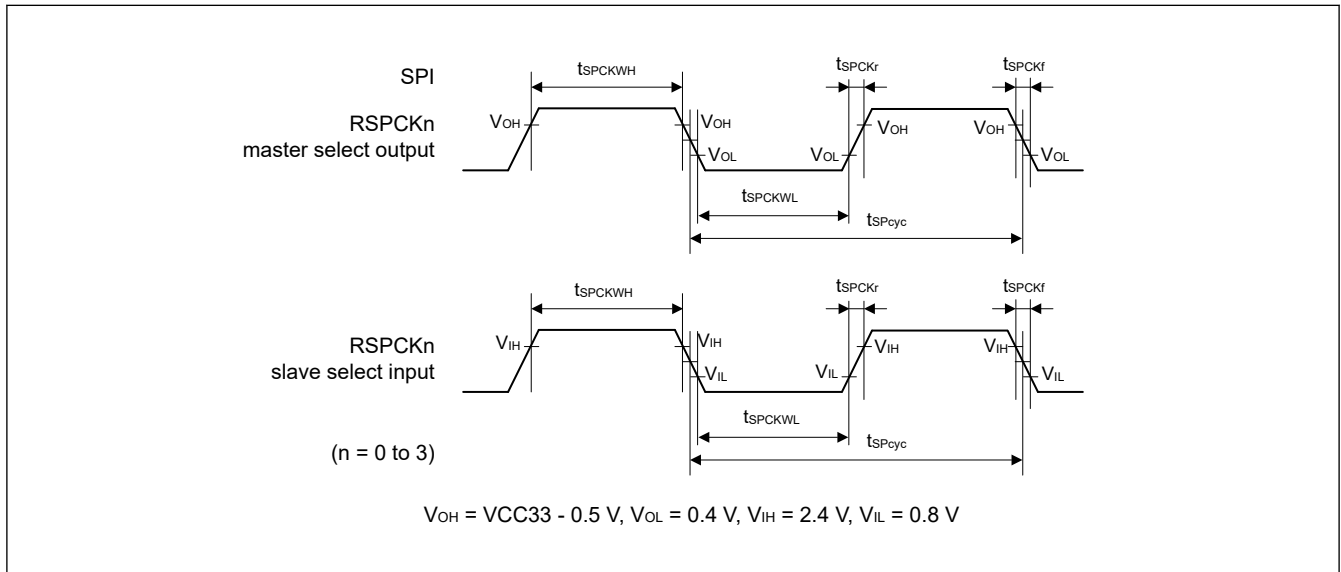


Figure 2.65 SPI clock timing

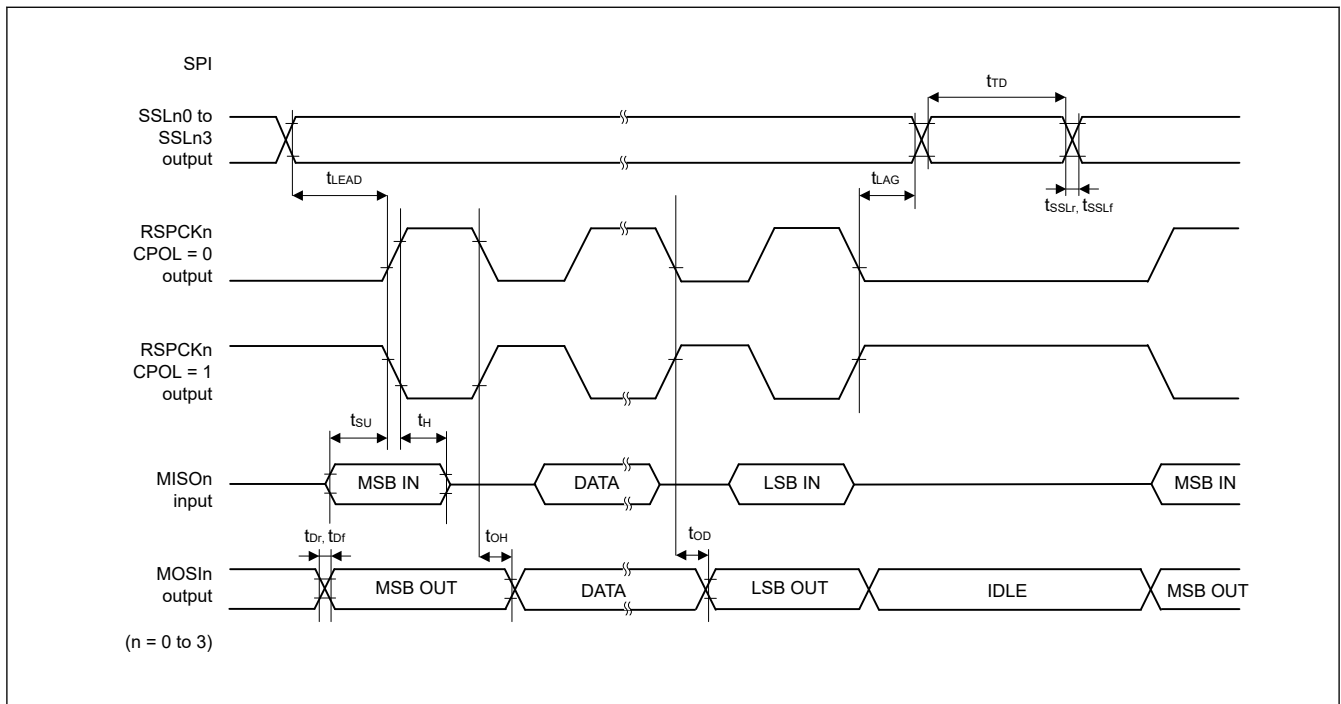


Figure 2.66 SPI timing (Master, Motorola SPI, CPHA = 0)

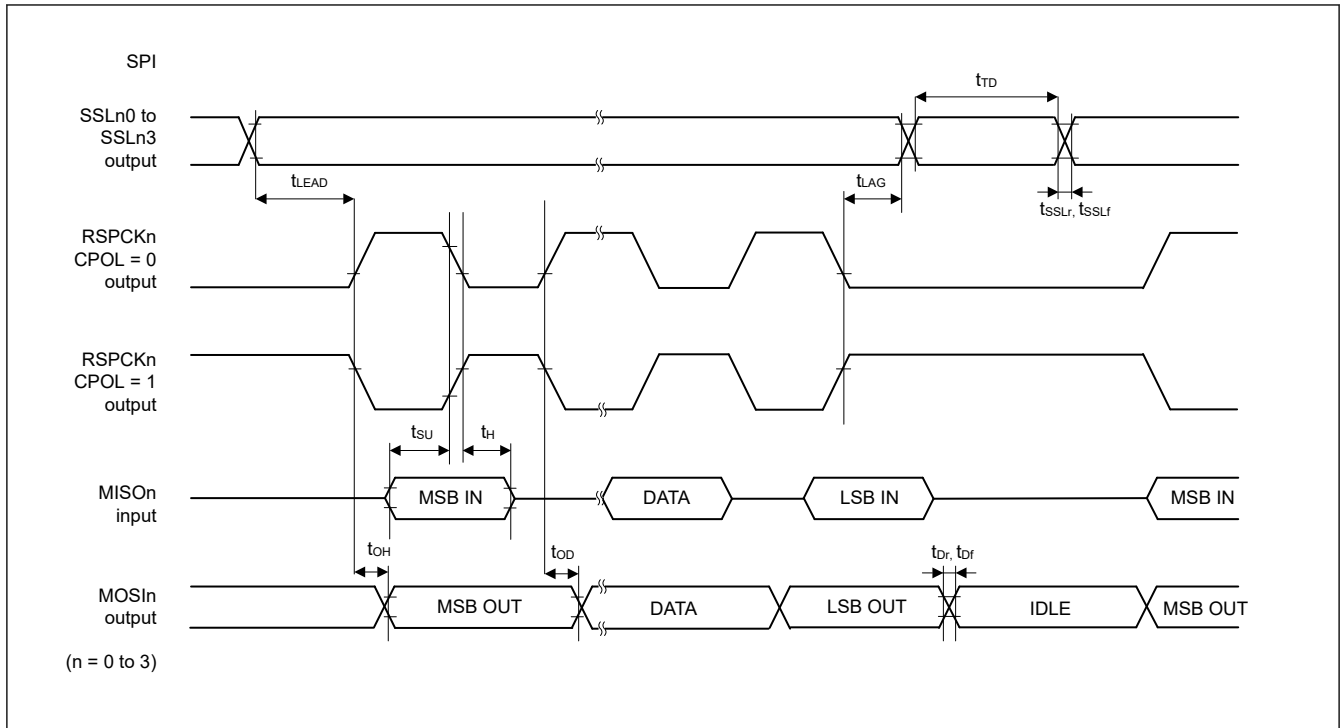


Figure 2.67 SPI timing (Master, Motorola SPI, CPHA = 1)

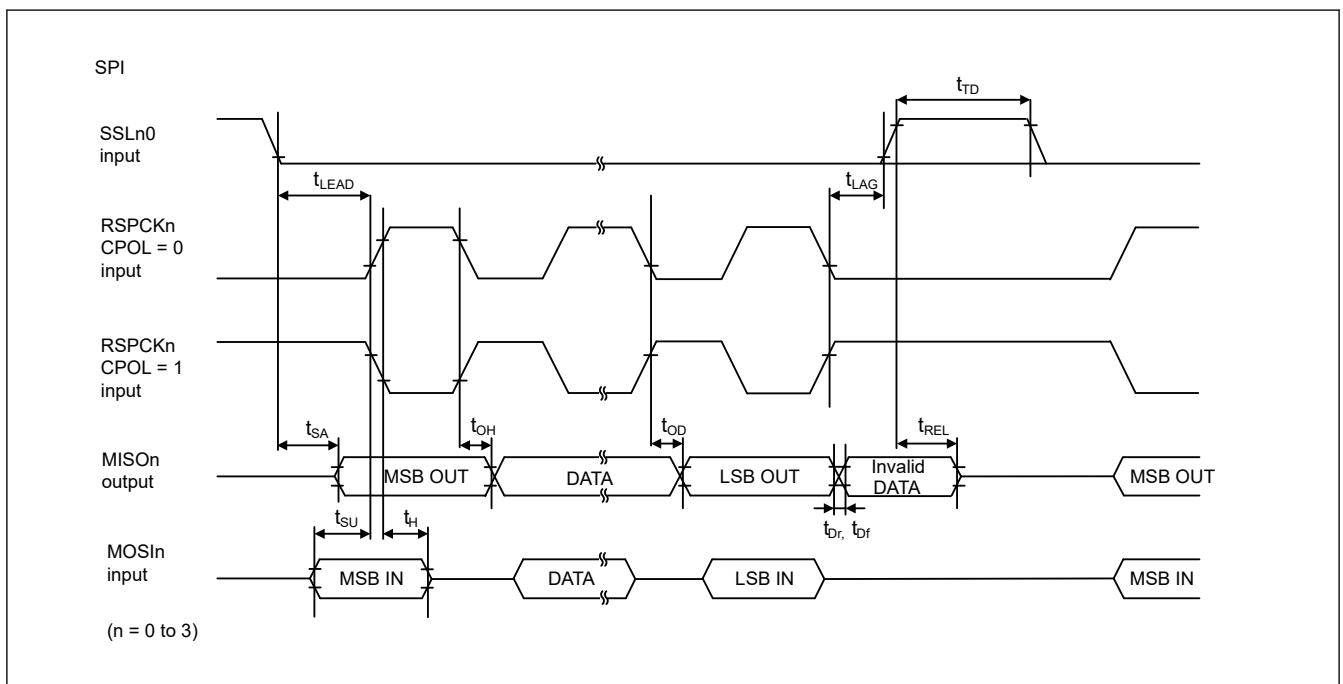


Figure 2.68 SPI timing (Slave, Motorola SPI, CPHA = 0)

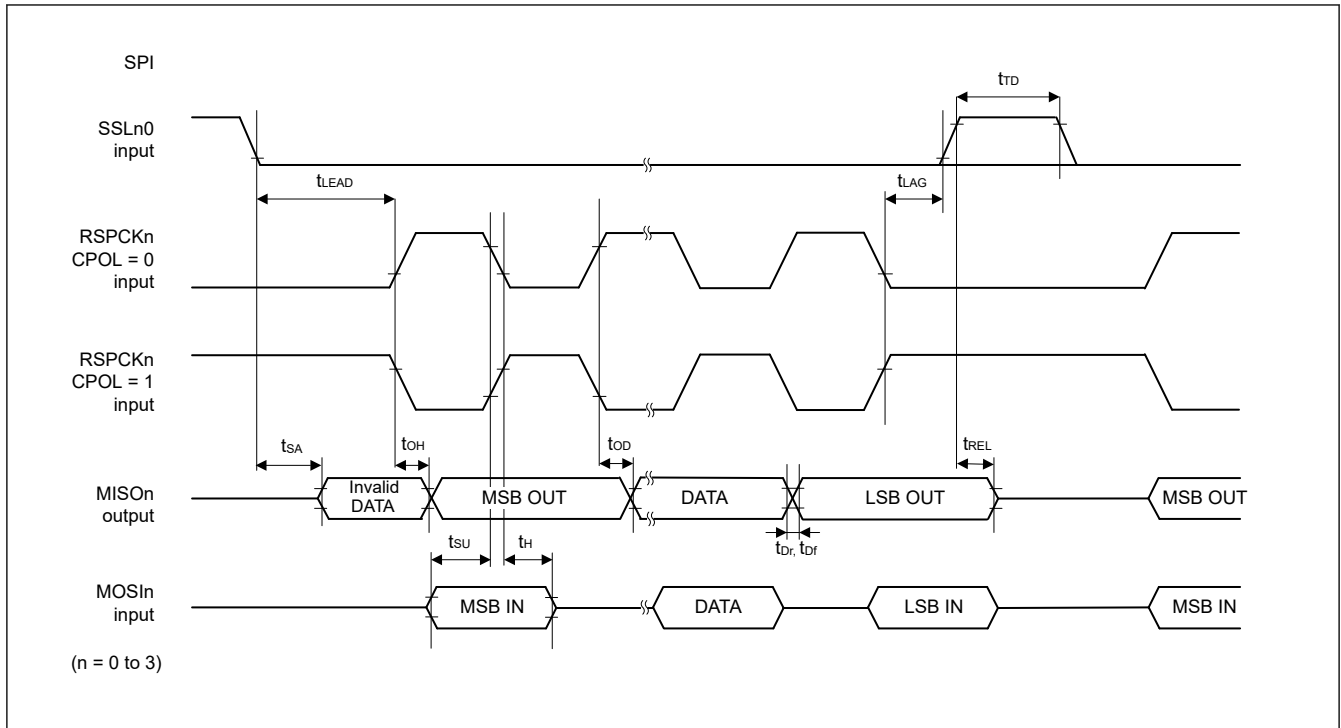


Figure 2.69 SPI timing (Slave, Motorola SPI, CPHA = 1)

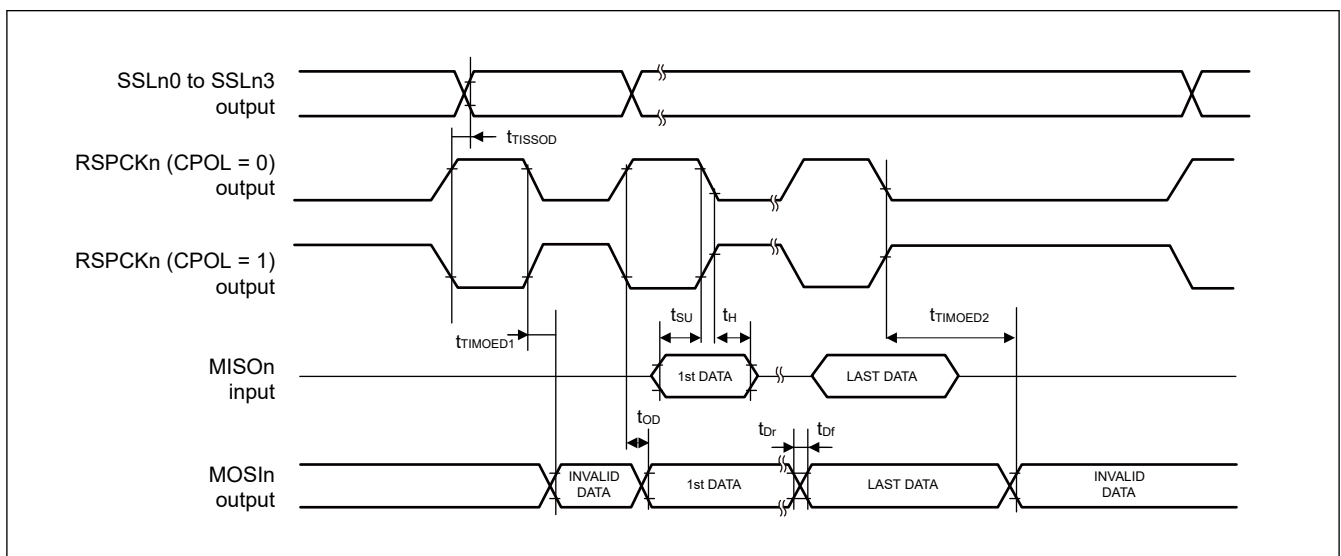


Figure 2.70 SPI timing (Master, TI SSP)

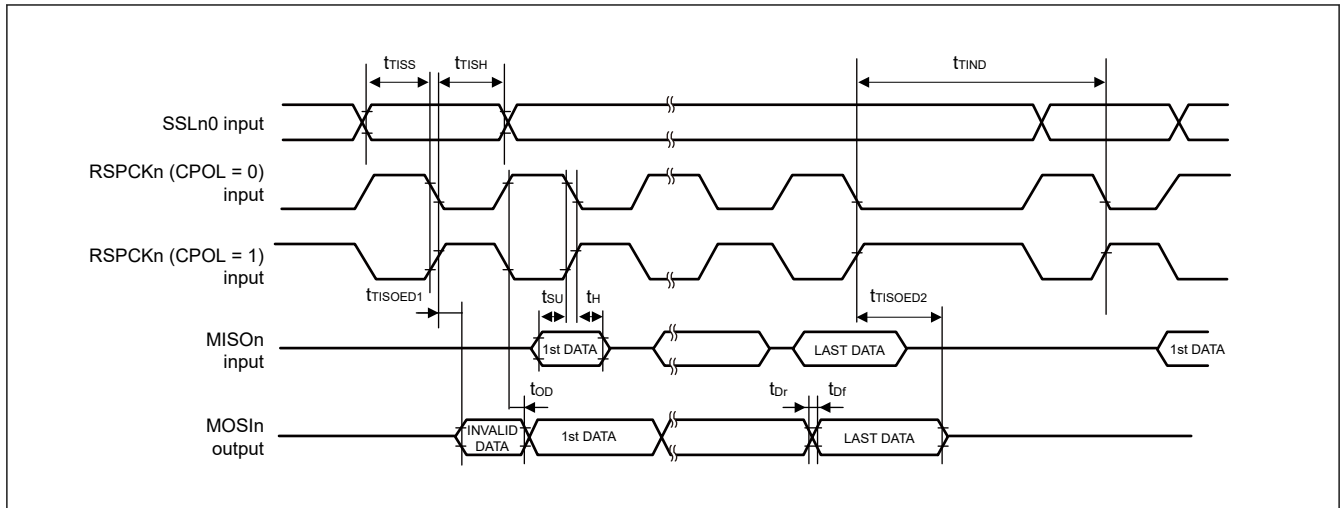


Figure 2.71 SPI timing (Slave, TI-SSP, with delay in burst transfer)

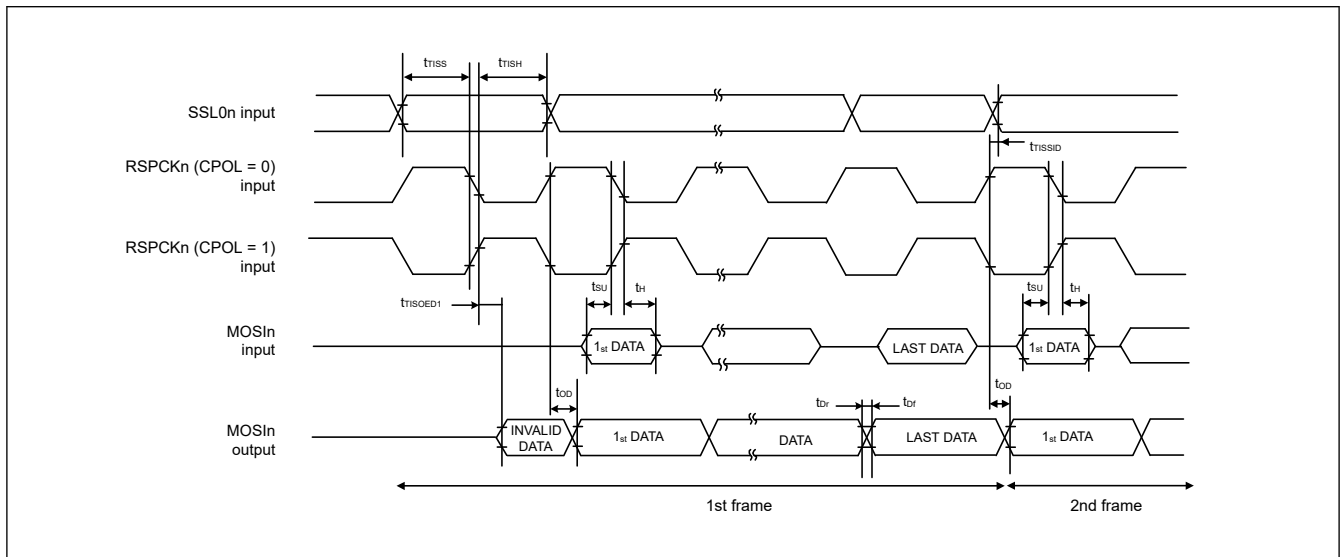


Figure 2.72 SPI timing (Slave, TI-SSP, without delay in burst transfer)

2.5.5.12 xSPI Timing

Conditions:

Single end Clock

$$V_{OH} = V_{CC18} \times 0.5, V_{OL} = V_{CC18} \times 0.5, C = 15 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 15 \text{ pF (3.3 V)}$$

Data

$$V_{OH} = V_{CC18} \times 0.5, V_{OL} = V_{CC18} \times 0.5, C = 15 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 15 \text{ pF (3.3 V)}$$

Table 2.36 xSPI timing

Parameter	Symbol	1.8 V		3.3 V		Unit	Reference figure	
		Min.	Max.	Min.	Max.			
Cycle time	SDR	t_{PERIOD}	7.5	—	13.3	—	ns	Figure 2.73
	DDR		10.0	—	13.3	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56 ^{*2}	—	0.56	—	V/ns	
Clock Duty cycle distortion		t_{CKDCD}	0.0	$t_{PERIOD} \times 0.05$	0.0	$t_{PERIOD} \times 0.05$	ns	
Clock Minimum Pulse width		t_{CKMPW}	$t_{PERIOD} \times 0.45$	—	$t_{PERIOD} \times 0.45$	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	$0.4 \times VCC18$	$0.6 \times VCC18$	—	—	V	
DS Duty cycle distortion		t_{DSDCD}	0.0	$t_{PERIOD} \times 0.04$	0.0	$t_{PERIOD} \times 0.04$	ns	
DS Minimum Pulse width		t_{DSMPW}	$t_{PERIOD} \times 0.41$	—	$t_{PERIOD} \times 0.41$	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56 ^{*2}	—	0.56	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.4	—	ns	Figure 2.74
Data input hold time (to CK)		t_H	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.0 ^{*3}	—	1.4 ^{*3}	ns	
Data output hold time		t_{OH}	-1.0	—	-2.3	—	ns	
Data output buffer off time		t_{BOFF}	-1.0	—	-2.3	—	ns	
Data input setup time (to DS)	DDR ^{*1} ^{*3}	t_{SU}	-0.8	—	-0.8	—	ns	Figure 2.75, Figure 2.76
Data input hold time (to DS)		t_H	$t_{PERIOD} \times 0.41 - 0.8$	—	$t_{PERIOD} \times 0.41 - 0.8$	—	ns	
Data output setup time (to CK)		t_{SUO}	1.0	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	1.0	—	1.0	—	ns	
CS Low to Clock High		t_{CSLCKH}	6.0/8.0 ^{*2} ^{*4}	—	8.0 ^{*4}	—	ns	Figure 2.74 to Figure 2.76
Clock Low to CS High		t_{CKLCSH}	6.0/8.0 ^{*2}	—	8.0	—	ns	
CS High time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS Low to CS High		t_{DSLCSH}	6.0/8.0 ^{*2}	—	10.6	—	ns	Figure 2.77
CS High to DS Tri-State		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS Low to DS Low		t_{CSLDSL}	0.0	—	0.0	—	ns	
DS Tri-State to CS Low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 01000b for xSPI200.

Note 2. Specification at 133 MHz / Specification at 100 MHz

Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1).

Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1).

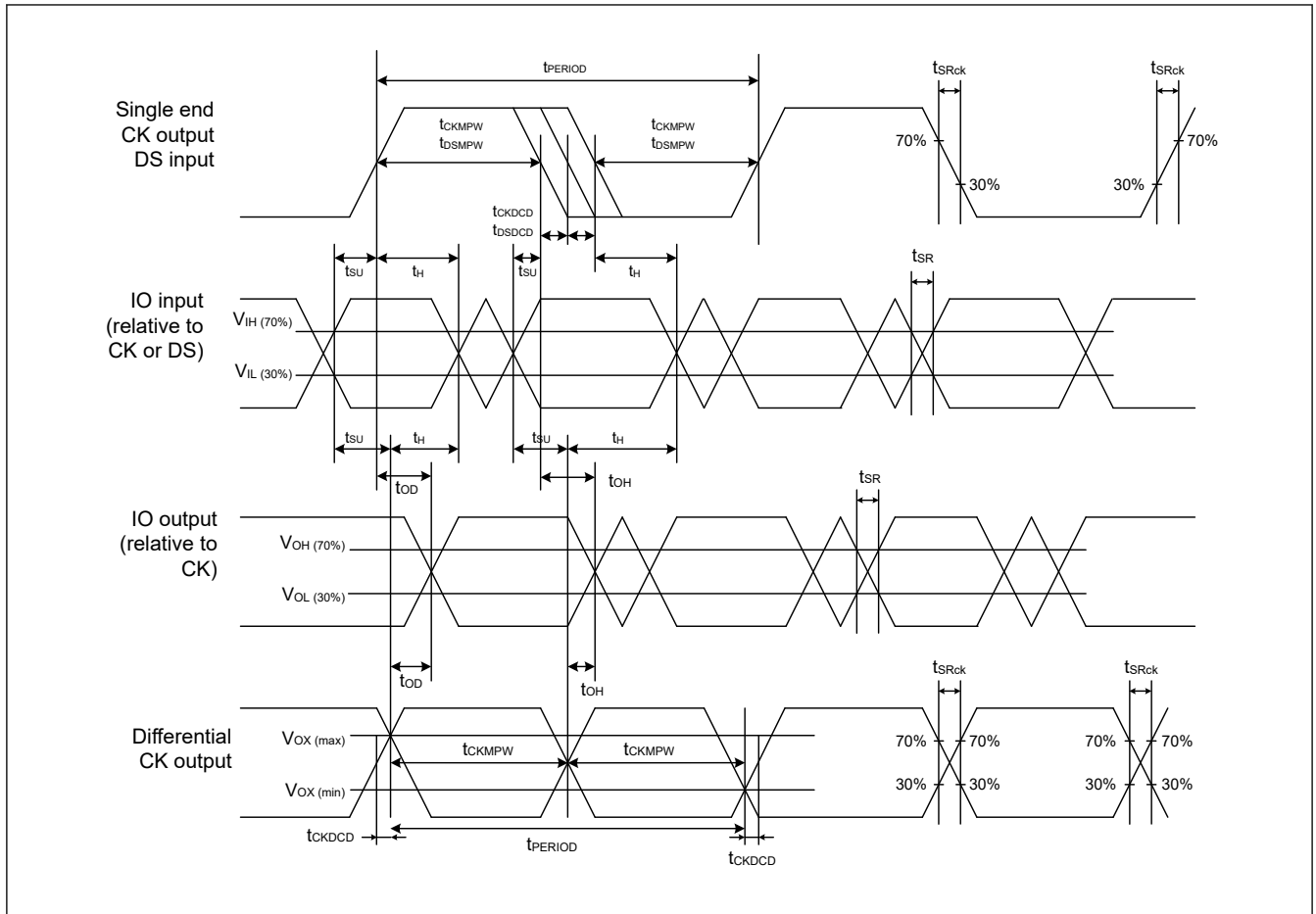


Figure 2.73 xSPI clock / DS timing

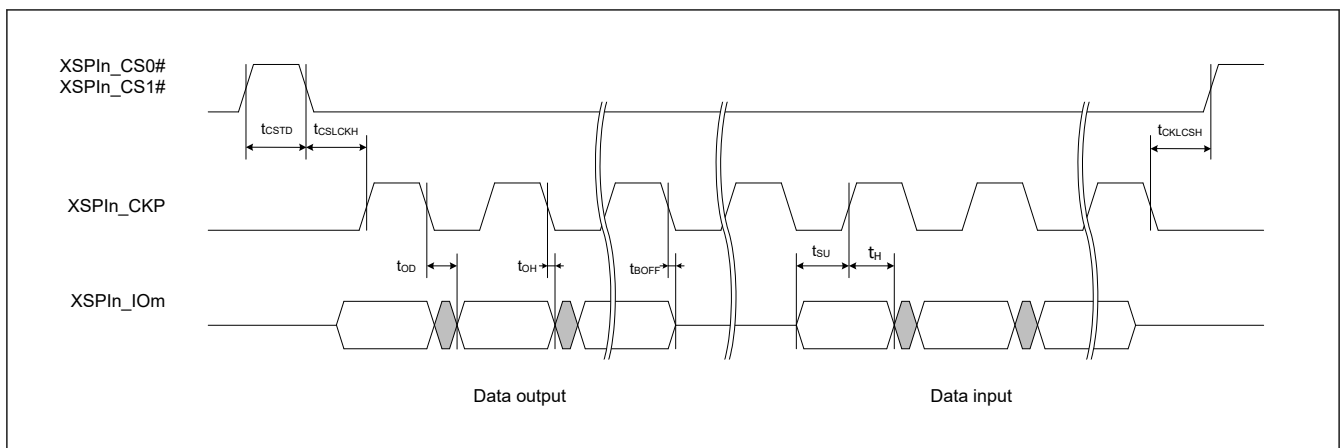


Figure 2.74 SDR transmit/receive timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

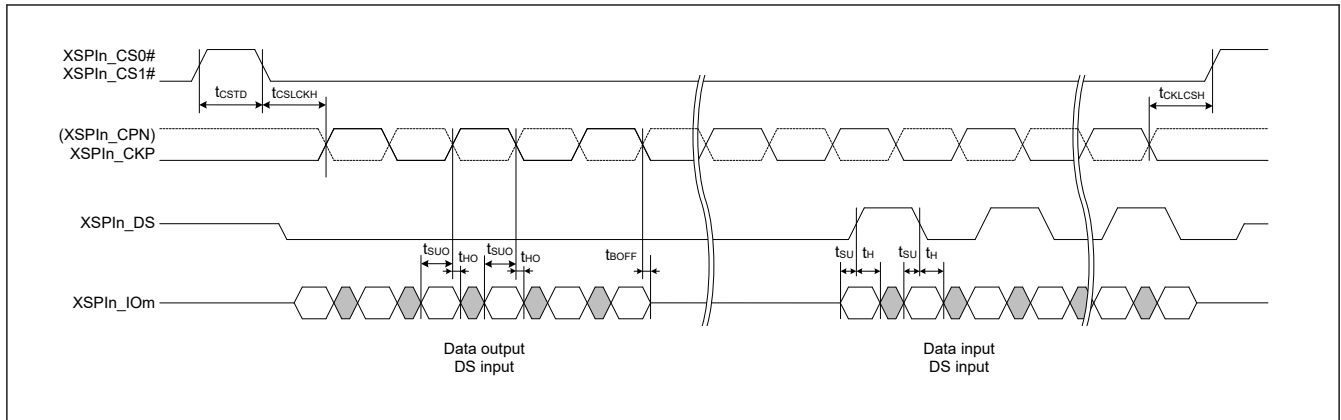


Figure 2.75 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

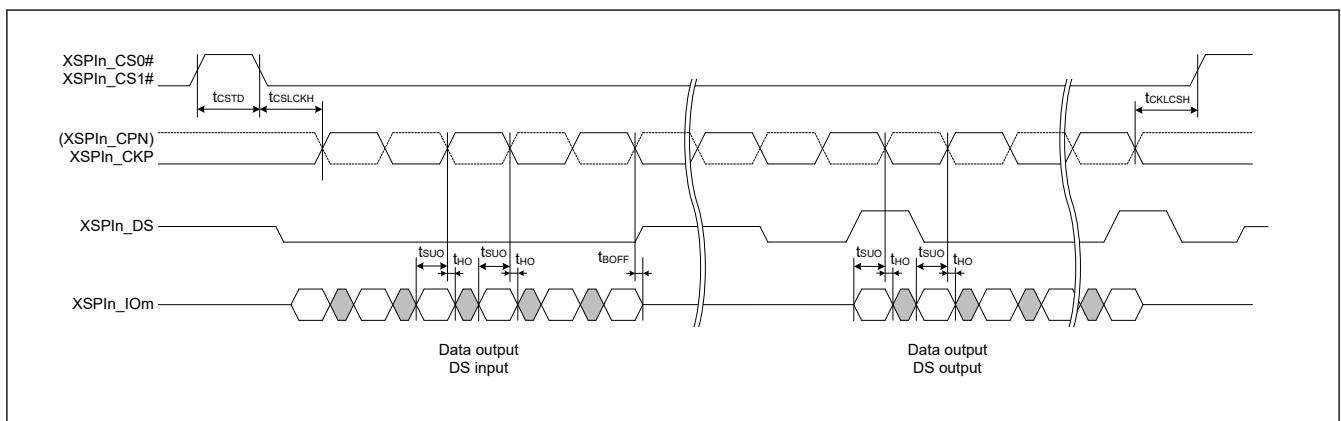


Figure 2.76 DDR transmit/receive timing (HyperRAM write)

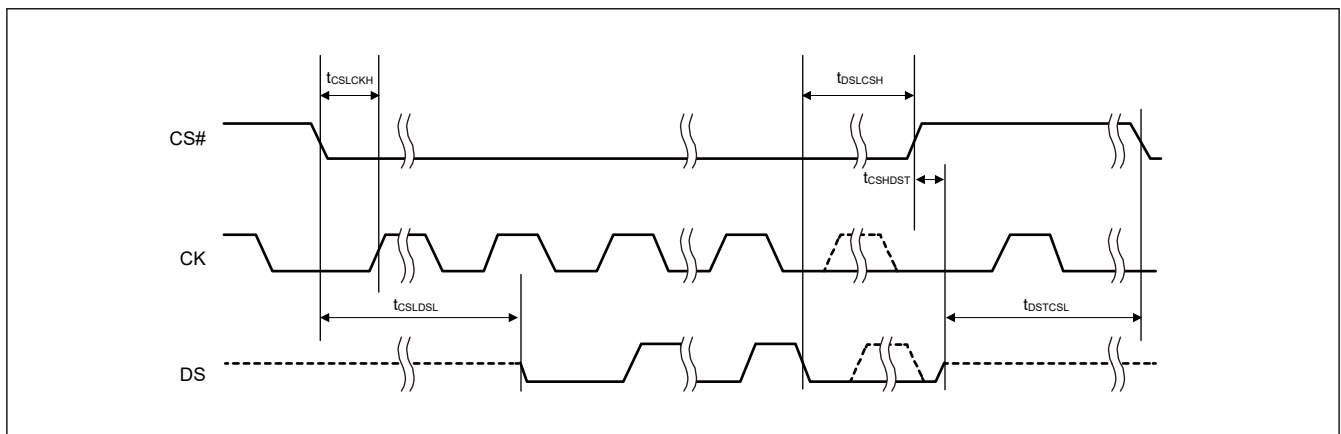


Figure 2.77 DS to CS signal timing

2.5.5.13 Delta-Sigma Interface Timing

Conditions: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$, $C = 30$ pF

Table 2.37 ΔΣ interface timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure	
DSMIF	Clock cycle	Master	t_{DSyc}	40	200	ns	Figure 2.78
		Slave		40	200		
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—		
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—		
Setup time	Master	t_{SU}	15	—	ns	Figure 2.79, Figure 2.80	
	Slave		10	—			
Hold time	Master	t_H	0	—	ns		
	Slave		10	—			

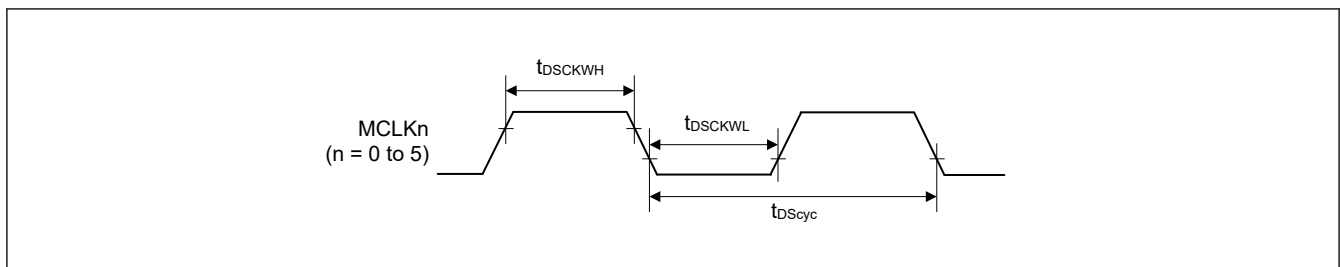


Figure 2.78 Clock input/output timing

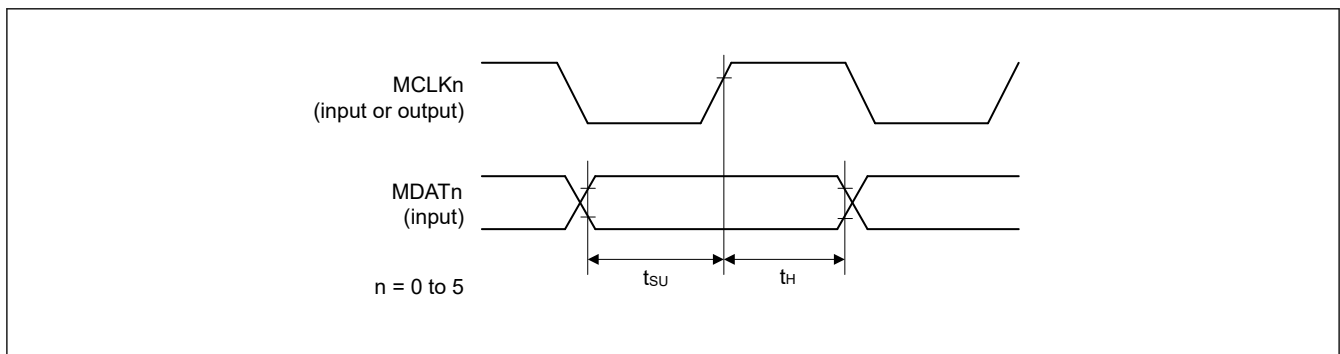


Figure 2.79 Reception timing (MCLKn rising synchronous)

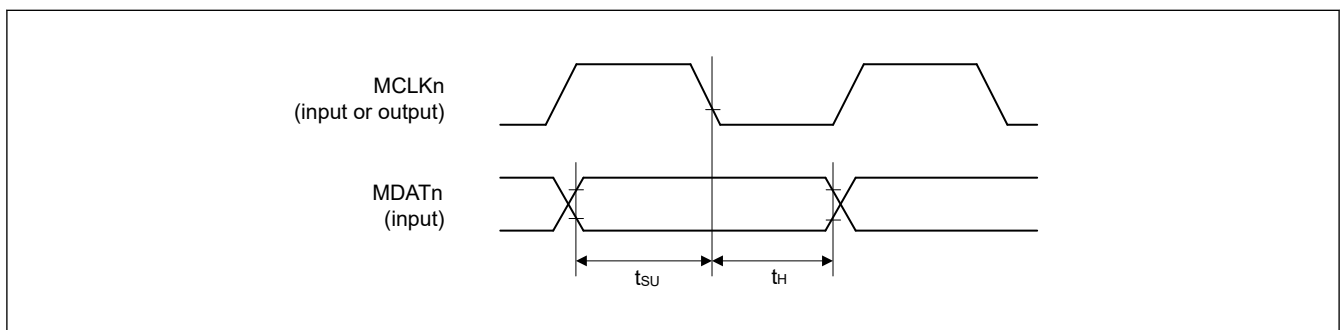


Figure 2.80 Reception timing (MCLKn falling synchronous)

2.5.5.14 Ethernet Interface Timing

Conditions:

$$V_{OH} = V_{CC18} \times 0.5, V_{OL} = V_{CC18} \times 0.5, C = 15 \text{ pF (RGMII)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 25 \text{ pF (RMII)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 30 \text{ pF (MII)}$$

Table 2.38 Ethernet interface timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure	
Ethernet (RGMII)	ETHn_TXCLK, ETHn_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 2.81
		100 Mbps		36	44		
		10 Mbps		360	440		
	ETHn_TXCLK, ETHn_RXCLK frequency	1 Gbps	—	125 – 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 – 50 ppm	25 + 50 ppm		
		10 Mbps		2.5 – 50 ppm	2.5 + 50 ppm		
	ETHn_TXCLK, ETHn_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60		
	ETHn_TXCLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL), ETHn_RXCLK, ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) rise/fall time		t_{RGMIIr} , t_{RGMIIl}	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) to ETHn_TXCLK output skew		$t_{RGMIIos}$	-0.5	0.5	ns	
ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) setup time		$t_{RGMIIls}$	1	—	ns		
ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) hold time		t_{RGMIIh}	1	—	ns		
Ethernet (RMII)	ETHn_RXCLK cycle time		t_{RMIIck}	20	—	ns	Figure 2.82
	ETHn_RXCLK frequency Typ. 50 MHz		—	50 – 50 ppm	50 + 50 ppm	MHz	
	ETHn_RXCLK duty		—	35	65	%	
	ETHn_RXCLK rise/fall time		$t_{RMIIckr}$, $t_{RMIIckf}$	0.5	3.5	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN output delay time		t_{RMIIld}	2.5	12	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time		t_{RMIIls}	4	—	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) hold time		t_{RMIIh}	2	—	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN, ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) rise/fall time		t_{RMIIr} , t_{RMIIl}	0.5	4	ns	
Ethernet (MII)	ETHn_TXCLK, ETHn_RXCLK cycle time	100 Mbps	t_{MIck}	40	—	ns	Figure 2.83
		10 Mbps		400	—		
	ETHn_TXCLK, ETHn_RXCLK frequency	100 Mbps	—	25 – 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 – 50 ppm	2.5 + 50 ppm		
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN, ETHn_TXER output delay time		t_{MIld}	1	20	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER setup time		t_{MIls}	10	—	ns	
ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER hold time		t_{MIlh}	10	—	ns		

Table 2.39 Ethernet interface timing (MAC to MAC connection mode)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETH2_TXCLK, ETH2_RXCLK cycle time	$t_{MRGMIIck}$	7.2	8.8	ns	Figure 2.84
	ETH2_TXCLK, ETH2_RXCLK frequency Typ. 125 MHz	—	125 – 50 ppm	125 + 50 ppm	MHz	
	ETH2_TXCLK, ETH2_RXCLK duty cycle	—	45	55	%	
	ETH2_TXCLK, ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL), ETH2_RXCLK, ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) rise/fall time	$t_{MRGMIIr}$, $t_{MRGMIIl}$	—	0.75	ns	
	ETH2_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) output skew	$t_{MRGMIIos}$	—	0.6	ns	
	ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL) output setup time	$t_{MRGMIIso}$	1.1	—	ns	
	ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN (TX_CTL) output hold time	$t_{MRGMIIho}$	1.1	—	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) input setup time	$t_{MRGMIIsi}$	-0.7	—	ns	
	ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV (RX_CTL) input hold time	$t_{MRGMIIhi}$	2.9	—	ns	
	Ethernet (MII)	ETH2_REFCLK cycle time	t_{MMIIck}	40	—	
ETH2_REFCLK frequency Typ. 25 MHz		—	25 – 50 ppm	25 + 50 ppm	MHz	
ETH2_TXD0 to ETH2_TXD3, ETH2_TXEN, ETH2_TXER output delay time		$t_{MMII d}$	11	25	ns	
ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV, ETH2_RXER setup time		$t_{MMII s}$	10	—	ns	
ETH2_RXD0 to ETH2_RXD3, ETH2_RXDV, ETH2_RXER hold time		$t_{MMII h}$	0	—	ns	

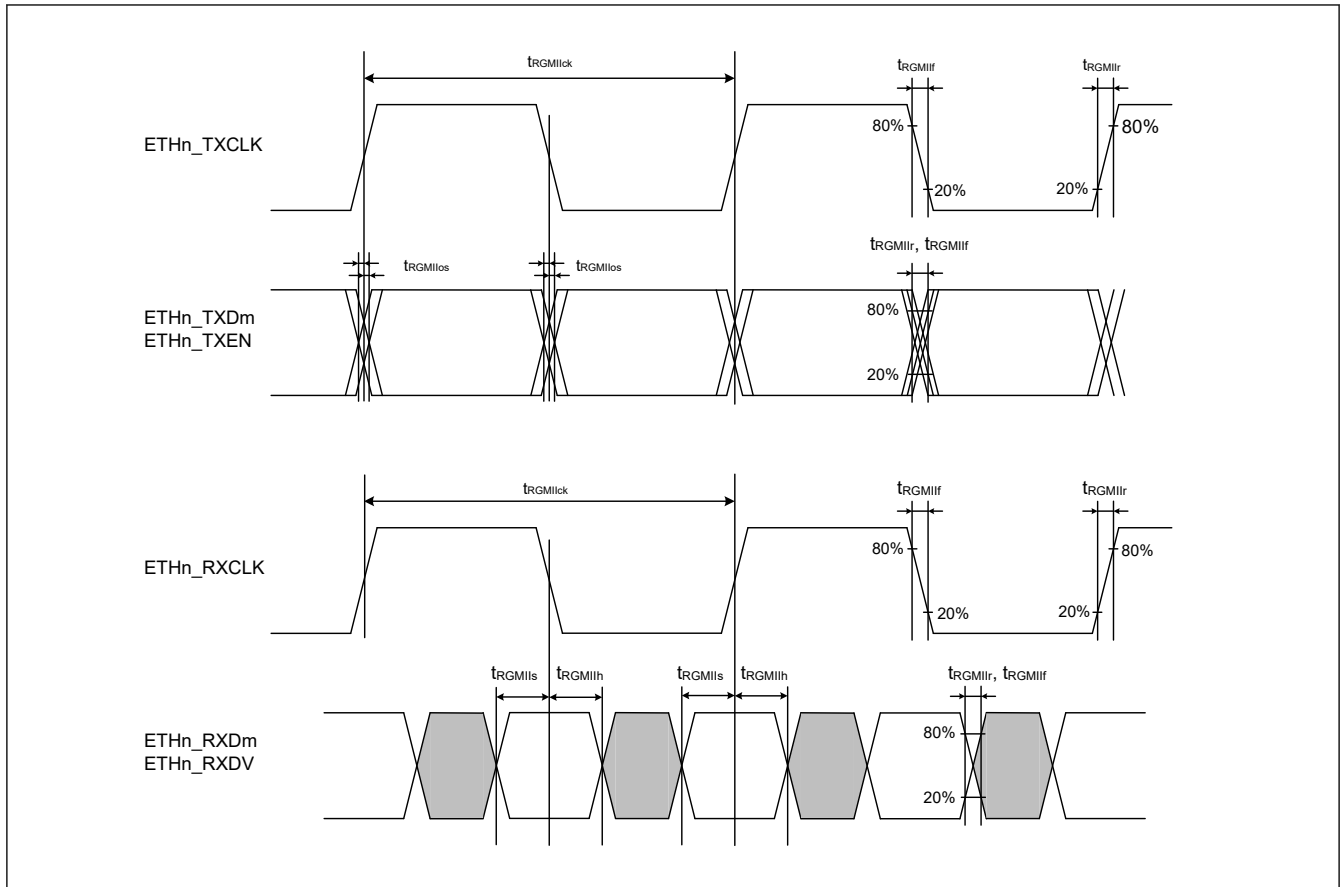


Figure 2.81 RGMII transmission and reception timing (n = 0 to 2, m = 0 to 3)

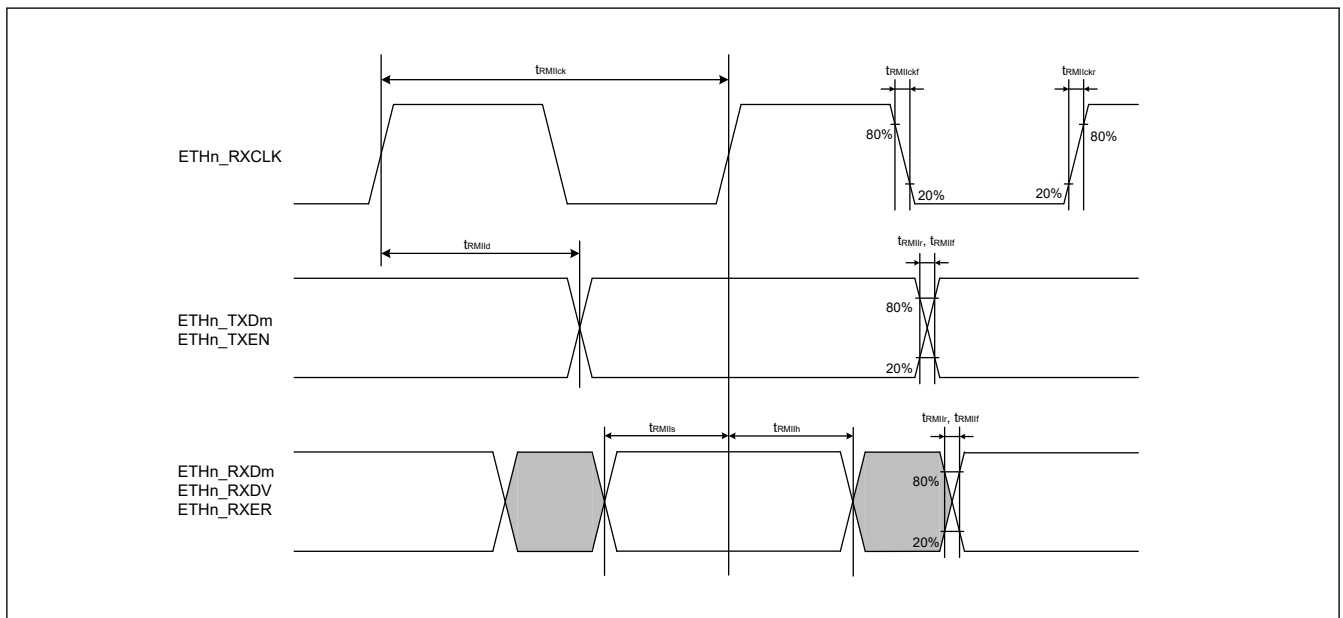


Figure 2.82 RMI1 transmission and reception timing (n = 0 to 2, m = 0 to 1)

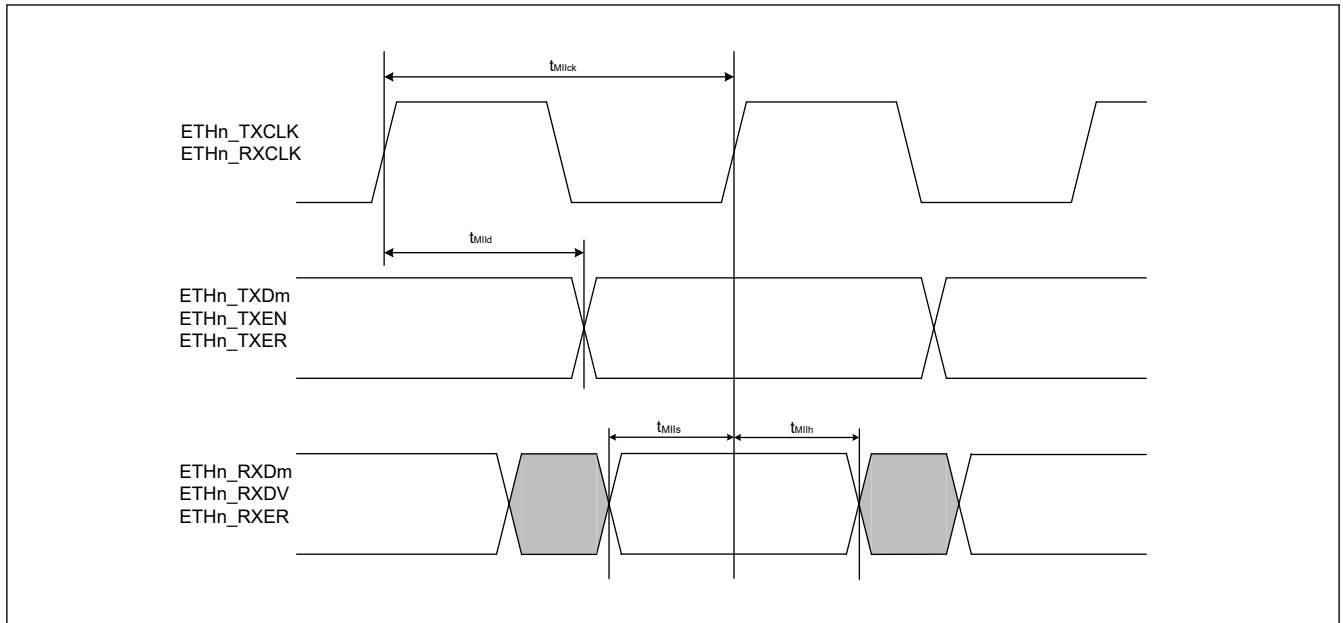


Figure 2.83 MII transmission and reception timing (n = 0 to 2, m = 0 to 3)

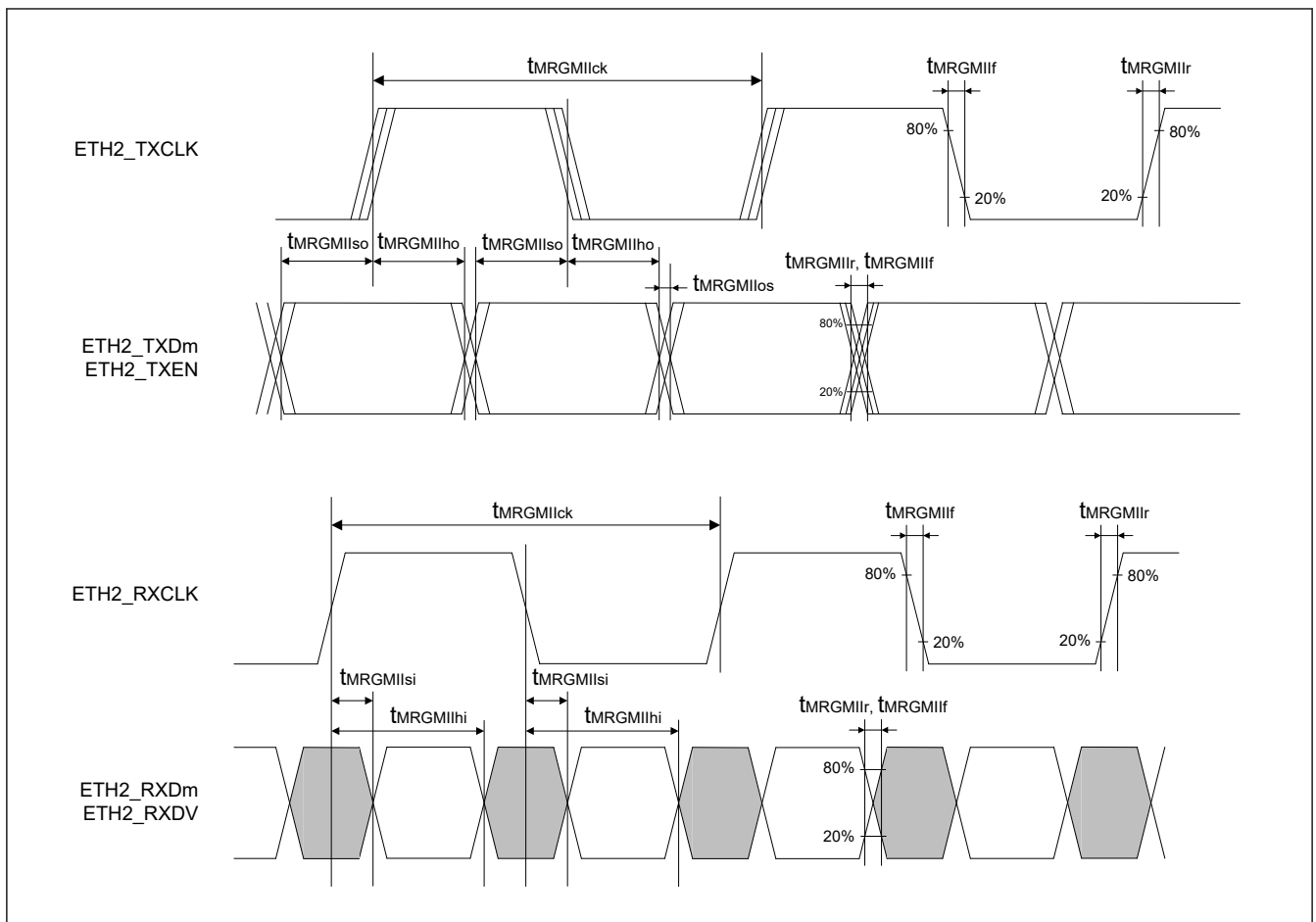


Figure 2.84 RGMII transmission and reception timing (MAC to MAC connection mode) (m = 0 to 3)

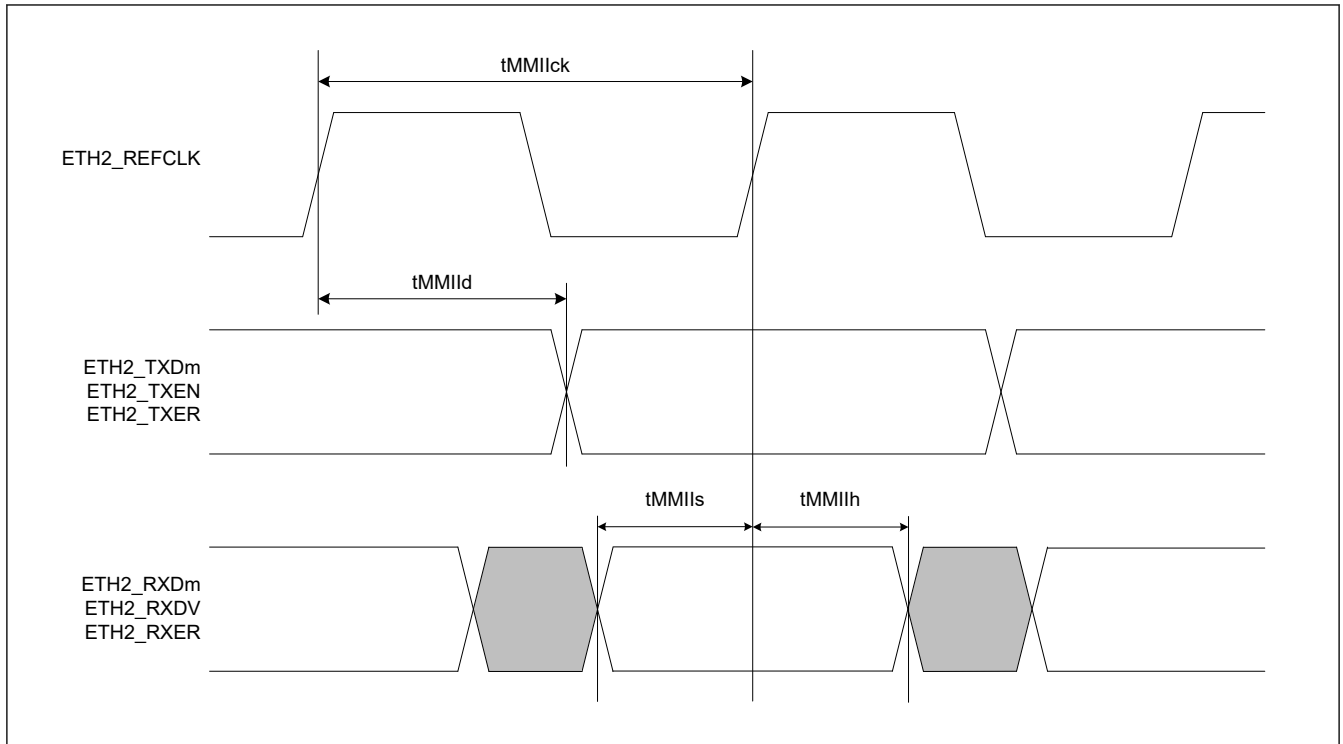


Figure 2.85 MII transmission and reception timing (MAC to MAC connection mode) (m = 0 to 3)

2.5.5.15 Serial Management Interface Timing

Conditions:

$$V_{OH} = V_{CC18} \times 0.5, V_{OL} = V_{CC18} \times 0.5, C = 30 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 30 \text{ pF (3.3 V)}$$

Table 2.40 Serial management interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
MDIO	MDC output cycle time	GMAC_MDC, ETHSW_MDC	T _{MDCck}	80	—	ns	Figure 2.86
		ESC_MDC		400	—	ns	
	MDIO output delay time (for MDC fall)*1		T _{MDIOd}	—	20	ns	
	MDIO input setup time (for MDC rise)		T _{MDIOs}	18	—	ns	
	MDIO input hold time (for MDC rise)	GMAC_MDC, ETHSW_MDC	T _{MDIOh}	0	—	ns	
ESC_MDC		10		—	ns		

Note 1. The output timing from ETHSW is based on the rising edge of MDC, and the output delay can be set in the register.

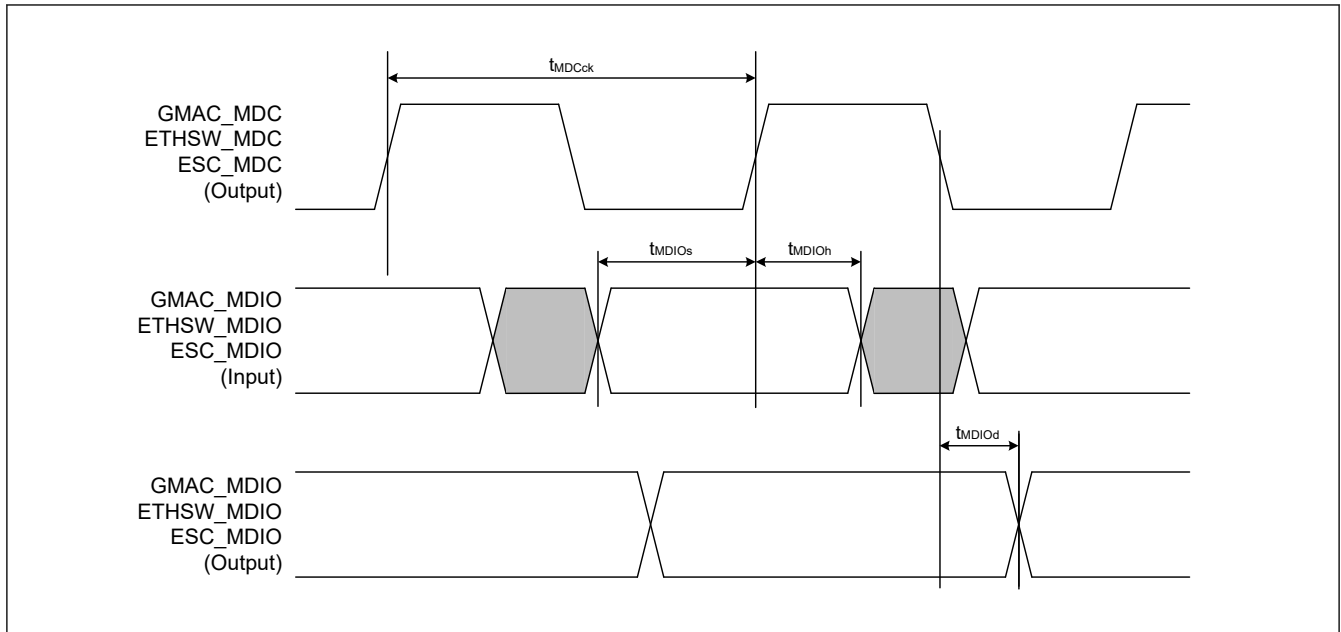


Figure 2.86 Serial management interface timing

2.5.5.16 SHOSTIF Timing

Conditions:

$$V_{OH} = V_{CC18} \times 0.5, V_{OL} = V_{CC18} \times 0.5, C = 30 \text{ pF (1.8 V)}$$

$$V_{OH} = V_{CC33} \times 0.5, V_{OL} = V_{CC33} \times 0.5, C = 30 \text{ pF (3.3 V)}$$

Table 2.41 SHOSTIF timing

Parameter	Symbol	Min.	Max.	Unit	Reference figure	
SHOSTIF	Clock cycle time	t_{SHck}	25	—	ns	Figure 2.87
	Clock high time	t_{CH}	0.45	0.55	t_{SHck}	
	Clock low time	t_{CL}	0.45	0.55	t_{SHck}	
	Clock rise slew rate	t_{CRT}	0.1	—	V/ns	
	Clock fall slew rate	t_{CFT}	0.1	—	V/ns	
	CS# high time	t_{CS}	2	—	t_{SHck}	
SHOSTIF	CS# active setup time	t_{CSS}	15	—	ns	Figure 2.88, Figure 2.89
	CS# active hold time	t_{CSH}	15	—	ns	
	Data input setup time	t_{SU}	3	—	ns	
	Data input hold time	t_{HD}	10.5	—	ns	
	Clock low to output valid	t_V	—	15.5	ns	
	Data output hold time	t_{HO}	6	—	ns	
	Data output disable time	t_{DIS}	—	18	ns	

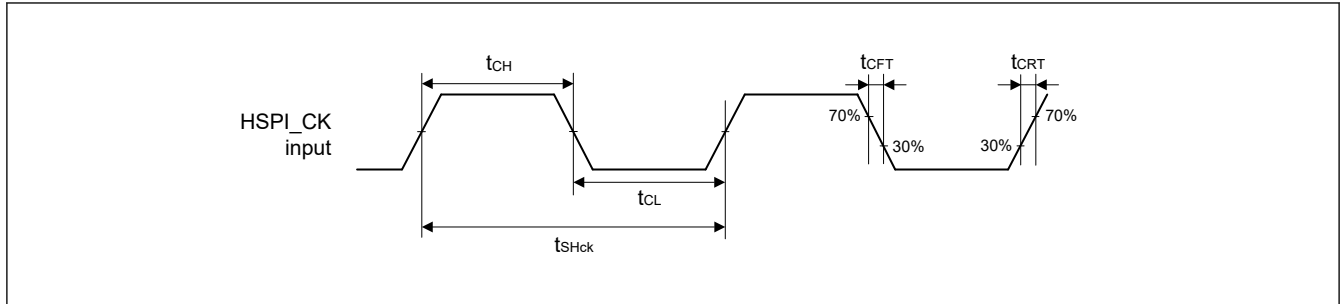


Figure 2.87 SHOSTIF clock timing

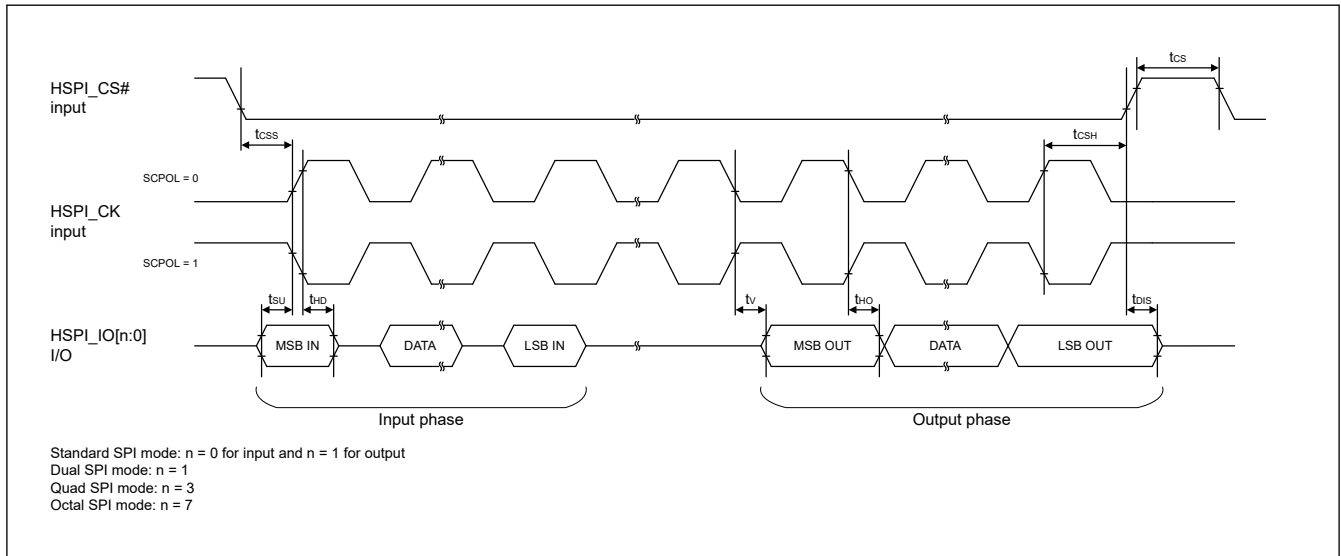


Figure 2.88 SHOSTIF timing (SCPH = 0)

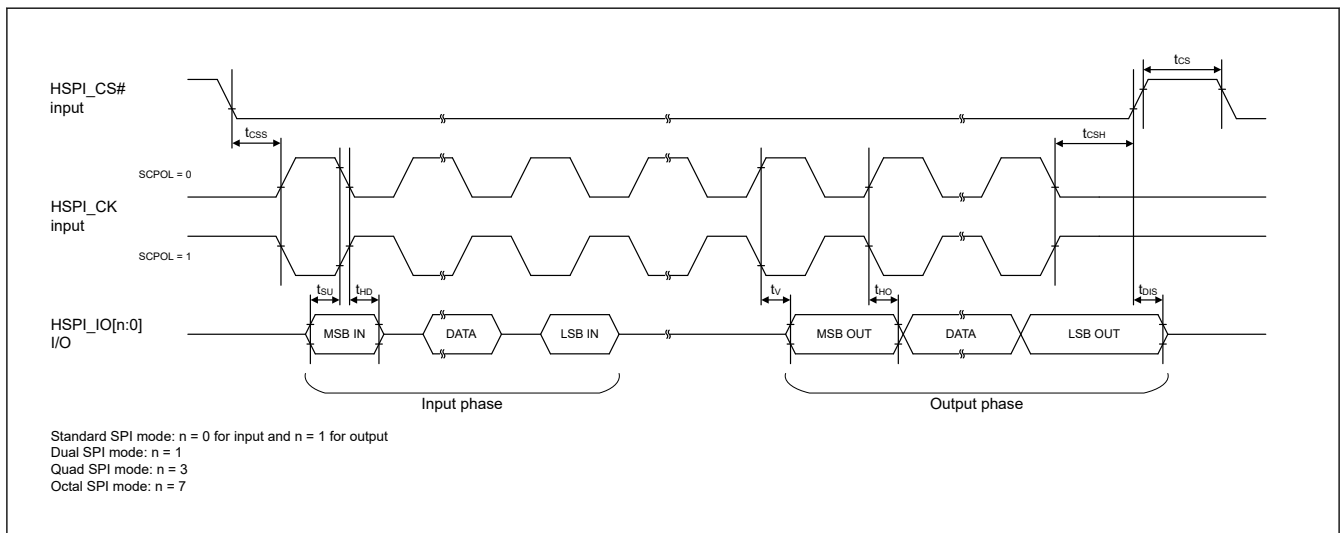


Figure 2.89 SHOSTIF timing (SCPH = 1)

2.6 USB Characteristics

Table 2.42 On-chip USB low-speed (host only) characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{LR}	75	—	300	ns	Figure 2.90, Figure 2.91
Falling time	t_{LF}	75	—	300	ns	
Rising/falling time ratio	t_{LR}/t_{LF}	80	—	125	%	

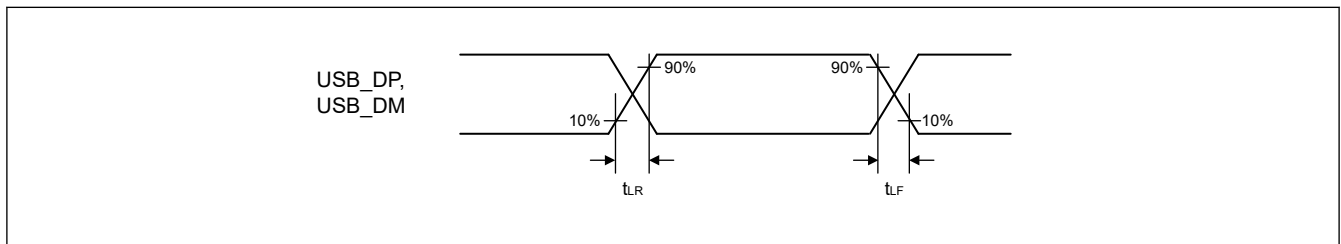


Figure 2.90 USB_DP, USB_DM output timing (low-speed/host only)

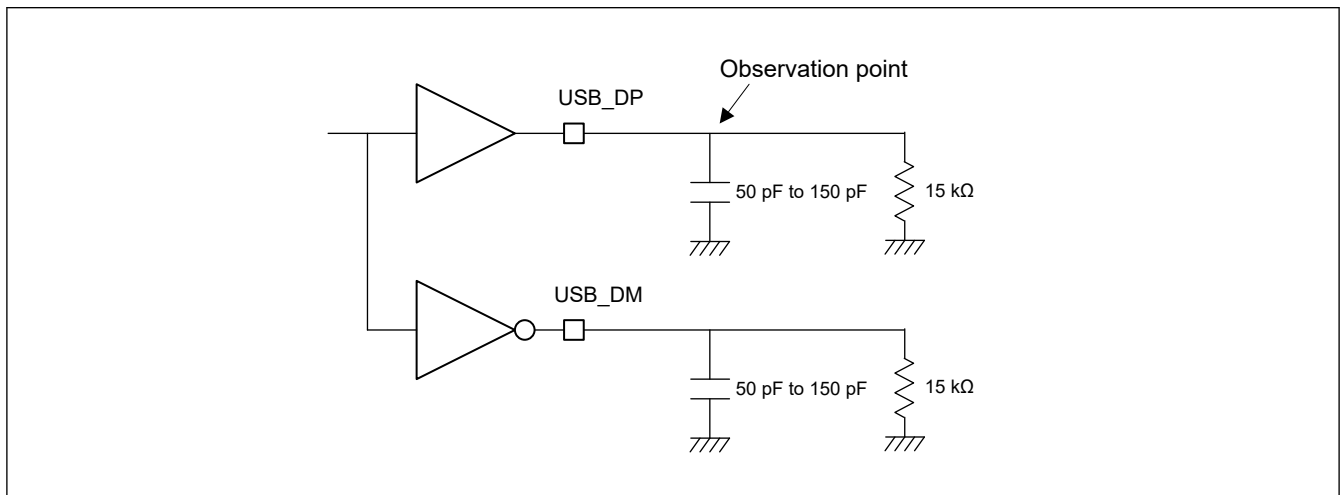


Figure 2.91 Measurement circuit (low-speed/host only)

Table 2.43 On-chip USB full-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{FR}	4	—	20	ns	Figure 2.92, Figure 2.93
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR}/t_{FF}	90	—	111.11	%	

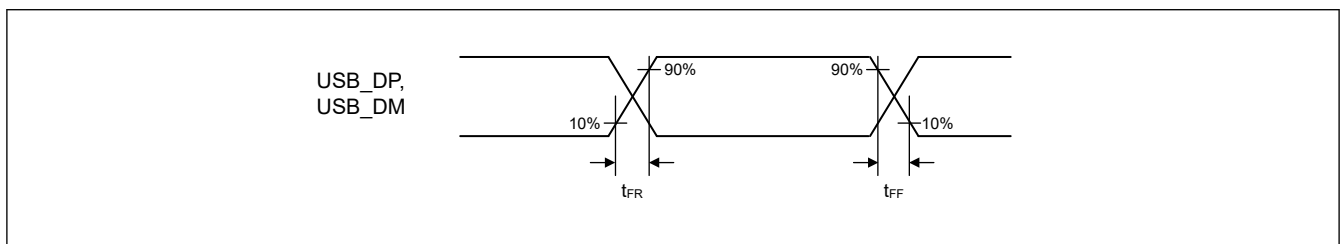


Figure 2.92 USB_DP, USB_DM output timing (full speed)

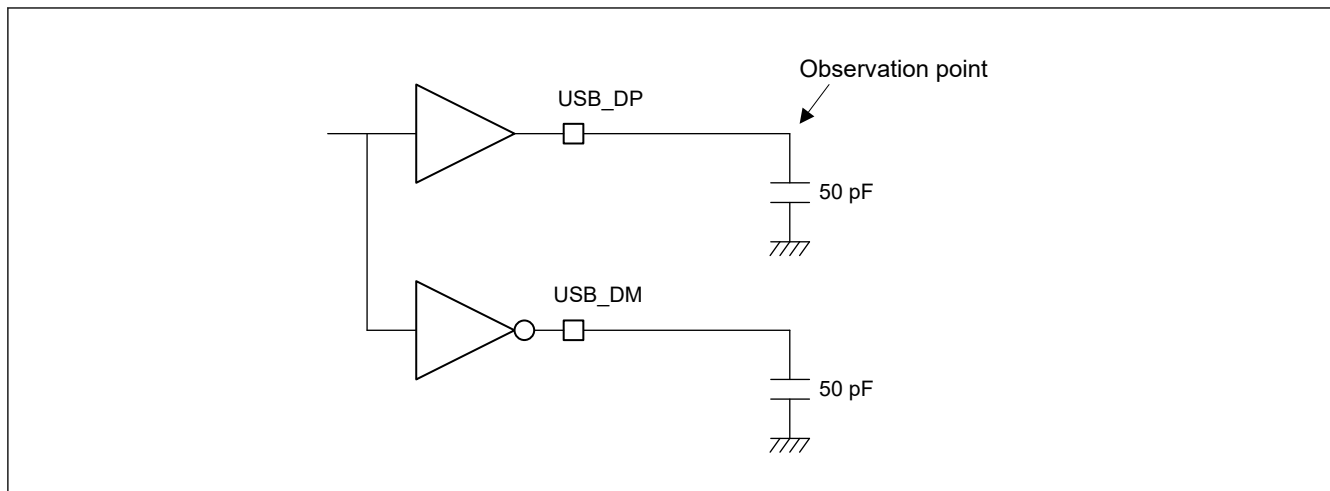


Figure 2.93 Measurement circuit (full speed)

Table 2.44 On-chip USB high-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{HSR}	—	—	2.133	V/ μ s	Figure 2.94, Figure 2.95
Falling time	t_{HSF}	—	—	2.133	V/ μ s	
Output resistors (also used as high-speed terminating resistor)	Z _{HSDRV}	40.5	—	49.5	Ω	—

Note: The output resistors (Z_{HSDRV}) for connection to the USB_DP and USB_DM pins are within the LSI.

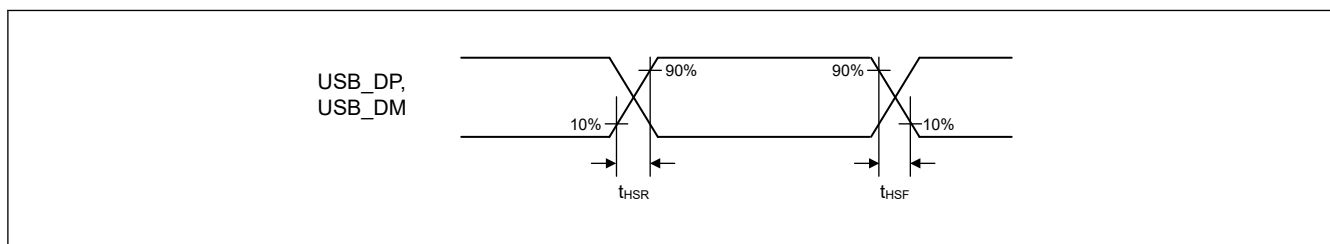


Figure 2.94 USB_DP, USB_DM output timing (high speed)

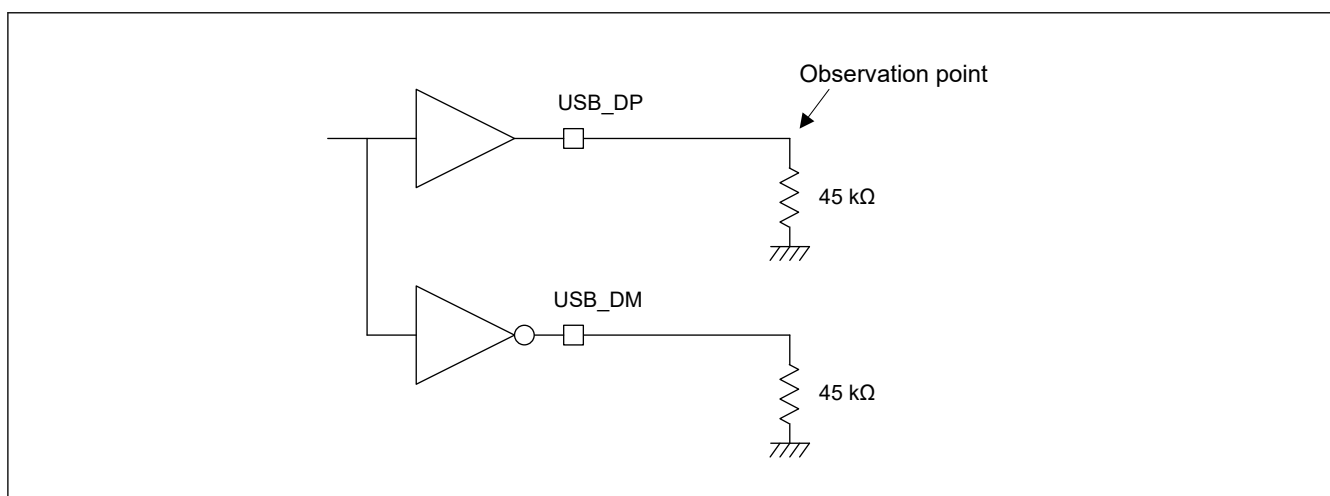


Figure 2.95 Measurement circuit (high speed)

2.7 A/D Conversion Characteristics

Table 2.45 12-Bit A/D conversion characteristics

Parameter		Min.	Typ.	Max.	Unit	Reference figure
Resolution		12			bits	—
Analog input capacitance		—	—	13	pF	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002, AN100 to AN102)	Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ	1.52	—	—	μs	—
	Offset error	—	—	±13	LSB	—
	Full-scale error	—	—	±13	LSB	—
	Quantization error	—	±0.5	—	LSB	—
	Absolute accuracy	—	—	±14	LSB	—
	DNL differential non-linearity error	—	—	±3	LSB	—
	INL integral non-linearity error	—	—	±4	LSB	—
	Holding characteristics of sample-and-hold circuits	—	—	2.67	μs	—
Dynamic range	0.15	—	VREFH0 - 0.15	V	—	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN003, AN100 to AN103)	Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ	0.84	—	—	μs	—
	Offset error	—	—	±11	LSB	—
	Full-scale error	—	—	±11	LSB	—
	Quantization error	—	±0.5	—	LSB	—
	Absolute accuracy	—	—	±12	LSB	—
	DNL differential non-linearity error	—	—	±3	LSB	—
	INL integral non-linearity error	—	—	±4	LSB	—

Note: The specified values in the table apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the specified ranges.

Note 1. The conversion time is the total of the sampling time and the comparison time.

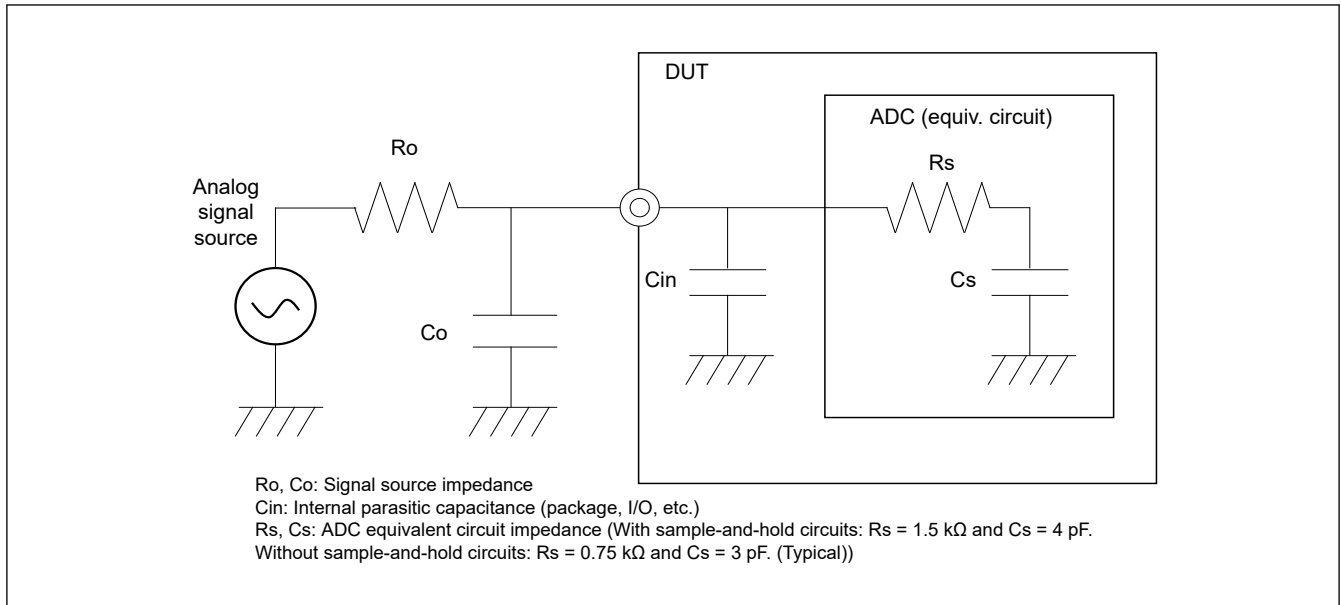


Figure 2.96 A/D converter equivalent circuit and peripheral configuration diagram

2.8 Temperature Sensor Characteristics

Table 2.46 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	*1
Temperature slope	—	0.0625	—	°C/LSB	—
Output code (at 25°C)	—	1545 (decimal)	—	—	TSUSAD register

Note 1. 2-point calibration ($T_j = 25^\circ\text{C}$ and $T_j = 85^\circ\text{C}$) and 8 times averaging.

2.9 Debug Interface Timing

Condition: $V_{OH} = V_{CC33} \times 0.5$, $V_{OL} = V_{CC33} \times 0.5$

Table 2.47 Debug interface timing (1 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
TCK cycle time	With an ICE connected	t_{TCKcyc}^{*1}	—	ns	Figure 2.97
	For use in BSCAN	80	—		
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	Figure 2.98 Output load: 30 pF
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	5	—	ns	
TDI hold time	t_{TDIH}	5	—	ns	
TMS/SWDIO setup time	t_{TMSS}	5	—	ns	
TMS/SWDIO hold time	t_{TMSh}	5	—	ns	
SWDIO delay time	t_{SWDO}	—	15	ns	
TDO delay time	With an ICE connected	t_{TDOD}	—	15	ns
	For use in BSCAN	—	22		
Capture register setup time	t_{CAPTS}	5	—	ns	Figure 2.99
Capture register hold time	t_{CAPTH}	5	—	ns	
Update register delay time	$t_{UPDATED}$	—	15	ns	

Table 2.47 Debug interface timing (2 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Trace clock cycle	t_{TCYC}	20	—	ns	Figure 2.100 Output load: 15 pF
Trace data delay time	t_{TDT}	1.3	8.7	ns	

Note 1. This value is the minimum cycle time for the normal operation of internal circuits.
The actual cycle time should be determined in consideration of the TCK capture edge timing and cable length of the connected ICE.

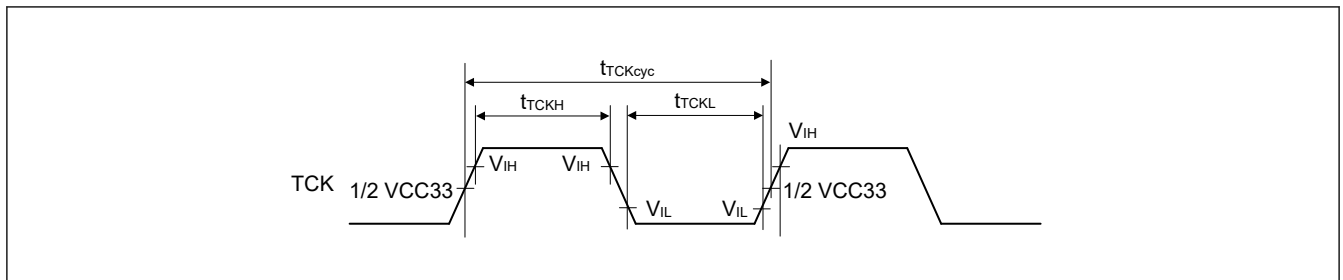


Figure 2.97 TCK input timing

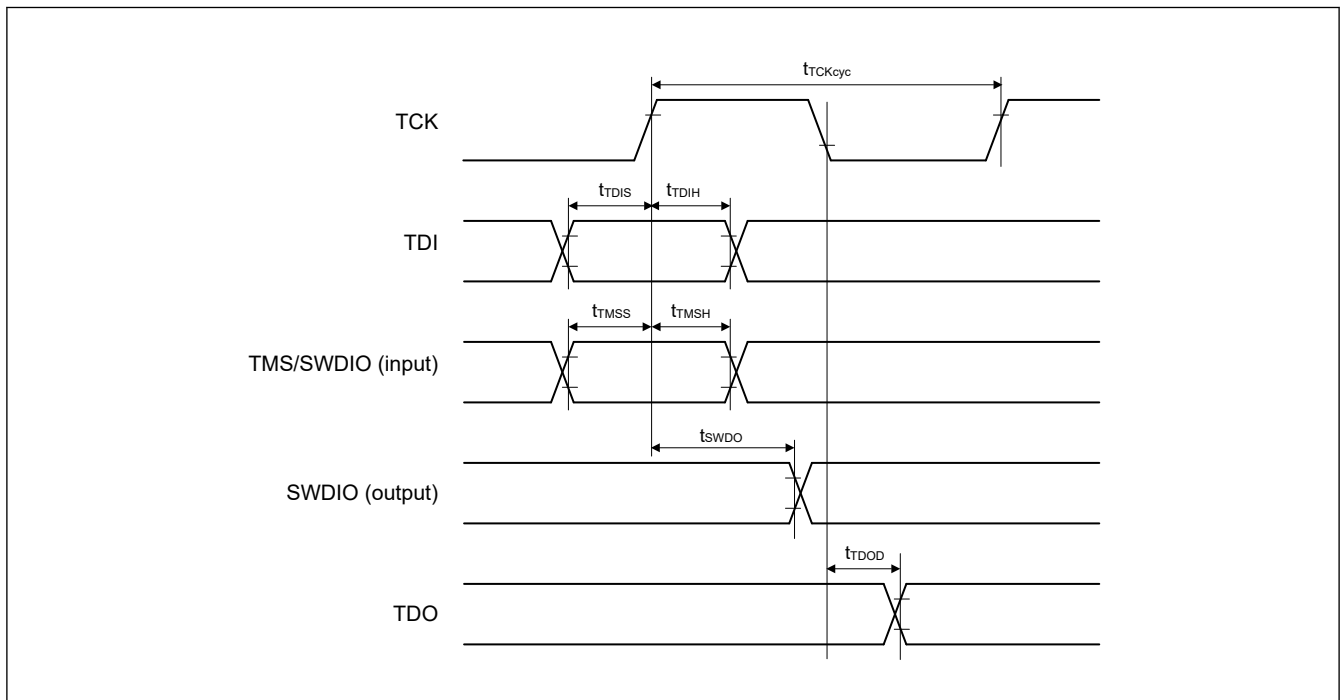


Figure 2.98 Data transfer timing

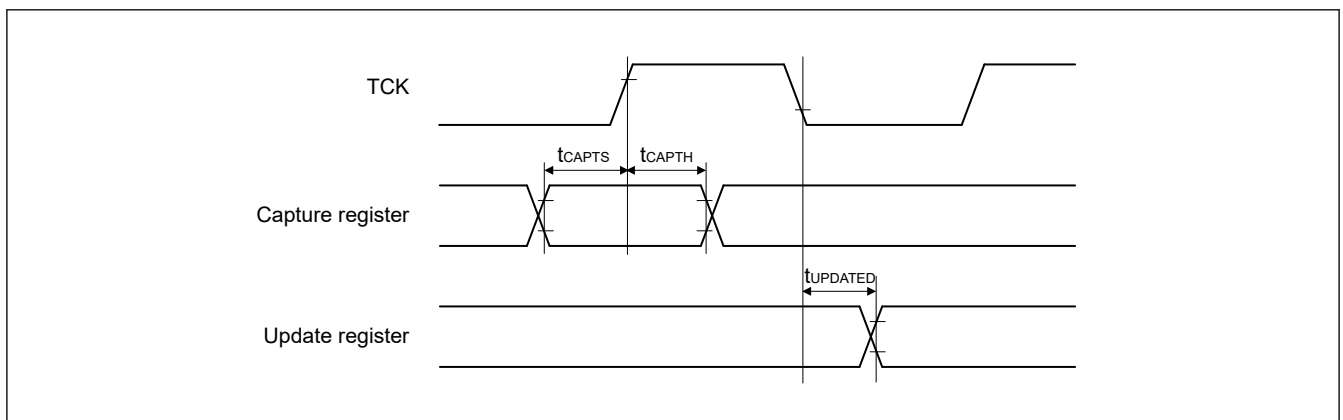
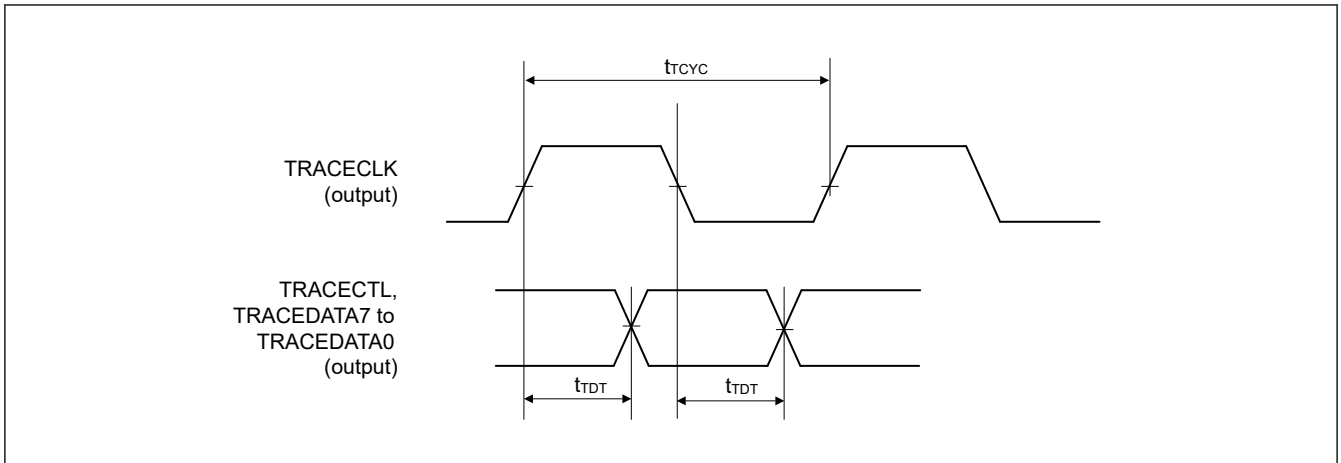


Figure 2.99 Boundary scan input/output timing

**Figure 2.100** Trace interface timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

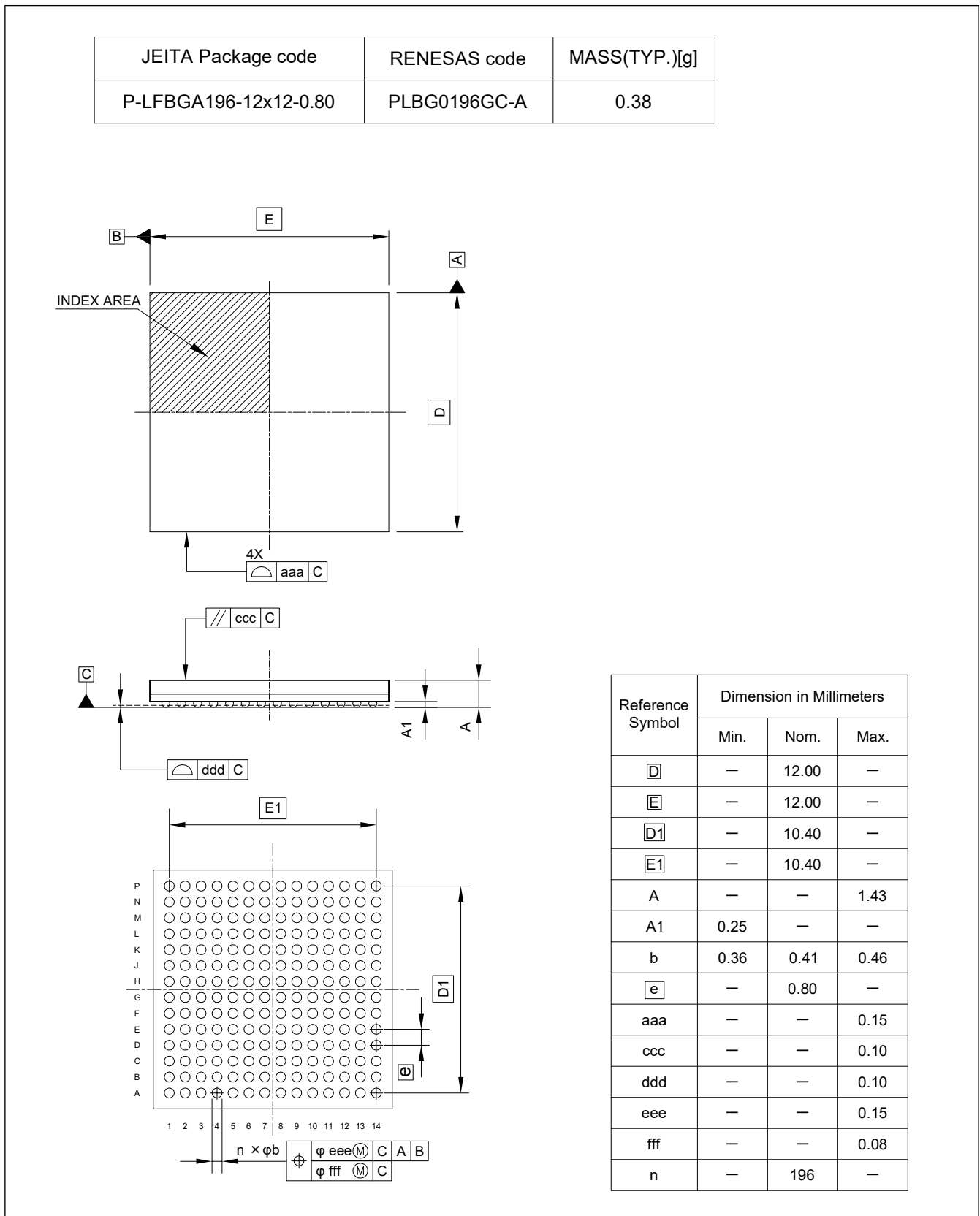


Figure 1.1 196-pin FBGA

Revision History

Revision 1.00 — November 30, 2022

- Initial release

Revision 1.10 — February 28, 2023**2. Electrical Characteristics:**

- Corrected Table 2.35 SPI timing.

Appx 1. Package Dimensions:

- Corrected Figure 1.1 196-pin FBGA.