



# 1. Overview

## 1.1 Typical Applications

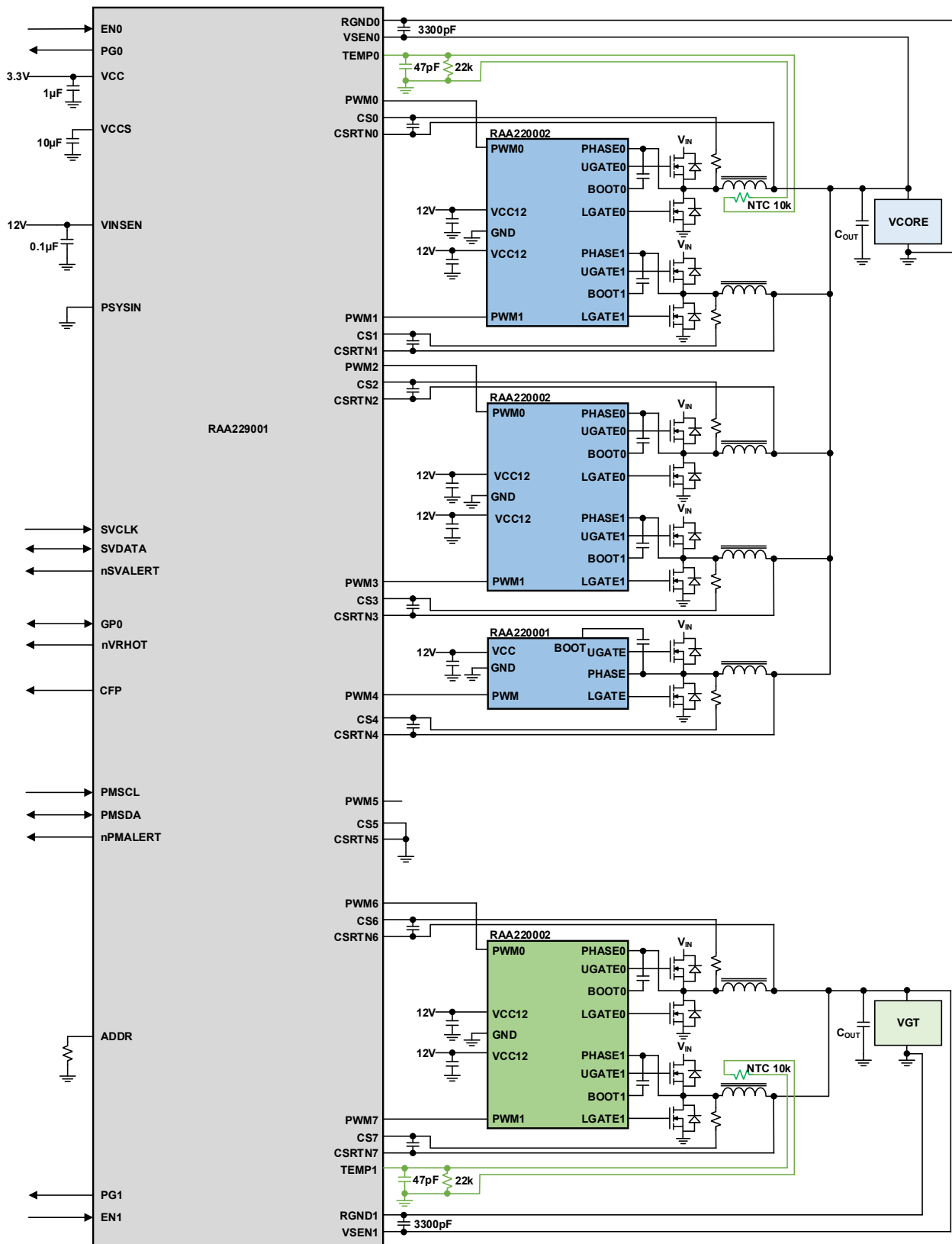


Figure 2. Intel 5+2 with Single-Dual Driver

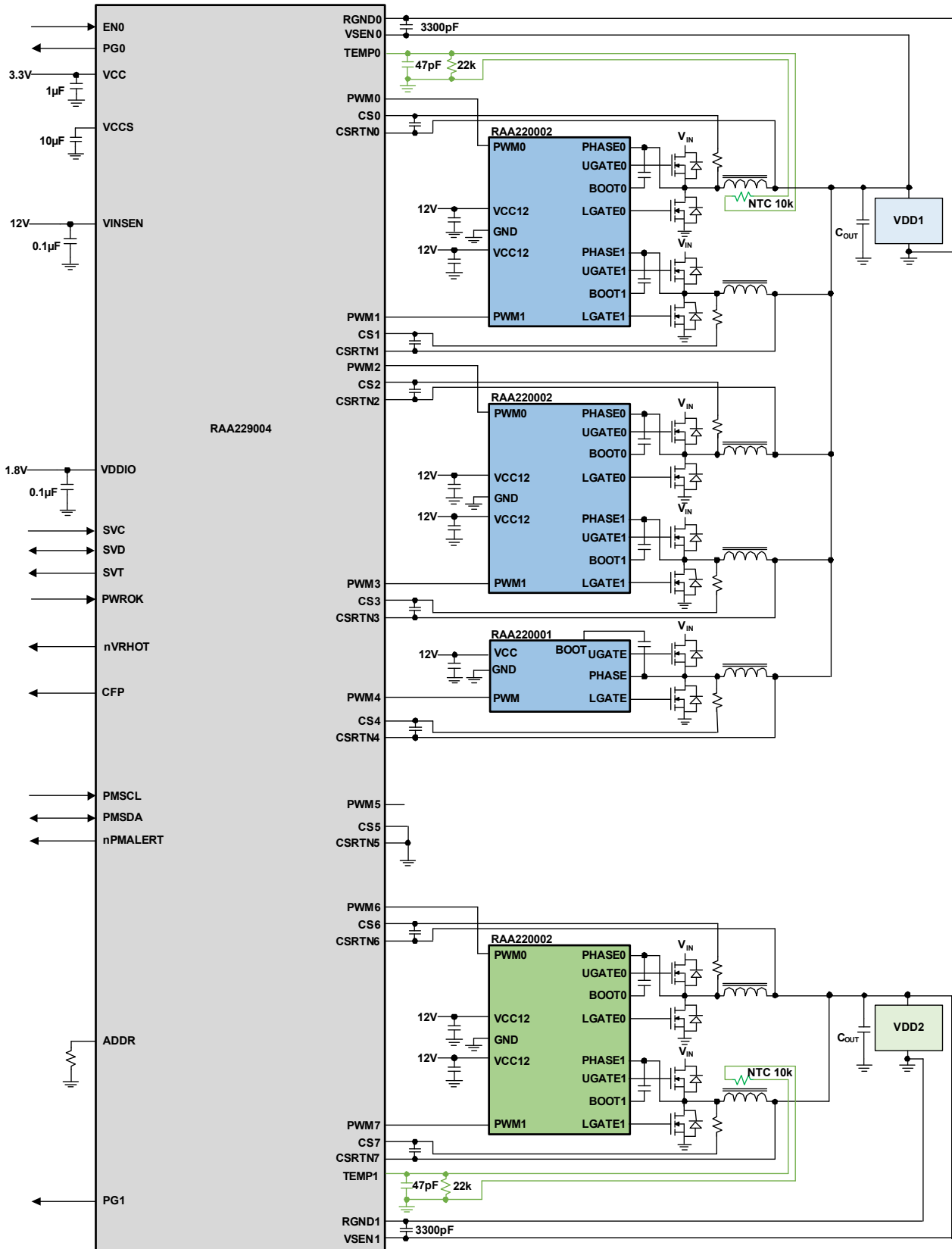


Figure 3. AMD 5+2 with Single-Dual Driver

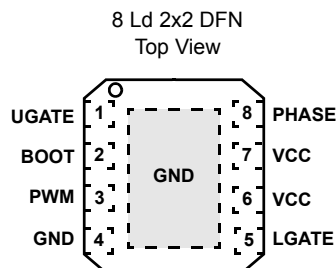
## 1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA220001GNP#HA0	001	-40 to +85	6k	8 Ld 2x2 DFN	L8.2x2D

Notes:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [RAA220001](#) device page. For more information about MSL, see [TB363](#).

## 1.3 Pin Configuration



## 1.4 Functional Pin Descriptions

Pin Number	Pin Name	Function
1	UGATE	Upper gate drive output. Connect to gate of high-side power N-channel MOSFET.
2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See <a href="#">"Internal Bootstrap Device" on page 8</a> for guidance in choosing the capacitor value.
3	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see <a href="#">"Three-State PWM Input" on page 8</a> for more details. Connect this pin to the PWM output of the controller.
4	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	LGATE	Lower gate drive output. Connect to gate of the low-side power N-channel MOSFET.
6, 7	VCC	The two VCC pins must tie to each other. Connect them to 12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
-	PAD	Connect this pad to the power ground plane (GND) using a thermally enhanced connection.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage ( $V_{CC}$ )		15	V
BOOT Voltage ( $V_{BOOT-GND}$ )		36	V
Input Voltage ( $V_{PWM}$ )	GND - 0.3	7	V
UGATE	$V_{PHASE} - 0.3V_{DC}$	$V_{BOOT} + 0.3$	V
	$V_{PHASE} - 3.5$ (<100ns Pulse Width, 2 $\mu$ J)	$V_{BOOT} + 0.3$	V
LGATE	GND - 0.3 $V_{DC}$	$V_{VCC} + 0.3$	V
	GND - 5 (<100ns Pulse Width, 2 $\mu$ J)	$V_{VCC} + 0.3$	V
PHASE	GND - 0.3	25	$V_{DC}$
	GND - 8 (<400ns, 20 $\mu$ J)	30 (<200ns, $V_{BOOT-GND} < 36V$ )	V
<b>ESD Rating</b>	<b>Value</b>		<b>Unit</b>
Human Body Model (Tested per JS-001-2017)	2.5		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

Thermal Resistance	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
2x2 DFN Package ( <a href="#">Notes 4, 5</a> )	90	25

Notes:

- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	$^{\circ}C$
Maximum Storage Temperature Range	-65	+150	$^{\circ}C$
Pb-Free Reflow Profile	See <a href="#">TB493</a>		

### 2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+85	$^{\circ}C$
Maximum Operating Junction Temperature		+125	$^{\circ}C$
Supply Voltage, $V_{CC}$	6.0	13.2	V

## 2.4 Electrical Specifications

Recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
<b>V<sub>CC</sub> Supply Current</b>						
No Load Switching Supply Current	I <sub>VCC</sub>	V <sub>VCC</sub> = 12V, F <sub>PWM</sub> = 300kHz		7.0		mA
	I <sub>VCC</sub>	V <sub>VCC</sub> = 12V, PWM = 1.65V		0.8		mA
<b>Power-On Reset</b>						
V <sub>CC</sub> Rising Threshold			4.5	4.7	4.95	V
V <sub>CC</sub> Falling Threshold			4.0	4.27	4.5	V
V <sub>CC</sub> POR hysteresis			0.4			V
<b>PWM Input (See <a href="#">"Timing Diagram" on page 7</a>)</b>						
Input Current	I <sub>PWM</sub>	V <sub>PWM</sub> = 3.3V, V <sub>CC</sub> = 12V		90		μA
		V <sub>PWM</sub> = 0V, V <sub>CC</sub> = 12V		-110		μA
Three-State Upper Gate Rising Threshold		V <sub>CC</sub> = 12V		2.64		V
Three-State Upper Gate Falling Threshold		V <sub>CC</sub> = 12V		2.17		V
Three-State Lower Gate Rising Threshold		V <sub>CC</sub> = 12V		0.90		V
Three-State Lower Gate Falling Threshold		V <sub>CC</sub> = 12V		1.07		V
UGATE Rise Time	t <sub>RU</sub>	V <sub>VCC</sub> = 12V, 3nF load, 10% to 90%		31		ns
LGATE Rise Time	t <sub>RL</sub>	V <sub>VCC</sub> = 12V, 3nF load, 10% to 90%		28		ns
UGATE Fall Time	t <sub>FU</sub>	V <sub>VCC</sub> = 12V, 3nF load, 90% to 10%		18		ns
LGATE Fall Time	t <sub>FL</sub>	V <sub>VCC</sub> = 12V, 3nF load, 90% to 10%		16		ns
UGATE Turn-On Propagation Delay	t <sub>PDHU</sub>	V <sub>VCC</sub> = 12V, 3nF load, adaptive		16		ns
LGATE Turn-On Propagation Delay	t <sub>PDHL</sub>	V <sub>VCC</sub> = 12V, 3nF load, adaptive		38		ns
UGATE Turn-Off Propagation Delay	t <sub>PDLU</sub>	V <sub>VCC</sub> = 12V, 3nF load		21		ns
LGATE Turn-Off Propagation Delay	t <sub>PDLL</sub>	V <sub>VCC</sub> = 12V, 3nF load		23		ns
<b>Output</b>						
Upper Drive Source Impedance	R <sub>U_SOURCE</sub>	20mA source current		3.9		Ω
Upper Drive Sink Impedance	R <sub>U_SINK</sub>	20mA sink current		1.4		Ω
Lower Drive Source Impedance	R <sub>L_SOURCE</sub>	20mA source current		2.7		Ω
Lower Drive Sink Impedance	R <sub>L_SINK</sub>	20mA sink current		0.9		Ω

Note:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.



## 3. Description

### 3.1 Operation and Adaptive Shoot-Through Protection

Designed for high-speed switching, the RAA220001 MOSFET driver controls both high-side and low-side N-channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see [Figure 4 on page 7](#)). After a short propagation delay [ $t_{PDLL}$ ], the lower gate begins to fall. Typical fall time [ $t_{FL}$ ] is provided in the “Electrical Specifications” on [page 6](#). Following a 25ns blanking period, adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [ $t_{PDHU}$ ] after the LGATE voltage drops below  $\sim 1.75V$ . The upper gate drive then begins to rise [ $t_{RU}$ ] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [ $t_{PDLU}$ ] is encountered before the upper gate begins to fall [ $t_{FU}$ ]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [ $t_{PDHL}$ ] after the upper MOSFET’s PHASE voltage drops below  $+0.8V$  or 40ns after the upper MOSFET’s gate voltage [UGATE-PHASE] drops below  $\sim 1.75V$ . The lower gate then rises [ $t_{RL}$ ], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with a large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. Therefore, the lower gate driver is sized much larger to meet this application requirement. The  $0.8\Omega$  ON-resistance and 3A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high  $dV/dt$  of the switching node.

### 3.2 Three-State PWM Input

A unique feature of the RAA220001 and other Renesas drivers is the addition of a three-state shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set hold-off time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the “Electrical Specifications” on [page 6](#) determine when the lower and upper gates are enabled. This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

### 3.3 Power-On Reset (POR) Function

During initial start-up, the  $V_{CC}$  voltage rise is monitored. When the rising  $V_{CC}$  voltage exceeds the rising POR threshold, operation of the driver is enabled and the PWM input signal takes control of the gate drives. If  $V_{CC}$  drops below the POR falling threshold, operation of the driver is disabled.

### 3.4 Pre-POR Overvoltage Protection

While  $V_{CC}$  is below its POR level, the upper gate is held low and LGATE is connected to the PHASE pin through an internal  $30k\Omega$  (typically) resistor. By connecting the PHASE node to the gate of the low-side MOSFET, the driver offers some passive protection to the load if the upper MOSFET(s) is or becomes shorted. If the PHASE node goes higher than the gate threshold of the lower MOSFET, it results in the progressive turn-on of the device and the effective clamping of the PHASE node’s rise. The actual PHASE node clamping level depends on the lower MOSFET’s electrical characteristics, and the characteristics of the input supply and the path connecting it to the respective PHASE node.

### 3.5 Internal Bootstrap Device

The RAA220001 features an internal bootstrap Schottky diode equivalent circuit implemented by switchers with typical on resistance of  $40\Omega$  and no typical diode forward voltage drop. Adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the



bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces the voltage stress on the BOOT to PHASE pins.

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for UVCC. Its minimum capacitance value can be estimated from [Equation 1](#):

$$(EQ. 1) \quad C_{BOOT\_CAP} \geq \frac{Q_{UGATE}}{\Delta V_{BOOT\_CAP}}$$

$$Q_{UGATE} = \frac{Q_{G1} \cdot UVCC}{V_{GS1}} \cdot N_{Q1}$$

where:

- $Q_{G1}$  is the amount of gate charge per upper MOSFET at  $V_{GS1}$  gate-source voltage.
- $N_{Q1}$  is the number of control MOSFETs.
- $\Delta V_{BOOT\_CAP}$  is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in [Figure 5 on page 9](#).

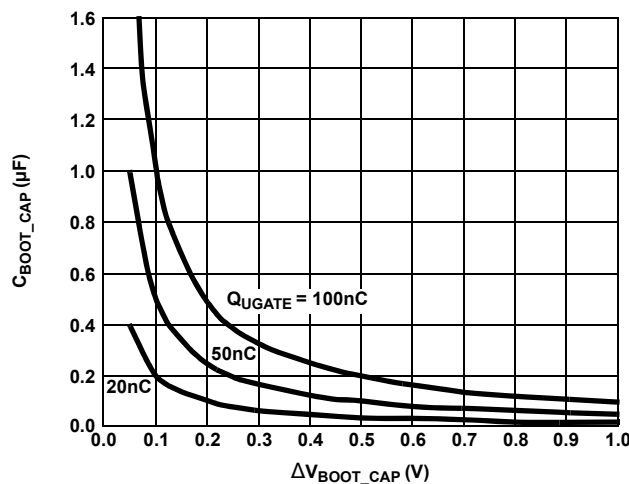


Figure 5. Bootstrap Capacitance vs Boot Ripple Voltage

### 3.6 Power Dissipation

Package power dissipation is mainly a function of the switching frequency ( $f_{SW}$ ), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge ( $Q_G$ ). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level can push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "[Layout Considerations](#)" on page 11 for thermal impedance improvement suggestions. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated using [Equations 2](#) and [3](#), respectively.

$$(EQ. 2) \quad P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \cdot VCC$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \cdot UVCC^2}{V_{GS1}} \cdot f_{SW} \cdot N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \cdot LVCC^2}{V_{GS2}} \cdot f_{SW} \cdot N_{Q2}$$

$$(EQ. 3) \quad I_{DR} = \left( \frac{Q_{G1} \cdot UVCC \cdot N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \cdot LVCC \cdot N_{Q2}}{V_{GS2}} \right) \cdot f_{SW} + I_Q$$

where:

- Gate charge ( $Q_{G1}$  and  $Q_{G2}$ ) is defined at a particular gate to source voltage ( $V_{GS1}$  and  $V_{GS2}$ ) in the corresponding MOSFET datasheet.
- $I_Q$  is the driver's total quiescent current with no load at both drive outputs.
- $N_{Q1}$  and  $N_{Q2}$  are the number of upper and lower MOSFETs, respectively.
- UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively.
- $I_Q \cdot VCC$  product is the quiescent power of the driver without a load.

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses, the remainder is dissipated by the external gate resistors ( $R_{G1}$  and  $R_{G2}$ ) and the internal gate resistors ( $R_{GI1}$  and  $R_{GI2}$ ) of MOSFETs. Figures 6 and 7 show the typical upper and lower gate drives turn-on current paths.

$$(EQ. 4) \quad P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \cdot VCC$$

$$P_{DR\_UP} = \left( \frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \cdot \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left( \frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \cdot \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \quad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

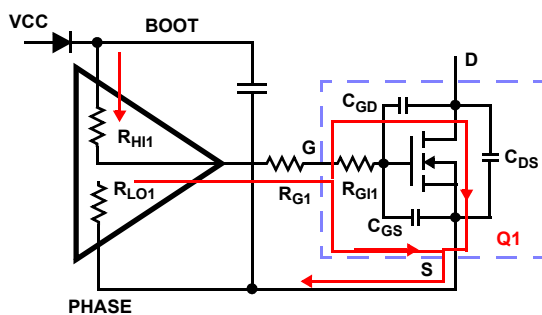


Figure 6. Typical Upper-Gate Drive Turn-On Path

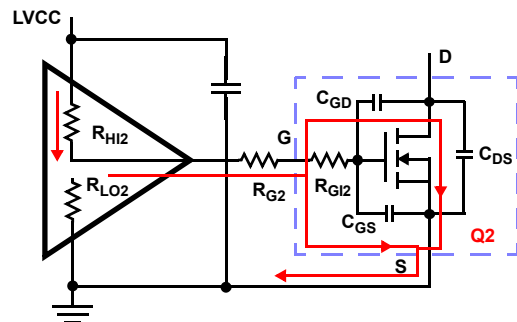


Figure 7. Typical Lower-Gate Drive Turn-On Path

## 4. Application Information

### 4.1 Layout Considerations

During switching of the devices, the parasitic inductances of the PCB and the power devices' packaging (both upper and lower MOSFETs) leads to ringing, possibly in excess of the absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice leads to an optimized layout:

- Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper MOSFET and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the input current loop. Connect the source of the lower MOSFET to ground as close to the transistor pin as feasible; place input capacitors (especially ceramic decoupling) as close as possible to the drain of the upper MOSFET and the source of lower MOSFET.

In addition, for improved heat dissipation, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended surface copper islands, and buried planes combine to allow the IC and the power switches to achieve their full thermal potential.

### 4.2 Upper MOSFET Self Turn-On Effect at Start-up

If the driver has insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high  $dV/dt$  rate while the driver outputs are floating (due to self-coupling through the internal  $C_{GD}$  of the MOSFET), the gate of the upper MOSFET can momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation is encountered, place a resistor ( $R_{UGPH}$ ) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the  $C_{GD}/C_{GS}$  ratio, and the gate-to-source threshold of the upper MOSFET. A higher  $dV/dt$ , a lower  $C_{DS}/C_{GS}$  ratio, and a lower gate-to-source threshold upper FET requires a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20k $\Omega$  resistor is sufficient, not affecting normal performance and efficiency.

$$(EQ. 5) \quad V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rSS} \left( 1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}} \right)$$

$$R = R_{UGPH} + R_{GI}$$

$$C_{rSS} = C_{GD}$$

$$C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with [Equation 5](#), which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. [Figure 8 on page 12](#) provides a visual reference for this phenomenon and its potential solution.

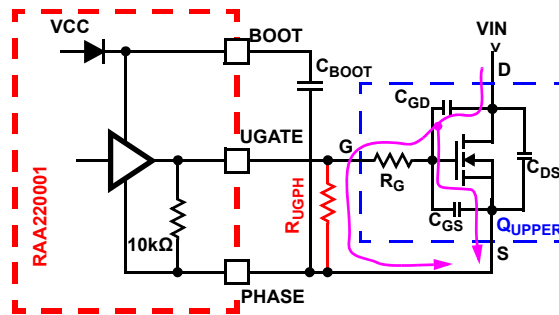


Figure 8. Gate-to-Source Resistor to Reduce Upper MOSFET Miller Coupling

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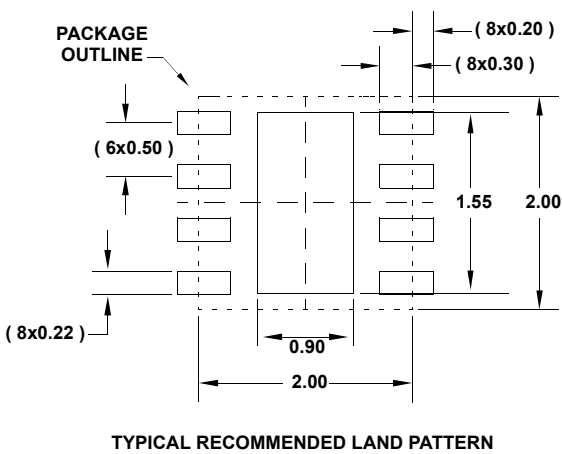
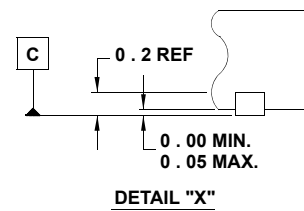
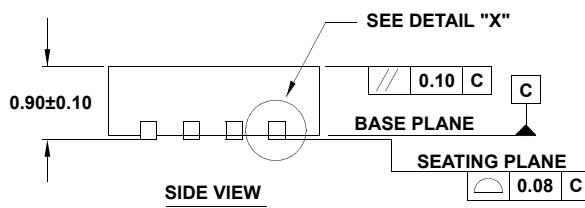
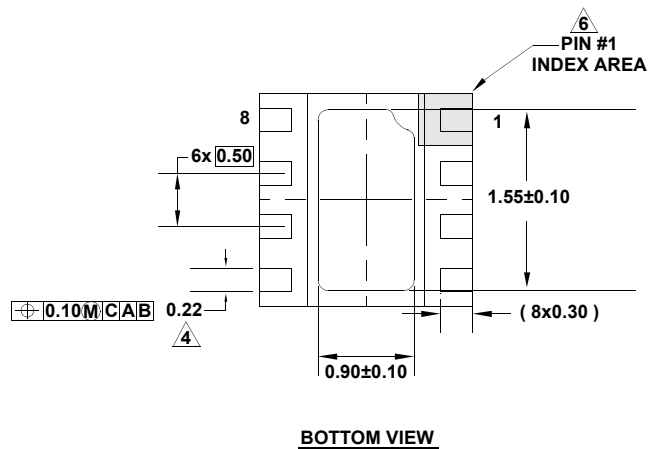
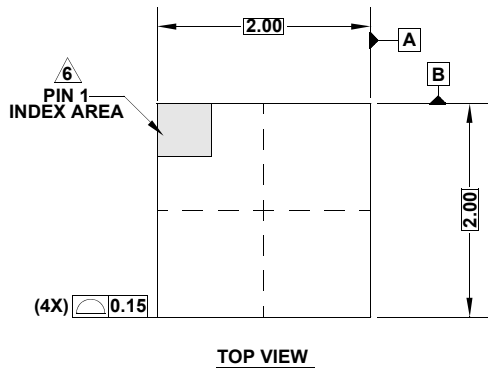
## 5. Revision History

Rev.	Date	Description
1.00	Jul.11.19	Initial release

## 6. Package Outline Drawing

For the most recent package outline drawing, see [L8.2x2D](#).

L8.2x2D  
 8 Lead Dual Flat No-Lead Plastic Package (DFN) with Exposed Pad  
 Rev 1, 3/15



**NOTES:**

1. Dimensions are in millimeters.  
 Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.