RAA271082

Automotive PMIC with Three Synchronous Buck Regulators and One Low Dropout Linear Regulator

The RAA271082 is a versatile multi-rail power IC comprised of a primary high voltage synchronous buck regulator, two secondary low voltage synchronous buck regulators, and an LDO regulator. It offers four overvoltage and undervoltage monitors, I^2C communications, a general-purpose I/O pin, and a dedicated reset output/fault indicator. RAA271082 was designed using an ASIL-D ISO-26262 development process and is intended to meet ASIL-B device metrics. The RAA271082 includes a second bandgap reference for the OV/UV monitors, built-in self-test at power-up, independent OV/UV monitoring, and continuous CRC error checking on internal registers and I^2C communications.

Requiring few external components and minimal board space, the RAA271082 provides a high-density power solution. It offers an extensive feature set configured using internal One-Time Programmable (OTP) memory. Nearly all device options such as each output voltage selection, power sequencing, and OV/UV thresholds are internally configured and require no external components for selection. The regulators also offer internal compensation. The bucks are synchronous to achieve high efficiency and are capable of operating in harsh environments requiring high ambient temperature.

The RAA271082 is available in a 4mm×4mm 24-lead Step Cut QFN (SCQFN) package with an exposed pad for improved thermal performance. It is AEC-Q100 qualified to Grade 1 and operates across an ambient temperature range of -40°C to 125°C and is electrically specified across a junction temperature range of -40°C to 150°C. Automotive PMIC for 32-bit Microcontrollers in BMS, Zone Controller, Domain Controller, and Gateway applications.

Applications

- Driver monitoring cameras
- Rear and surround view HD automotive cameras
- Microcontroller PMIC for battery management systems
- Microcontroller PMIC for zone and domain controllers
- Microcontroller PMIC for gateway units

Features

- ASIL-D ISO26262 Development Process
- VIN Operating Range from 4.0 to 42V
  - Start Range 4.5 to 42V
- Fixed Switching frequency: 2.2MHz with optional pseudo-random spread spectrum
- Three synchronous bucks with internal compensation and one LDO
  - Buck1 output range: 2.8V to 5.05V, up to 1A
  - Buck2/3 output range: 0.85V to 3.3V, up to 1A
  - LDO4 output range: 2.7V to 3.4V, up to 300mA
- OTP UV/OV Thresholds: ±4%, ±6%, ±8%, ±12%
- OTP power up/down sequence and delay
- Optional output discharge on Buck2, Buck3, and LDO4
- Configurable GPIO pin
- Dual EN pins
- Protection Features
  - Input Voltage UVLO
  - Output OV/UV
  - Overcurrent protection on internal and output LDOs
  - Over-temperature shutdown
- Functional Safety Features
  - Built-in Self Test (BIST) at power up
  - Dual Bandgap/Reference Chains
  - Independent UV/OV sense path for Buck1 Output
  - Configurable Window Watchdog Timer (WWDT)
  - Continuous CRC checking of OTP shadow registers
  - CRC protected I^2C communication
  - Configurable fault manager
- AEC-Q100 Qualified, Grade 1: -40°C to +125°C (T_J = 150°C)

Contents

1. Overview

1.1 Typical Application Schematic

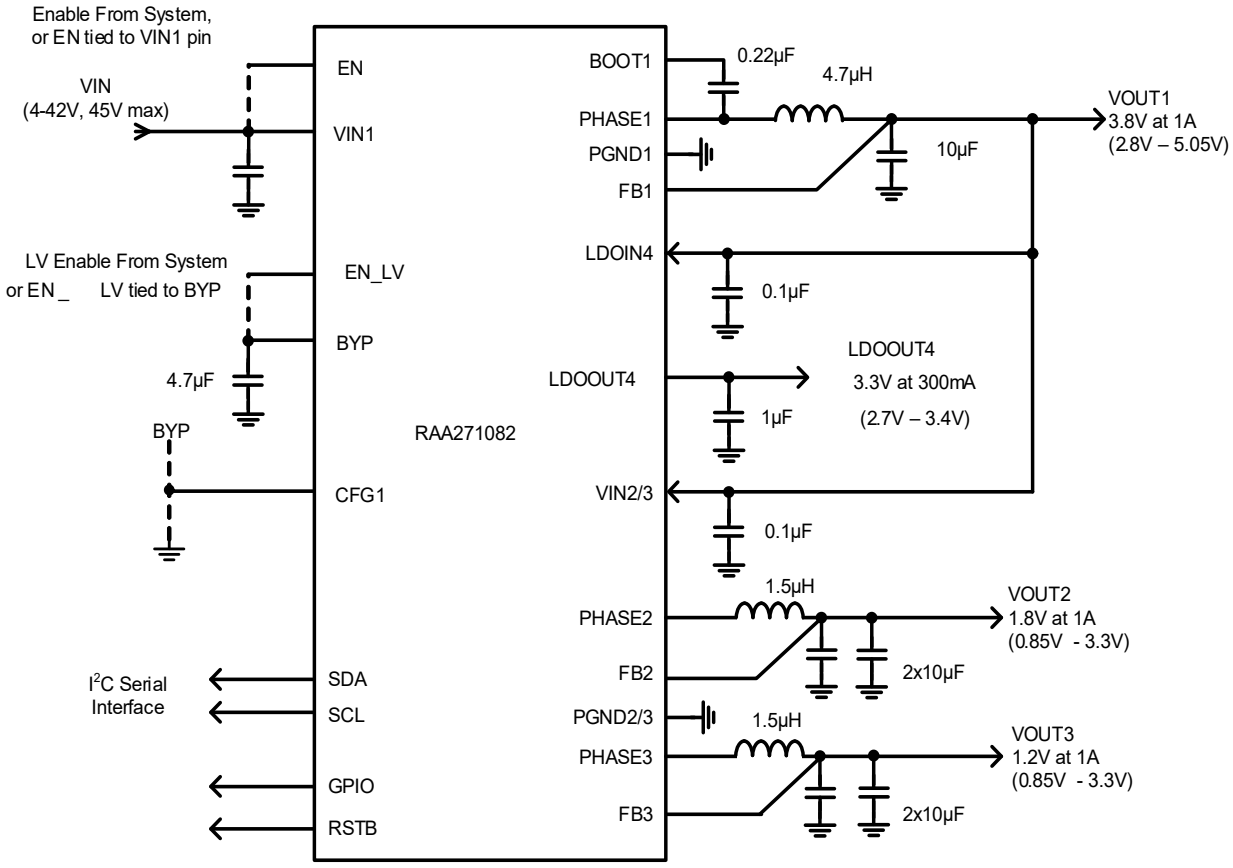


Figure 1. Typical Application Schematic

1.2 Block Diagram

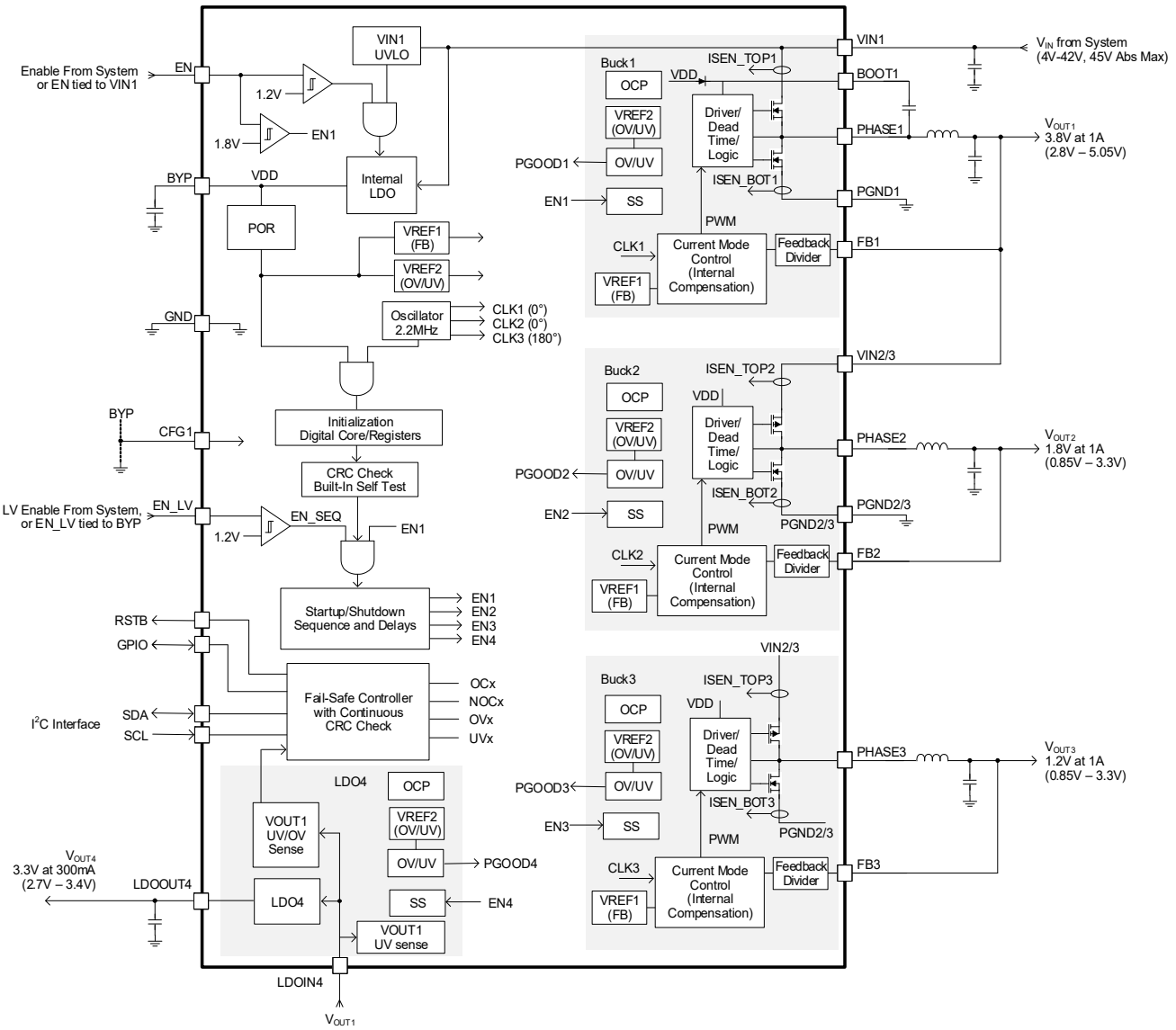
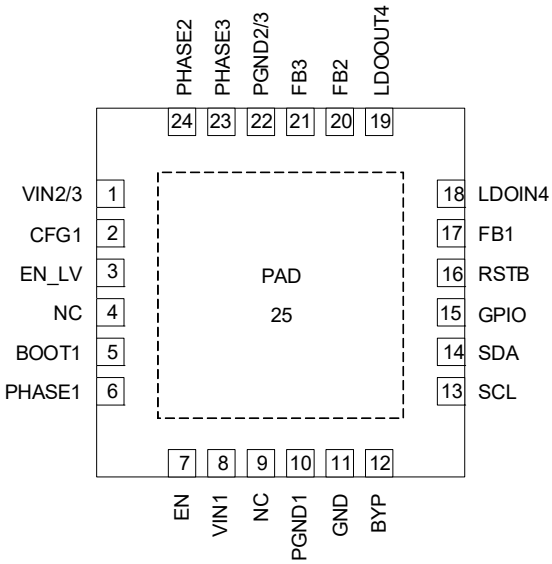


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Name	Pin #	Description
VIN2/3	1	**Supply input for Buck2 and Buck3.** VIN2/3 must be connected to VOUT1. VIN2/3 is the input to the Buck2 and Buck3 switching regulators. Place a ceramic decoupling capacitor (10µF) from VIN2/3 to PGND2/3, located as close as possible. The DC voltage applied to VIN2/3 should not exceed 5.5V during normal operation.
CFG1	2	**Buck1 configuration input.** CFG1 is a tri-level input that configures the Buck1 regulator loop compensation. For details see Configure Pin in Buck1 Electrical Specifications. The three levels are (a) tied low to GND, (b) tied to BYP, and (c) open or floating. In the floating state, the CFG1 voltage is internally pulled to 50% (typical) of the BYP supply voltage. **Note:** The CFG1 pin state is read once and latched during Startup.
EN_LV	3	**Enable Input for Low Voltage Outputs.** EN_LV is the enable input that controls the low voltage outputs (Buck2, Buck3, and LDO4). When EN_LV is high, the low voltage regulator startup sequence begins. When EN_LV is set low, the low voltage outputs turn off in reverse sequence. The EN_LV pin has an input range of 0V to VBYP. **Note:** The EN_LV pin is ignored when VOUT1 is off.
NC	4	**No connection.** Not internally connected. **Note:** This pin must be unconnected to provide spatial clearance between high-voltage and low-voltage pins on the IC. Do not connect this pin to any net nor to GND.
BOOT1	5	**Buck1 high-side MOSFET driver supply.** BOOT1 provides bias voltage for the Buck1 high-side MOSFET driver. Place a 0.22µF ceramic capacitor between the BOOT1 and PHASE1 pins. The internal bootstrap circuit recharges the boot capacitor when the Buck1 low-side switch is on.
PHASE1	6	**Switching node of Buck1.** PHASE1 is the connection point of the high-side N-channel MOSFET and low-side N-channel MOSFET switches of Buck1.

Pin Name	Pin #	Description
EN	7	**Enable control input.** EN is a tri-level input. When EN is below 0.95V, the IC is disabled and all faults are cleared. When EN is between 1.2V and 1.6V, the device enters Standby Mode. The BYP LDO is enabled and factory OTP registers are scanned, but all outputs and switching are disabled. Standby Mode allows changes to be made to the Option Registers using the I^2C interface. When EN exceeds 1.85V, the HV Buck1 is enabled and switching begins. The LV outputs (Buck2, Buck3, and LDO4) are also enabled if the EN_LV input is logic high. The DC voltage applied to EN should not exceed 42V during normal operation. The EN pin can withstand transients up to 45V.
VIN1	8	**Supply input for the IC and Buck1 switching regulator.** VIN1 supplies the Buck1 switching regulator and also supplies the BYP regulator that powers IC circuits. Place a minimum 2.2µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor from VIN1 to PGND1, located as close as possible to the IC.
NC	9	**No connection.** Not internally connected.This pin must be unconnected to provide spatial clearance between high-voltage and low-voltage pins on the IC. Do not connect this pin to any net nor to GND.
PGND1	10	**Ground return of Buck1.** Provides the return path for the low-side MOSFET and drivers of Buck1. The traces connecting this pin to the decoupling capacitor between VIN1 and PGND1 should be as short as possible. Any sensitive signal traces should not connect directly to this ground path. Connect this pin to the ground copper plane and add multiple ground vias close to this pin.
GND	11	**System ground.** Analog ground pin for internal sensitive analog circuits. Connect GND to a large copper ground plane free from large noisy signals. Connect this pin to PGND1 (pin 10) directly at the pins, with separate ground islands for PGND1 and GND for the associated components. In layout power flow planning, divert any noisy high currents away from the area around this pin and the analog sense pins of the IC.
BYP	12	**BYP LDO bypass.** Bypass/output node of the BYP regulator that supplies bias voltage for the IC. Connect a 4.7µF ceramic capacitor between this pin and PGND1. The BYP LDO supplies a fixed 4.3V bias but the bias operating range is 3V to 5.5V.
SCL	13	**Digital clock input.** The serial clock input to the I^2C interface. Requires external pull-up.
SDA	14	**Digital Data input/output.** Serial data input/output to I^2C interface. Requires external pull-up.
GPIO	15	**Digital general-purpose I/O.** The GPIO pin is an open-drain pin that can serve as a status monitor, windowed watchdog timer, or general-purpose I/O. At power-up, the pin is low while the device initializes. When initialization is complete, the GPIO remains low and the outputs begin switching. The GPIO pin function can then be reassigned through the I^2C interface using register 0xA4.
RSTB	16	**System reset output.** The RSTB is an active low/active high output that provides a reset (low) signal to the system MCU when a fault occurs. Faults that trigger the RSTB output are listed in the RSTB information section. Any faults detected can be read from the Fault Status Registers. Note: When the RSTB output is high, it is internally driven to the BYP voltage, typically 4.3V. Devices connected to this pin must be able to tolerate signal levels up to the BYP voltage or use a resistor divider to reduce the voltage at the receiving end.
FB1	17	**Buck1 output voltage sensing input.** Connect FB1 to the output of Buck1 to provide the feedback sense voltage for the Buck1 regulator. The Buck1 output voltage is factory-programmable from 2.8V to 5.05V. The Buck1 UV/OV thresholds are factory-programmable also. Route the FB1 trace away from noisy or high-dV/dt signals. **Note:** Buck1 UV/OV is sensed through the LDOIN4 input, not through the FB1 input.
LDOIN4	18	**Input to LDO4.** LDOIN4 is the input of the low-dropout linear regulator LDO4. LDO4IN must be connected to the output of Buck1. (The Buck1 output voltage is sensed at FB1, the pin adjacent to LDO4IN.) **Note:** LDOIN4 also functions as the UV/OV sense point for Buck1.
LDOOUT4	19	**Output of LDO4.** LDOOUT4 is the output of the low-dropout linear regulator LDO4. The output voltage is factory-programmable from 2.7V to 3.4V.

Pin Name	Pin #	Description
FB2	20	**Buck2 output voltage sensing input.** Connect FB2 to the output of Buck2 to provide the feedback sense voltage for the Buck2 regulator. The FB2 pin is also the sense point for the Buck2 UV and OV comparators. Route the FB2 trace away from noisy or high-dV/dt signals.
FB3	21	**Buck3 output voltage sensing input.** Connect FB3 to the output of Buck3 to provide the feedback sense voltage for the Buck3 regulator. The FB3 pin is also the sense point for the Buck3 UV and OV comparators. Route the FB3 trace away from noisy or high-dV/dt signals.
PGND2/3	22	**Shared ground return for Buck2 & Buck3**. Return path for the low-side MOSFETs and gate drivers of Buck2 and Buck3. The decoupling capacitor between VIN2/3 and PGND2/3 should be routed using direct, short PCB traces. Any sensitive signal traces should not share traces with this PGND2/3 return path. Connect this pin to the ground copper plane and add multiple ground vias close to the pin.
PHASE3	23	**Switching node of Buck3.** Connection point of the high-side and low-side MOSFET switches of Buck3.
PHASE2	24	**Switching node of Buck2.** Connection point of the high-side and low-side MOSFET switches of Buck2.
PAD	-	**Package thermal pad.** PAD must be soldered to a large ground plane on the PCB. Use multiple vias to provide a heat path for the IC package. PAD is not connected internally.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Buck1 Power			
VIN1 to PGND1	-0.3	+45	V
PHASE1 to PGND1 (DC)	-0.3	VIN + 0.3	V
PHASE1 to PGND1 (20ns)	-2	VIN + 0.3	V
BOOT1 to PHASE1	-0.3	+6.0	V
Buck2, Buck3, LDO4 Power			
VIN2/3 to PGND2/3 (DC)	-0.3	5.8	V
VIN2/3 to PGND2/3 (20ns)	-0.3	7.0	V
PHASE2, PHASE3 to PGND2/3 (DC)	-0.3	VIN2/3 + 0.3	V
PHASE2, PHASE3 to PGND2/3 (20ns)		7.0	V
PHASE2, PHASE3 to PGND2/3 (100ns)	-2.0		V
LDOIN4, LDOOUT4 to PGND2/3	-0.3	5.8	V
Analog and Digital I/O			
EN to GND	-0.3	+45	V
BYP, FB1, FB2, FB3 to GND	-0.3	+6.5	V
SCL, SDA, GPIO to GND	-0.3	+6.5	V
EN_LV, CFG1, RSTB to GND	-0.3	BYP + 0.3	V

3.2 ESD Ratings

ESD Model/Test	Pins	Ratings	Unit
Human Body Model (Tested per AEC-Q100-002)	All Pins	2	kV
Charged Device Model (Tested per AEC-Q100-011)	Corner	750	V
	Other	500	V
Latch-Up (Tested per AEC-Q100-004; Class 2, Level A)	-	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
24 Ld SCQFN Package	35.6	1.2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range	-55	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
V_{IN1} Supply Voltage	4[1]	42	V
EN to GND	0	42	V
EN_LV to GND	0	5.5	V
$V_{IN2/3}$ Supply Voltage Range	2.8	5.5	V
Buck1 Output Current	0	1.0	A
Buck2, Buck3 Output Current	0	1.0	A
LDO4 Output Current	0	0.3	A
Operating Junction Temperature Range	-40	+150	°C
Ambient Temperature Range	-40	+125	°C
CFG1 to GND	0	BYP	V

1. Minimum VIN1 voltage for startup is 4.5V. After startup, the device can operate down to 4.0V.

3.5 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN1 Startup Threshold Voltage	$V_{IN1(UV)}$	VIN1 rising (Factory Options)	-5%	4.5 (5.0, 6.5, 7.0)	5%	V
		VIN1 falling	3.45	3.60	3.77	V
		VIN1 hysteresis				
VIN1 Operating Voltage Range	V_{IN1}		4		42	V
VIN1 Supply Shutdown Current	I_{SD}	EN ≤ 0.4V, VIN1 = 12V		1.6	10	µA
VIN1 Supply Standby Current		EN = 1.5V, VIN1 = 12V, EN_LV = GND		4		mA
VIN1 Supply Operating Current[1]		Figure 1. EN = VIN1 = 12V, EN_LV = BYP. No load on BYP, VOUT1, VOUT2, VOUT3, VOUT4.		17		mA
EN Pin						
EN Shutdown Threshold Voltage	$V_{EN(OFF)}$				0.4	V
EN Enable Standby Threshold Voltage	$V_{EN(LDO)}$	EN Rising (Standby)	0.71	1.2	1.70	V
		EN Falling (Standby)	0.52	0.86	1.23	V
		Falling Hysteresis		-340		mV

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V. **(Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Enable Buck1 Threshold Voltage	$V_{EN(BK1)}$	EN Rising (Buck1 On)	1.72	1.78	1.83	V
		EN Falling (Buck1 On)	1.54	1.59	1.64	V
		Falling Hysteresis		-190		mV
EN Disable Off-Delay		Delay from EN falling edge to commencing shutdown sequence.		300		µs
EN Pin Input Leakage		EN = 4V to 42V		0.01		µA
EN_LV Pin						
EN_LV Input Leakage Current			-1		1	µA
EN_LV Low-Level Input Voltage	V_{IL}	(Schmitt input)			0.5	V
EN_LV High-Level Input Voltage	V_{IH}		1.7			V
		Falling Hysteresis		315		mV
EN_LV Off-Delay		Delay from EN_LV falling edge to commencing VOUT2/3/4 shutdown sequence.		300		µs
Internal LDO (BYP)						
Internal LDO Voltage (BYP Pin)	$V_{DD(INT)}$	VIN1 = 12V, EN = 1.6V, I_{BYP} = 0mA	4.0	4.3	4.5	V
		VIN1 = 12V, EN = 1.6V, I_{BYP} = 20mA	4.0	4.3	4.5	V
Internal LDO Dropout Voltage (VDROPOUT = VIN1 – BYP)		VIN1 = 4V, EN = 1.6V, I_{BYP} = 20mA		71	145	mV
Power-On Reset Threshold Voltage (BYP Pin)	V_{POR}	BYP Falling	2.80	3.15	3.50	V
		BYP Rising	3.42	3.60	3.85	V
		Rising Hysteresis		450		mV
Thermal Shutdown[1]	T_{SD}	Temperature Rising	151	160	170	°C
	$T_{SD(HYS)}$	Falling Hysteresis		15		°C
Switching Frequency	f_{SW}	Spread Spectrum Disabled	1.98	2.20	2.42	MHz
Fault Protection Hiccup Mode Interval	t_{HICCUP}	Hiccup Timeout Period	180	200	220	ms
Buck2 On-Edge to Buck1 On-Edge Phase Relationship				0		°
Buck3 On-Edge to Buck1 On-Edge Phase Relationship		Factory default, (0° option available)		180, (0)		°

1. Assured by design.

3.5.1 Buck1 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Configure Pin						
CFG1 Input Low Voltage			1.283	1.498	1.685	V
CFG1 Input Open Voltage		DC voltage measured at open pin	2.119	2.187	2.255	V
CFG1 Input High Voltage			2.615	2.854	3.026	V
CFG1 Leakage		CFG1 driven by DC source, 0V to BYP.	-29.3		+31	µA
FB1 Pin Input Impedance	R_{FB1}			89		kΩ
FB1 Pin Voltage Accuracy at VOUT1 = 3.8V[1][2]	V_{FB1}	T_J = -40°C to +150°C, I_{VOUT1} = 0mA Factory Programmed. Other voltage options available.	3.743 [-1.5%]	3.8	3.857 [+1.5%]	V
Buck1 Soft-Start Ramp Time		VOUT1 = from 0% to 95%, (factory options, see Output Soft-Start Ramp)		1.2		ms
Upper Pulse-Skipping Threshold		VIN1 rising	18.99	19.55	20.14	V
		VIN1 falling Hysteresis		1.0		V
Undervoltage Threshold	$V_{FB1(UV)}$	VFB1 falling (Factory options)	-1.5	-8 (-4, -6, -12)	+1.5	%
		VFB1 rising hysteresis	+0.4%	+0.8%	+1.2%	%
Severe Undervoltage Threshold		VFB1 Falling	-24	-20	-16	%
Undervoltage Fault Delay		FB1 < $V_{FB1(UV)}$ (Factory options additional delay)		2 (10, 25, 45)		µs
Overvoltage Threshold	$V_{FB1(OV)}$	VFB1 rising (Factory options)	-1.5	+8 (+4, +6, +12)	+1.5	%
		VFB1 falling hysteresis	-0.4	-0.8	-1.2	%
Overvoltage Fault Delay				2		µs
Severe Undervoltage Threshold		VFB1 falling	-24	-20	-16	%
Severe Overvoltage Threshold		VFB1 rising	-16	+20	24	%
Buck1 Output Current Protection						
OC1 Overcurrent Limit, Cycle-by-Cycle	$I_{1(OC1)}$	Factory programmed. (Factory options)	1.2	1.5 (1.2, 1.75)	1.8	A
Overcurrent Limit Blanking Time				75	105	ns
OC2 Overcurrent Limit, Hiccup/Latch-Off	$I_{1(OC2)}$		1.61	2.00	2.42	A
Overcurrent Hiccup Delay		Consecutive cycles on $I_{1(OC2)}$		7		cycles
Negative Current Limit Detection	$I_{1(NLIM)}$	Factory programmed. (Factory options)		-0.80 (-1.0)		A
High-side Switch On-Resistance	R_{HDS}	I_{PHASE1} = 100mA, VIN1 = 12V, BYP = 3.8V, BOOT = 3.8V		430		mΩ
Low-side Switch On-Resistance	R_{LDS}	I_{PHASE1} = 100mA, VIN1 = 12V, BYP = 3.8V		336		mΩ

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V. **(Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum On-Time[3]	t_{ON}	VIN1 = 5.5V	20	35	49	ns
Minimum Off-Time[3]	t_{OFF}		24	36	49	ns
PHASE1 Rise Time[1]	t_{RISE1}	Figure 1. VIN1 = 12V, V_{OUT1} at 200mA load.		4		ns
PHASE1 Fall Time [1]	t_{FALL1}			4		ns
PHASE1 Leakage Current		VOUT1 not switching			460	nA

1. Buck1 not in Pulse Skipping Mode and Buck1 On-time is greater than the minimum on-time.
2. Electrical Specification limits apply only for the factory-programmed settings.
3. Minimum on-time and minimum off-time required to maintain loop stability and output regulation.

3.5.2 Buck2 and Buck3 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN2/3 Voltage Range		Internal compensation	2.8		5.5	V
VIN2/3 Undervoltage Threshold	$V_{IN2/3\_UV}$	Rising. No output load.		2.42	2.60	V
		Falling. No output load.	2.10	2.30		V
VIN2/3 Quiescent Supply Current[1]	$I_{VIN2/3}$	Figure 1 VIN1 = 12V, f_{SW} = 2.2MHz. VIN2/3 = 3.8V. VOUT2 = 1.8V, VOUT3 = 1.2V. No load on all outputs.		10		mA
VIN2/3 Shutdown Supply Current	$I_{SD\_VIN2/3}$	EN_LV = 0V, VIN2/3 = 5.5V		11	18.3	µA
Output Regulation						
FB2 Pin Voltage Accuracy at VOUT2 = 1.8V	V_{FB2}	T_J = -40°C to +150°C, I_{VOUT2} = 0mA (Factory options)	1.773 [-1.5%]	1.8 (0.85V – 3.3V)	1.827 [-1.5%]	V
FB3 Pin Voltage Accuracy at VOUT3 = 1.8V	V_{FB3}	T_J = -40°C to +150°C, I_{VOUT3} = 0mA (Factory options)	1.182 [+1.5%]	1.2 (0.85V – 3.3V)	1.218 [+1.5%]	V
Buck2 Soft-Start Ramp Time		V_{OUT2} = 1.8V, from 0% to 95% (factory options, see Output Soft-Start Ramp)		1.2		ms
Buck3 Soft-Start Ramp Time		V_{OUT3} = 1.2V, from 0% to 95% (factory options, see Output Soft-Start Ramp)		0.82		ms
Output Voltage Protection						
Undervoltage Threshold[1]	$V_{FB2(UV)}$	V_{FB2} falling (Factory options)	-1.5	-8 (-4, -6, -12)	+1.5	%
		V_{FB2} Undervoltage tolerance With respect to Programmed UV target	-1.5		+1.5	%
		V_{FB2} Undervoltage Hysteresis	+0.4	+0.8	+1.2	%

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C VIN1 = 12V. **(Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overvoltage Threshold[1]	$V_{FB2(OV)}$	V_{FB2} rising (Factory options)	-1.5	+8 (+4, +6, +12)	+1.5	%
		V_{FB2} Overvoltage tolerance With respect to Programmed OV target	-1.5		+1.5	%
		V_{FB2} Overvoltage Hysteresis	-0.4%	-0.8%	-1.2%	%
Undervoltage Threshold[1]	$V_{FB3(UV)}$	V_{FB3} falling (Factory options)	-1.5	-8 (-4, -6, -12)	+1.5	%
		V_{FB3} Undervoltage tolerance With respect to Programmed UV target	-1.5		+1.5	%
		V_{FB3} Undervoltage Hysteresis	+0.4	+0.8	+1.2	%
Overvoltage Threshold[1]	$V_{FB3(OV)}$	V_{FB3} rising (Factory options)	-1.5	+8 (+4, +6, +12)	+1.5	%
		V_{FB3} Overvoltage tolerance With respect to Programmed OV target	-1.5		+1.5	%
		V_{FB3} Overvoltage Hysteresis	-0.4%	-0.8%	-1.2%	%
Undervoltage Fault Delay		FB2 < V_{FB2}(UV) (Factory options)		2 (10, 25, 45)		µs
		FB3 < V_{FB3}(UV) (Factory options)		2 (10, 25, 45)		µs
Output Current Protection						
Overcurrent Limit, Cycle-by-cycle	$I_{2(LIM)}$, $I_{3(LIM)}$	Buck2 and Buck3 (Factory options: Buck2 and Buck3 overcurrent limits are independent)		1.2 (0.96, 1.56)		A
Overcurrent Fault Delay				100		cycles
Negative Current Limit	$I_{2(NLIM)}$, $I_{3(NLIM)}$		-1.30	-0.88	-0.49	A
Feedback Pin						
FB2, FB3 Pin Input Impedance	R_{FB2}, R_{FB3}			64		kΩ
Power MOSFETs						
High-side PMOS Switch On-Resistance		$I_{PHASE2,3}$ = 100mA, VIN2/3 = 3.8V		372		mΩ
Low-side NMOS Switch On-Resistance		$I_{PHASE2,3}$ = 100mA, VIN2/3 = 3.8V		161		mΩ
PHASE2, PHASE3 Maximum Duty				90		%
PHASE2, PHASE3 Minimum On-Time					100	ns

1. Undervoltage and Overvoltage factory programmed selections for VOUT1, VOUT2, VOUT3, and LDO4 are independent.

3.5.3 LDO4 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
Input Voltage Range	V_{IN4}	Connected to VOUT1, VIN2/3	2.6		5.5	V
Output Regulation						
Output Voltage	$V_{LDOOUT4}$	VIN2/3 = 3.8V, $V_{LDOOUT4}$ = 3.3V (Factory options)	3.251 [-1.5%]	3.300 (2.7V-3.4V)	3.350 [+1.5%]	V
Dropout Voltage		$V_{LDOOUT4}$ = 3.3V, $I_{LDOOUT4}$ = 300mA, 2% drop at $V_{LDOOUT4}$		112	240	mV
Power Supply Rejection Ratio[1]		At 1kHz, T_A = 25°C, VIN2/3 = 3.8V, Typical Application Schematic on page 3, $V_{LDOOUT4}$ = 3.3V, $I_{LDOOUT4}$ = 300mA		55		dB
LDOOUT4 Soft-Start Ramp Time		V_{OUT4} = 3.3V, from 0% to 95%		1.55		ms
Output Voltage Protection						
Undervoltage Threshold[2]	$V_{LDO4(UV)}$	$V_{LDOOUT4}$ falling (Factory options)		-8 (-4, -6, -12)		%
		$V_{LDOOUT4}$ Undervoltage tolerance With respect to Programmed UV target	-1.5%		+1.5%	
		$V_{LDOOUT4}$ rising Hysteresis	+0.4%	+0.8	+1.2%?	%
Overvoltage Threshold[2]	$V_{LDO4(OV)}$	$V_{LDOOUT4}$ rising (Factory options)		+8 (+4, +6, +12)		%
		$V_{LDOOUT4}$ Overvoltage tolerance With respect to Programmed OV target	-1.5%		+1.5%	
		$V_{LDOOUT4}$ falling Hysteresis	-0.4%	-0.8%	-1.2%	%
Undervoltage Fault Delay		$V_{LDOOUT4}$ < $V_{LDO4(UV)}$ (Factory options)		2 (10, 25, 45)		µs
Output Current Protection						
Overcurrent Limit	$I_{4(LIM)}$		322	422	526	mA

1. Assured by design.
2. Undervoltage and Overvoltage factory programmed selections for FB1, FB2, FB3, and LDO4 are independent.

3.5.4 Digital I/O Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RSTB Output High $r_{DS(ON)}$		BYP = 4.0V RSTB source current 2mA		60		mΩ
RSTB Output Low $r_{DS(ON)}$		BYP = 4.6V RSTB sink current 2mA		97		mΩ
GPIO Input High Threshold	$VIH_{(GPIO)}$	BYP = 4.3V, GPIO configured as input	2.24			V
GPIO Input Low Threshold	$VIL_{(GPIO)}$	BYP = 4.3V, GPIO configured as input			1.60	V
GPIO Output Open-Drain Leakage Current	$I_{(GPIOLK)}$	GPIO configured as output, GPIO pull-up voltage 3.8V.			1	µA
GPIO Output Low Voltage	$VOL_{(GPIO)}$	GPIO configured as output, BYP = 4.0V GPIO pin sink current = 5mA			0.4	V

3.5.5 I^2C Interface Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50 °C and VIN1 = 12V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA Input High Threshold			1.14			V
SCL, SDA Input Low Threshold					0.8	V
SCL, SDA Input Hysteresis				134		mV
SCL Clock Frequency					400	kHz
SCL Falling Edge to SDA Valid Time				1		µs
SCL, SDA Output Open-Drain Leakage Current		V_{SCL} = 5V			1	µA
SCL, SDA Pin Capacitance				5		pF
SDA Output Low Voltage	$VOL_{(SDA)}$	SDA sink current = 3mA			0.5	V

4. Typical Performance Curves

4.1 Efficiency, Input Current

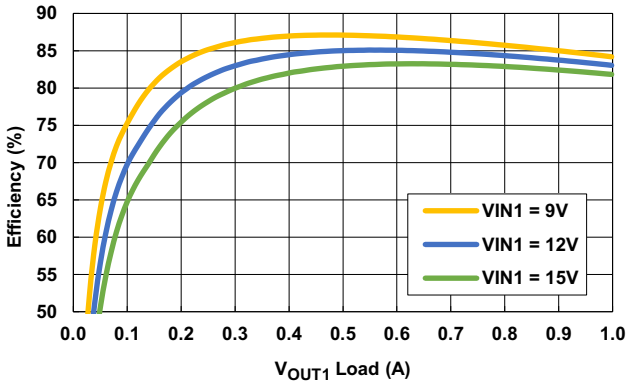


Figure 3. V_{IN} to V_{OUT1} = 3.8V, Efficiency vs Load

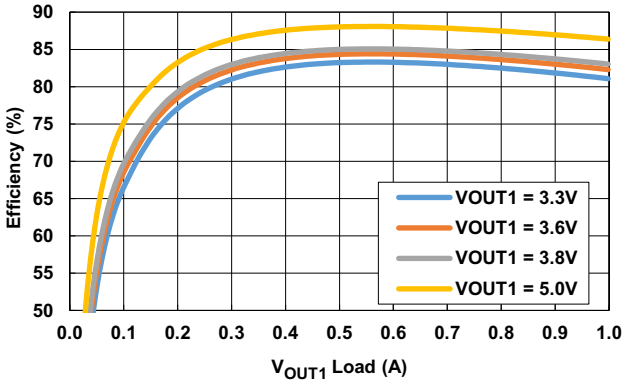


Figure 4. V_{IN} = 12V to V_{OUT1}, Efficiency vs Load

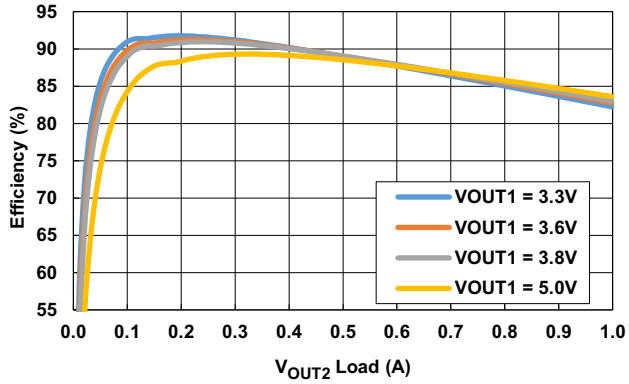


Figure 5. V_{OUT1} to V_{OUT2} = 1.8V, Efficiency vs Load

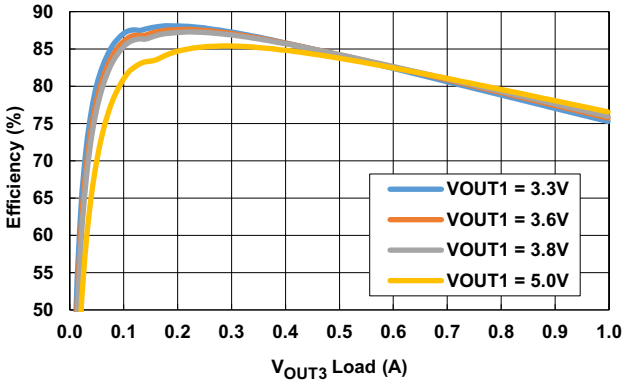


Figure 6. V_{OUT1} to V_{OUT3} = 1.2V, Efficiency vs Load

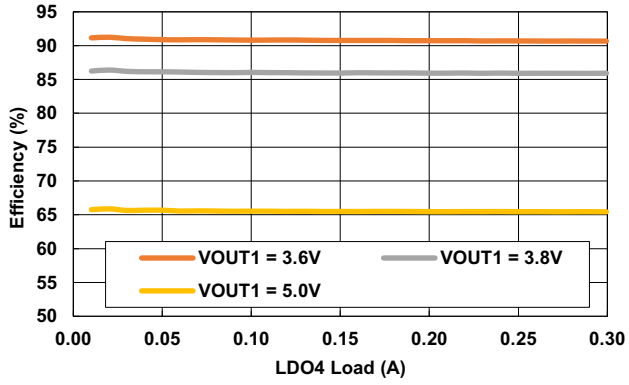


Figure 7. V_{OUT1} to LDO4 = 3.3V, Efficiency vs Load

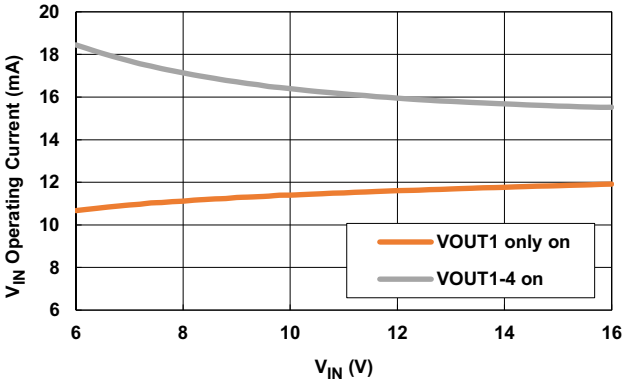


Figure 8. V_{IN} Operating Current, No Load

4.2 Load Regulation

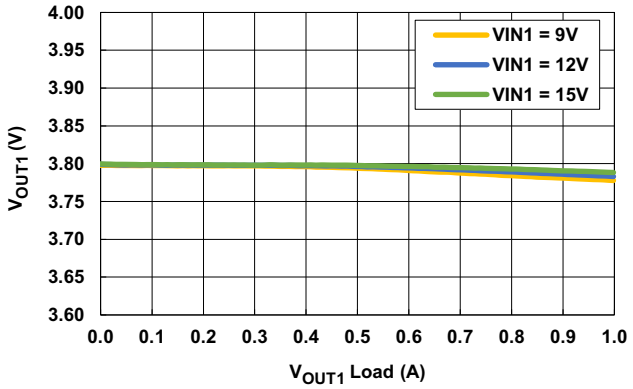


Figure 9. V_{OUT1} = 3.8V, Load Regulation

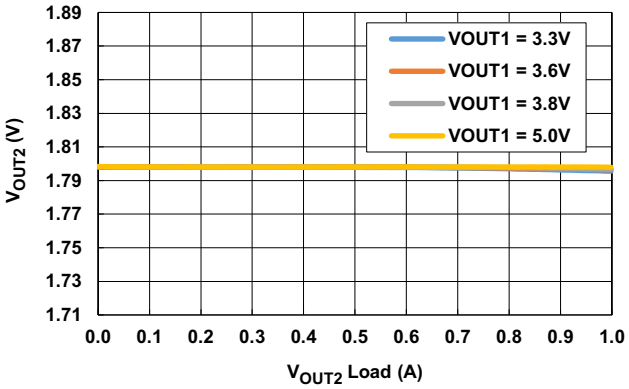


Figure 10. V_{OUT2} = 1.8V, Load Regulation

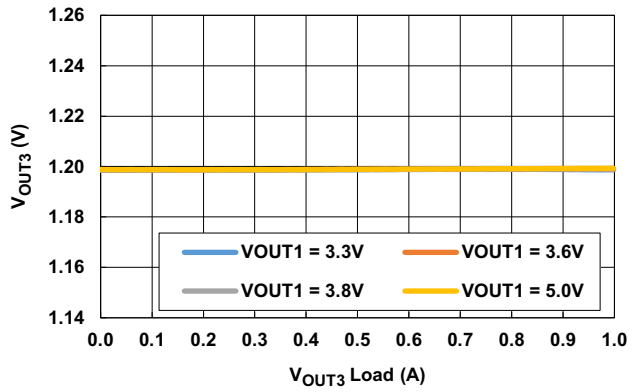


Figure 11. V_{OUT3} = 1.2V, Load Regulation

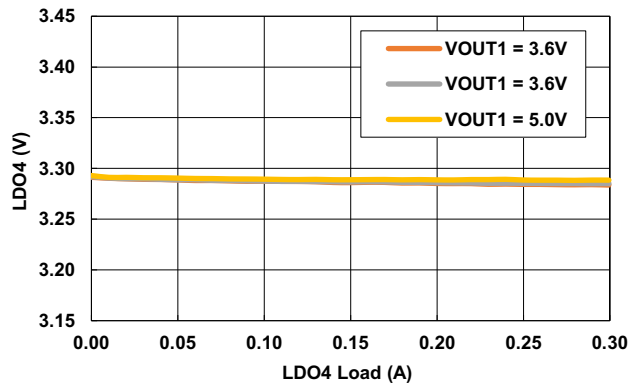


Figure 12. LDO4 = 3.3V, Load Regulation

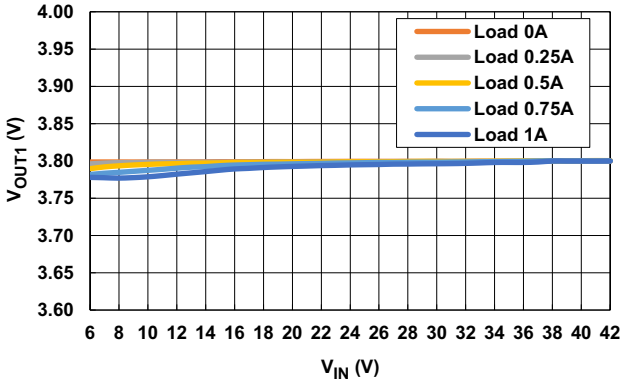


Figure 13. V_{OUT1} = 3.8V, Line Regulation

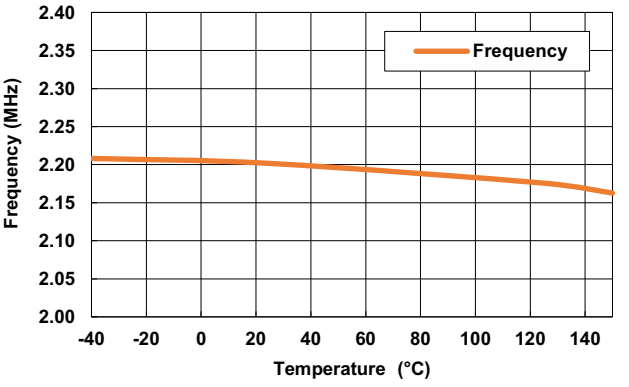


Figure 14. Frequency vs Temperature

4.3 Line Regulation, Switching Waveforms

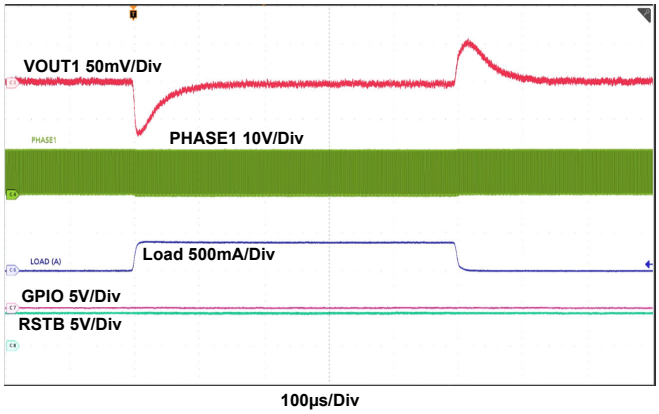


Figure 15. V_{OUT1} Load Transient, 0A to 0.375A

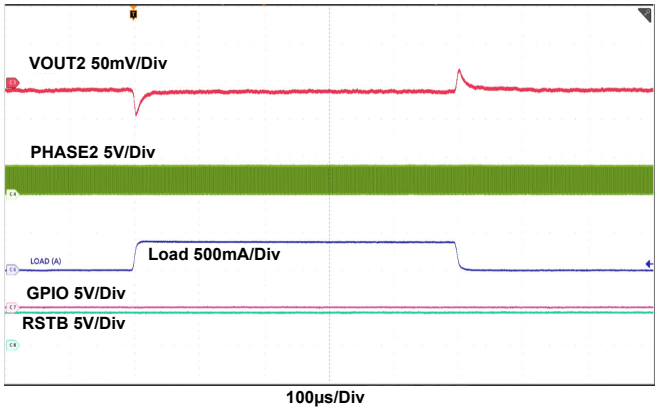


Figure 16. V_{OUT2} Load Transient, 0A to 0.375A

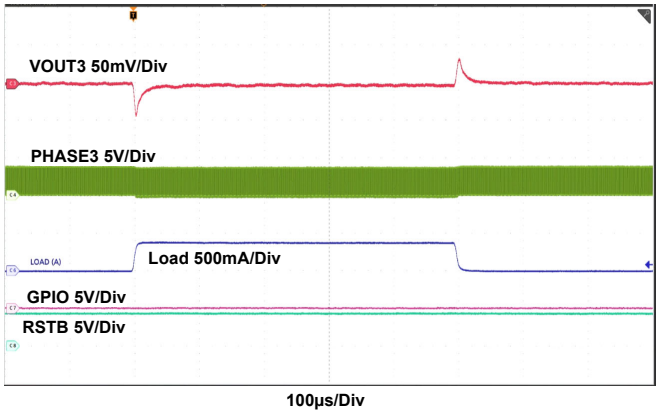


Figure 17. V_{OUT3} Load Transient, 0A to 0.375A

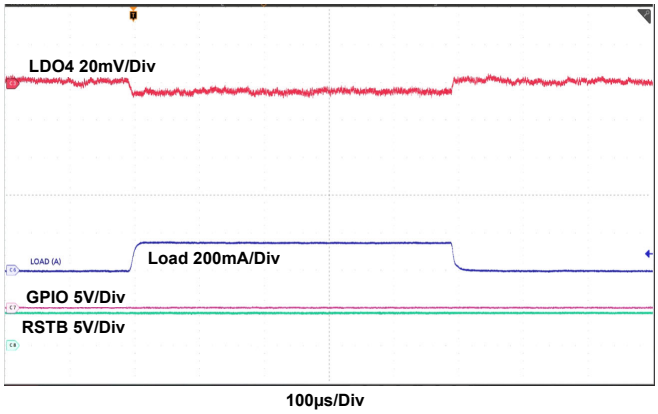


Figure 18. V_{OUT4} Load Transient, 0A to 0.375A

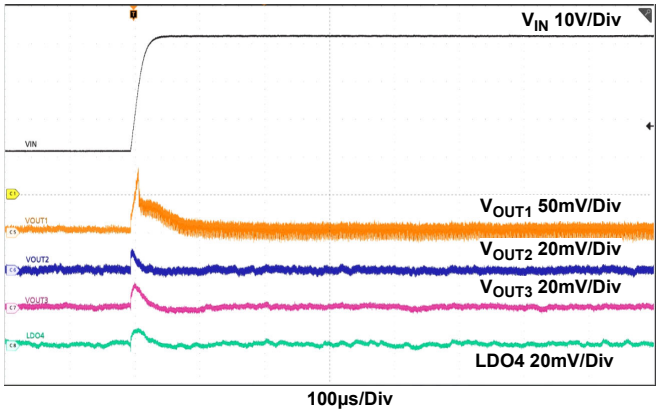


Figure 19. V_{IN} Transient, 12V to 42V, No Load

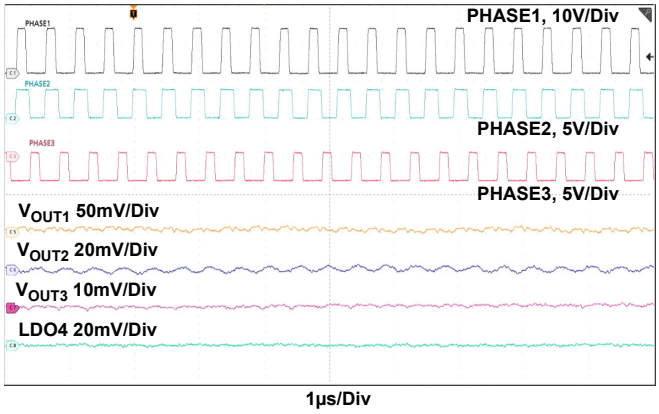


Figure 20. Switching Operation

4.4 Load and Line Transient Response

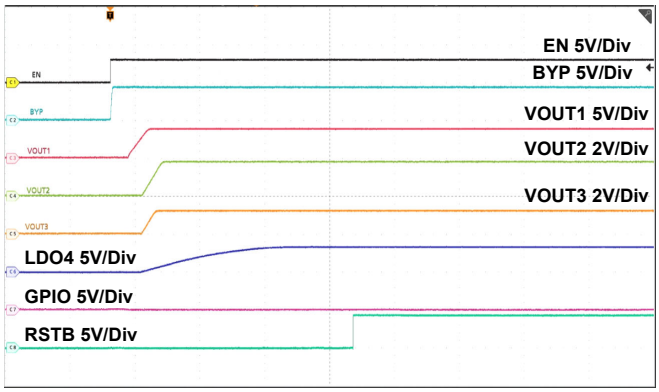


Figure 21. Startup using EN toggle, V_{IN} = 12V

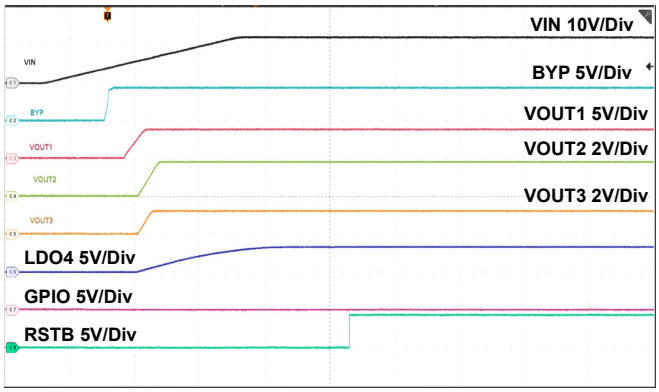


Figure 22. Startup using V_{IN} Ramp, EN Connected to VIN

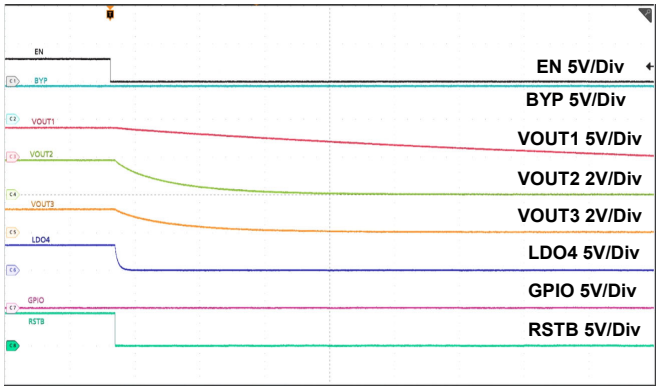


Figure 23. Shutdown using EN toggle, V_{IN} = 12V

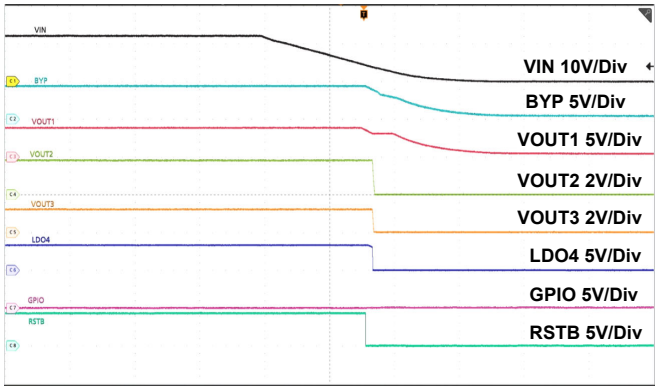


Figure 24. Shutdown using V_{IN} ramp, EN connected to VIN

5. Functional Descriptions

5.1 I²C Programming Options

The RAA271082 multi-rail regulator has numerous options which are factory-set through one-time-programming (OTP). Additionally, the device contains an I²C interface that allows the user to select other options, enabling the device to be tested in different configurations. Most of the OTP options cannot be changed unless the device is first placed in Standby mode, in which the required options can be selected using I²C commands, and then re-enable the outputs. The following are the options that can be changed using the I²C interface.

An OTP creation tool is available to aid in the selection of programming options.

5.1.1 Voltage Options

- Output voltage options for Buck1, Buck2, Buck3, LDO4. All options are independently selectable.

5.1.2 Sequence and Switching Options

- Output Sequencing, Startup delay, and Shutdown delay. All options are independently selectable.
- Direct startup and shutdown control of each output (disable the internal output sequencing).
- Enable/disable output discharge for Buck2, Buck3, LDO4. All options are independently selectable.
- Spread Spectrum (Off or seven options for spread spectrum).
- Phase shift between Buck1 and Buck3 (0° or 180°).

5.1.3 Fault Detection Options

All Fault Detection options can be disabled except for over-temperature. Disabling detection masks the fault from affecting the RSTB or GPIO pins but does not disable the response to the fault. Some fault responses can be changed or disabled, as listed in Table 1.

Table 1. Fault Detection Options

Fault	Options	Register(s)
Output Overvoltage All OV thresholds are independently selectable.	+4%, +6%, +8% (default), +12%	0x72 (Buck1) 0x74 (Buck2) 0x76 (Buck3) 0x78 (LDO4) Bits 1:0, all registers
Output Undervoltage All UV thresholds are independently selectable.	-4%, -6%, -8% (default), -12%	0x72 (Buck1) 0x74 (Buck2) 0x76 (Buck3) 0x78 (LDO4) Bits 5:4, all registers
Buck1 Severe OV, Buck1 Severe UV	Fixed +20% (OV) and -20% (UV). Fault detection and shutdown response cannot be disabled.	N/A
UV detection delay	0 (default), 10, 25, 45 µs (all are added to fixed 2 µs delay)	0x7B Bits 5:4
Negative Overcurrent, Buck1	-0.8A (default), -1.0A	0x7C Bit 2
Buck1 Overcurrent	1.2A, 1.5A (default), 1.75A	0x7C Bits 1:0
Buck2 Overcurrent	0.96A, 1.20A (default), 1.56A	0x7D Bits 5:4
Buck3 Overcurrent	0.96A, 1.20A (default), 1.56A	0x7C Bits 7:6
VIN1 Undervoltage	Rising edge 4.5V (default), 5.0V, 6.5V, 7.0V	0x70
Over-Temperature	Fault detection and shutdown response cannot be disabled.	N/A

Table 1. Fault Detection Options (Cont.)

Fault	Options	Register(s)
Sequence Fault	Fault detection and shutdown response cannot be disabled.	N/A
Watchdog Timer Fault	Too-slow, Restart (2x too-slow), too-fast	0xA0 through 0xA4
Built-In Self Test (BIST) Faults	Fault detection and shutdown response cannot be disabled.	N/A
CRC recheck	Fault detection and shutdown response cannot be disabled.	N/A
I^2C CRC check	I^2C transactions with or without CRC checking	0x7C Bit 4

Note: Fault detection for an output is locked if the detected fault causes the output to shut down. For example, it is possible to program VOUT1 to shut down on normal overcurrent (OC1). If a slight overload is applied to VOUT1, such that VOUT1 detects the OC1 condition but VOUT1 remains above the Undervoltage threshold, the output shuts down and VOUT1 falls to zero. The device reflects an OC1 fault through register 0x80 Bit 2. The device does not report an Undervoltage or Severe Undervoltage error, because fault detection stops as soon as the output shuts down. Fault detections are all re-enabled when the output attempts the next start-up cycle.

5.1.4 Fault Response Options

- **Shutdown enable/disable for faults:** UV, OV, Negative OC, Buck1 Severe UV/OV, Watchdog Timer
- **Fault response** (restart, latch-off, fixed count restart with latch-off)
- 200ms or 20ms RSTB pulse width on faults for the Windowed Watchdog Timer and the output Sequence controller.
- **30ms delay on RSTB assertion for OV or UV faults.** (Note: If a shutdown fault response is also enabled for the same OV or UV fault, the RSTB pin drives low immediately on the fault. This is because the fault response acts immediately and RSTB drives low because one or more outputs are being shut down.)
- **RSTB pin options:** Can be configured as an indicator for one or more faults.
- **GPIO pin options:** Can be configured as indicator for one or more faults, or as a kick input for Watchdog timer.
- **Latch-off disable:** Clears a latch-off event and allows the regulators to restart.

5.1.5 Status Indicators

- **Fault status on outputs:** Overvoltage, Undervoltage, Overcurrent, Negative Overcurrent
- **Fault status on device:** Over-temperature, Sequence controller, Built-In Self Test, CRC recheck, DAC Reference comparison
- **Fault status on external devices:** Watchdog Timer, I^2C CRC check
- **Restart lockout:** Notifies if the device is in the 200ms timeout, which delays the output restart.
- **Buck1/2/3 and LDO4 regulator status:** Disabled (off), in soft-start, in hiccup or latch-off, enabled (on)

5.2 Programmable Output Voltages

The RAA271082 is comprised of a primary high voltage buck converter (Buck1), two secondary low voltage buck converters (Buck2 and Buck3), and one low dropout linear regulator (LDO4).

All voltage options for Buck1, Buck2, Buck3, and LDO4 are programmed at the factory. The I^2C interface allows users to change the output voltage settings for any of these outputs. This is done by placing the device into Standby mode using the Enable (EN) pin, making the required register changes, then fully enabling the device through the EN pin. This feature allows users to test different configurations.

In typical camera power applications, the primary buck typically takes its input (VIN1) from a filtered 12V car battery, and produces an intermediate voltage typically between 2.8V and 5V. The output voltage of Buck1 is selectable when the part is ordered, and is programmed at the factory. See Table 2 for the list of possible Buck1 output voltages.

The secondary bucks share a common input pin (VIN2/3) that is supplied by Buck1. They produce low voltage supply rails, for example 1.8V and 1.2V. The output voltages of Buck2 and Buck3 are independently selectable and are programmed at the factory. See Table 2 for the list of Buck2 and Buck3 output voltages.

Note: For VOUT1 voltages below 3.2V, Renesas recommends selecting Buck2 and Buck3 voltages with a value of less than 40% of VOUT1.

The linear regulator LDO4 uses the Buck1 output as an input through the LDOIN4 pin. The output voltage of LDO4 is selectable and is programmed at the factory. See Table 2 for the list of LDO4 output voltages.

Note: The voltage level for each output is independently selectable. VOUT2, VOUT3, and LDO4 are derived from VOUT1, and therefore VOUT1 must be set to a higher voltage, with some margin for duty cycle and I*R losses.

Output voltage settings can be changed by the user using the I^2C interface. This is done by placing the device in Standby mode using the Enable (EN) pin, making the required register changes, and then re-enabling the device, see Option Programming for the procedure.

Note: VOUT1 can be set to a value higher than the VIN Undervoltage Lockout (default 4.5V), which can result in repeated unsuccessful startup attempts until VIN1 is high enough to sustain VOUT1. In this case, Renesas recommends selecting a higher VIN UVLO threshold such as 6.5V or 7V, to ensure successful startup of VOUT1. See VIN Undervoltage Lockout. Also, the falling edge of VIN UVLO is a fixed 3.5V. As VIN1 drops, if VOUT1 falls to the Severe UV threshold, all outputs shut down and the RSTB indicator drives low, even if VIN1 is still above the lower VIN UVLO threshold.

Table 2. Output Voltage Options

Register 0x71	
Option Code (hex)	**Buck1 Output (V)**
00	3.60
01	2.80
02	2.85
03	2.90
04	2.95
05	3.00
06	3.05
07	3.10
08	3.15
09	3.20
0A	3.25
0B	3.30
0C	3.35
0D	3.40
0E	3.50
0F	3.60
10	3.70

Register 0x73	
Option Code (hex)	**Buck2 Output (V)**
00	1.80
01	0.85
02	0.90
03	0.95
04	1.00
05	1.05
06	1.10
07	1.15
08	1.20
09	1.25
0A	1.30
0B	1.35
0C	1.40
0D	1.45
0E	1.50
0F	1.55
10	1.60

Register 0x75	
Option Code (hex)	**Buck3 Output (V)**
00	1.20
01	0.85
02	0.90
03	0.95
04	1.00
05	1.05
06	1.10
07	1.15
08	1.20
09	1.25
0A	1.30
0B	1.35
0C	1.40
0D	1.45
0E	1.50
0F	1.55
10	1.60

Register 0x77	
Option Code (hex)	**LDO4 Output (V)**
00	3.30
01	2.70
02	2.75
03	2.80
04	2.85
05	2.90
06	2.95
07	3.00
08	3.10
09	3.20
0A	3.25
0B	3.30
0C	3.35
0D	3.40

Table 2. Output Voltage Options (Cont.)

Register 0x71	
Option Code (hex)	Buck1 Output (V)
11	3.80
12	5.00
13	5.05

Register 0x73	
Option Code (hex)	Buck2 Output (V)
11	1.65
12	1.70
13	1.75
14	1.80
15	1.85
16	1.90
17	1.95
18	2.00
19	2.05
1A	2.10
1B	2.20
1C	2.30
1D	2.40
1E	2.45
1F	2.50
20	2.55
21	2.80
22	3.30

Register 0x75	
Option Code (hex)	Buck3 Output (V)
11	1.65
12	1.70
13	1.75
14	1.80
15	1.85
16	1.90
17	1.95
18	2.00
19	2.05
1A	2.10
1B	2.20
1C	2.30
1D	2.40
1E	2.45
1F	2.50
20	2.55
21	2.80
22	3.30

Register 0x77	
Option Code (hex)	LDO4 Output (V)

5.3 Undervoltage and Overvoltage Protection Thresholds

The RAA271082 offers factory-programmable undervoltage (UV) and overvoltage (OV) threshold levels for Bucks1, 2, 3, and LDO4. Buck2 and Buck3 output voltages are sensed at the FB2 and FB3 pins respectively, while LDO4 is sensed at the LDOOUT4 pin. Buck1 UV and OV sensing uses the LDOIN4 input pin; Buck1 output regulation uses the FB1 input pin. This separation on Buck1 provides protection against cases where the feedback path is interrupted because of events such as an opened solder joint. See Tables 2A and 2B for UV and OV threshold options. **Note:** UV and OV thresholds for each output may be chosen independently.

An undervoltage fault is detected when a Buck or LDO4 output voltage falls below the preset threshold. The delay time for detection and response to undervoltage is typically 2µs, with options of additional delay of 10µs, 25µs, and 45µs. The same delay applies to all outputs. See Table 3 for the UV delay filter options. **Note:** Undervoltage detection is disabled until the soft-start cycle is complete and the RSTB pin drives high.

An overvoltage fault is detected when a Buck or LDO4 output voltage exceeds the preset threshold. The delay time for detection and response to overvoltage is typically 2µs.

For both undervoltage and overvoltage faults, there is an optional persistence filter of 30ms, see register 0x7C Bit 5. This filter delays RSTB response for 30ms from the onset of fault. When enabled, this 30ms delay applies to all outputs and to both undervoltage and overvoltage faults. However, if the fault also causes an output shutdown, RSTB drives low immediately and ignores the 30ms delay.

For the Bucks, detection of an overvoltage immediately tri-states the corresponding output switches.

UV and OV faults on Bucks 1, 2, and 3, and LDO4 set the corresponding fault register bits, see registers 0x80, 0x81, 0x82.

If a UV or OF fault occurs on one output, the other outputs continue to regulate normally. For protection on Buck1, there is also Severe UV and Severe OV detection, fixed at -20% and +20%, either of which cause immediate shutdown of Buck1 and the other outputs.

Table 3. Undervoltage Options for Bucks 1, 2, and 3, and LDO4

Option Code (hex)	Buck1 UV Threshold Register 0x72, Bits 0-3	Buck2 UV Threshold Register 0x74, Bits 0-3	Buck3 UV Threshold Register 0x76, Bits 0-3	LDO4 UV Threshold Register 0x78, Bits 0-3
0	-4%	-4%	-4%	-4%
1	-6%	-6%	-6%	-6%
2	-8%	-8%	-8%	-8%
3	-12%	-12%	-12%	-12%

Table 4. Overvoltage Options for Bucks 1, 2, and 3, and LDO4

Option Code (hex)	Buck1 OV Threshold Register 0x72, Bits 4-7	Buck2 OV Threshold Register 0x74, Bits 4-7	Buck3 OV Threshold Register 0x76, Bits 4-7	LDO4 OV Threshold Register 0x78, Bits 4-7
0	+4%	+4%	+4%	+4%
1	+6%	+6%	+6%	+6%
2	+8%	+8%	+8%	+8%
3	+12%	+12%	+12%	+12%

Table 5. Undervoltage Filter Delay Options (All Outputs)

Option Code (hex)	UV Filter Delay (µs) Register 0x7B, Bits 4-5[1]
0	0
1	+10
2	+25
3	+45

1. There is a fixed ~2µs delay in addition to the selected delay.

5.4 Protection Features

For enhanced protection the RAA271082 provides one reference for the output regulation of Bucks 1, 2, 3, and LDO4, and a separate reference for UV/OV fault detection. For Buck1, output UV/OV is sensed at the LDOIN4 input, whereas output regulation is sensed at the FB1. This separation prevents a single-point failure in the Buck1 feedback path from causing a severe overvoltage at the output of Buck1. **Note:** FB1, LDOIN4, and the output of Buck1 must all be tied together on the PCB.

The RAA271082 also provides continuous CRC checking of internal registers and can optionally apply CRC checking to I^2C communications.

5.5 Built-In Self Test (BIST) and CRC Recheck

The RAA271082 contains Built-in Self Test features for increased reliability. On power-up, the UV and OV comparators for VOUT1-4 are all BIST tested to detect stuck-low or stuck-high status. Any fault sets the bist_fail bit high (register 0x82, Bit 3) and all outputs are prevented from starting up.

Additionally, the device contains two separate voltage references to prevent single-point reference failures from causing severe overvoltage. The first reference (DAC1) is the reference for output regulation. The second reference (DAC2) is used by the OV and UV comparators. The device continually compares these two references. If these references drift apart more than 10%, a fault bit is set (0x83 Bit 6 or Bit 7) and the outputs latch off. If the references drift back to normal alignment, the fault bit remains set high until the bit is cleared using I^2C and the outputs remain off until the EN pin or the VIN supply is cycled.

To validate register data at power-up, the device performs a CRC recheck on all registers that are factory-programmable (that is registers containing fused bits). If the CRC recheck succeeds, initialization continues, and when complete, the outputs power up. This CRC recheck is repeated every 5ms thereafter. If register data gets corrupted, the fault is detected within 5ms; the crc_recheck_fault bit is set high (register 0x83 Bit 4) and all outputs shut down. The device continues to perform a CRC recheck every 5ms. The outputs remain off indefinitely while the CRC recheck fault exists. If the CRC recheck fault is removed, the device goes through a 200ms fault time-out, and then the outputs power up normally.

5.6 VIN Undervoltage Lockout

The VIN1 Undervoltage Lockout has four options for the rising edge threshold, see Table 6. The falling threshold for all options is fixed at 3.5V. **Note:** VIN1 must exceed the rising UVLO Threshold before the IC can power up. The default setting is code 0, which is 4.5V. **Note:** Although the device is capable of operating with VIN1 as low as 4V, the device cannot startup until VIN1 reaches 4.5V.

Table 6. VIN1 UVLO Options

Option Code (hex) Register 0x70	VIN1 UVLO Rising Threshold (V)	VIN1 UVLO Falling Threshold (V)
0	4.5	3.5
1	5.0	
2	6.5	
3	7.0	

5.7 Output Sequencing at Startup and Shutdown

The RAA271082 provides staggered startup and shutdown sequencing for the outputs. Startup and shutdown are initiated using the EN and EN_LV pins. If EN is driven high while EN_LV is held low, only Buck1 starts. If EN_LV is driven high after Buck1 has started, the low voltage outputs (Buck2, Buck3, LDO4) start up using the sequence and startup delay options described below.

Options for the startup delay and shutdown delay are shown in Table 7. At startup, the outputs are started in sequence, with the same startup delay between the different outputs. **Note:** The delay only controls the starting time of for each output, not the actual rise time of each output, which depends on the voltage setting and the internal soft-start ramp.

Table 7. Startup and Shutdown Delay Options

Option Code (hex) Register 0x79 Bits 0:2	Startup Delay Typical [ms]	Option Code (hex) Register 0x79 Bits 3:5	Shutdown Delay Typical [ms]
0	0	0	0
1	0.5	1	0.5
2	1	2	1
3	2	3	2
4	4	4	4

Table 7. Startup and Shutdown Delay Options (Cont.)

Option Code (hex) Register 0x79 Bits 0:2	Startup Delay Typical [ms]	Option Code (hex) Register 0x79 Bits 3:5	Shutdown Delay Typical [ms]
5	8	5	8
6	16	6	16
7	32	7	32

The shutdown delay time is also factory programmable and is independent of the startup delay time. Similar to the startup delay, all shutdown delays between outputs are identical. **Note:** The shutdown delay only controls the output disable timing, not the actual fall time of each output, which varies based on output capacitance and load. Outputs Buck2, Buck3, and LDO4 have internal pull-downs to actively discharge the output during shutdown. Each pull-down can be disabled or disabled through I^2C control factory programming using the MISC1_OPT register, Bits 1-3. The pull-downs are active for 200ms after the outputs are disabled, after which the pull-downs are disabled. **Note:** If V_{IN} falls below 3.5V during the pull-down interval, the device shuts down from VIN UVLO and the pull-downs do not complete the 200ms time-out.

The following are the two options for startup sequencing. Table 8 shows the register options for the startup sequence.

- Buck1 → Buck2 → Buck3→ LDO4
- Buck1 → LDO4 → Buck2 → Buck3

The shutdown sequence follows the reverse order of the startup sequence. **Note:** Buck1 always powers up before the low-voltage outputs, and always powers down after the low-voltage outputs.

Table 8. Startup and Shutdown Sequence Options

Option Code (hex) Register 0x79 Bit 7	Startup Sequence (EN high, EN_LV high)	Shutdown Sequence (EN low)
0	Buck1 -> Buck2 -> Buck3 -> LDO4	LDO4 -> Buck3 -> Buck2 -> Buck1
1	Buck1 -> LDO4 -> Buck2 -> Buck3	Buck3 -> Buck2 -> LDO4 -> Buck1

If the EN_LV falls while EN remains high, the low voltage outputs are shutdown in sequence while Buck1 remains enabled. If EN is driven low, the low voltage outputs are shutdown in sequence and then Buck1 shuts down.

If EN or EN_LV fall in the middle of a startup sequence, the startup is halted and shutdown sequencing begins from the current state. The startup sequence does not need to complete before the shutdown sequence proceeds when the EN or EN_LV signal falls. **Note:** Both EN and EN_LV have a 300µs delay before reacting to a falling edge.

When a shutdown sequence is started and completed, the outputs remain off for 200ms and the input that initiated the shutdown (EN and/or EN_LV input) is also ignored for 200ms. After the 200ms delay is completed the outputs can be restarted.

Figure 25 shows the startup and shutdown sequence timing (Option Code 0 for Sequencing).

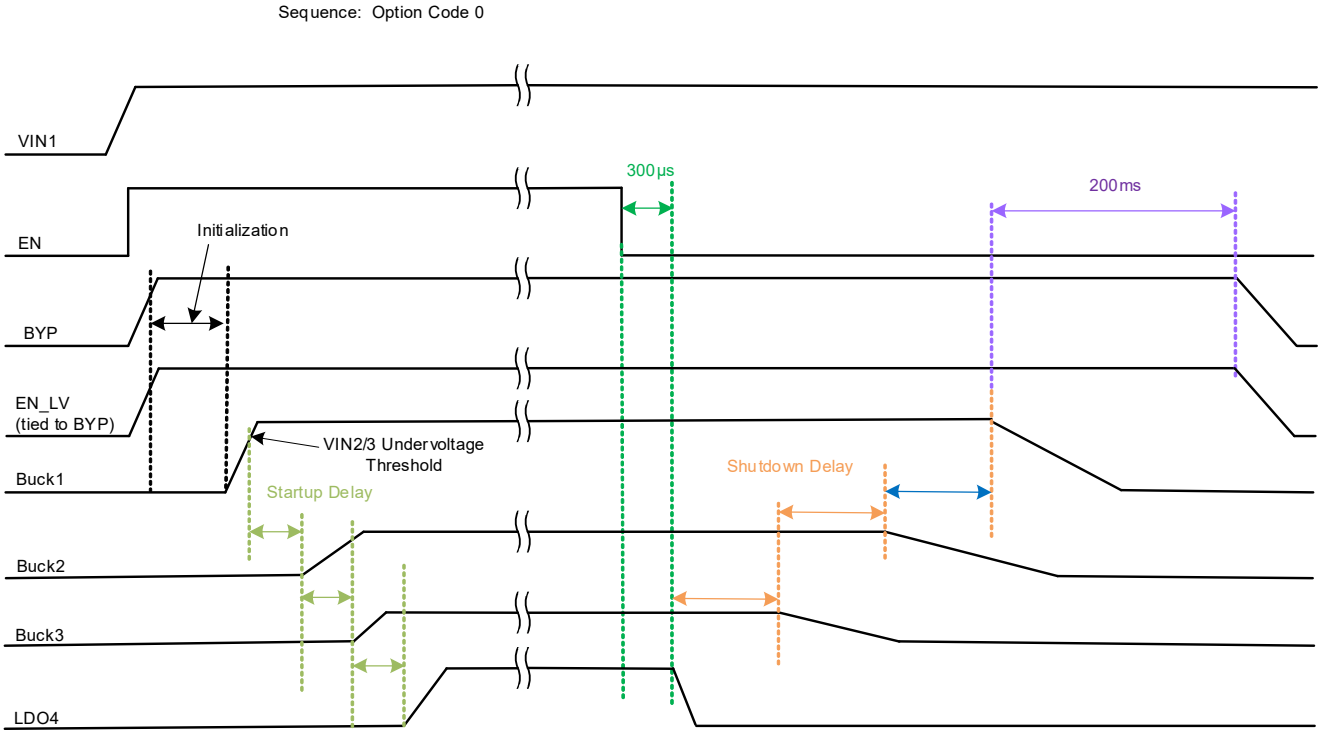


Figure 25. Sequence Timing Diagram

5.8 Output Soft-Start Ramp

Each output features a soft-start ramp during power-up. This ramp is factory-programmable but cannot be altered by the I^2C. VOUT1 and LDO4 have three independent soft-start options. Table 9 shows the soft-start ramp options for VOUT1 and LDO4.

VOUT2 and VOUT3 have three soft-start options but they share the same ramp option. **Note:** VOUT2 and VOUT3 have different ramp rates for VOUT2,3 ≤ 1.95V and VOUT2,3 > 2.0V. Table 10 shows the soft-start ramp options for VOUT2 and VOUT3.

Table 9. VOUT1 and LDO4 Soft-Start Ramp Options

Option Code	VOUT1 Soft-Start Ramp Rate (V/ms)	VOUT1 = 3.8V Soft-Start Ramp Time (ms) (from 0% to 95%)	LDO4 Soft-Start Ramp Rate (V/ms)	LDO4 = 3.3V Soft-Start Ramp Time (ms) (from 0% to 95%)
0	3.01	1.20	2.02	1.55
1	1.47	2.45	1.08	2.90
2	0.58	6.19	0.43	7.25

Table 10. VOUT2 and VOUT3 Soft-Start Ramp Options

	VOUT2, VOUT3 ≤ 1.95V		VOUT2, VOUT3 > 1.95V	
Option Code	VOUT2 Soft-Start Ramp Rate (V/ms)	VOUT2, VOUT3 = 1.8V Soft-Start Ramp Time (ms) (from 0% to 95%)	VOUT2 Soft-Start Ramp Rate (V/ms)	VOUT2, VOUT3 = 2.0V Soft-Start Ramp Time (ms) (from 0% to 95%)
0	1.43	1.2	2.71	2.71
1	0.72	2.36	1.37	1.37
2	0.29	5.91	0.72	0.72

The soft-start ramp times shown in Table 9 and Table 10 are for specific voltages as shown. If the required output voltage is a different value from the shown value, the ramp time scales linearly with the voltage. For VOUT2, the ramp rates are different depending on whether the output voltage is 2.0V or greater.

5.9 Output Pull-Downs

Buck2, Buck3, and LDO4 have pull-downs using pins FB2, FB3, and LDO4 to discharge their output capacitors when the output is shut off. These pull-downs can be disabled using register 0x7B, Bits 3:0. When an output is turned off, the pull-down is active for 200ms and then the pull-down is released.

Note: If V_{IN} falls below the V_{IN} UVLO falling edge threshold before 200ms has elapsed, the device shuts down and the pull-downs are disabled immediately before the 200ms time-out has completed.

5.10 I²C Programmability

Device parameters are programmable using the I²C interface. These options are provided to allow the user flexibility during system testing and integration. **Note:** When changing settings, the Electrical Specifications are maintained only for the original factory-programmed options.

To prevent parameter changes from adversely affecting normal operation, some I²C options can be programmed only while the device is in Standby. The following options are locked out during normal operation and cannot be changed when the device has begun switching: Output Voltage setting, UV and OV thresholds, Startup and Shutdown Delay and Sequencing, Spread Spectrum, Fault Response options, and Buck3 phase selection. See Registers 0x70 through 0x7B in the Register Map and Register Descriptions. To select these options, first set the EN pin to the Standby state, make the required selections, and then raise EN to the Buck1 ON state.

Registers with an address of 0x80 or higher are accessible and controllable during switching operation.

5.11 I²C and GPIO Bus Connection

Because of their silicon structure, the I²C pins (SCL, SDA) and the GPIO pin have intrinsic diode connections to the BYP supply. If the device is not powered (VIN1 not present or EN tied to GND), the BYP regulator is off and the BYP voltage is zero. The diodes on the pins tend to pull the SCL, SDA, and GPIO signals low, affecting any other devices on the bus. To prevent this, one solution is to derive the pull-up voltage from one of the RAA271082 outputs, ensuring that the BYP voltage is always present before the bus pull-up voltage is used.

5.12 CRC Fault Detection on Registers and I²C Transactions

The RAA271082 continuously verifies register contents through CRC (Cyclic Redundancy Check) fault detection, at 5ms intervals. CRC fault detection cannot be disabled. For CRC fault detection the device performs the following steps:

1. Read all registers and calculate a 9-bit CRC_result.
2. Compare the CRC_result value to the trim_CRC value stored in registers 0x7E and 0x7F.
   a. The trim_CRC value is programmed at the factory but can be overwritten.
3. Write the 9-bit CRC_result value to registers 0xB6 (Bit 7) and 0xB7.
4. If the CRC_result and trim_CRC values are not identical, a CRC fault is detected which causes:
   a. Immediate shut down of all outputs.
   b. RSTB asserts low indicating a fault condition.
   c. The CRC fault status bit is flagged (register 0x83, Bit 4)
   d. All outputs are latched off, regardless of whether a hiccup/restart option has been selected.
   e. The device remains off until a full power-on reset occurs by either cycling the EN pin or decreasing the VIN1 supply until the BYP voltage falls below the Power-On Reset Threshold.

The RAA271082 has the option to perform CRC fault detection on I²C communications. To enable I²C CRC fault detection, set Bit 4 of register 0x7C to 1. When enabled, the device performs CRC fault detection on every I²C transaction. A detected I²C CRC fault does not affect IC operation but flags the I²C CRC fault status bit (register 0x83, Bit 5). The I²C CRC fault indication can also be routed to the GPIO pin by setting Bit 7 of register 0x83 to 1.

Note: If one of the factory-programmed options is changed, the change in register contents causes a CRC fault within 5ms, resulting in all outputs shutting down. The outputs remain off until one of the following occurs: the CRC fault is corrected, the EN pin is cycled low then high, or the VIN supply is removed and restored. **Note:** If the CRC fault is corrected, there is a 200ms delay before the outputs power on.

5.13 Option Programming

All RAA271082 options are selected by changing register contents, which causes a CRC fault for factory-programmed devices. The following steps prevent a CRC fault and allow options to be selected as required.

Note: If the device is shut down and restarted using the EN input, the device begins a new power-up cycle and reverts to the original factory settings for all options and registers. All previous changes made through the I²C interface are removed. The same occurs if the device shuts down and restarts because of VIN1 undervoltage, power-on reset (BYP undervoltage), or over-temperature.

1. Set the device in Standby mode (EN = 1.2V)
   a. All outputs are turned off but I²C transactions are enabled.
2. Select required options by writing values into the designated registers.
3. Write 0 to trim_CRC registers 0x7D (Bit 7 only) and register 0x7E.
4. Wait 10ms. The device calculates a new CRC_result based on current register contents and:
   a. Compares the CRC_result value to the trim_CRC values which are set to zero.
   b. Detects a CRC fault (CRC_result does not match trim_CRC).
   c. Sets the CRC_fault bit high in register 0x83, Bit 4.
   d. Writes the CRC_result value to the CRC_result registers 0xB6 (Bit 7 only) and 0xB7.
      i. The CRC_result registers now contain the value needed to prevent a CRC fault.
   e. Read the new CRC_result from registers 0xB6 (Bit 7 only) and 0xB7.
   f. Write the CRC_result value into trim_CRC registers 0x7D (Bit 7 only) and register 0x7E.

g. Clear the CRC fault flag by writing 0 to register 0x83, Bit 4.

h. Wait 10ms. The device calculates a new CRC_result based on current register contents.

i. Verify that a CRC fault has not been detected, the CRC_fault flag bit (register 0x83 Bit 4) should remain 0.

   i. If the CRC_fault flag is non-zero, return to step 3 and repeat until the CRC_fault flag reads 0.

j. Re-enable the outputs (EN = 1.84V). The device starts up with the selected options.

5.14 EN Input

EN is a high-voltage input that can tolerate voltages up to 42V DC. The EN input can be in one of 3 states as shown.

- **Shutdown state:** EN is logic low (EN at ground). The device is fully shut down and current draws from VIN1 is typically 1µA.
- **Standby state:** When EN is set to 1.2V (typical) the device enters the Standby state. If this is an initial power up, the BYP regulator ramps to provide bias for the device. When the BYP pin exceeds the Power-On Reset threshold (3.6V), the device performs initialization and Built-in Self Test (BIST). After BIST is successfully completed, if the EN pin remains at 1.2V, the device remains in Standby and all switching is disabled. In the Standby state it is possible to change the various options for output voltage, UV and OV thresholds, and other parameters. On initial power-up, the time required to complete initialization and BIST is approximately 1ms.
- **Buck1 On state:** When EN exceeds 1.8V (typical) and the BYP voltage is above the Power-On Reset threshold, the device begins the Startup cycle for Buck1. If the EN_LV input is logic low, Buck1 powers up and remains on while the low-voltage outputs (Buck2/3, LDO4) are off. If EN_LV is logic high and VIN2/3 is above the VIN2/3 Undervoltage Threshold (2.42V typical), the device begins startup for Buck2/3 and LDO4, using the startup sequence and delay options selected as in Table 7 and Table 8.

Note: It is not required to use the Standby state during operation. If the EN input is switched from ground (Shutdown) to the Buck1 On state, the device initially goes through the same steps as in the Standby State. When initialization and BIST are completed, typically 1ms, the device powers up the outputs according to the EN and EN_LV inputs.

Falling edges on EN are filtered to prevent spurious shutdowns. When the EN input moves from a higher threshold to a lower threshold, the EN signal must remain at the lower threshold for 300µs before the device responds. Falling edges on EN are handled differently depending on the threshold (state) and the state of the EN_LV pin.

- **EN falling edge, from Buck1 ON state to Standby state:** After the EN pin falls to the Standby state threshold for 300µs, the device shuts down Buck1/2/3/LDO4, using the shutdown sequence and delay options selected. If the low-voltage outputs (Buck2/3/LDO4) are already off because of EN_LV at logic low, the Buck1 regulator shuts down after the shutdown delay has elapsed. In both cases, when Buck1 has shut down, the EN input is ignored for 200ms and all outputs remain off.
- **EN falling edge, from Buck1 ON state to Shutdown state:** After the EN pin falls to the Shutdown threshold for 300µs, the device shuts down all outputs in the same sequence as described in the previous case (Buck1 ON state to Standby state). After Buck1 has shut down, if V_{IN} remains above the V_{IN} UVLO threshold (3.5V typical), the BYP regulator remains on for 200ms and the EN input is ignored during this time. After 200ms, if the EN pin remains low (Shutdown state), the BYP regulator and all internal circuits shut off, and the device goes into full shutdown with input (VIN1) current typically 1µA. If V_{IN} falls below the V_{IN} UVLO threshold before the 200ms time-out is completed, the 200ms timer is stopped and BYP turns off immediately.

Note: Many of the I^2C-programmable options cannot be changed when EN1 is above 1.8V (Buck1 ON); I^2C commands for these options must be performed while the device is in Standby with the BYP LDO enabled and all outputs off.

5.15 EN_LV Input

EN_LV is a logic level input that controls the low-voltage outputs (Buck2/3/LDO4). When EN_LV is set to logic high, the low-voltage outputs start up using the sequence and startup delay selected, if the EN input is in the Buck1 ON state and the VIN2/3 input is above its Undervoltage Lock-out threshold of 2.42V. If the EN input is in the Standby or Shutdown state, Buck1 is shut down and the low-voltage outputs do not start.

To prevent spurious shutdowns, falling edges on EN_LV must be low for 300µs before the device responds. After EN_LV is at logic low for 300µs, the low-voltage outputs shut down using the sequence and shutdown delay is selected. After the last output is shut off, the EN_LV pin is ignored for 200ms and the outputs remain off.

Table 11 summarizes the behavior associated with the EN and EN_LV pins.

Table 11. EN and EN_LV Control

EN State	EN voltage	EN_LV state	BYP LDO	Buck1	Buck2/3/LDO4
Shutdown	VEN ≤ 0.4V	Logic high or low	Off	Off	Off
Standby	VEN = 1.5V	Logic high or low	On	Off	Off
Buck1 On	VEN ≥ 1.8V	Logic low	On	On	Off
Buck1 On	VEN ≥ 1.8V	Logic high	On	On	On

5.16 Buck1

The primary synchronous buck regulator, Buck1, has a minimum start up voltage of 4.5V. When started, the operating input range is 4V to 42V, with a programmable output voltage range from 2.8V to 5.05V. Output voltage is connected to the FB1 pin for voltage feedback sensing. Column 2 of Table 2 details the available output voltage settings. Buck1 is an internally-compensated PWM current mode converter that always operates in forced continuous current mode (FCCM). It shares a fixed 2.2MHz switching frequency with Buck2 and Buck3. The regulator's output voltage is sense at the FB1 pin, which incorporates an internal resistive voltage divider.

Reliability features for this converter include glitch-filtered undervoltage and overvoltage threshold (see Undervoltage and Overvoltage Protection Thresholds), tri-stating switches on OV, cycle-by-cycle overcurrent protection (two-levels), cycle-by-cycle negative current limiting, and Hiccup mode protection. UV and OV fault sensing on Buck1 is done using the LDOIN4 input pin.

The Buck1 component selection and configuration bit settings are summarized in Table 12.

Table 12. CFG1 Buck1 Configurations

CFG1 Connection	VOUT1 (V)	Lout1 (µH)	Cout1 Minimum (µF)
Float	2.8V to 5.05V	4.7	10µF

5.17 Buck2 and Buck3

The secondary buck regulators Buck2 and Buck3 have a factory-programmable output voltage range from 0.85V to 3.3V. Table 2 lists the available output voltage settings. Both are internally-compensated PWM current mode converters that operate in forced continuous current mode (FCCM). They share a fixed 2.2MHz switching frequency with Buck1. Buck2 is clocked in-phase with Buck1, while Buck3 can be programmed for either in-phase or 180°out of phase with Buck1. The output voltages of Buck2 and Buck3 are sensed at the FB2 and FB3 pins respectively; both incorporate internal resistive voltage dividers. Protection features for both Buck2 and Buck3 include undervoltage and overvoltage thresholds (see Undervoltage and Overvoltage Protection Thresholds), tri-stating switches on OV, cycle-by-cycle overcurrent protection, cycle-by-cycle negative current limiting, and Hiccup mode protection.

5.18 LDO4

The LDO4 linear regulator has a programmable output voltage range from 2.7V to 3.4V. Table 2 shows the available output voltage settings. The LDO4 input (LDOIN4) must be connected to the Buck1 output. The LDOIN4 input also functions as the Undervoltage and Overvoltage sense point for Buck1. LDO4 can provide up to 300mA. Reliability features for this linear regulator include undervoltage and overvoltage thresholds (see Undervoltage and Overvoltage Protection Thresholds) and overcurrent limiting. LDO4 typically does not shut down during overcurrent; if shutdown and attempt to restart (hiccup) is required, this can be factory-programmed or selected using I^2C using register 0x87, Bit 2.

5.19 Oscillator and Spread Spectrum

The three buck regulators share a fixed 2.2MHz oscillator. The phase shift between Buck1 and Buck2 is zero degrees. The phase shift between Buck1 and Buck3 can be programmed to either zero or 180 degrees.
The device has seven algorithm options for spread spectrum operation as shown in Table 13. The options are selected using register 0x7A, Bits 2:0. When spread spectrum is enabled, the clock selects one of 32 different frequencies, with a maximum variation of approximately ±4% centered at 2.2MHz. The frequency selection can be pseudo-random or can follow a specific modulation.

Table 13. Spread Spectrum Options

Option Code (hex) Register 0x7A Bits 2:0	Frequency Modulation	Dwell Cycles
0	Off	Off
1	9.13kHz 2-slope	3 or 6 cycle
2	pseudo-random	pseudo-random 1 to 8 cycles
3	pseudo-random	pseudo-random 4 to 32, 4-cycle increments
4	8.85kHz triangular	4
5	pseudo-random	4
6	pseudo-random	8
7	pseudo-random	24

5.20 RSTB

The RSTB output is an active-high/active-low fault indicator which can be activated by various faults. Under normal operation, the RSTB output is high; a fault condition is indicated when the RSTB output is connected to ground. Table 14 lists the fault conditions which can trigger a RSTB fault indication, along with the default (yes/no) setting for each fault. Each fault can be factory-programmed or programmed using I^2C to have the RSTB output either assert or ignore a fault condition. Control of faults, which can trigger the RSTB output is in registers 0x7D Bits 1:0, and register 0x8D.

Table 14. RSTB Fault Indications and Default Settings

Fault	Default enabled	Note
Buck1 Over/Undervoltage	Yes	cannot be disabled
Buck2 Over/Undervoltage	Yes	can be disabled
Buck3 Over/Undervoltage	Yes	
LDO4 Over/Undervoltage	Yes	
Sequence Fault	No	can be enabled

Table 14. RSTB Fault Indications and Default Settings (Cont.)

Fault	Default enabled	Note
Watchdog Timer Too slow	no	can be enabled
Watchdog Timer Too fast	no	
Watchdog Timer Restart	no	
CRC (internal registers)	Yes	cannot be disabled
Over-temperature	Yes	cannot be disabled

Note: If an Over-temperature fault or a CRC error-checking fault occurs, the RSTB pin is asserted low and the outputs are immediately shut down. These faults cannot be disabled and their fault responses cannot be disabled.

When the RSTB output is high, the RSTB pin is connected internally to the BYP voltage, typically 4.3V. Circuits or logic signals connected to RSTB must be capable of withstanding 4.3V. Alternatively, a resistor divider can be placed on the RSTB output to reduce the voltage seen at the receiver end. Because RSTB is high during normal operation, the resistor divider dissipates a small amount of power.

Note: The RAA271082 detects and responds to a fault even if RSTB notification for that fault is disabled.

RSTB Block Diargram is shown in Figure 26.

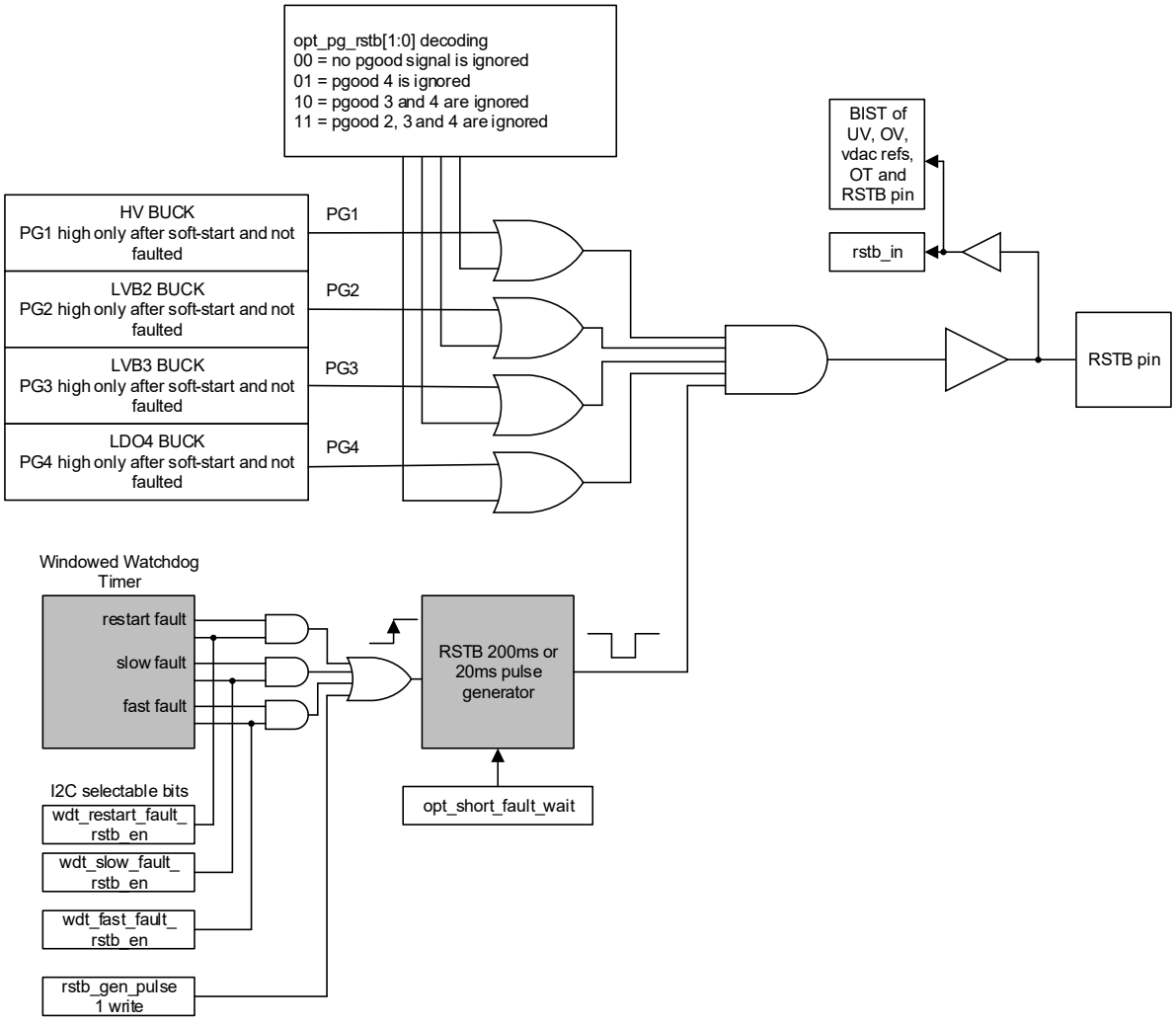


Figure 26. RSTB Block Diagram

5.21 GPIO

The RAA271082 provides a configurable open-drain general purpose I/O (GPIO) pin. A pull-up voltage and pull-up resistor are required if the GPIO pin connects to a logic device. On power-up, the GPIO pin is asserted high (open drain) during device initialization, and then asserts low when the device has successfully completed initialization and switching can begin. The GPIO functions can factory-programmed or programmed using I^2C to perform one of the following functions, refer to register 0xA4 in the Register Descriptions.

- GPIO is high (open drain) during initialization and then drives low when all register operations are finished and initialization is completed). This is the default state of the device, register 0xA4 Bits 2:0 set to 0,0,0.
- General fault indicator. The pin can be programmed to show fault status for any selection of bits in the FLT_GPIO_EN registers (Registers 0x8A, 0x8B, and 0x8C). This requires register 0xA4 Bits 2:0 set to 0,0,1. The selected fault bits are OR'd, a fault on any selected bit triggers a GPIO fault indication. The registers may be polled using I^2C to determine which faults have occurred.
- GPIO is a logic output which reflects the bit value in register 0xA4 Bit 4. This requires register 0xA4 Bits 2:0 set to 1,1,0.
- Clock output. The 2.2MHz internal clock can be sent to the GPIO pin. The GPIO clock signal is in phase with the Buck1 clock. This requires register 0xA4 Bits 2:0 set to 0,1,1.
- General input. The GPIO output drive can be disabled to configure the pin as an input kick to the Windowed Watchdog Timer, or for sampling the pin using register 0xA4. Configuring the GPIO pin as an input requires register 0xA4 Bits 2:0 set to 1,0,0. Bit 7 of the register then reflects the input logic state of the pin.

Note: The GPIO pin has an intrinsic diode connected from the GPIO pin to the BYP supply. See I^2C and GPIO Bus Connections for more information.

Table 15 shows the GPIO default settings for fault indication. **Note:** Register 0xA4 must first be written with value 0x04 to configure GPIO as a fault indicator.

Table 15. GPIO Fault Indicator Default Settings

Fault		Default enabled?
Undervoltage (UV)	Buck1	No
	Buck2	No
	Buck3	No
	LDO4	No
Overvoltage (OV)	Buck1	No
	Buck2	No
	Buck3	No
	LDO4	No
Overcurrent (OC)	Buck1	No
	Buck2	No
	Buck3	No
	LDO4	No
Negative Overcurrent (NOC)	Buck1	No
	Buck2	No
	Buck3	No
Overcurrent2 (OC2)	Buck1	No
Severe Undervoltage (Sev UV)	Buck1	Yes

Table 15. GPIO Fault Indicator Default Settings (Cont.)

Fault		Default enabled?
Severe Overvoltage (Sev OV)	Buck1	Yes
Sequence Fault		No
Watchdog Too Fast Fault		No
Watchdog Too Slow Fault		No
Watchdog Restart Fault		No
CRC Recheck Fault		No
I^2C CRC Fault		No
Over-Temperature		No

The GPIO block diagram is shown in Figure 27.

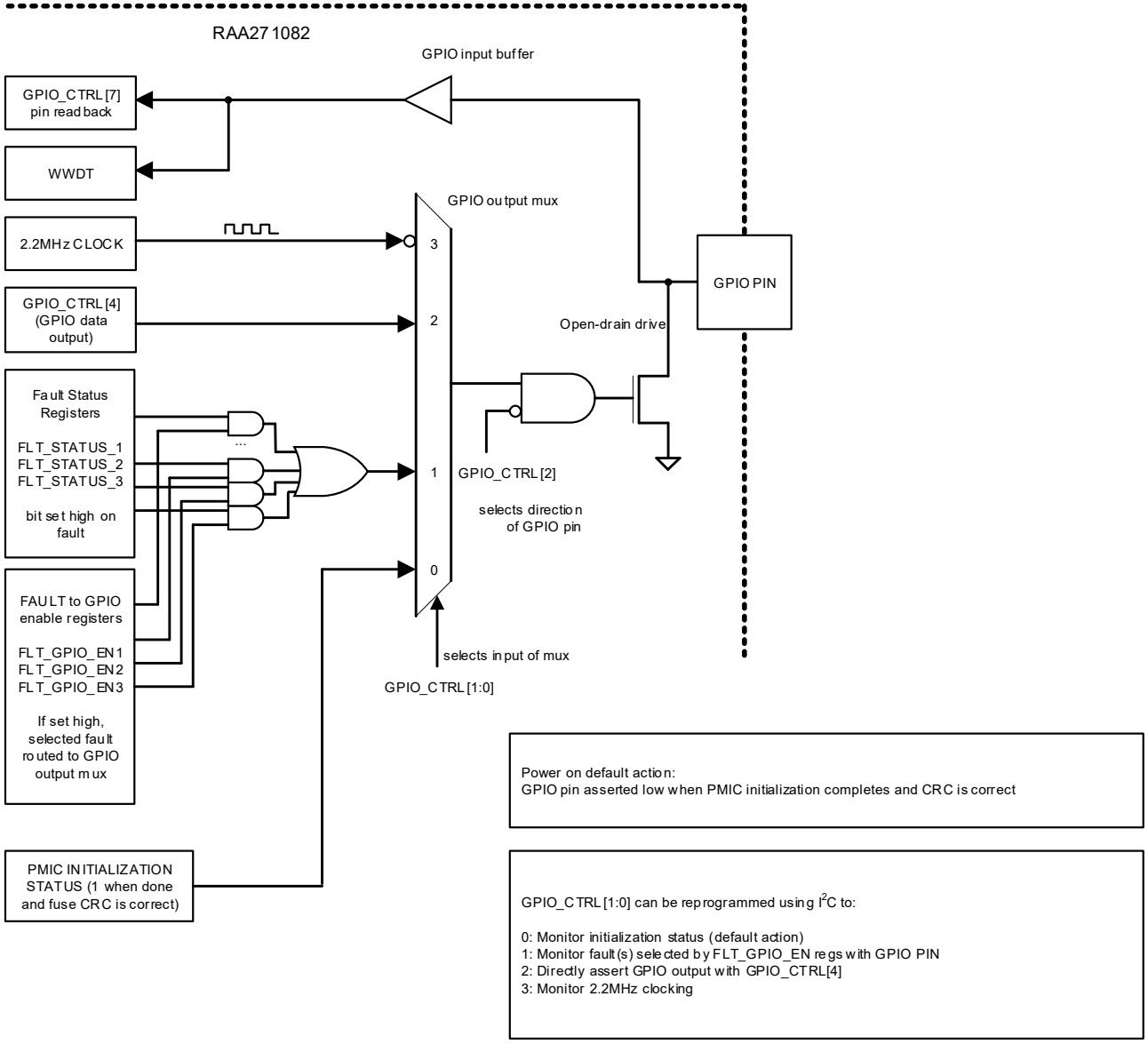


Figure 27. GPIO Block Diagram

5.22 Windowed Watchdog Timer

The RAA271082 provides a Windowed Watchdog Timer (WWDT) to aid in detection and warning of system faults. The WWDT timing and response can be factory-programmed or configured using I²C (RAA271082) to as explained below.

The input (kick) signal to the WWDT is always available using I²C, by periodically writing the correct kick value (hex 2A) into the KICK_REG register 0xA4. Additionally, the GPIO pin can be used as the WWDT input (kick), as set by the kick_select bits in register WWDT_CFG 0xA0. **Note:** If the GPIO input provides the WWDT kick signal, the GPIO must be configured as an input and cannot be used as a fault indicator. To configure the GPIO input as the WWDT kick, write register 0xA4 with value 0x04.

The WWDT provides programmability for both the upper limit (too slow) and lower limit (too fast) time periods which trigger a WWDT fault. The upper and lower limits are programmed through the registers WWDT_ULW (too slow, 0xA1) and WWDT_LLW (too fast, 0xA2). The WWDT can also be configured to trigger a fault on a restart fault, which is a too slow fault which triggers at twice the timing period defined by the upper limit (too slow) register 0xA1.

Figure 28 shows the WWDT configured to use the GPIO input as the input (kick) signal.

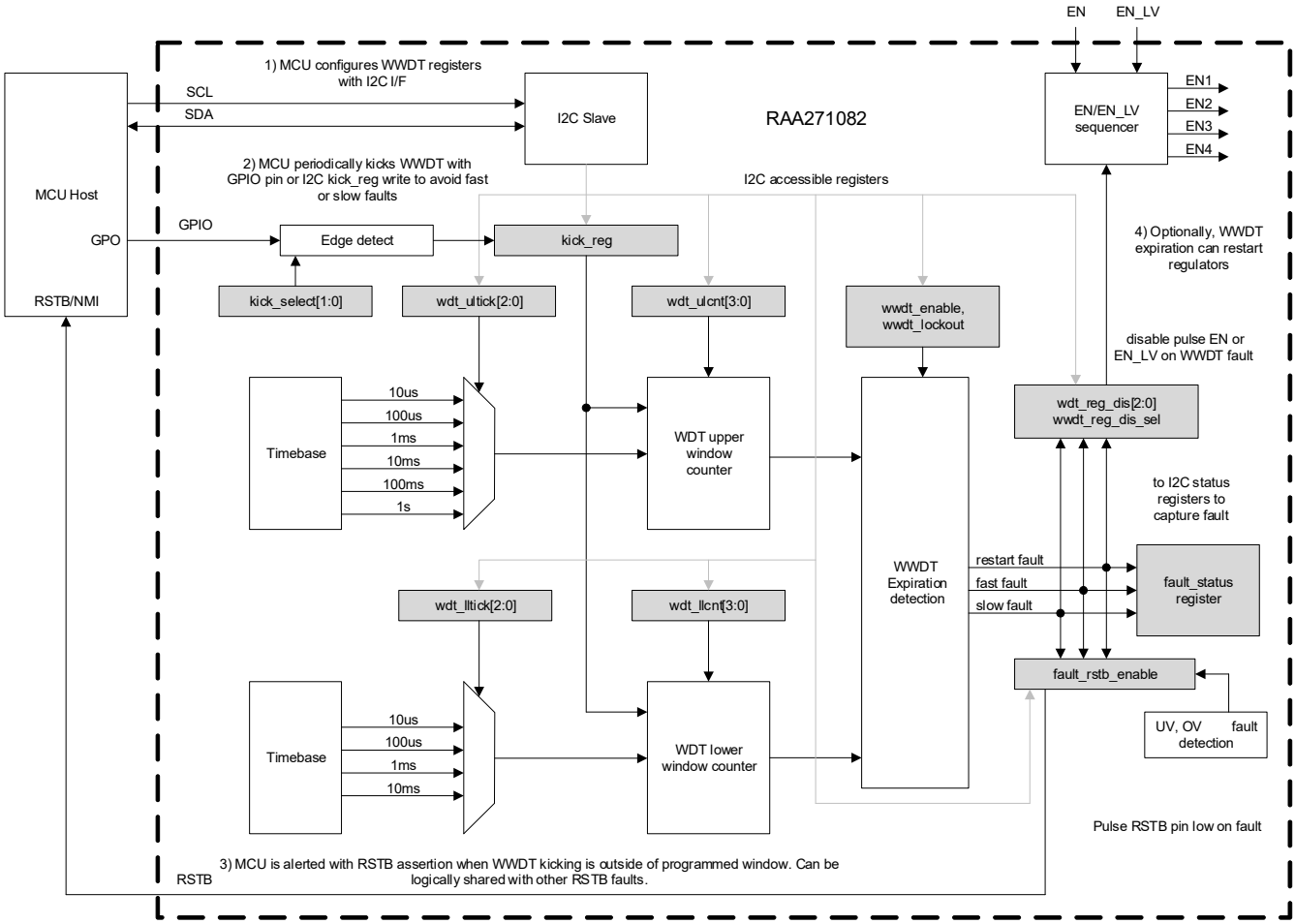


Figure 28. WWDT Operation using GPIO as WWDT Input

Figure 29 shows the WWDT configured to use only the kick register (0xA3) through the I²C interface as the WWDT input (kick) signal. This allows the GPIO pin to be used for other system functions.

Note: Loading a non-zero value into either the upper or lower window counter enables the WWDT fault detection. If the kick timing is outside the limits set by the window counter, a fault bit is set high in register 0x83. Renesas recommends keeping the window counter value at zero until all other WWDT options have been enabled, and then load the non-zero value into the counter.

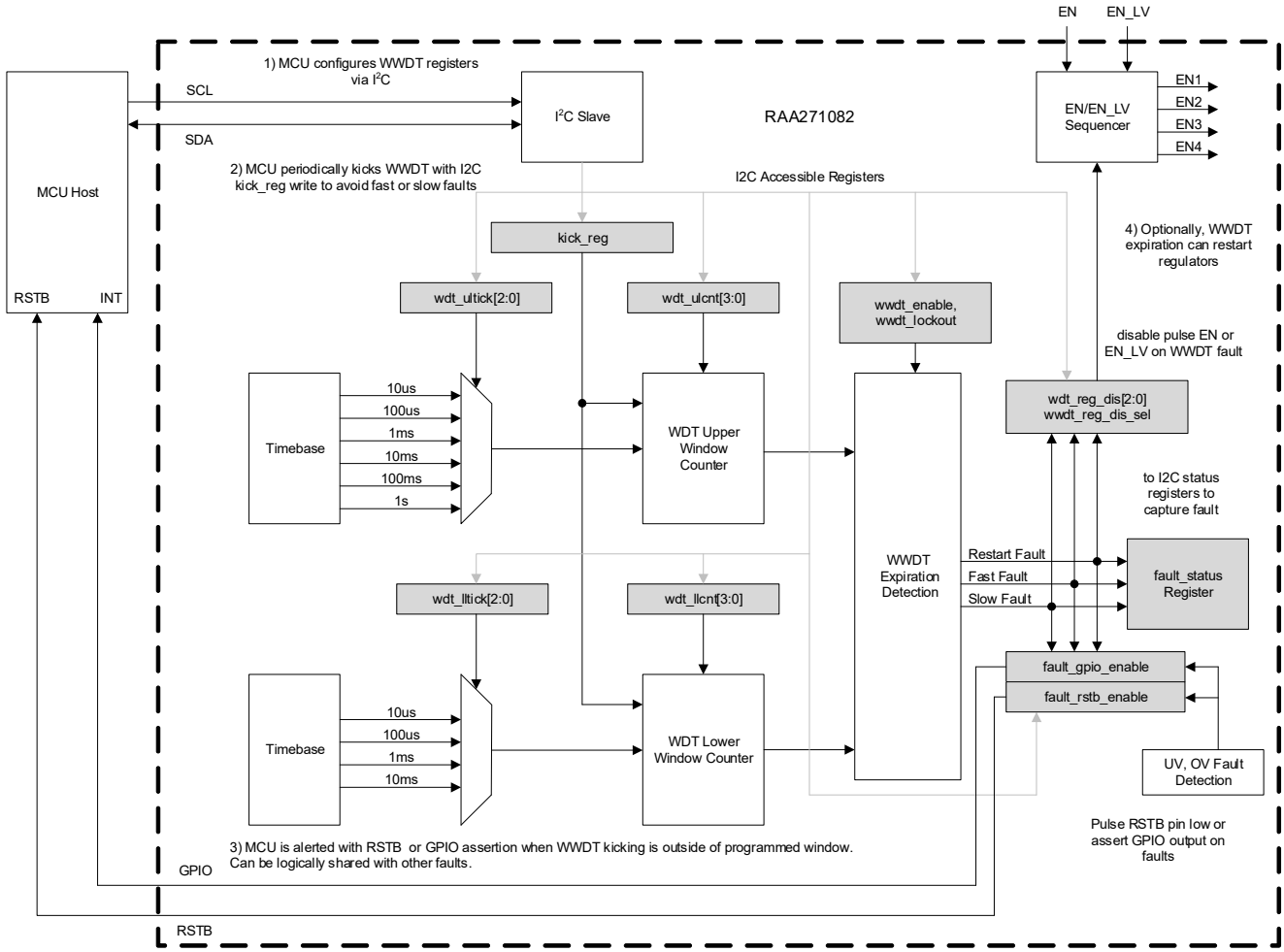


Figure 29. WWDT Operation using the Kick Register as WWDT Input

The following steps explain how to program the watchdog timer. **Note:** The WWDT cannot be factory-programmed and must be programmed using I2C each time the device powers up.

1. At power-up, GPIO drives low during initialization.
2. When initialization is done, GPIO remains low and the outputs start switching. It is possible to write to the WWDT registers at this point, but RSTB remains low until after the outputs are in regulation.
3. RSTB drives high about 5ms after all outputs are in regulation.
4. Before programming any WWDT parameters, set Bit 7 of register 0x0A to zero: this disables the WWDT until all parameters are set.
5. Select the kick to use for the WWDT. The kick can be supplied through the GPIO pin or using periodic I2C register writes.
   a. Bits 1:0 of register 0xA0 determine the kick selection:
   b. Bits 1,0 = 0,0: this selects GPIO pin as kick, on falling edge. It also allows kicks using the I2C kick register.
   c. Bits 1,0 = 0,1: this selects GPIO pin as kick, on rising edge. It also allows kicks using the I2C kick register.
   d. Bits 1,0 = 1,0: identical to Bits 1:0 = 0,1.

e. Bits 1,0 = 1,1: selects I^2C kick register and the GPIO pin is ignored.

f. To kick the WWDT using I^2C kick register, write value 0x2A to register 0xA3.

g. If GPIO is to be used as an I^2C kick input, the GPIO pin must be configured as an input. On power-up, the pin is high while the device initializes. After initialization the pin drives low, switching begins, and the GPIO pin can be configured as an input. To configure the pin as an input, write value 0x04 to register 0xA4.
Note: When the register write occurs, GPIO reads high because it is now an input and cannot actively pull the pin low.

6. Select the WWDT timing parameters. Note, all these WWDT registers are set to value 0x00 at power-up.
   a. Too-fast setting: write to register 0xA2 (WWDT_LLW - 0xA2). Bits 3:0 set the tick count. Bits 6:4 set the timebase per tick.
   b. Too-slow setting: write to register 0xA1 (WWDT_ULW - 0xA1). Bits 3:0 set the tick count. Bits 6:4 set the timebase per tick.
   c. Restart setting: the restart timing is twice the too-slow period. Example: if the too-slow setting is 10ms, restart is 20ms.
7. Select which WWDT faults create a shutdown, using register WWDT_CFG - 0xA0 Bits 6:4.
   Each shutdown below can be enabled or disabled separately.
   a. Bit 6 = 1: Enables shutdown on restart fault.
   b. Bit 5 = 1: Enables shutdown on too-slow fault.
   c. Bit 4 = 1: Enables shutdown on too-fast fault
   d. Set each bit to 1 to create a fault. Each fault can be disabled or enabled independently.
8. Select which outputs to shut down upon WWDT fault, using register WWDT_CFG - 0xA0 Bit 3.
   a. Bit 3 = 0: causes all outputs to shut down.
   b. Bit 3 = 1: shuts down only the LV outputs while VOUT1 remains on.
9. Select whether the WWDT timing specs are locked out when the WWDT is enabled, using WWDT_CFG - 0xA0 Bit 2.
   a. Bit 2 = 0: WWDT parameters can be altered at any time.
   b. Bit 2 = 1: WWDT parameters are locked and cannot be changed unless the IC is reset by EN or VIN recycling.
10. Enable the WWDT by changing WWDT_CFG - 0xA0 Bit 7 from 0 to 1. The WWDT does not activate until the first kick is received.

When the WWDT is enabled, the WWDT detects WWDT faults and responds according to the options selected. If one or more WWDT faults are configured to cause output shutdown, the outputs shutdown and try to restart according to the hiccup/latch-off selection.

6. Layout Guidelines

As with all switching regulators, the Printed Circuit Board (PCB) layout requires careful attention to achieve good performance. Proper PCB layout as detailed below minimizes the effects of voltage and current spikes present in fast-switching MOSFET circuits.

- The PCB should have a minimum of four copper layers. Use a full ground plane in the internal layer directly below the top layer. For all components that connect to ground, make sure that each component has one or more vias nearby, to provide a low-impedance path to the ground plane.
- VIN1 input capacitance: Place the input filter capacitor (CIN1) between VIN1 and PGND, as close to the IC pins as possible. Place the high-frequency decoupling capacitor closest to the IC. The loop formed by the input capacitors, VIN1, and PGND must be small to minimize high frequency noise. The copper traces between the capacitors and the IC should be as short and direct as possible.

- Place the Buck1 inductor L1 near the PHASE1 pin of the IC and connect directly to the pin with short, wide copper.
- Place the boot capacitor (CBOOT) next to Pins 5 and 6 and use short, direct copper connections.
- Place the VIN2/3 input capacitor (CIN2/3) near the VIN2/3 pin of the IC. Place the high-frequency decoupling capacitor closest to the IC. Connect the capacitors to the VIN2/3 pin using short, wide copper. Place multiple ground vias at the ground connection of each capacitor, to provide a low-impedance ground path to the ground of the IC (PGND2/3, pin 22).
- Place Buck2 and Buck3 inductors (L2 and L3) next to their respective pins, PHASE2 and PHASE3. Route to the inductors using short, wide copper.
- Place the Buck2 and Buck3 output capacitors (COUT2 and COUT3) near the inductor and connect using short, wide traces. Use multiple vias and copper on other layers if needed to connect from COUT2 or COUT3 to their load circuit.
- Place multiple ground vias at the ground connection of COUT2 and COUT3, to provide a low-impedance ground path to the Buck2/3 ground return at the IC (PGND2/3, pin 22).
- Route the feedback for Buck3 directly from COUT3 to the FB3 pin (Pin 21), as seen in the layout in light blue color. Provide some space clearance between the FB3 trace (which is noise-sensitive) and the high-noise PHASE3 trace.
- Route the feedback for Buck2 on an inner layer, connecting from COUT2 to FB2 (Pin 22). FB2 is a noise-sensitive input. Route the trace so that it avoids passing underneath the inductors L2, L3, or L1, and also avoids passing underneath under the PHASE signals or pins. Renesas recommends routing the trace on an inner layer, going around COUT3, and then routing to Pin 22. VOUT2 (Buck2 output) and the FB2 pin are shown in yellow in Figure 30.
- LDOIN4 and FB1 (Pins 18 and 17) must be connected to VOUT1, which is the output of Buck1 and is connected to the VIN2/3 pin (Pin 1). Use wide copper to route from VOUT1 to LDOIN4. The LDOIN4 pin is the input for the LDOOUT4 output, which dictates that the LDOIN4 trace must carry all the LDO load current. When routing the connection from VOUT1 to LDOIN4, avoid routing underneath any of the inductors and also any PHASE nodes. Renesas recommends using inner layer copper, connecting from VOUT1 to LDOIN4 (all shown in white), routing directly underneath the IC, while avoiding the PHASE and BOOT pins of the IC (Pins 5, 6, 23, 24). Note: The LDOIN4 pin also functions as the overvoltage and undervoltage sense point for Buck1. To minimize I•R voltage drop because of copper resistance, use a wide trace to route to LDOIN4.
- FB1 (Pin 17) is the feedback input for Buck1. This pin ultimately connects to the same net as LDOIN4. It is possible to combine the path for FB1 and LDOIN4 into a single trace, however the trace needs to be wide to minimize I•R voltage drop because of the LDOIN4 loading. Alternatively, a separate trace on an inner layer can route from the VOUT1 output to the FB1 pin. Route this trace away from all high-noise nodes and components, including the inductors, capacitors CIN1 and CIN2/3, and the PHASE and BOOT nodes.
- Place input and output capacitors for the LDO (100nF and CLDOOUT4) near the IC and routed directly with short wide traces. Place multiple ground vias at the ground connection of the capacitors to provide a low-impedance ground path to the ground return at the IC.
- Connect all the grounds pins (Pins 10, 11, and 22) and the thermal PAD (Pin 25) together using a single wide copper pad under the IC. Connect this copper pad to the ground plane using multiple vias, to provide a low-impedance path to the ground plane and also to provide heatsinking through the PCB copper.
- Place the BYP capacitor (CBYP) near the BYP pin (Pin 12). Route to the capacitor using a short, wide PCB trace, for both the BYP and the ground paths. If needed, place multiple ground vias at the ground connection of CBYP, to provide a low-impedance ground path to the ground of the IC (PGND2/3, Pin 22).

An example PCB layout is shown in Figure 30.

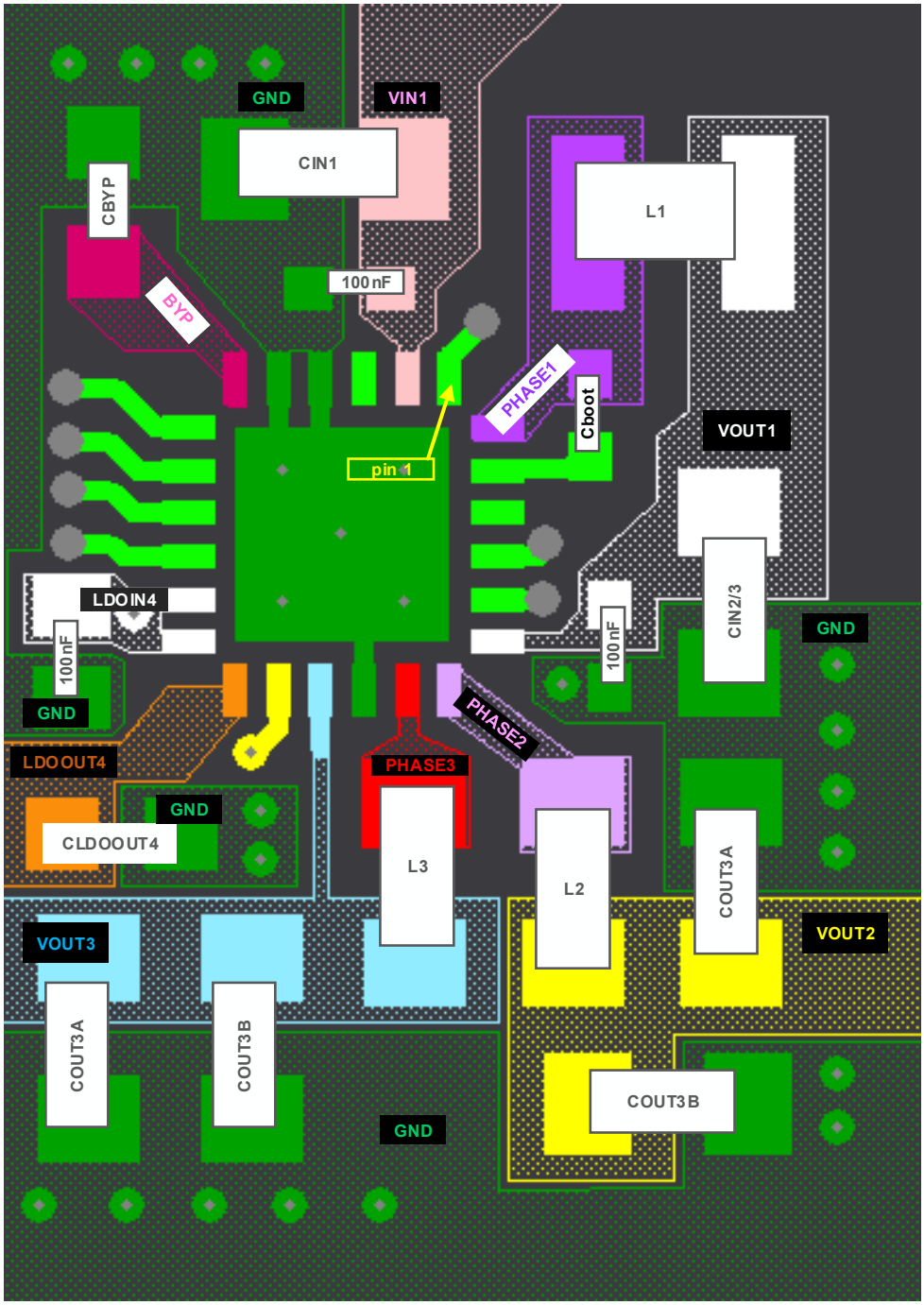


Figure 30. PCB Layout

7. I²C Bus Operation

The chip supports 7-bit addressing. The RAA271082 I²C device address is reconfigurable through factory programming as either 0x4d (default) or 0x4e. The address selection is done using register 0x7C, Bit 7.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are Reserved for indicating START and STOP conditions, see Figure 31.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The RAA271082 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

An Acknowledge (or ACK) indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (Figure 31). The RAA271082 responds with an ACK after recognition of a START condition, followed by a valid Identification (also known as I²C Address) Byte. The RAA271082 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

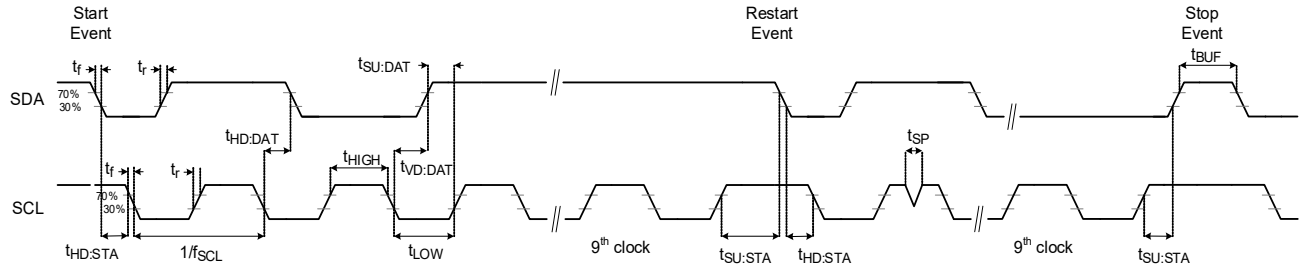


Figure 31. I²C Timing

7.1 Write Operation

A Write operation requires a START condition, followed by an RAA271082 I2C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. After each byte, the RAA271082 responds with an ACK. A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

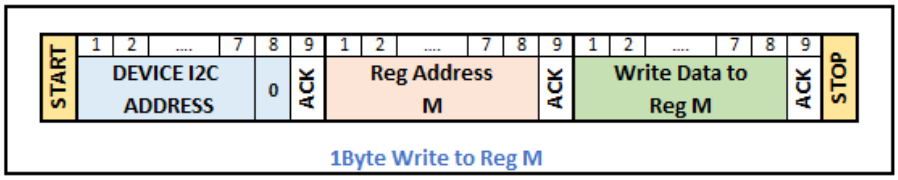


Figure 32. 1-Byte Write to Register M

7.2 Read Operation

A Read operation consists of a dummy write instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation, issuing the following sequence: a START condition, followed by an RAA271082 I²C Address byte with the R/W bit set to 0, a Register Address Byte, a second START, and a second RAA271082 I²C Address byte with the R/W bit set to 1. After each of the three bytes, the RAA271082 responds with an ACK. The RAA271082 then transmits Data Bytes. The master

terminates the Read operation from the RAA271082 by issuing a STOP condition following the last bit of the last data byte.

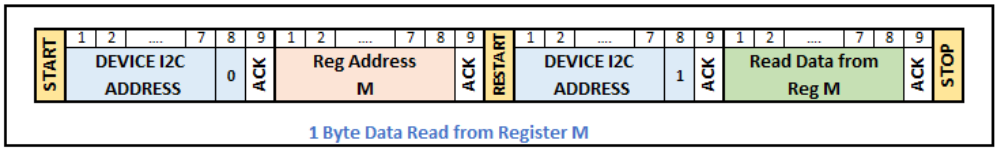


Figure 33. 1-Byte Read from Register M

7.3 I²C Timing

The timing specifications of the I²C I/O from the I²C specification are shown in Table 16. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in Standard and Fast modes.

Table 16. Timing Specifications

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	t_{HD};STA	4000	-	600	-	ns
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	ns
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	ns
Rise Time of SCL	t_{rCL}	-	1000	20	300	ns
Fall Time of SCL	t_{fCL}	-	300	20 × (V_{DD}/5.5V)	300	ns
Rise Time of SDA	t_{rDA}	-	1000	20	300	ns
Fall Time of SDA	t_{fDA}	-	300	20 × (V_{DD}/5.5V)[1]	300	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400	pF
Output Fall Time from V_{IHmin} to V_{ILmax}	t_{of}	-	250	20 × (V_{DD} /5.5V)	250	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	ns

1. Only valid for V_{DD} < 4V.

8. Register Information

The following is the TYPE definition for each address bit in the Register Descriptions.

Type	Description
R	Readable
W	Writable
F	Default value selectable by fuse. Default column lists value prior to fuse programming. These bits are included in the CRC Recheck calculation.
P	Programmable by factory only.
E	Writable and readable only when EN sets the device in Standby mode. Read-only when the EN pin enables the output regulators.
W1S	Writing a 1 sets bit and prevents future clearing of this bit. Writing a 0 has no effect.
W0C	Writing a 0 clears fault status bit. Bit remains cleared if fault was removed. Writing a 1 has no effect.

8.1 Register Address Map

Below is the address map for the I^2C-accessible registers

Offset	Name	Description
0x60	DEV_ID_LO_BYTE	RAA271082 ID low byte.
0x61	DEV_ID_HI_BYTE	RAA271082 ID high byte (0 is omitted)
0x62	DEV_REV_LO_BYTE	Device revision low byte
0x63	DEV_REV_HI_BYTE	Device revision high byte
0x64	BUCK_LDO_STATUS1	PGOOD status and t_{ON}/t_{OFF} sequencer status for each regulator
0x65	BUCK_LDO_STATUS2	Restart lockout status
0x66	BUCK_LDO_REG_STATE	Regulator states (off, soft start, normal, hiccup/latch-off) for each regulator
0x67	BUCK_LDO_EN	Regulator sequencer override (requires factory programming to access this option). Used to individually enable/disable regulators, and enable/disable all LV output pull-downs.
0x70	VIN1_UV_THRESH_OPT	VIN1 under voltage threshold option
0x71	VOUT1_VOLTAGE_OPT	VOUT1 output voltage option
0x72	VOUT1_THRESH_OPT	VOUT1 UV and OV threshold options
0x73	VOUT2_VOLTAGE_OPT	VOUT2 output voltage option
0x74	VOUT2_THRESH_OPT	VOUT2 UV and OV threshold options
0x75	VOUT3_VOLTAGE_OPT	VOUT3 output voltage register
0x76	VOUT3_THRESH_OPT	VOUT3 UV and OV threshold options
0x77	VOUT4_VOLTAGE_OPT	VOUT4 output voltage option
0x78	VOUT4_THRESH_OPT	VOUT4 UV and OV threshold options
0x79	SEQUENCE_OPT	Sequence and Timing Delay on/off options
0x7A	SS_OPT	Spread spectrum modulator options
0x7B	MISC1_OPT	Hiccup algorithm, UV pre-filter, LV output pull-downs, Buck3 phase options
0x7C	MISC2_OPT	I2C address, manual enable control, 30ms UV/OV assertion filter, I^2C CRC checking, RSTB low time, and Buck1 NOC/OC1 options

Offset	Name	Description
0x7D	MISC3_OPT	Buck2/3 OC, NOC usage, and PGOODx configure of RSTB options
0x7E	TRIM_CRC_LOW	CRC low byte
0x7F	TRIM_CRC_HIGH	CRC high byte
0x80	FLT_STATUS_1	Buck 1 and Over-temperature fault status
0x81	FLT_STATUS_2	Buck 2 and Buck 3 fault status
0x82	FLT_STATUS_3	LDO 4 fault status
0x83	FLT_STATUS_4	Watchdog timer, Sequencer, CRC Recheck, I2C CRC, and VDAC Compare fault status
0x84	FLT_LATCHOFF_RESTART	Latch-off Restart Control
0x85	FLT_RESP_MASK1	Buck 1 fault response mask
0x86	FLT_RESP_MASK2	Buck 2 and Buck 3 fault response mask
0x87	FLT_RESP_MASK3	LDO 4 fault response mask
0x8A	FLT_GPIO_EN1	Over-temperature and Buck1 fault GPIO enable control
0x8B	FLT_GPIO_EN2	Buck2 and Buck 3 fault GPIO enable control
0x8C	FLT_GPIO_EN3	LDO4, CRC Recheck, Watchdog timer, I^2C CRC fault GPIO enable control
0x8D	FLT_RSTB_EN	RSTB control for Sequence and Watchdog timer faults
0xA0	WWDT_CFG	Windowed watchdog timer (WWDT) configuration register
0xA1	WWDT_ULW	WWDT upper limit (too slow) counter control
0xA2	WWDT_LLW	WWDT lower limit (too fast) counter control
0xA3	KICK_REG	WWDT timer kick register
0xA4	GPIO_CTRL	GPIO Pin Control. Sets pin direction and usage of GPIO pin.
0xA5	RSTB_CTRL	RSTB Pin Control
0xB6	CRC_RESULT_LO_BIT	LSB of CRC result
0xB7	CRC_RESULT_HI_BITS	MSB of CRC result

8.2 Register Descriptions

The following are the address, bit descriptions, options, and default settings for the I^2C -accessible registers.

8.2.1 DEV_ID_LO_BYTE - 0x60

Name	Bit	Type	Default	Description
dev_id_lo_byte	7:0	R	0x82	RAA271082 ID low byte

8.2.2 DEV_ID_HI_BYTE - 0x61

Name	Bit	Type	Default	Description
dev_id_hi_byte	7:0	R	0x10	RAA271082 ID high byte (27 is omitted)

8.2.3 DEV_REV_LO_BYTE - 0x62

Name	Bit	Type	Default	Description
dev_rev_lo_byte	7:0	R	0x01	Device revision low byte

8.2.4 DEV_REV_HI_BYTE - 0x63

Name	Bit	Type	Default	Description
dev_rev_hi_byte	7:0	R	0xCC	Device revision high byte

8.2.5 BUCK_LDO_STATUS1 - 0x64

Name	Bit	Type	Default	Description
ldo4_pgood	7	R	0x0	LDO4 PGOOD status; 0 = Not good; 1 = Good
buck3_pgood	6	R	0x0	Buck3 PGOOD status; 0 = Not good; 1 = Good
buck2_pgood	5	R	0x0	Buck2 PGOOD status; 0 = Not good; 1 = Good
buck1_pgood	4	R	0x0	Buck1 PGOOD status; 0 = Not good; 1 = Good
ldo4_enabled	3	R	0x0	LDO4 t_{ON}/t_{OFF} status; 0 = Disabled; 1 = Enabled
buck3_enabled	2	R	0x0	Buck3 t_{ON}/t_{OFF} status; 0 = Disabled; 1 = Enabled
buck2_enabled	1	R	0x0	Buck2 t_{ON}/t_{OFF} status; 0 = Disabled; 1 = Enabled
buck1_enabled	0	R	0x0	Buck1 t_{ON}/t_{OFF} status; 0 = Disabled; 1 = Enabled

8.2.6 BUCK_LDO_STATUS2 - 0x65

Name	Bit	Type	Default	Description
Reserved	7:1	R	0x0	
restart_lockout	0	R	0x0	Restart lockout status when EN and/or EN_LV are manually taken low. (Does NOT apply to faults that may cause restart.) 0 = HV and LV regulators are past the 200ms Restart Lockout Period (200ms), and therefore restart can or does happen. 1 = HV and regulators are in Restart Lockout Period (200ms), therefore restart must wait.

8.2.7 BUCK_LDO_REG_STATE - 0x66

Name	Bit	Type	Default	Description
ldo4_state	7:6	R	0x0	LDO4 state 00 = disabled; 01 = soft starting 11 = enabled; 10 = in hiccup or latch-off
buck3_state	5:4	R	0x0	Buck3 state 00 = disabled; 01 = soft starting 11 = enabled; 10 = in hiccup or latch-off
buck2_state	3:2	R	0x0	Buck2 state 00 = disabled; 01 = soft starting 11 = enabled; 10 = in hiccup or latch-off
buck1_state	1:0	R	0x0	Buck1 state 00 = disabled; 01 = soft starting 11 = enabled; 10 = in hiccup or latch-off

8.2.8 BUCK_LDO_EN - 0x67

Name	Bit	Type	Default	Description
reg_direct_en	7	RW	0x0	Direct regulator enable control This is available only when opt_EN_manual bit is set to 1, in register MISC2_OPT (reg 0x7C, Bit 6). 0 = Use the programmed TON_DLY/TOFF_DLY sequence. 1 = Direct output control using Bits [4:0] of this register. (Disables the TON_DLY/TOFF_DLY sequencer.)
Reserved	6:5	R	0x0	
reg_lv_pden	4	RW	0x0	Control output pull-downs for Buck2/3 and LDO4. This is valid only when reg_direct_en (Bit 7) is 1; otherwise, the pull-downs are controlled by the output sequencer. 0 = Disable the pull-downs for Buck2/3 and LDO4. 1 = Enable the pull-downs for Buck2/3 and LDO4.
reg_ldo4_en	3	RW	0x0	Enable LDO4. Requires EN pin high and EN_LV pin high. Only valid when reg_direct_en (Bit 7) is 1; otherwise the output sequencer controls LDO4. 0 = Disabled; 1 = Enabled
reg_buck3_en	2	RW	0x0	Enable BUCK3. Requires EN pin high and EN_LV pin high. Only valid when reg_direct_en (Bit 7) is 1; otherwise the output sequencer controls Buck3. 0 = Disabled; 1 = Enabled
reg_buck2_en	1	RW	0x0	Enable BUCK2. Requires EN pin high and EN_LV pin high. Only valid when reg_direct_en (Bit 7) is 1; otherwise the output sequencer controls Buck2. 0 = Disabled; 1 = Enabled
reg_buck1_en	0	RW	0x0	Enable BUCK1. Requires EN pin high. Only valid when reg_direct_en (Bit 7) is 1; otherwise the output sequencer controls Buck1. 0 = Disabled; 1 = Enabled

8.2.9 VIN1_UV_THRESH_OPT - 0x70

Name	Bit	Type	Default	Description
Reserved	7:2	R	0x0	
opt_vin1_uv_thres	1:0	FERW	0x00	VIN1 Undervoltage Threshold Voltage 0 = 4.5V; 1 = 5.0V; 2 = 6.5V; 3 = 7.0V

8.2.10 VOUT1_VOLTAGE_OPT - 0x71

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	
opt_vout1_output_voltage	4:0	FERW	0x00	VOUT1 Voltage Option Select Decimal (Hex) Voltage 0 (0x00): 3.60V 1 (0x01): 2.80V 2 (0x02): 2.85V 3 (0x03): 2.90V 4 (0x04): 2.95V 5 (0x05): 3.00V 6 (0x06): 3.05V 7 (0x07): 3.10V 8 (0x08): 3.15V 9 (0x09): 3.20V 10 (0x0A): 3.25V 11 (0x0B): 3.30V 12 (0x0C): 3.35V 13 (0x0D): 3.40V 14 (0x0E): 3.50V 15 (0x0F): 3.60V 16 (0x10): 3.70V 17 (0x11): 3.80V 18 (0x12): 5.00V 19 (0x13): 5.05V others: 3.60V

8.2.11 VOUT1_THRESH_OPT - 0x72

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	
opt_vout1_uv_thres	5:4	FERW	0x00	VOUT1 Undervoltage Threshold select 0 = -4% 1 = -6% 2 = -8% 3 = -12%
Reserved	3:2	R	0x0	
opt_vout1_ov_thres	1:0	FERW	0x00	VOUT1 Overvoltage Threshold select 0 = +4% 1 = +6% 2 = +8% 3 = +12%

8.2.12 VOUT2_VOLTAGE_OPT - 0x73

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	
opt_vout2_output_voltage	5:0	FERW	0x00	VOUT2 Voltage Option Select Decimal (Hex) Voltage 0 (0x00): 1.80V 1 (0x01): 0.85V 2 (0x02): 0.90V 3 (0x03): 0.95V 4 (0x04): 1.00V 5 (0x05): 1.05V 6 (0x06): 1.10V 7 (0x07): 1.15V 8 (0x08): 1.20V 9 (0x09): 1.25V 10 (0x0A): 1.30V 11 (0x0B): 1.35V 12 (0x0C): 1.40V 13 (0x0D): 1.45V 14 (0x0E): 1.50V 15 (0x0F): 1.55V 16 (0x10): 1.60V 17 (0x11): 1.65V 18 (0x12): 1.70V 19 (0x13): 1.75V 20 (0x14): 1.80V 21 (0x15): 1.85V 22 (0x16): 1.90V 23 (0x17): 1.95V 24 (0x18): 2.00V 25 (0x19): 2.05V 26 (0x1A): 2.10V 27 (0x1B): 2.20V 28 (0x1C): 2.30V 29 (0x1D): 2.40V 30 (0x1E): 2.45V 31 (0x1F): 2.50V 32 (0x20): 2.55V 33 (0x21): 2.80V 34 (0x22): 3.30V others: 1.80V

8.2.13 VOUT2_THRESH_OPT - 0x74

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	
opt_vout2_uv_thres	5:4	FERW	0x00	VOUT2 Undervoltage Threshold select 0 = -4% 1 = -6% 2 = -8% 3 = -12%
Reserved	3:2	R	0x0	
opt_vout2_ov_thres	1:0	FERW	0x00	VOUT2 Overvoltage Threshold select 0 = +4% 1 = +6% 2 = +8% 3 = +12%

8.2.14 VOUT3_VOLTAGE_OPT - 0x75

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	
opt_vout3_output_voltage	5:0	FERW	0x00	VOUT3 Voltage Option Select Decimal (Hex) Voltage 0 (0x00): 1.20V 1 (0x01): 0.85V 2 (0x02): 0.90V 3 (0x03): 0.95V 4 (0x04): 1.00V 5 (0x05): 1.05V 6 (0x06): 1.10V 7 (0x07): 1.15V 8 (0x08): 1.20V 9 (0x09): 1.25V 10 (0x0A): 1.30V 11 (0x0B): 1.35V 12 (0x0C): 1.40V 13 (0x0D): 1.45V 14 (0x0E): 1.50V 15 (0x0F): 1.55V 16 (0x10): 1.60V 17 (0x11): 1.65V 18 (0x12): 1.70V 19 (0x13): 1.75V 20 (0x14): 1.80V 21 (0x15): 1.85V 22 (0x16): 1.90V 23 (0x17): 1.95V 24 (0x18): 2.00V 25 (0x19): 2.05V 26 (0x1A): 2.10V 27 (0x1B): 2.20V 28 (0x1C): 2.30V 29 (0x1D): 2.40V 30 (0x1E): 2.45V 31 (0x1F): 2.50V 32 (0x20): 2.55V 33 (0x21): 2.80V 34 (0x22): 3.30V others: 1.20V

8.2.15 VOUT3_THRESH_OPT - 0x76

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x0	
opt_vout3_uv_thres	5:4	FERW	0x00	VOUT3 Undervoltage Threshold select 0 = -4% 1 = -6% 2 = -8% 3 = -12%
Reserved	3:2	R	0x0	
opt_vout3_ov_thres	1:0	FERW	0x00	VOUT3 Overvoltage Threshold select 0 = +4% 1 = +6% 2 = +8% 3 = +12%

8.2.16 VOUT4_VOLTAGE_OPT - 0x77

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	
opt_vout4_output_voltage	3:0	FERW	0x00	VOUT4 Voltage Option Select Decimal (Hex) Voltage 0 (0x0): 3.30V 1 (0x1): 2.70V 2 (0x2): 2.75V 3 (0x3): 2.80V 4 (0x4): 2.85V 5 (0x5): 2.90V 6 (0x6): 2.95V 7 (0x7): 3.00V 8 (0x8): 3.10V 9 (0x9): 3.20V 10 (0xA): 3.25V 11 (0xB): 3.30V 12 (0xC): 3.35V 13 (0xD): 3.40V others: 3.30V

8.2.17 VOUT4_THRESH_OPT - 0x78

Name	Bit	Type	Default	Description
Reserved	7:6	R	0x00	
opt_vout4_uv_thres	5:4	FERW	0x00	VOUT4 Undervoltage Threshold select 0 = -4% 1 = -6% 2 = -8% 3 = -12%
Reserved	3:2	R	0x00	
opt_vout4_ov_thres	1:0	FERW	0x00	VOUT4 Overvoltage Threshold select 0 = +4% 1 = +6% 2 = +8% 3 = +12%

8.2.18 SEQUENCE_OPT - 0x79

Name	Bit	Type	Default	Description
opt_seq	7	FERW	0x00	Sequence Option Select for LV regulators - Selects startup and shutdown order for the low voltage regulators 0 = Startup order is BUCK2, BUCK3, and LDO4. Shutdown order is LDO4, BUCK3, and BUCK2. 1 = Startup order is LDO4, BUCK2, and BUCK3. Shutdown order is BUCK3, BUCK2, and LDO4.
Reserved	6	R	0x0	
opt_toff_delay	5:3	FERW	0x00	t_{OFF} delay select for regulator sequence. This is the delay between outputs shutting off in sequence. 0 = 0ms 1 = 0.5ms 2 = 1ms 3 = 2ms 4 = 4ms 5 = 8ms 6 = 16ms 7 = 32ms
opt_ton_delay	2:0	FERW	0x00	t_{ON} delay select for regulator sequence. This is the delay between outputs turning on in sequence. 0 = 0ms 1 = 0.5ms 2 = 1ms 3 = 2ms 4 = 4ms 5 = 8ms 6 = 16ms 7 = 32ms

8.2.19 SS_OPT - 0x7A

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x00	
opt_ss_algorithm	2:0	FERW	0x00	Selects spread spectrum algorithm 0 = Spread spectrum disabled 1 = Two slope modulation, 9.13kHz 2 = Pseudo-random dwell between 1 and 8 cycles, with pseudo-random frequency 3 = Pseudo-random dwell periods 4 and 32 cycles in steps of 4 cycles, with pseudo-random frequency 4 = Triangular modulation, 8.85kHz 5 = Fixed dwell for 4 cycles with pseudo-random frequency 6 = Fixed dwell for 8 cycles with pseudo-random frequency 7 = Fixed dwell for 24 cycles with pseudo-random frequency

8.2.20 MISC1_OPT - 0x7B

Name	Bit	Type	Default	Description
opt_hicn_lat	7:6	FERW	0x00	Fault Response Option for Hiccup and Latch-off. Hiccup response shuts down regulator(s) for 200ms then attempts to restart. **Note:** For all latched shutdowns, if outputs have gone into a latched shutdown, they can be restarted by setting Bit 4 and/or Bit 0 of register 0x84 to zero. See register 0x84. 0 = Hiccup on fault: repeat startup/shutdown indefinitely until fault is cleared. 1 = Hiccup on fault: repeat startup/shutdown 5 times maximum then latch-off if fault remains. 2 = Hiccup on fault: repeat startup/shutdown 10 times maximum then latch-off if fault remains. 3 = Latch-off on fault: shuts down regulator(s) on fault. Do not attempt restart.
opt_enUV_preFilt	5:4	FERW	0x00	Filter for UV detection. This applies only to undervoltage faults. The filter selected applies to VOUT1/2/3 and LDO4. 0 = No additional filter 1 = Enable additional 10µs filter 2 = Enable additional 25µs filter 3 = Enable additional 45µs filter **Note:** For all options, there is also a fixed delay of approximately 2µs.
opt_disPD_LDO4	3	FERW	0x00	LDO 4 pull-down control (at LDO4 shutoff) 0 = Output pull-down is enabled for 200ms 1 = Output pull-down is disabled
opt_disPD_buck3	2	FERW	0x00	Buck 3 pull-down control (at Buck3 shutoff) 0 = Output pull-down is enabled for 200ms 1 = Output pull-down is disabled
opt_disPD_buck2	1	FERW	0x00	Buck 2 pull-down control (at Buck2 shutoff) 0 = Output pull-down is enabled for 200ms 1 = Output pull-down is disabled
opt_phase180_buck3	0	FERW	0x00	Buck 3 switching phase option 0 = 180 degrees phase shifted with Buck1 1 = In phase with Buck1

8.2.21 MISC2_OPT - 0x7C

Name	Bit	Type	Default	Description
opt_i2c_addr	7	FPRW	0x00	Sets two LSBs of the 7-bit I²C slave address The five MSBs of the RAA271082 I²C address bits are always 10011. 0 = Set 01 for LSBs. Slave address is 1001101 (0x4D) 1 = Set 10 for LSBs. Slave address is 1001110 (0x4E)
opt_EN_manual	6	FPRW	0x00	Set to 1 allows manual I²C control of regulators using register 0x67 Bits 3:0. This bit can be set to 1 only by factory programming. If set to 1, register BUCK_LDO_EN (reg 0x67) can be used for manual on/off control of the regulators. 0 = Prohibit I²C direct control of regulators. EN/EN_LV sequencer is enabled. 1 = Allow I²C direct control of regulators using register 0x67. EN/EN_LV sequencer is disabled.
opt_enUVOV_pgFilt	5	FERW	0x00	30ms UV/OV low assertion persistence filter. This filter applies to both OV and UV faults, and inserts a 30ms delay on the RSTB response to a fault. **Note:** This 30ms delay does not apply to fault response. If the device is configured to shut down an output on a UV or OV fault, the fault triggers an immediately shut down of the output, which may also drive the RSTB pin low immediately before the 30ms timer has elapsed. 0 = Disable 30ms filter 1 = Enable 30ms filter
opt_use_I2C_CRC	4	FERW	0x00	Transactional I²C CRC checking 0 = Disabled. No additional CRC bytes are inserted in I²C transactions 1 = Enabled. Additional CRC bytes are inserted in I²C transactions
opt_short_fault_wait	3	FERW	0x00	RSTB low period and Hiccup wait time. This applies only to WWDT faults and a Sequence fault. All other faults result in a 200ms RSTB low pulse. **Note:** The EN, EN_LV restart lockout time also follows the below selection. 0 = 200ms; 1 = 20ms
opt_NOCLimHigh	2	FERW	0x00	Select NOC threshold. 0 = NOC = -0.8A, LSFLT = +1.8A 1 = NOC = -1.0A, LSFLT = +1.8A **Note:** LSFLT is an OC2 (overcurrent 2) detector for Buck1 that detects a severe overcurrent fault in the Buck1 low-side MOSFET. This is separate from the OC2 detector for Buck1 that detects severe overcurrent in the high-side MOSFET.
opt_OC1LimHigh	1	FERW	0x00	Select among three OC1 levels for HV Buck 1 (OC1LimHigh,OC1LimLow = 1:0) 00 = 1.50A (default) x1 = 1.20A 10 = 1.75A
opt_OC1LimLow	0	FERW	0x00	See opt_OC1LimHigh description.

8.2.22 MISC3_OPT - 0x7D

Name	Bit	Type	Default	Description
opt_LVBOC_buck3	7:6	FERW	0x00	Options for LV Buck 3 Overcurrent limit 0x = 1.20A 10 = 0.96A 11 = 1.56A
opt_LVBOC_buck2	5:4	FERW	0x00	Options for LV Buck 2 Overcurrent limit 0x = 1.20A 10 = 0.96A 11 = 1.56A
Reserved	3:2	R	0x0	
opt_pg_rstb	1:0	FERW	0x00	Each output has an internal Power-Good signal that reflects if the output is in regulation. Bits 1:0 determine which outputs are ignored by the RSTB indicator if an output moves outside its PGOOD (OV/UV) window. When opt_seq = 0 (register 0x79 Bit 7 = 0): ▪ 00 = no PGOOD signal is ignored ▪ 01 = LDO4 PGOOD is ignored ▪ 10 = LDO4 and Buck3 PGOODs are ignored ▪ 11 = LDO4, Buck3, and Buck2 PGOODs are ignored When opt_seq = 1 (register 0x79 Bit 7 = 1): ▪ 00 = no PGOOD signal is ignored ▪ 01 = Buck3 PGOOD is ignored ▪ 10 = Buck3 and Buck2 PGOODs are ignored ▪ 11 = Buck3, Buck2, and LDO4 PGOODs are ignored

8.2.23 TRIM_CRC_LOW - 0x7E

Name	Bit	Type	Default	Description
trim_CRC_low_bit	7	FERW	0x00	Bit 0 of CRC Because the CRC-rechecker is actively checking all OPT and TRIM bit values, any alteration of the OPT bits triggers a CRC-recheck error within 5ms and shutdown regulation. It also sets the CRC recheck fault bit, register 0x83 Bit 4. **Note:** The CRC recheck fault bit, unlike other fault bits, automatically clears if the cause of the fault is removed. To modify factory-programmed options, use the following procedure: 1. Set EN to Standby (EN = 1.5V). This places the device in standby with no switching. 2. Alter all OPT bits as needed. 3. Write 0 to trim_CRC_low_bit (register 0x7E, Bit 7) and 0x00 to trim_CRC_high_bits (register 0x7F). 4. Wait 5ms. PMIC auto-calculates a new CRC value. 5. Read the auto-calculated crc_result_lo_bit (register 0xB6) and crc_result_hi_bits values (register 0xB7). 6. Write those values into the trim_CRC_low_bit (register 0x7E, Bit 7) and trim_CRC_high_bits fields (register 0x7F). 7. Wait 5ms. The CRC recheck fault should clear (0x83 Bit 4 should now be zero) and the device can be started with the new selected options, by setting EN above 1.8V.
Reserved	6:0	R	0x0	

8.2.24 TRIM_CRC_HIGH - 0x7F

Name	Bit	Type	Default	Description
trim_CRC_high_bits	7:0	FERW	0x00	Bits 8:1 of CRC See description of trim_CRC_low_bit

8.2.25 FLT_STATUS_1 - 0x80

Name	Bit	Type	Default	Description
Reserved	7	WOC	0x0	
buck1_severe_UV_fault	6	W0C	0x0	Buck1 severe UV fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_severe_OV_fault	5	W0C	0x0	Buck1 severe OV fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_NOC_fault	4	W0C	0x0	Buck1 negative overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_OC2_fault	3	W0C	0x0	Buck1 overcurrent fault 2 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_OC1_fault	2	W0C	0x0	Buck1 overcurrent fault 1 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_OV_fault	1	W0C	0x0	Buck1 overvoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.
buck1_UV_fault	0	W0C	0x0	Buck1 undervoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if the fault was removed.

8.2.26 FLT_STATUS_2 - 0x81

Name	Bit	Type	Default	Description
buck3_NOC_fault	7	W0C	0x0	Buck3 negative overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck3_OC_fault	6	W0C	0x0	Buck3 overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck3_OV_fault	5	W0C	0x0	Buck3 overvoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck3_UV_fault	4	W0C	0x0	Buck3 undervoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck2_NOC_fault	3	W0C	0x0	Buck2 negative overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck2_OC_fault	2	W0C	0x0	Buck2 overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck2_OV_fault	1	W0C	0x0	Buck2 overvoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
buck2_UV_fault	0	W0C	0x0	Buck2 undervoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.

8.2.27 FLT_STATUS_3 - 0x82

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	
bist_fail	3	R	0x0	Built-in Self Test diagnostic status 0 = Pass; 1 = Fail
ldo4_OC_fault	2	W0C	0x0	LDO4 overcurrent fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
ldo4_OV_fault	1	W0C	0x0	LDO4 overvoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.
ldo4_UV_fault	0	W0C	0x0	LDO4 undervoltage fault 0 = No fault detected 1 = Fault detected Write 0 to clear the fault_status bit. Bit remains cleared if fault was removed.

8.2.28 FLT_STATUS_4 - 0x83

Name	Bit	Type	Default	Description
vdac21_gt90_fault	7	W0C	0x0	DAC2 to DAC1 Compare fault VDAC21 > 90% fault error 0 = No fault detected 1 = Fault detected DAC1 is the regulation DAC. DAC2 is the OV/UV monitor DAC.
vdac12_gt90_fault	6	W0C	0x0	DAC1 to DAC2 Compare fault VDAC12 > 90% fault error 0 = No fault detected 1 = Fault detected DAC1 is the regulation DAC. DAC2 is the OV/UV monitor DAC.
i2c_crc_fault	5	W0C	0x0	I^2C transactional CRC fault 0 = No fault detected 1 = Fault detected
crc_recheck_fault	4	W0C	0x0	CRC recheck Fault 0 = No fault detected 1 = Fault detected This bit is continually updated at approximately 5ms intervals.
seq_fault	3	W0C	0x0	Enable/Disable Sequencer Fault Set high in the unlikely event of incorrect output sequencing. 0 = No fault detected 1 = Fault detected
wdt_restart_fault	2	W0C	0x0	WWDT restart_fault. Activated when the WWDT reaches 2 times the upper (too-slow) window counter period before receiving a kick. 0 = No fault detected 1 = Fault detected
wdt_slow_fault	1	W0C	0x0	WWDT slow_fault. Activated when the WWDT reaches the upper (too-slow) window counter period before receiving a kick. 0 = No fault detected 1 = Fault detected
wdt_fast_fault	0	W0C	0x0	WWDT fast_fault. Activated when the WWDT detects kicking is faster than the lower (too-fast) window counter period. 0 = No fault detected 1 = Fault detected

8.2.29 FLT_LATCHOFF_RESTART - 0x84

Name	Bit	Type	Default	Description
Reserved	7:5	R	0x0	
lo_flt_LV	4	W0C	0	Latch-off LV regulator restart control Read back of 1 indicates that a latch-off fault has occurred on a LV regulator (Buck2, Buck3, or LDO4). Writing a 0 to this bit allows a LV regulators to restart from a latch-off fault.

Name	Bit	Type	Default	Description
Reserved	3:1	R	0x0	
lo_flt_HV	0	W0C	0	Latch-off HV buck restart control Read back of 1 indicates that a latch-off fault has occurred on the Buck1 regulator. Writing a 0 to this bit allows the Buck 1 regulator to restart from a latch-off fault.

8.2.30 FLT_RESP_MASK1 - 0x85

Name	Bit	Type	Default	Description
Reserved	7	PRW	0x00	
buck1_severe_uv_fault_resp_mask	6	RW	0x00	Buck 1 severe UV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_severe_ov_fault_resp_mask	5	RW	0x00	Buck 1 severe OV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_noc_fault_resp_mask	4	RW	0x01	Buck 1 NOC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_oc2_fault_resp_mask	3	RW	0x00	Buck 1 OC2 fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_oc1_fault_resp_mask	2	RW	0x01	Buck 1 OC1 fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_ov_fault_resp_mask	1	RW	0x01	Buck 1 OV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck1_uv_fault_resp_mask	0	RW	0x01	Buck 1 UV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault

8.2.31 FLT_RESP_MASK2 - 0x86

Name	Bit	Type	Default	Description
buck3_noc_fault_resp_mask	7	RW	0x01	Buck 2 NOC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck3_oc_fault_resp_mask	6	RW	0x00	Buck 2 OC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck3_ov_fault_resp_mask	5	RW	0x01	Buck 2 OV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck3_uv_fault_resp_mask	4	RW	0x01	Buck 2 UV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck2_noc_fault_resp_mask	3	RW	0x01	Buck 2 NOC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck2_oc_fault_resp_mask	2	RW	0x00	Buck 2 OC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck2_ov_fault_resp_mask	1	RW	0x01	Buck 2 OV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
buck2_uv_fault_resp_mask	0	RW	0x01	Buck 2 UV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault

8.2.32 FLT_RESP_MASK3 - 0x87

Name	Bit	Type	Default	Description
Reserved	7:3	R	0x0	
ldo4_oc_fault_resp_mask	2	RW	0x01	LDO4 OC fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
ldo4_ov_fault_resp_mask	1	RW	0x01	LDO4 OV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault
ldo4_uv_fault_resp_mask	0	RW	0x01	LDO4 UV fault response mask 0 = Respond to fault per opt_hicn_lat, register 0x7B Bits 7:6 1 = No response to fault

8.2.33 FLT_GPIO_EN1 - 0x8A

Name	Bit	Type	Default	Description
ot2_fault_gpio_enable	7	RW	0x00	Over-temperature fault GPIO enable 0 = Do not assert GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_severe_uv_fault_gpio_enable	6	RW	0x1	Buck 1 severe UV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_severe_ov_fault_gpio_enable	5	RW	0x1	Buck 1 severe OV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_noc_fault_gpio_enable	4	RW	0x00	Buck 1 NOC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_oc2_fault_gpio_enable	3	RW	0x00	Buck 1 OC2 fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_oc1_fault_gpio_enable	2	RW	0x00	Buck 1 OC1 fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_ov_fault_gpio_enable	1	RW	0x00	Buck 1 OV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck1_uv_fault_gpio_enable	0	RW	0x00	Buck 1 UV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault

8.2.34 FLT_GPIO_EN2 - 0x8B

Name	Bit	Type	Default	Description
buck3_noc_fault_gpio_enable	7	RW	0x00	Buck 3 NOC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck3_oc_fault_gpio_enable	6	RW	0x00	Buck 3 OC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck3_ov_fault_gpio_enable	5	RW	0x00	Buck 3 OV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck3_uv_fault_gpio_enable	4	RW	0x00	Buck 3 UV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck2_noc_fault_gpio_enable	3	RW	0x00	Buck 2 NOC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck2_oc_fault_gpio_enable	2	RW	0x00	Buck 2 OC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck2_ov_fault_gpio_enable	1	RW	0x00	Buck 2 OV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
buck2_uv_fault_gpio_enable	0	RW	0x00	Buck 2 UV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault

8.2.35 FLT_GPIO_EN3 - 0x8C

Name	Bit	Type	Default	Description
i2c_crc_fault_gpio_enable	7	RW	0x00	I^2C fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
wdt_restart_fault_gpio_enable	6	RW	0x00	WWDT restart fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
wdt_slow_fault_gpio_enable	5	RW	0x00	WWDT slow fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
wdt_fast_fault_gpio_enable	4	RW	0x00	WWDT fast fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
crc_recheck_fault_gpio_enable	3	RW	0x00	CRC recheck fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
ldo4_oc_fault_gpio_enable	2	RW	0x00	LDO4 OC fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
ldo4_ov_fault_gpio_enable	1	RW	0x00	LDO4 OV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault
ldo4_uv_fault_gpio_enable	0	RW	0x00	LDO4 UV fault GPIO enable 0 = Do not assert the GPIO pin on fault 1 = Assert GPIO pin low on fault

8.2.36 FLT_RSTB_EN - 0x8D

Name	Bit	Type	Default	Description
Reserved	7:4	R	0x0	
seq_fault_rstb_enable	3	RW	0x00	Sequencer fault RSTB enable 0 = Do not assert the RSTB pin on fault 1 = Assert RSTB pin low on fault, for the time defined by opt_short_fault_wait register 0x7C Bit 3.
wdt_restart_fault_rstb_enable	2	RW	0x00	WWDT restart fault RSTB enable 0 = Do not assert the RSTB pin on fault 1 = Assert RSTB pin low on fault, for the time defined by opt_short_fault_wait register 0x7C Bit 3.
wdt_slow_fault_rstb_enable	1	RW	0x00	WWDT slow fault RSTB enable 0 = Do not assert the RSTB pin on fault 1 = Assert RSTB pin low on fault, for the time defined by opt_short_fault_wait register 0x7C Bit 3.
wdt_fast_fault_rstb_enable	0	RW	0x00	WWDT fast fault RSTB enable 0 = Do not assert the RSTB pin on fault 1 = Assert RSTB pin low on fault, for the time defined by opt_short_fault_wait register 0x7C Bit 3.

8.2.37 WWDT_CFG - 0xA0

Name	Bit	Type	Default	Description
wwdt_enable	7	RW	0x0	WWDT enable: windowed watchdog timer enable control. This bit should be set only after all of the WWDT control, tick, and count registers have been initialized. **Note:** This bit enables the fault response to WWDT fault, as set by Bits 6:4. This bit does not enable or disable detection of a WWDT fault. Detection of WWDT faults is automatically enabled when a non-zero value is entered for the Counter values in registers 0xA1 and 0xA2. WWDT detected faults are reflected in the WWDT fault status bits (register 0x83 Bits 2:0), even if fault response to a WWDT fault is disabled. 0 = Timer disabled from fault response 1 = Timer enabled for fault response
wwdt_reg_dis	6:4	RW	0x0	WWDT fault mask. These bits select the WWDT faults that trigger an output shut down. The wwdt_reg_dis_sel bit (Bit 3) selects which regulators are disabled on WWDT faults. 200ms after the shutdown completes, regulators restart depending on the EN/EN_LV pin values. Bit 6 = 1 restart fault creates shutdown event Bit 5 = 1 slow fault creates shutdown event Bit 4 = 1 fast fault creates shutdown event
wwdt_reg_dis_sel	3	RW	0x0	WWDT output shutdown select. 0 = EN (high voltage regulator enable) and EN_LV (low voltage regulator enable) toggled. All outputs are shut down. 1 = EN_LV (low voltage regulator) toggled. Low voltage outputs are shut down, high voltage regulator remains enabled.
wwdt_lockout	2	W1S	0	WWDT Lockout bit. If set, the device locks out all future attempts to change or disable the WWDT registers, including this bit. This protects against erroneous reprogramming of the WWDT parameters. Locked out registers include WWDT_CFG (0xA0), WWDT_LLW (0xA1), and WWDT_ULW (0xA2). Writes to the kick register KICK_REG (0xA3) are not locked out. When this bit is set, the only way to reprogram or change the WWDT settings is by cycling VIN1 or the EN input. 0 = WWDT programmable 1 = WWDT reprogramming locked out.
kick_select	1:0	RW	0x0	WWDT Kick selection - selects actions that can kick (restart) the WWDT timer Minimum pulse width high or low is 25ns for positive edge GPIO kicks. The I^2C kick register address is 0xA3. 0 = Negative edge GPIO pin kick or I^2C kick_reg write 1, 2 = Positive edge GPIO pin kick or I^2C kick_reg write 3 = I^2C kick_reg write only

8.2.38 WWDT_ULW - 0xA1

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	
wdt_ultick	6:4	RW	0x0	Selects the timebase units for the WWDT upper window (kicking is too slow) counter. This also sets the timing for the WWDT Restart timer, which is twice the time for the too-slow counter. This register and the wdt_ulcnt bits below set the threshold period for the too-slow kicking limit. Kicks less frequent than this value are handled as a slow fault condition. This also sets the restart kicking limit, which is always 2x the too-slow period. 0 = Upper window function disabled 1 = 10µs tick 2 = 100µs tick 3 = 1ms tick 4 = 10ms tick 5 = 100ms tick 6 = 1s tick 7 = Upper window function disabled
wdt_ulcnt	3:0	RW	0x00	WWDT upper limit window counter value using the timebase as selected in the wdt_ultick register. **Note:** When this register has a non-zero value, detection of the WWDT too-slow and restart faults is enabled.

8.2.39 WWDT_LLW - 0xA2

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	
wdt_lltick	6:4	RW	0x0	Selects the timebase units for the WWDT lower window (kicking is too fast) counter. This register and the wdt_llcnt bits set the threshold period for the too fast kicking limit. Kicks more frequent than this value are handled as a fast fault condition. 0 = Lower window function disabled 1 = 10µs tick 2 = 100µs tick 3 = 1ms tick 4 = 10ms tick 5 = 100ms tick Others = Lower window function disabled
wdt_llcnt	3:0	RW	0x00	WWDT lower limit window counter value using the timebase as selected in the wdt_lltick register. **Note:** When this register has a non-zero value, detection of the WWDT too-slow and restart faults is enabled.

8.2.40 KICK_REG - 0xA3

Name	Bit	Type	Default	Description
kick_reg	7:0	R	0x00	WWDT kick register - when enabled using register 0xA0 Bits 1:0, writing valid kick data to this register kicks the WWDT. Writing 0x2A kicks the WWDT Writing other values does not kick

8.2.41 GPIO_CTRL - 0xA4

Name	Bit	Type	Default	Description
gpio_in	7	R	0x0	GPIO pin input value. Read-only.
gpio_out	6	R	0x0	GPIO output drive feedback.
Reserved	5	R	0x0	
gpio_dout	4	RW	0x0	GPIO pin direct data output, used when gpio_out_sel below (Bits 1:0) is set to 2. This bit is used, when GPIO is configured as an output, to force the GPIO pin to a logic 1 or 0.
Reserved	3	R	0x0	
gpio_dir	2	RW	0x0	GPIO pin direction setting 0 = Open-drain output. Used when GPIO is used to indicate fault status according the FLT_GPIO registers 0x8A, 0x8B, 0x8C. 1 = Input. Used to set the GPIO pin as an input. This can be used as a kick for the WWDT, or as a separate input which can be read using I^2C. With GPIO configured as an input, the input logic state is available on Bit 7.
gpio_out_sel	1:0	RW	0x0	GPIO pin output select 0 = GPIO output is driven high during PMIC initialization. Open-drain drives low when initialization is complete. 1 = GPIO output drives low according to FAULT_GPIO_ENABLE register selection. 2 = GPIO output is controlled by the gpio_dout bit. 3 = Output SYNC at 2.2MHz

8.2.42 RSTB_CTRL - 0xA5

Name	Bit	Type	Default	Description
Reserved	7	R	0x0	
rstb_out	6	R	0x0	RSTB output drive feedback.
Reserved	5:4	R	0x0	
rstb_gen_pulse	3	WO	0x0	RSTB pulses low when 1 is written to this bit. Pulse width is controlled by opt_short_fault_wait When opt_short_fault_wait = 0, pulse is 200ms When opt_short_fault_wait = 1, pulse is 20ms
Reserved	2:0	R	0x0	

8.2.43 CRC_RESULT_LO_BIT - 0xB6

Name	Bit	Type	Default	Description
crc_result_lo_bit	7	R	0x0	Bit 0 of the 9-bit CRC result. Under fuse non-CRC error conditions, this bit should be a zero.
Reserved	6:0	R	0x0	

8.2.44 CRC_RESULT_HI_BITS - 0xB7

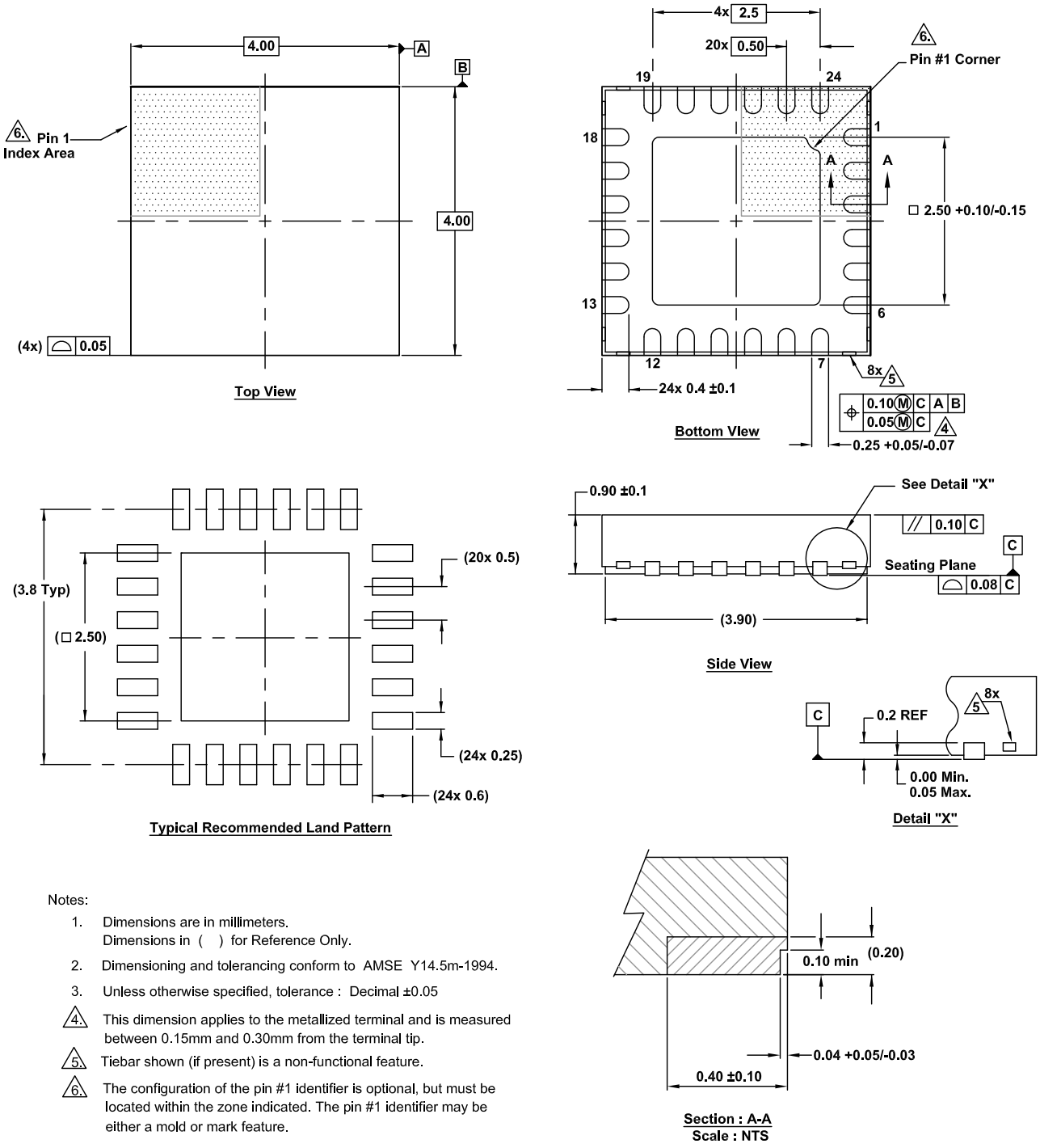
Name	Bit	Type	Default	Description
crc_result_hi_bits	7:0	R	0x0	Bits 8 to 1 of the 9-bit CRC result. Under fuse non-CRC error conditions, these bits should be a zero.

9. Package Outline Drawing

For the most recent package outline drawing, see L24.4x4K.

L24.4x4K

24 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 2, 12/18



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA271082A4HNP#AA0	271082 A4H	24 Ld SCQFN	L24.4x4K	Tray	-40 to +150°C
RAA271082A4HNP#HA0				Reel, 6k	
RAA271082A4HNP#MA0				Reel, 250	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA271082 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

11. Revision History

Revision	Date	Description
1.00	Jul 13, 2022	Initial release.