RAA489220

4 to 10 Cell Battery Front End and Protector

The RAA489220 is a 10-cell Battery management Front End (BFE IC) with both autonomous protection functions and battery health monitoring for packs with MCU control (Figure 1).

The RAA489220 monitors each cell for overvoltage, undervoltage, pack temperature, charge currents, and discharge currents. This device includes internal self test to confirm its own health, and system checks to confirm the system state.

The I^2C interface includes optional CRC to reliably communicate with an MCU. The device has low-side charge and discharge FET controls to disconnect the pack from a load or charger. The RAA489220 has a low typical Low Power Mode current consumption of 3µA to maximize battery shelf life and operational time.

The RAA489220 is offered in a 32pin 4mm×4mm QFN package.

Features

- VPACK voltages: 5V to 44V
- Hot plug tolerance
- Built-in low-side FET drivers
- Charger/load presence detection
- Cell open wire and system checks
- Autonomous detection and actions
- HVGPIO fuse blow configurable
- Support for wide range of current-sense resistors

Applications

- Power tools
- Hand held electronics
- Battery protector

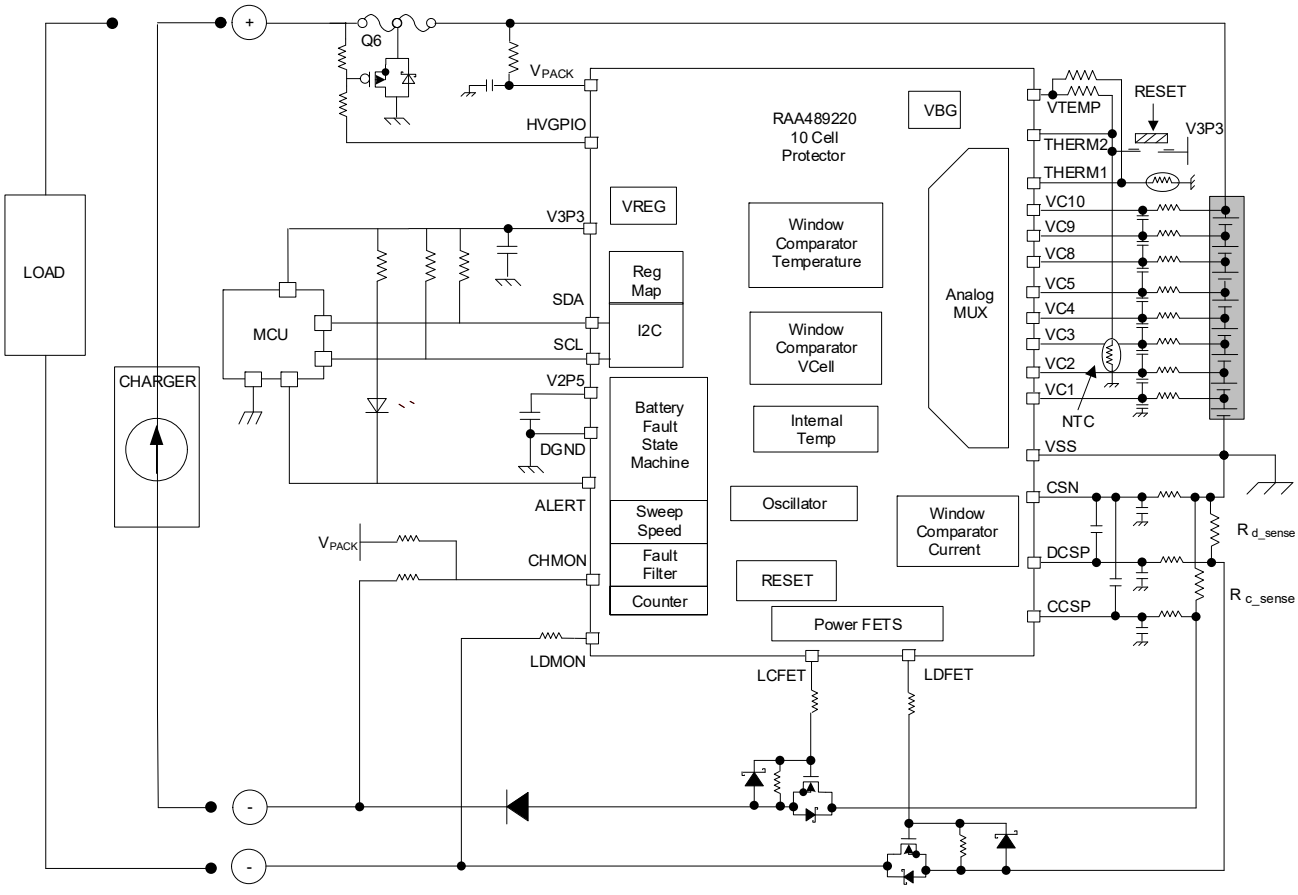


Figure 1. BFE Application

Contents

1. Overview

1.1 Block Diagram

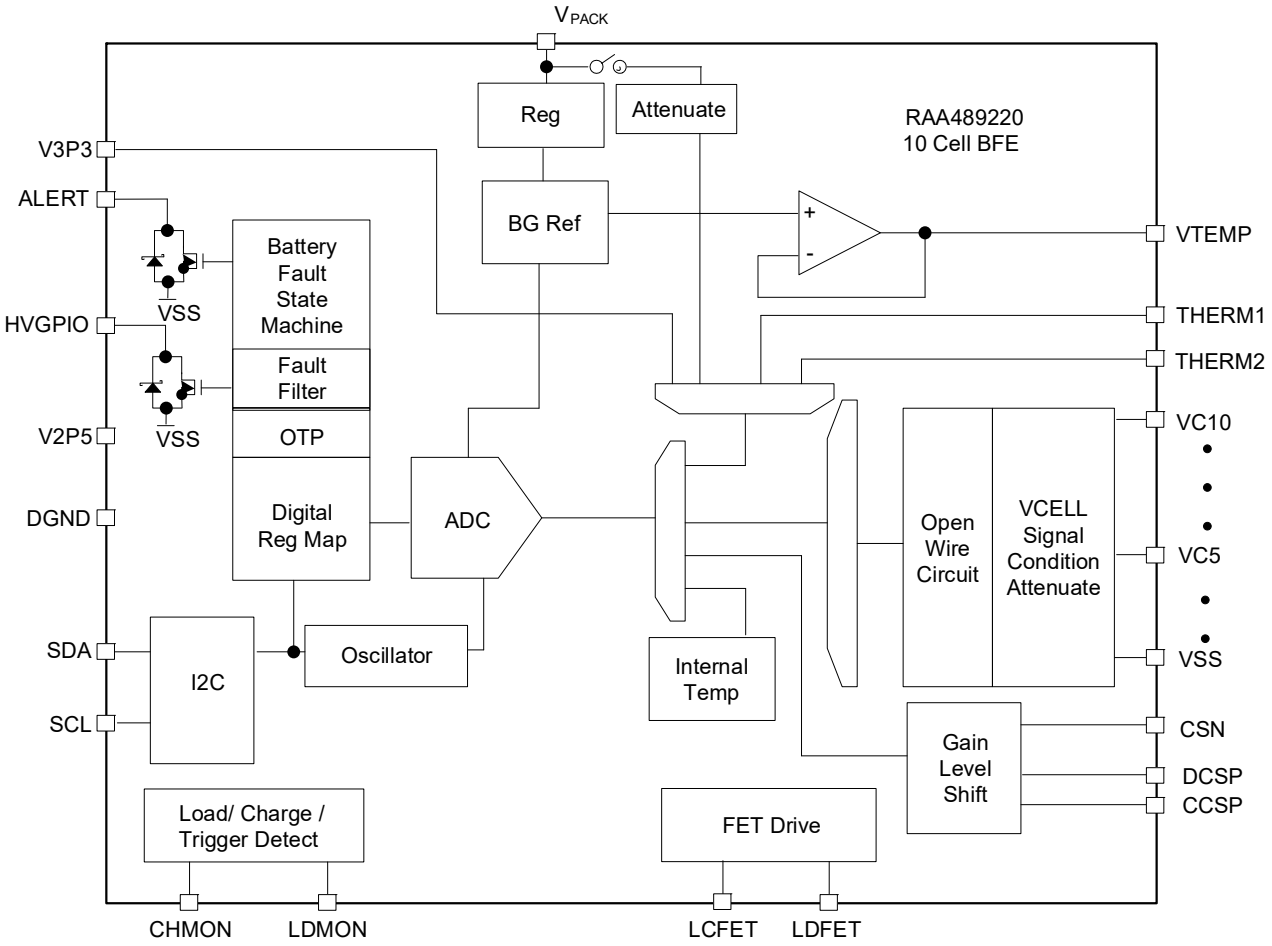
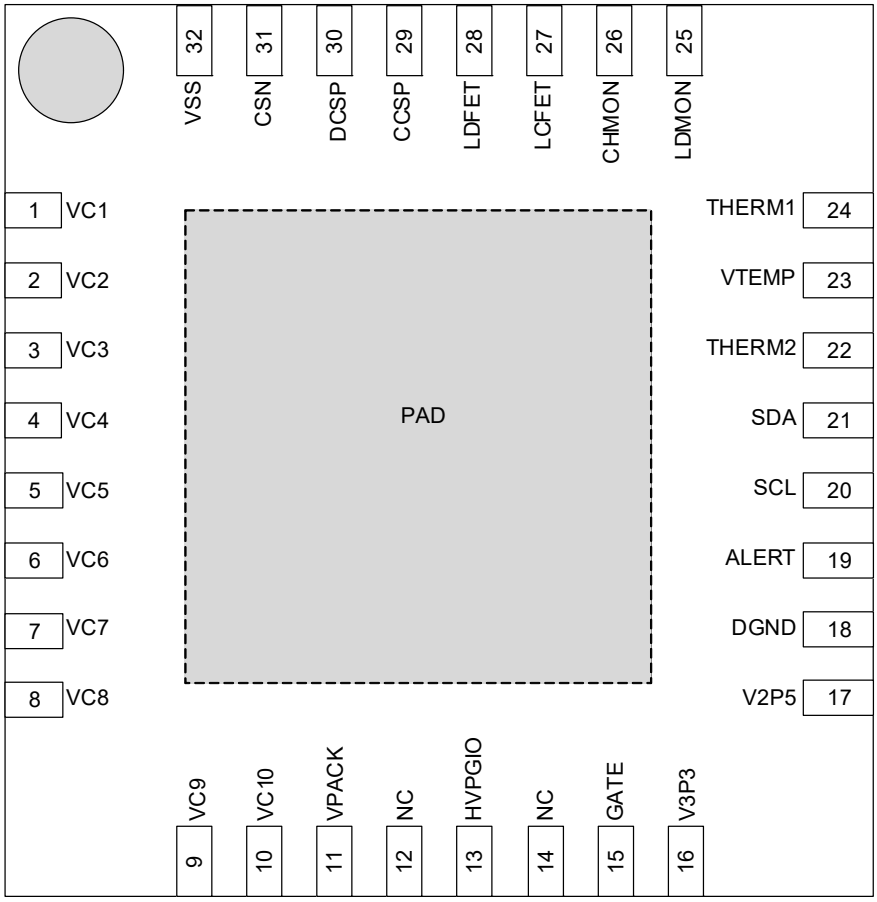


Figure 2. RAA489220 Block Diagram

2. Pin Information

2.1 Pin Configuration



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10	VCn (n = 1 to 10)	**Battery cell voltage inputs.** For applications with a 10-cell battery string, where cell number 1 connects to the lowest voltage and cell number 10 connects to the highest voltage, VCn connects to the positive terminal of cell n. The negative terminal of cell n connects to VC n-1. All connections from cell to pin are made as a Kelvin sense route and through a low-pass filter network (VC10 connects only to the positive terminal of Cell 10).
11	VPACK	**VPACK Pin.** Connect this pin to the pack voltage. A voltage at this pin powers the IC. Connect a minimum of 10µF capacitor from pin to VSS.
12, 14	NC	No Connected
13	HVGPIO	**High Voltage GPIO Pin.** The function of the pin can be configurable as a secondary alert or as a high voltage GPIO.
15	GATE	**Regulator Feedback Pin.** Connect this pin to the V3P3 pin.
16	V3P3	**3.3V supply voltage input.** Connect directly to the source of the external NMOS FET, Connect a 4.7µF capacitor between this pin and VSS.
17	V2P5	**Internal 2.5v supply decoupling Pin.** Connect a 10µF capacitor between V2P5 and DGND.

Pin Number	Pin Name	Description
18	DGND	Digital Ground.
19	$\overline{\text{ALERT}}$	**$\overline{\text{ALERT}}$ Pin.** The pin is the fault and status indicator for the pack. The Fault and Status bits can change the state of the $\overline{\text{ALERT}}$ pin. The pin is an open-drain NMOS. The pin asserts to the VSS level when an unmasked fault or status bit is set. Otherwise, the pin is in a high impedance state. A pull-up resistor greater than 10kΩ to MCU voltage is typically required.
20	SCL	**Serial Clock Pin.** This pin is the clock signal for the I^2C communication interface. An optional pull-up resistor greater than 4.7kΩ to 3.3V can be attached.
21	SDA	**Serial Data Pin.** This is an open-drain serial data I/O for the I^2C communication interface. A pull-up resistor greater than 4.7kΩ to 3.3V is required.
23	VTEMP	**VTEMP Pin.** Connect this pin to the pull-up resistors of the thermistor circuits.
24	THERM1	**Thermistor Pins.** Connect a thermistor to each of these pins. COTn, CUTn, DOTn, and DUTn thresholds are compared to the measurement of the respective thermistor. Reset the device by connecting the THERM2 pin to V3P3 pin.
22	THERM2	
25	LDMON	**Load Monitor Pin.** When the voltage difference between VPACK and LDMON falls below threshold V_{CHTHR}, the LD PRESI bit transitions from 0 to 1.Connect this pin to the negative load terminal. This pin has an internal pull-down resistor connected to VSS.
26	CHMON	**Charge Monitor Pin.** When the voltage on CHMON pin falls below the V_{CHTHR}, the CH PRESI bit transition from 0 to 1. Connect this pin to the negative charger terminal. The pin could be used as a triggered wakeup. This pin has an internal pull-down resistor and requires an external pull-up resistor to VPACK for some applications.
27	LCFET	**Low-Side Charge FET control Pin.** When the FET Driver is disabled, the pin is resistively connected to VSS. When the FET Driver is enabled, the gate of the power FET is pulled up.
28	LDFET	**Low-Side Discharge FET control Pin.** When the FET Driver is disabled, the pin is resistively connected to VSS. When the FET Driver is enabled, the gate of the power FET is pulled up.
29	CCSP	**Charge Current Sense Positive.** Connect a resistor between this pin and the CSN pin to detect charge current.
30	DCSP	**Discharge Current Sense Positive.** Connect a resistor between this pin and the CSN pin to detect discharge current.
31	CSN	**Current Sense Negative.** Connect this pin to the PCB ground and the negative terminal of the battery pack.
32	VSS	**Analog Ground.** VSS is the negative reference voltage for the chip. In most applications, the pin is connected to GND. This pin also serves as the negative reference pin for cell1 voltage measurement.
	EPAD	**Electrical Pad.** Connect to VSS

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VPACK, CHMON, LDMON, HVGPIO	-0.3	+54	V
LCFET, LDFET	-0.3	VPACK	V
VPACK - LDMON	-0.7	+54	V
VC9, VC10	-0.3	VPACK	V
VC8	-0.3	+50	V
VC7	-0.3	+42.5	V
VC6	-0.3	+36.5	V
VC5	-0.3	+30	V
VC4	-0.3	+25	V
VC3	-0.3	+19	V
VC2	-0.3	+13	V
VC1	-0.3	+6.5	V
VCn - VC(n-1) (n = 2 to 10)	-0.3	6.5	V
DGND	-0.3	0.5	V
V3P3, GATE	-0.3	6.5	V
V2P5	-0.3	2.9	V
CCSP, DCSP, CSN, THERM1,VTEMP, THERM2	-0.3	6.5	V
SDA, SCL, $\overline{\text{ALERT}}$	DGND -0.3	6.5	V
LDMON, CHMON	0	10	mA
$\overline{\text{ALERT}}$, SDA, HVGPIO	-10	0	mA
LCFET, LDFET	0	5	mA

3.2 ESD Ratings

ESD Model/Test	Value	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
32 Ld 4x4 QFN Package	38	2.5

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, VPACK	6	44	V
Ambient Temperature	-40	+85	°C
VCn - VC(n-1) (n = 2 to 10); VC1 - VSS	1.5	4.5	V
CCSP - CSN, DCSP - CSN	-50	50	mV
HVGPIO, LDMON, CHMON	0	VPACK	V
$\overline{\text{ALERT}}$, SDA, SCL	0	3.3	V
THERM1, THERM2	0	1.9	V
VTEMP	2.048		V
V2P5	2.5		V
V3P3, GATE	3.3		V
DGND-VSS, CSN - VSS	-0.1	0.1	V
LDFET	0	10	V

3.5 Electrical Specifications

T_A = +25°C, VPACK = 36V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Supply						
Power-On Reset Voltage at VPACK	V_{PORf}	Falling Edge			5	V
	V_{PORr}	Rising Edge		6	7	V
Power-On Hysteresis	V_{PORhys}			1.8		V
Current Consumed by the IC	I_{VPACK}	SCAN Mode (During Scan), FETS ON		750	980	µA
		IDLE Mode; FETS ON		110	160	µA
		LOW POWER Mode, LP Reg =1		35	55	µA
		LOW POWER Mode, LP Reg = 0		3	8	µA
V_{CELL}						
Cell Measurement Error	V_{CELL_ME}	Cells 1 to 10; T = 0°C to 60°C; V_{CELL} = 1.5V to 4.25V, RS = 1kΩ, CS = 0.1µF, Single Triggered Measure	-16	±5	16	mV
V_{CELL} Leakage Current OFF	V_{Cell_IbOff}		-200		200	nA
V_{CELL} Bias Current ON	V_{Cell_IbOn}			3		µA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CELL} Bias Current Match ON	V_{Cell_Ios}			±0.3		µA
I_{PACK} (xCSP - CSN)						
I_{PACK} Comparison Vos	I_{PACK_VOS}	xCSP = CSN = 0V		110		µV
I_{PACK} Comparison Vos TC	I_{PACK_VOSTC}	xCSP = CSN = 0V		0.3		µV/C
I_{PACK} Bias Current	I_{PACK_LC}		-1.9	-1.7	-0.5	µA
I_{PACK} Bias Current Offset	I_{PACK_IOS}			±500		nA
I_{PACK} Gain Error	I_{PACK_GE}	Vdischarge = 10mV to 50mV; Vcharge = -10mV to -50mV	-3	±0.5	3	%
I_{PACK} Charge Detect (CHRGI)	I_{CHRGI}	Digital Compare (0x012E)		-0.6		mV
I_{PACK} Discharge Detect (DCHRGI)	I_{DCHRGI}	Digital Compare (0x012E)		0.6		mV
I_{PACK} Threshold (xCSP - CSN)						
DSC Hysteresis (DCSP-CSN)	DSC_{Hys}			12		mV
Charge Short-Circuit Voltage Analog Compare Range (CCSP-CSN)	CSC			-200		mV
CSC Hysteresis (CCSP-CSN)	CSC_{Hys}			12		mV
CSC Delay (CCSP-CSN)	CSC_{dly}			0.1		ms
V_{Pack}						
VPACK Attenuation	$V_{PACKAttn}$			40		V/V
VPACK Measurement Error	V_{PACK_ME}	15V < VPACK < 42.5V		±0.5		%
VPACK Measurement Error TC	V_{PACKME_TC}			±100		ppm/°C
V_{TEMP}						
V_{TEMP} Voltage Accuracy		0.5mA load	2.03	2.06	2.09	V
V_{TEMP} Measurement Error	V_{VTEMP_ME}			±4.5		mV
Settling Time for VTEMP before a THERM1, THERM2 measurement	t_{VTEMP}	V_{TEMP} Turn ON to 1st thermistor measurement.		18		ms
V_{TEMP} Threshold						
V_{TEMP} Max Threshold	V_{TEMP_max}	Code > 0x06CC = OWF		2.253		V
V_{TEMP} Min Threshold	V_{TEMP_min}	Code < 0x0533 = OWF		1.843		V
Thermistor						
Thermistor Leakage Current			-1		1	µA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Open-Wire Threshold Code	OW_{VTHERM}	Code greater than 0x0FD7 = OWF		1.9		V
RESET Voltage Threshold (THERM2)	RST_{VTHERM}	Threshold Voltage above V2P5.		0.4		V
RESET time (THERM2)	t_{RESET}	The time the THERM2 pin is above RST_{VTHERM} before the device resets		500		ms
Power-On Reset Startup Time to the completion of the first system scan.	$t_{StartUp}$	VPACK > V_{POR}, RESET falling edge or soft reset or exiting LOW POWER Mode to the first measure command			100	ms
Thermistor Measurement Error	$THERM_{ME}$	VTHERMx = 1V		±4		mV
Internal Over-Temperature Sensor						
Internal Temperature Sensor Output Code		@25C		1577		Bits
Internal Over-Temperature Threshold	IOT	Analog Comparator		100		C
V3P3 Regulator						
Regulation Voltage Accuracy	$V3P3_V$	At V3P3 Pin, 0-5mA load	3.201	3.32	3.399	V
Pin Measurement Error	REG_{ME}			±7.5		mV
V3P3 & V2P5 Thresholds						
V3P3 Overvoltage Threshold	$dV3P3_{OV}$	Digital Comparator (Self Test) (0xBE0)		3.553		V
V3P3 Undervoltage Threshold	$dV3P3_{UV}$	Digital Comparator (Self Test) (0x999)		2.97		V
V3P3 Power-Good OV Threshold	PG_{V3P3_OV}	Analog Comparator		3.8		V
V3P3 Power-Good UV Threshold	PG_{V3P3_UV}	Analog Comparator		2.57		V
V2P5 Overvoltage Threshold	$dV2P5_{OV}$	Digital Comparator (Self Test) (0x8BD)		2.75		V
V2P5 Undervoltage Threshold	$dV2P5_{UV}$	Digital Comparator (Self Test) (0x6CA)		2.25		V
V2P5 Power-Good OV Threshold	PG_{V2P5_OV}	Analog Comparator		2.8		V
V2P5 Power-Good UV Threshold	PG_{V2P5_UV}	Analog Comparator		2.0		V
Low-Side FET Drivers (LCFET and LDFET)						
Pull-Up Voltage	$LxFET_{GV}$	LxFET En = 1, VPACK >11V	9	10.5	12	V
		LxFET En = 1, VPACK <11V		VPACK - 1.5V		V
LxFET Pull-Up Resistance	R_{LxFET}	LxFET En = 1		6		kΩ

T_A = +25°C, VPACK = 36V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
LCFET Pull-Down Resistance	R_{LCFET}	First 500µs after LCFET_EN = 0 (to VSS)		2.3		kΩ
LCFET Off-Resistance	R_{LCFET_OFF}	Beyond 500µs after LCFET En = 0		1		MΩ
LDFET Pull-Down to VSS Resistance	R_{LDFET}			2.5		kΩ
LxFET Input Low Threshold (Status)	$LxFET_{VIL}$	LxFET - VSS (Pin Voltage, Falling Edge)		1.62		V
LxFET Input Hysteresis (Status)	$LxFET_{HY}$			350		mV
Charge Detection Monitor (CHMON)						
Charge Detection Threshold	V_{CHTHR}	Falling Edge, V_{CHMON} - V_{SS}	0.8	1.2	1.6	V
Charge Detection Hysteresis	V_{CHHys}			100		mV
CHMON Detection Current	CH_{DC}	CHMON ON (>3V), into pin		3		µA
CHMON Pin Internal Pull-Down	R_{CHPD}	0V to VPACK; CHMON OFF		15		MΩ
Charge Monitor Debounce	t_{CHdb}	The time the pin is in a state before the device reacts		4		ms
CHMON Enable Delay Time	t_{CHEN}	FET(s) off to CHMON Detect		100		ms
Load Detection Monitor (LDMON)						
Load Detection Threshold	V_{LDThr}	Rising Edge, VPACK - V_{LDMON}	0.9	1.5	1.8	V
Load Detection Hysteresis	V_{LDHys}			100		mV
LDMON Pull-down Resistance	R_{LDPD}	From LDMON to VSS	0.7	1	1.2	MΩ
LDMON Enable Delay Time	t_{LDEN}	FET(s) off to LDMON Detect		100		ms
Open-Wire						
Open-Wire Current	CUR_{OW}	From VC pin to VSS		275		µA
Open-Wire Detection Time	t_{OWON}	Open-wire current source on-time		15		ms
Open-Wire ADC read time		Reference to OW Assertion. Time to first compare		10		ms
Detection Threshold (Cells)	V_{OWth1}	All VCells (ADC code 0x0058)		0.6		V
Detection Threshold (VSS)	V_{OWth3}	VSS - VC1		0.25		V
Detection Threshold (VPACK)	V_{OWth2}	VC10 - VPACK		0.5		V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System						
4MHz Oscillator Accuracy			-7.5		7.5	%
31.5kHz Oscillator Accuracy			-25		25	%
$\overline{\text{ALERT}}$						
$\overline{\text{ALERT}}$ Low-Level Output Voltage	AT_{VOL}	I_{sink} = 2mA		0.25	0.6	V
$\overline{\text{ALERT}}$ Low-Level Input Voltage	AT_{VIL}		0		0.8	V
$\overline{\text{ALERT}}$ Leakage Current	AT_{LIH}	$\overline{\text{ALERT}}$ = 0V to 3.3V	-1	±0.25	1	µA
HVGPIO						
HVGPIO Low-Level Output Voltage	$HVGPIO_{VOL}$	I_{sink} = 2mA;		0.1	0.6	V
HVGPIO Low-Level Input Voltage	$HVGPIO_{VIL}$		0		0.8	V
HVGPIO Leakage Current	$HVGPIO_{LIH}$	HVGPIO = VPACK			1	µA
I^2C Interface Specifications						
SDA and SCL Input Buffer LOW Voltage	V_{IL}		-0.3		0.3×V3p3	V
SDA and SCL Input Buffer HIGH Voltage	V_{IH}		$0.7 \times V_{3p3}$		V_{3p3}+0.3	V
SDA and SCL Input Buffer Hysteresis	$I2C_{Hysteresis}$			$0.05 \times V_{3p3}$		V
SDA Output Buffer LOW Voltage	V_{OL}	Sinking 2mA	0	0.25	0.6	V
Pin Leakage Current for SDA and SCL Pins	I_{leak}		-1		1	µA
SCL Frequency	f_{SCL}				400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the max spec is suppressed			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300			ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{DD} crossing	1300			ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{DD} crossing	600			ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SDA Low Timeout I^2C communication is reset bus released	$t_{TIMEOUT}$		25	32		ms
8th Bit to ACK Bit Delay (Applies to reading ADC Output Data Only)	$I^2C\_t_{WAIT}$	Time between the rising edge of the clock pulse corresponding to the last bit of any byte, and the falling edge of the clock pulse corresponding to the Acknowledge bit	7			µs
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	20		900	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600	17		ns
STOP Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	600	45		ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0	150		ns
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{DD}	20+0.1x Cb		300	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{DD}	20+0.1x Cb		300	ns

4. Typical Performance Curves

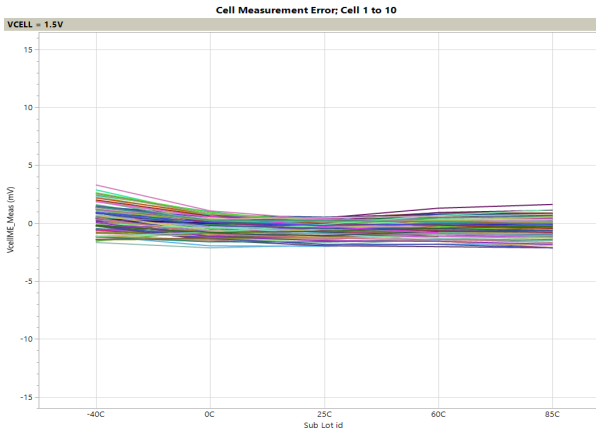


Figure 3. Average Cell ME at 1.5V

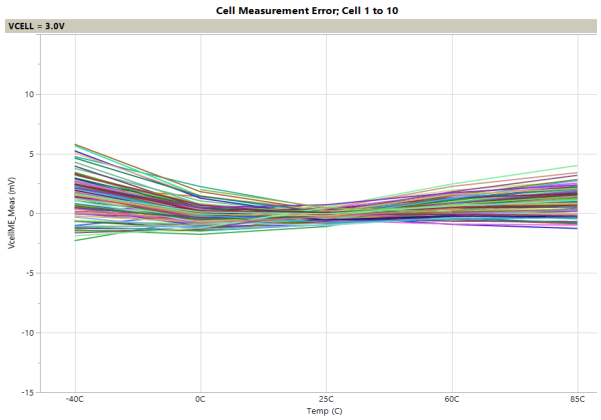


Figure 4. Average Cell ME at 3.0V

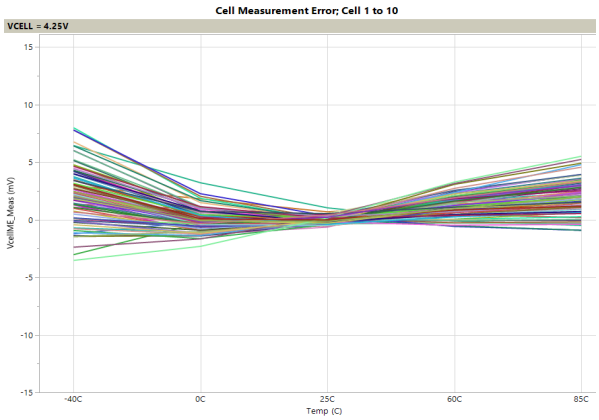


Figure 5. Average Cell ME at 4.25V

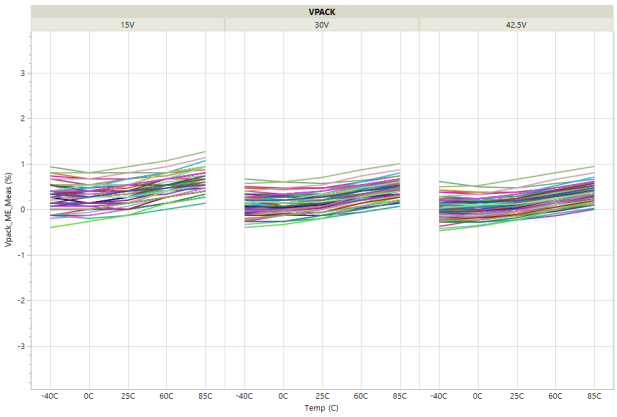


Figure 6. VPACK Pin Voltage ME

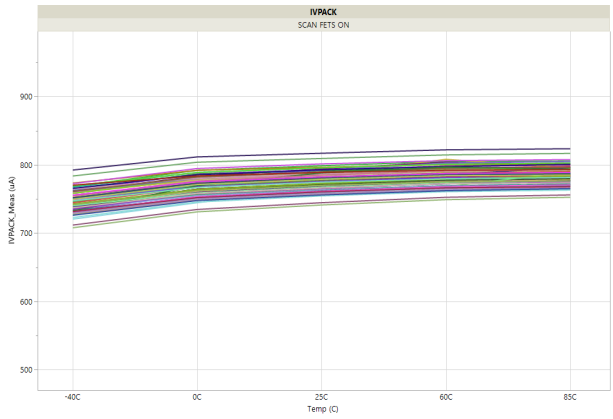


Figure 7. VPACK Current (SCAN, FETS on)

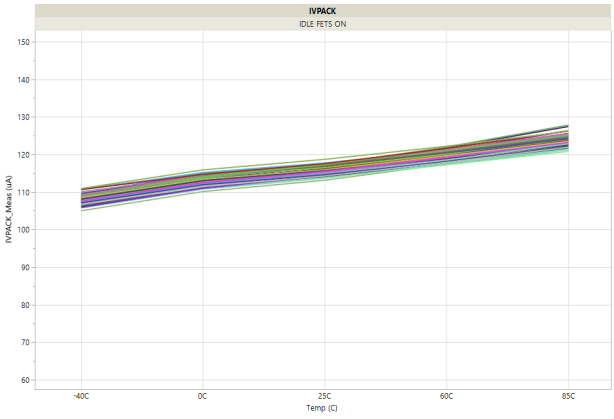


Figure 8. VPACK Current (IDLE, FETS on)

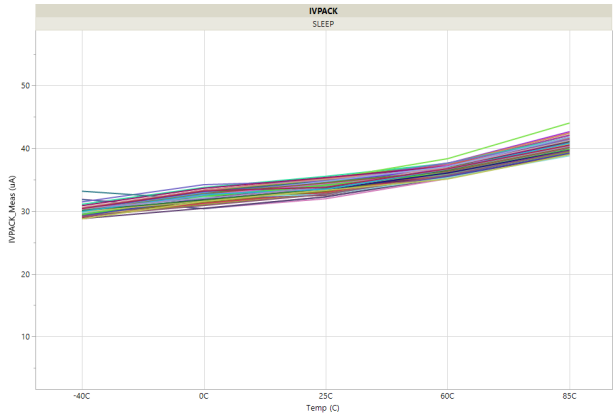


Figure 9. VPACK Current (SLEEP)

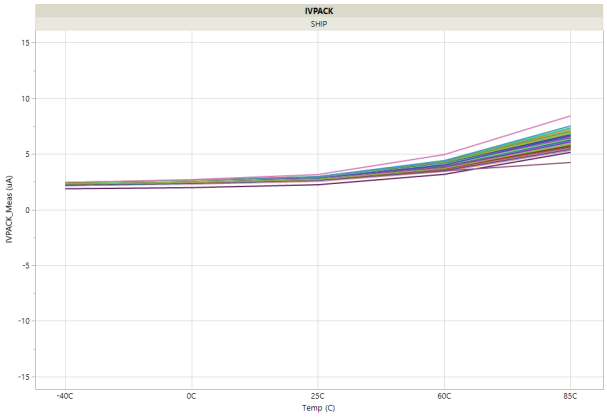


Figure 10. VPACK Current (SHIP)

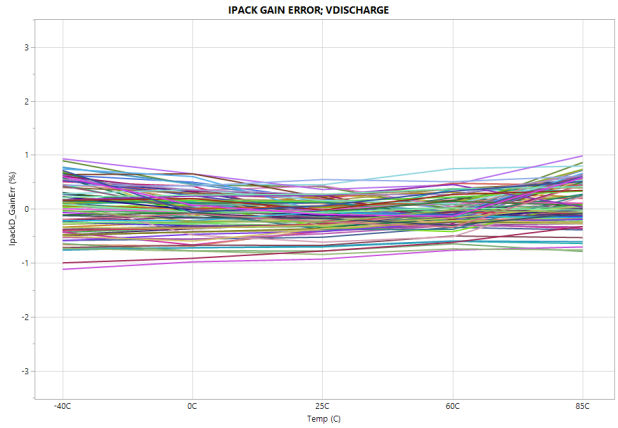


Figure 11. Discharge Current GE

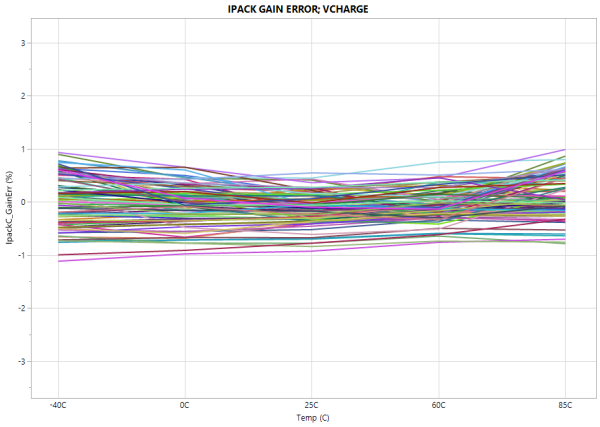


Figure 12. Charge Current GE

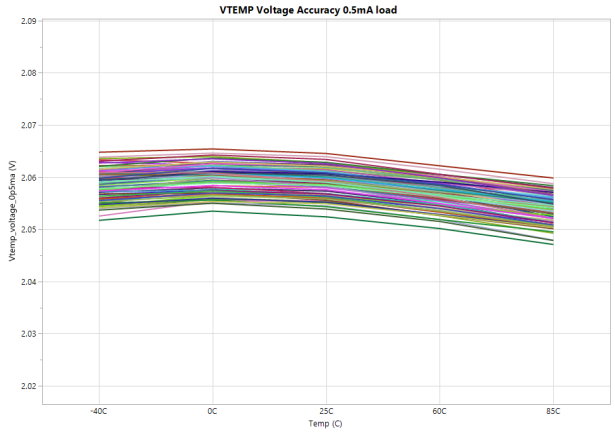


Figure 13. VTEMP Pin Voltage

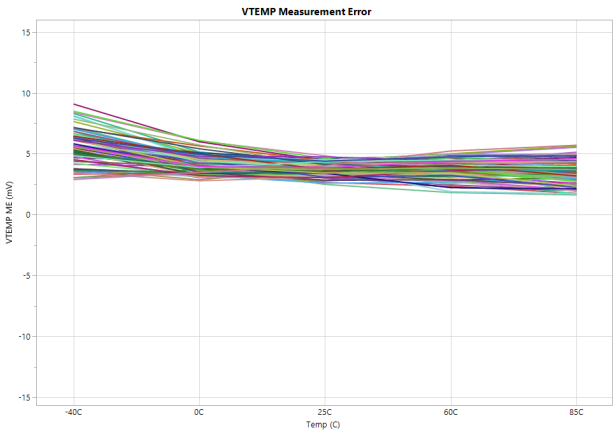


Figure 14. VTEMP Pin Voltage ME

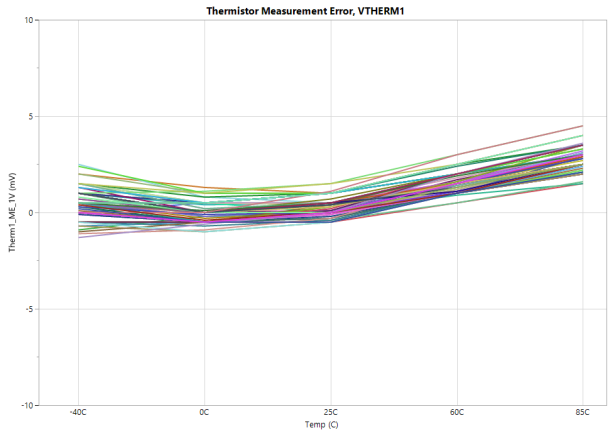


Figure 15. THERM1 Pin Voltage ME

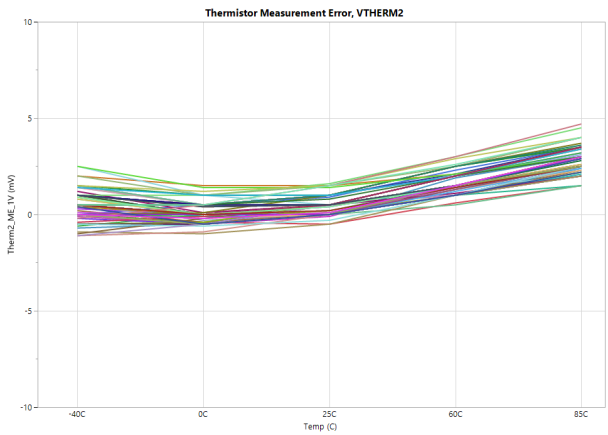


Figure 16. THERM2 Pin Voltage ME

5. State Machine Overview

The State Machine flow diagram is illustrated in Figure 17. This diagram shows the relationships between the device States and Modes. A State executes its function and then moves to the next state or Mode, while Modes can loop or remain static until another function or status change forces a transition out of the Mode.

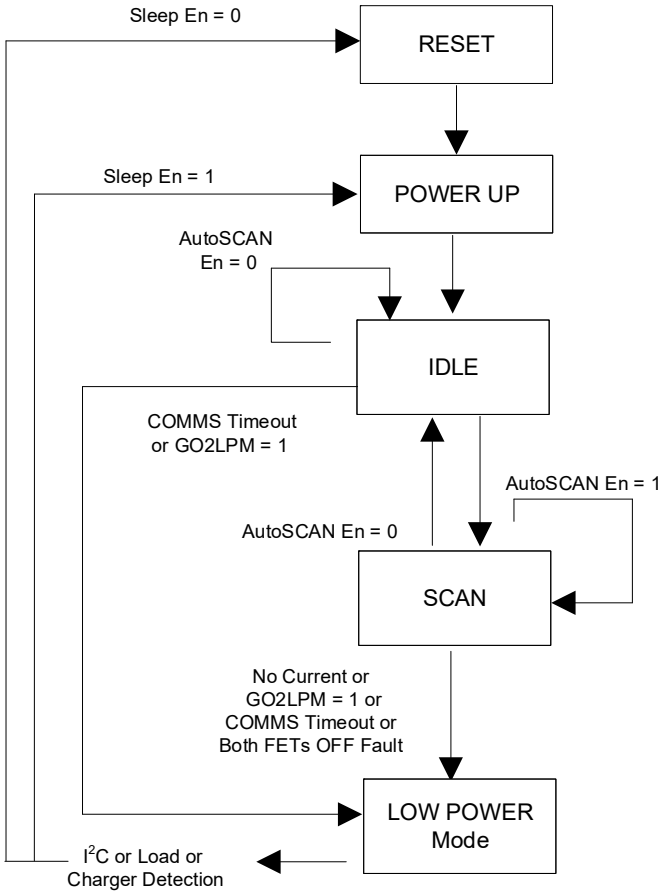


Figure 17. State Machine Flow Diagram

5.1 Reset State

At initial device power-up, the RAA489220 enters the RESET State. This state has the highest priority and is initiated by a momentary connection of the THERM2 pin to the V3P3 pin (Hard RESET) or a VPACK voltage lower than V_{POR} (page 8) or the V2P5 or V3P3 voltages (page 10) falling below their Power On Reset (POR) thresholds. A RESET interrupts any action the device is performing. Entering the RESET State also occurs when exiting the LOW POWER Mode if the bit 0x80.7 Sleep En is clear or from a Soft RESET (0x40.7 Soft Reset).

The device turns off all regulators and oscillators when entering this state from a Hard RESET or Soft RESET. On completion of RESET, the device transitions to the Power Up State.

5.2 Power Up State

The Power Up State is entered from the RESET State, or LOW POWER Mode if the bit 0x80.7 Sleep En is set. This state prepares the device for normal operation by executing device initialization followed by a self test that checks the status of the IC.

The device turns on and checks the 4MHz oscillator and initializes logic states. It then reads trim/fuse settings, checks for pin faults, powers the monitor pins, powers the analog comparators and measurement amps, and enables the FET driver and the ADC. Any faults detected in the Power Up State, set the bit 0x10.10 STF and force the device to transition to LOW POWER Mode.

When successful completion of initialization and self test (no faults that force both power FETs to turn OFF) occurs, the device transitions to IDLE Mode.

5.3 IDLE Mode

By default the MCU is in control of the system with the device in IDLE Mode (bit 0x80.8 AutoSCAN En is clear unless otherwise noted). The MCU is responsible for triggering device measurements, enabling/disabling the power FETs and fault reaction. Faults detected in this state do not automatically turn off the power FETs, except for short-circuit detections.

In IDLE Mode, the device executes commands from the MCU. The MCU is responsible for the state of the power FETs and acting on faults or status changes. Section Fault Detection and Recovery lists the analog and digital faults. The $\overline{\text{ALERT}}$ pin asserts for faults and can assert for status bits provided the respective mask bit is cleared (see 0x81 OV and EOC Thresholds).

Communication timeout in IDLE Mode is controlled by bits 0x80.[14:13] Communication TO. If the SDA pin does not make a high to low transition while the SCL pin is high within the selected period of time, the device transitions to LOW POWER Mode. Setting bit 0x40.5 Go2LPM to 1 also transitions the device to LP Mode.

Executing 0x41.7 Trigger Measurement causes a temporary transition to SCAN Mode to execute the 0x41.[4:0] Measurement Selection. When completed, the device transitions back to IDLE Mode to await the next MCU instruction.

Setting bit 0x80.8 AutoSCAN En to 1 causes the device to transition to SCAN Mode. Renesas recommends setting 0x40.6 Clear All Faults to 1 before enabling AutoSCAN to initialize counters to 0.

5.4 SCAN Mode

SCAN Mode operation is dependent on the setting of the AutoSCAN Enable bit. If the bit is clear (default), the device enters SCAN from IDLE when a measurement is triggered, and remains in SCAN Mode until the triggered measurement completes, then it transitions back to IDLE. If the AutoSCAN Enable bit is set to 1, the device continuously loops through the system scan sequence (Figure 18) and remains in SCAN Mode. The only exceptions to these two cases is a fault or Go2LPM instruction, which causes a transition to LP Mode.

In SCAN Mode with AutoSCAN enabled, the device continuously performs a scan sequence that measures the pack current, pack and cell voltages during each scan (Normal Loop). Every four scans, the thermistor voltages are measured. Every 100 scans, a series of self tests are executed. Measurement results are compared to the

relevant thresholds during each scan they are executed. If the pack current is too low to register either a 0x11.0 CHRGI or 0x11.1 DCHRGI for more than six complete system scans, the device transitions to LP Mode.

If a fault is detected during AutoSCAN that requires both power FETs to turn OFF, the device asserts the $\overline{\text{ALERT}}$ pin to signal the MCU to read the fault and status registers, then transitions to LP Mode after a 100ms delay. During the transition, no other functions are allowed.

After exiting LP back to IDLE Mode, the MCU should issue a 0x40.6 Clear All Faults to initialize counters to 0.

Communications Timeout is active in both IDLE and SCAN Modes. The MCU has to initiate communication with the device within the selected time period (0x80.[14:13] Communication TO). Allowing the communication timer to expire causes a transition from IDLE or SCAN to LOW POWER Mode.

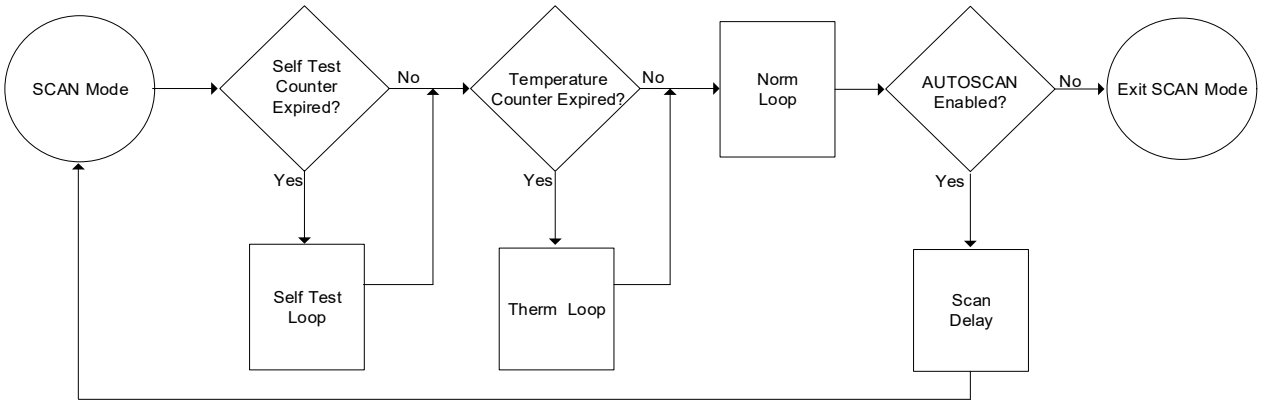


Figure 18. System Scan Sequence

5.5 LOW POWER Mode

The RAA489220 consumes the lowest current in LOW POWER (LP) Mode. Power FETs and non-essential circuitry are OFF. In LP Mode, the device waits for a 0x11.3 CH PRESI or 0x11.2 LD PRESI bit transition from low to high to exit. Asserting the SDA pin while the SCL pin is high also exits this state.

The device transitions to LP Mode when any faults that require both power FETs to turn OFF, when a communication timeout occurs, when the bit 0x40.5 Go2LPM is set to 1, or if a sufficient number of scans with no current flow is detected.

Entry into LP Mode turns off both power FETs and stops the communication timeout timer. The $\overline{\text{ALERT}}$ pin is asserted, and then the state does nothing for 100ms before proceeding to turn OFF the remainder of the sub blocks. The 100ms time delay allows the MCU to read the fault and status registers and prepare itself for LP Mode. No other functions are allowed during this 100ms.

Two bits control power dissipation during and status on exit from LP Mode. The regulator has two possible settings in this Mode (see 0x42.13 LP Regulator) one keeps it fully enabled, and the other reduces current consumption to a minimum. The 0x80.7 Sleep En determines if register settings are retained in LP Mode and which state the device exits to. The lowest powered state of the device is selected by setting both LP Reg and Sleep En bits to 0, see Table 1.

When the Sleep En bit is set to 0, the register values are not retained in LP Mode, and the device exits to the RESET state. If the Sleep En bit is set to 1, the register values are retained in LP Mode, and the device exits to the Power Up state. If the LP Reg bit is clear, only the weak regulator is enabled, so register values may or may not be retained.

After exiting LOW POWER back to IDLE Mode, the MCU should issue a 0x40.6 Clear All Faults to initialize counters to 0.

Table 1. LP Mode Settings

LP REG (0x42.13)	Sleep En (0x80.7)	Result
0	0	Lowest Power, Weak Regulators; Register values are not retained
0	1	Weak Regulators; Register values may or may not be retained
1	0	Strong Regulator; Register values are not retained
1	1	Strong Regulator; Register and counter values are retained; VTEMP can be Active

6. FAULTS

6.1 Fault Detection and Recovery

A fault is reported when the related fault threshold is exceeded for consecutive readings. For digital comparisons fault delay is implemented with counters that are incremented for consecutive faulty readings; for analog comparisons, fault delay is accomplished with timers. These counters/timers are cleared if the fault condition clears before they reach their limit(s).

A counter is incremented each time the device detects a fault while in SCAN Mode. If the fault counter exceeds the threshold, the device sets the respective fault bit and then transitions to LP Mode.

When an analog comparison threshold is exceeded a timer is started. If the timer also exceeds its threshold, the device sets the respective fault bit and then transitions to LP Mode.

When a fault is reported, action is taken to turn OFF the respective FET(s). Table 2, Table 4, and Table 5 show the power FET action related to specific fault conditions. These tables list the number of consecutive faults required before setting the fault bit.

Faults that only turn OFF one power FET have recovery thresholds. Recovery thresholds are compared to the most recent measurement as long as the fault is present. Cell over/undervoltage, and charge over/under-temperature faults have separate recovery thresholds. The recovery threshold is fixed relative to the fault detection threshold voltage plus/minus a hysteresis. Overvoltage and charge over-temperature recovery thresholds are defined as the original threshold minus the respective hysteresis threshold. Under-temperature and undervoltage recovery thresholds are defined as the original threshold value plus the respective hysteresis value. If a measurement parameter does not have a recovery threshold, the fault detection threshold is also used for the recovery limit.

If a fault detection occurs during a thermistor, cell voltage, or pack current measurement as part of a system scan, the device completes the scan before dropping to LP Mode.

During the first and every 100th scan that follows, the Self Test Loop is executed. A Self Test fault (0x10.10 STF) requires two consecutive detections to set. The device executes the Self Test Loop twice to determine if a fault is present. If a fault is present with each check, the fault is set and the device transition to LP Mode.

6.2 Power FET Fault Response

The following tables show the FET reaction for each specific fault. Table 2 details the fault response for Self Test (if enabled) digital compare faults that have no dependency on the power FET configuration bit 0x82.7 CPWR. Digital Compares occur following a measurement while in Scan Mode and require consecutive violations to set the fault bit. Table 3 details the fault response for analog compare faults that have no dependency on the CPWR bit. Analog compares do not require measurements and include debounce timers.

Table 2. Self Test Fault Response

FAULT (Fault Flag)	FET State		Compare Type	Seq Count	Comments
	CFET	DFET			
V3P3 (REGF)	Off	Off	Digital	2	Device controls FETs only in AutoSCAN Mode
V2P5 (REGF)	Off	Off	Digital	2	
VBG2 (REGF)	Off	Off	Digital	2	
OWF	Off	Off	Digital	2	
VTMPF	Off	Off	Digital	2	
OW THERM	Off	Off	Digital	2	

Table 3. Analog Fault Response

FAULT (Flag)	FET State		Compare Type	Time Base	Debounce Rise/Fall Time (ms)	Comments
	CFET	DFET				
Oscillator, VPACK & VSS OW (STF)	Off	Off	Analog	No	0.5	Device controls FETs in SCAN and IDLE Modes. An STF, COMMTO or SCF disables the FETs and forces a transition to Low-Power Mode.
COMMTO	Off	Off	Timer	Yes	0x80.[13:12]	
DSCF (SCF)	Off	Off	Analog	No	0x83.[15:14]	
CSCF (SCF)	Off	Off	Analog	No	0.1/ 0.1	
V3P3F	Off	Off	Analog	No	1/1	A low level detection sets state machine to WAIT Device controls FETs in SCAN and IDLE Modes
V2P5	Off	Off	Analog	No	1/0.002	A low level detection triggers POR
IOTF	Off	Off	Analog	No	1/ 1	Device controls FETs in SCAN and IDLE Modes

The power FET fault response for the parallel FET configuration setting (CPWR = 1) is shown in Table 4.

The power FET fault response for the series FET configuration setting (CPWR = 0) is shown in Table 5.

The RAA489220 controls the FETs when bit 0x80.8 AutoSCAN En is enabled for CPWR dependent faults; otherwise, the MCU is expected to control the power FETs in IDLE Mode.

Table 4. Parallel FET Digital Fault Response

CPWR = 1	Power FET State		Delay Time(s)	Number Of Faults	Comments
FAULT (Flag)	CFET	DFET			
DOT (OTF)	Off	Off	0x80.[10:9] Fault Delay	2	CPWR=1 FET Fault response is not dependent on current direction bits
COT (OTF)	Off	On	0x80.[12:11] Scan Delay	2	
CUT (UTF)	Off	On	0x80.[12:11] Scan Delay	2	
DUT (UTF)	Off	Off	0x80.[10:9] Fault Delay	2	
OVLO (OVF)	Off	Off	0x80.[10:9] Fault Delay	2	
OV (OVF)	Off	On	0x80.[12:11] Scan Delay	2	
UV (UVF)	On	Off	0x80.[12:11] Scan Delay	2	
UVLO (UVF)	Off	Off	0x80.[10:9] Fault Delay	2	
DCVF	Off	Off	0x80.[10:9] Fault Delay	8	
IEOC	Off	On	0x80.[12:11] Scan Delay	2	
DOCF	Off	Off	0x80.[12:11] Scan Delay	8	
COCF	OFF	OFF	0x80.[12:11] Scan Delay	8	

Table 5. Series FET Digital Fault Response

CPWR = 0	Current Direction		FET State		Delay Time(s)	Number Of Faults	Comments
FAULT (Flag)	CHRGI	DCHRGI	CFET	DFET			
DOT (OTF)	X	X	Off	Off	0x80.[10:9] Fault Delay	2	
COT (OTF)	0	1	On	On	N/A	N/A	FETs remain on as long as a discharge current is detected (0x11.1 DCHRGI).
COT (OTF)	X	0	Off	On	0x80.[12:11] Scan Delay	2	
CUT (UTF)	0	1	On	On	N/A	N/A	
CUT (UTF)	X	0	Off	On	0x80.[12:11] Scan Delay	2	
DUT (UTF)	X	X	Off	Off	0x80.[10:9] Fault Delay	2	
OVLO (OVF & LOF)	X	X	Off	Off	0x80.[10:9] Fault Delay	2	
OV (OVF)	0	1	On	On	N/A	N/A	FETs remain on as long as a discharge current is detected (0x11.1 DCHRGI).
OV (OVF)	X	0	Off	On	0x80.[12:11] Scan Delay	2	
UV (UVF)	1	0	On	On	N/A	N/A	FETs remain on as long as a charge current is detected (0x11.0 CHRGI).
UV (UVF)	0	X	On	Off	0x80.[12:11] Scan Delay	2	
UVLO (UVF & LOF)	X	X	Off	Off	0x80.[10:9] Fault Delay	2	
DCVF	X	X	Off	Off	0x80.[10:9] Fault Delay	8	
IEOC	X	X	Off	Off	0x80.[12:11] Scan Delay	2	
DOCF	X	1	Off	Off	0x80.[12:11] Scan Delay	8	
COCF	1	X	Off	Off	0x80.[12:11] Scan Delay	8	

7. System Registers

Table 6. System Register List

Addr (Hex)	Register Name	Pg#	Register Description[1]	Default (Hex)
Measurement Results (RO)				
00	Pack Voltage	24	[11:0] Step: 20mV; Range: 5.12V to 46.08V (Code 0x200 to 0xA00)	0000
01	Cell Max Voltage	24	[11:0] Step: 1mV; Range: 0.512V to 4.608V	0000
02	Cell Min Voltage	24	[11:0] Step: 1mV; Range: 0.512V to 4.608V	0000
03	Thermistor 1	24	[11:0] Step 0.5mV; Range -0.128V to 1.92V	0000
04	Thermistor 2	24	[11:0] Step 0.5mV; Range -0.128V to 1.92V	0000
05	Discharge Current	24	[11:0] Step 13.16µV; Range -3.368mV to 50.52mV	0000
06	Charge Current	24	[11:0] Step 13.16µV; Range -50.52mV to 3.368mV	0000
Faults And Status				
10	Faults (**RO**)	27	[15] REGF [14] OWF [13] IOTF [12] VTMPF [11] LOF [10] STF [9] RSV [8] COMMTO [7] DCVF [6] OVF [5] UVF [4] OTF [3] UTF [2] SCF [1] DOCF [0] COCF	0000
11	Masks & Status ([15:8] **R/W**; [7:0] **RO**)	31	[15] Busy Mask [14] HVGPIO Mask [13] V/IEOC Mask [12] RSV [11] LD/CH PRESI Mask [10:9] RSV [8] V3P3OK [7] Busy [6] VTEMP [5] VEOC [4] IEOC [3] CH PRESI [2] LD PRESI [1] DCHRGI [0] CHRGI	FE00
Set Up				

Table 6. System Register List (Cont.)

Addr (Hex)	Register Name	Pg#	Register Description[1]	Default (Hex)
40	System Config 1 ([15:8] **RO**; [7:0] **R/W**)	34	[15:12] RSV [11] HVGPIO Status 1 - High (>VIL), 0 - Low (< VIL) [10] $\overline{\text{ALERT}}$ Pin Status 0 - High (>VIL), 1 - Low (<VIL) [9] LDFET Pin Status 1- LDFET Hi, 0 - LDFET Low [8] LCFET Pin Status 1- LCFET Hi, 0 - LCFET Low [7] Soft Reset, 0 - **No Action**, 1 - Reset [6] Clear All Faults 0 - **No Action**, 1 - clear All Faults and Counters [5] GO2LPM, 0 - **No Action**, 1 - Transition to the Fault state [4] RSV [3] HVGPIO Pin Assert 1 - Assert Pin, **0 - De-assert** [2] $\overline{\text{ALERT}}$ Pin Assert 1 - Assert Pin, **0 - De-assert** [1] LDFET En 1 - LDFET ON, **0 - LDFET OFF** [0] LCFET En 1 - LCFET ON, **0 - LCFET OFF**	0000
41	Measure Select ([15:8] **RO**; [7:0] **R/W**)	35	[15] Busy Measuring, 1- Busy 0 - **No Action** [14:8] RSV [7] Trigger Measurement, 1- Trigger 0 - **No Action** [4:0] Measurement Select;	0000
42	System Config 2 (**R/W**)	37	[15] VTEMP OFF/ON: **0 - OFF**, 1 - ON [14] Self Test En: 0 - Disable, **1 - Enable** [13] LP Reg - **0 - Weak Regulator**, 1 -Strong Regulator [9:0] Cell Current Source 1 - ON, **0 - OFF**	4000
Thresholds (R/W with Key)				
80	System Config 3	38	[15] OW En Cells; 0- Disable, 1 - **Enable** [14:13] Comm Timeout 00- OFF, 01- 0.1s, 10- 1s, **11- 5s** [12:11] Scan Delay 00 -0s, 01 - **0.1s**, 10 - 1s, 11 - 5s [10:9] Fault Delay 00 -0s, 01 - **0.1s**, 10 - 0.5s, 11 - 1s [8] AutoSCAN En; **0 - Disable**, 1 - Enable [7] Sleep En; 0- Disable, **1 - Enable** [6:0] Product Id	EAA0
81	OV & EOC	39	[15:9]OV: Step 10mV; 3.23V to 4.5V; Default **4.25V**; [8:7] IEOC; 00- **0.65mV**, 01 - 0.7mV, 10- 1mV, 11 - 3mV [6:4] OV Hysteresis Range: -25mV to -400mV Default **-100mV** [3:0] OVLO Step 100mV; 3.0V to 4.5V Default **4.3V**	CC2D
82	DV_{CELL} OV & UV	41	[15:12] DVCell OV; Step 100mV; Range 500mV to 2V; Default: **500mV** [11:8] UV Step 100mV; Range 1.5V to 3.0V Default **2.7V** [7] CPWR: 0 - **Serial Power FET Config**, 1 - Parallel Power FET Config [6:4] UV Hysteresis Step 100mV; Range 100mV to 800mV; Default **300mV** [3:0] UVLO: Step 100mV 1.5V to 3.0V Default **2.0V**	0C25
83	SCC, OT & UT	42	[15:14] SCC Delay: 00-OFF, 01- 0.1ms, 10 -**1ms**, 11-10ms [13:11] DOT [10:8] DUT [7:6] Therm Enable (Off/THERM1/ **Both** / RSV) [5:3] COT [2:0] CUT	98B4

Table 6. System Register List (Cont.)

Addr (Hex)	Register Name	Pg#	Register Description[1]	Default (Hex)
84	Current	45	[15] DOC/COC Delay Time 0 - use Scan Delay time, 1- **use Fault Delay time** [14:12] SCC 000- RSV, 001-25mV, 010- 50mV, 011- 100mV, **100 - 200mV** [11:6] DOC step 1mV: 1mV to 51mV; Default **50mV** [5:0] COC step 1mV: 1mV to 51mV Default **50mV**	CC71
Product Information (Read Only Bits)				
FD	Die Revision		[3:0] Die Revision	0003
FE	Manufacturing ID		[7:0] Manufacturing ID	0049
FF	Device ID		[7:0] Device ID	0010

1. Bold text indicates default value.

Table 7. Command Codes

Reg Addr	Register Name	Pg#	Register Description	Bytes
C1	Fault and Status	50	Read Fault and Status registers	3 + 4
C2	Read Measurements		Read VPACK, Cell Max, Cell Min, THERM1, THERM2, DISCHARGE, CHARGE registers	3 + 14
C3	I_{PACK}		Read DISCHARGE and CHARGE registers	3 + 4

7.1 Calculating Thresholds and Readings

7.1.1 Measurement Reads

The RAA489220 stores the results of seven measurements (V_{CELL} Max, V_{CELL} Min, VPACK, I_{PACK} Discharge, I_{PACK} Charge, THERM1, and THERM2) with every complete scan sequence. Additional measurements are accessible by executing a single triggered scan (0x41.[4:0] Measurement Selection).

Table 8. Measurement Registers

Register Name	Bit Function								Default Value (Hex)
	7 (MSB)	6	5	4	3	2	1	0 (LSB)	
Measurement (Upper Byte)	RSV	RSV	RSV	RSV	Bit11	Bit10	Bit9	Bit8	00
Measurement (Lower Byte)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00

Use Equation 1 to calculate the decimal result from the register value.

(EQ. 1) $$MEAS = (RegVal) \cdot MEAS_{Step} + 0.5 \cdot MEAS_{Step} + MEAS_{Min}$$

Table 9 shows the constants used in Equation 1 to calculate the voltage for each of the 10 possible measurement result types.

Table 9. Measurement Constants

Measured Parameter	Electrical Spec pg#	Coefficients		Max Val ADC Code 0xFFF	Min Val ADC Code 0x000	Units	Comments
		$MEAS_{Step}$	$MEAS_{Min}$				
VPACK	9	0.02	-5.12	76.79	-5.11	V	Usable range are codes 5.12V (0x200) to 46.08V (0xA00)
V_{CELL}	8	0.001	0.512	4.6085	0.5125	V	
Thermistors (1 & 2)	9	0.0005	-0.128	1.92025	-0.12775	V	Usable range begins at 0V (0x100)
I_{PACK}	9	0.0132	-3.368	±50.5266	-3.3614	mV	Usable range begins at D/CHRGI Thresholds = ±200µV (0x110)
DV_{CELL}	8	0.001	0	4.608	0	V	Do not include 0.5 $Meas_{step}$ in calculation equation.
VTEMP	9	0.001	0.512	4.6085	0.5125	V	
V3P3	10	0.001	0.512	4.6085	0.5125	V	
V2P5	10	0.001	0.512	4.6085	0.5125	V	

7.1.1.1 Internal Temperature

The Internal temperature sensor is not calibrated and is only intended for comparisons to the internal over-temperature fault threshold. This sets bit 0x10.13 IOTF to shutdown the device at extreme high temperatures. The sensor is not provided to indicate die temperature significantly below the IOTF threshold.

7.1.2 Digital Thresholds

Digital Thresholds are compared to the relevant ADC measurement results during a Single System Scan (0x41.[4:0] Measurement Selection) executed in IDLE Mode, and set the related fault bit if a threshold is violated, but do not shut off the power FETs. Threshold violations in AutoSCAN (0x80.8 AutoSCAN En) can shut off the power FETs in specific cases. The power FET response and the conditions required to set the fault are found in Fault Detection and Recovery.

The faults related to these thresholds are automatically cleared when a subsequent measurement indicates the voltage has moved to within the allowed range determined by the threshold combined with its hysteresis. See Recovery Threshold for more information.

7.1.2.1 V_{CELL} Thresholds

The RAA489220 has programmable thresholds to monitor cell voltages. Cell Overvoltage Lockout (0x81.[3:0] V_{CELL} OVLO), Cell Overvoltage (0x81.[15:9] V_{CELL} OV), Cell Undervoltage (0x82.[11:8] V_{CELL} UV), Cell Undervoltage Lockout (0x82.[3:0] V_{CELL} UVLO), and Delta Cell Overvoltage (0x82.[15:12] DV_{CELL} OV) thresholds are digitally compared after every cell voltage measurement. The device has two levels of thresholds for overvoltage and undervoltage detection.

OV and OVLO threshold violations set bit 0x10.6 OVF to 1 when a cell voltage reading is above either threshold. Conversely, UV and UVLO threshold violations set bit 0x10.5 UVF to 1 when a cell voltage reading is below either threshold.

The DV_{CELL} threshold is compared to the difference between the maximum and minimum cell voltages after all cells have been measured. If the maximum cell voltage difference is greater than the threshold, bit 0x10.7 DCVF is set to 1.

7.1.2.2 Temperature Thresholds

Discharge Over-Temperature (0x83.[13:11] DOT), Charge Over-Temperature (0x83.[5:3] COT), Charge Under-Temperature (0x83.[2:0] CUT), and Discharge Under-Temperature (0x83.[10:8] DUT) thresholds are compared to the THERM pin measurements. The thresholds assume a negative temperature coefficient thermistor, see VTEMP and THERM Pins.

The temperature thresholds are digitally compared to each THERM pin measurement. If the voltage measurement at the pin is lower than the threshold, the bit 0x10.4 OTF is set to 1. The under-temperature thresholds operate in a similar manor as the over-temperature thresholds. These thresholds detect when a thermistor voltage is above either threshold, which sets bit 0x10.3 UTF to 1.

If bit 0x11.0 CHRGI is set, the voltages are compared to the Charge thresholds. If bit 0x11.1 DCHRGI is set, the voltages are compared to the discharge thresholds.

7.1.2.3 I_{PACK} Thresholds

The discharge overcurrent threshold (0x84.[11:6] DOC) is digitally compared to the discharge current measurement. Results are greater than this threshold, set bit 0x10.1 DOCF to 1.

The charge overcurrent threshold (0x84.[11:6] DOC) operates in a similar manor as the discharge overcurrent threshold. The device detects when a charge current measurement is below the threshold and sets bit 0x10.0 COCF to 1.

7.1.2.4 Threshold Equations

Use Equation 2 to calculate the decimal threshold value from the digital value.

(EQ. 2) $$THRESHOLD = (RegVal) \cdot THRESHOLD_{Step} + THRESHOLD_{MIN}$$

Use Equation 3 to calculate the digital threshold value from the decimal value.

(EQ. 3) $$REGVal = Integer\left[\frac{(THRESHOLD_{Value} - THRESHOLD_{MIN})}{THRESHOLD_{STEP}}\right]$$

Table 10 lists the constants to be used in Equation 2 and Equation 3 for each threshold.

Table 10. Threshold Constants

Threshold Type	Reg Val Hex	# Of Bits	Coefficients		Max Val ADC Code	Min Val ADC Code	Units
			$Threshold_{Step}$	$Threshold_{Min}$			
OVLO	81.[3:0]	4	0.1	3.0	4.5	3.0	V
OV	81.[15:9]	7	0.01	3.23	4.5	3.23	V
UV	82.[11:8]	4	0.1	1.5	3.0	1.5	V
UVLO	82.[3:0]	4	0.1	1.5	3.0	1.5	V
DVCell	82.[15:12]	4	0.1	0.0	2.0	0.5	V
DOC	84.[11:6]	6	1	-1	51	1	mV
COC	84.[5:0]	6	-1	-1	51	-1	mV

7.1.2.5 Recovery Threshold

Thermistor temperature (COT, CUT), cell overvoltage (OV), and undervoltage (UV) thresholds have recovery threshold hysteresis settings. When a thermistor or cell voltage reading exceeds its respective threshold, the device signals by setting the related fault bit. After detecting the fault, the device compares subsequent readings to the threshold with hysteresis before clearing the fault.

The OV Hysteresis threshold value is used for cell overvoltage recovery and to indicate to a charger when to switch from constant current to constant voltage while charging a pack, this is the VEOC threshold value. See 0x11.5 VEOC for details on VEOC functionality.

The remaining thresholds do not have adjustable hysteresis, the recovery voltage to clear the faults is set by the threshold alone.

7.1.2.6 Hysteresis Setting

The hysteresis setting is a value added to or subtracted the original threshold to set a voltage recovery level. Use Equation 4 to calculate the recovery threshold value. OV_{hys} (0x81.[6:4] V_{CELL} OV Hysteresis) and UV_{hys} (0x82.[6:4] V_{CELL} UV Hysteresis) have programmable hysteresis settings.

(EQ. 4) $$HystersisThresh = THRESHOLD + HysteresisVal$$

Use Equation 5 and the constants listed in Table 10 to calculate the digital hysteresis value.

(EQ. 5) $$REGVal = Integer\left[\frac{(Hysteresis_{Value} - Hysteresis_{MIN})}{Hysteresis_{STEP}}\right]$$

Use Equation 6 and the constants listed in Table 10 to calculate the decimal hysteresis value.

(EQ. 6) $$Hysteresis_{Value} = (RegVal) \cdot Hysteresis_{Step} + Hysteresis_{MIN}$$

For an OV threshold setting of 4.2V and a hysteresis setting of -100mV, the recovery threshold becomes 4.1V. Following an OVF, the device uses the recovery threshold of 4.1V to compare each cell voltage until the max cell voltage reads below the 4.1V threshold, which then clears the OVF bit.

Table 11. Hysteresis Constants

Hysteresis Threshold Type	Reg Val Hex	# Of Bits	Constants		Max Val ADC Code	Min Val ADC Code	Units
			$Hysteresis_{Step}$	$Hysteresis_{Min}$			
OV	81.[6:4]	3	-0.05	-0.05	-0.4	-0.05	V
UV	82.[6:4]	3	+0.1	+0.1	0.8	0.1	V

7.2 Register Definitions

RAA489220 operation is controlled by configuration registers and monitored by measurement result, status, and fault registers. Default values for settings using multiple bits are highlighted in gray.

7.2.1 0x10 Faults

The Fault Register is Read Only.

Table 12. 0x10 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x10.[15:8]	REGF	OWF	IOTF	VTMPF	LOF	STF	RSV	COMMTO	00
0x10.[7:0]	DCVF	OVF	UVF	OTF	UTF	SCF	DOCF	COCF	00

7.2.1.1 0x10.15 REGF

The REG Fault bit reports undervoltage and overvoltage conditions at the V3P3 and V2P5 pins. The bit also reports overvoltage and undervoltage failures with the VBG2 block. VBG2 is the reference that generates the V3P3 voltage and is also used for comparison to the band-gap reference for the ADC.

The bit is set to 1 and the $\overline{\text{ALERT}}$ pin is asserted when the measured voltage exceeds the digital threshold for the respective limit. The device immediately transitions to LP Mode when this fault is set.

The bit is cleared on exit from LP Mode.

The V3P3 and V2P5 regulators have power-good analog comparators (page 10) that monitor these pins. If a violation occurs, the device performs a power on reset.

The second Band Gap reference (VBG2) has digital compare thresholds, 0x0CB8 for OV and 0x08D0 for UV.

7.2.1.2 0x10.14 OWF

The Open-Wire Fault bit is set to 1 when a VCn pin fails the V_{CELL} open-wire test. The device transitions to LP Mode if bit 0x80.8 AutoSCAN En is set and the $\overline{\text{ALERT}}$ pin is asserted when the bit is set. The test is performed in the Self Test loop of the system scan or with a trigger action in IDLE Mode.

The bit is cleared on exit from LP Mode.

7.2.1.3 0x10.13 IOTF

The Internal Over-Temperature Fault bit is set and the $\overline{\text{ALERT}}$ pin is asserted when the device die temperature exceeds 100°C. The device continuously monitors its temperature in IDLE and SCAN Modes. When IOTF sets, the device transitions to LP Mode.

The bit clears when the die temperature drops below ~100°C.

7.2.1.4 0x10.12 VTMPF

The VTEMP Fault bit is set and the $\overline{\text{ALERT}}$ pin is asserted when the measured voltage exceeds the digital thresholds or when at least one thermistor pin (THERM1 or THERM2) fails the open-wire test for thermistors. With a failed reading, the device immediately transitions to LP Mode. These tests are performed in the Self Test Loop of the system scan.

The bit is to set to 0 on exit from LP Mode.

7.2.1.5 0x10.11 LOF

The Lockout Fault bit is set following a threshold violation detection from either 0x81.[3:0] V_{CELL} OVLO or 0x82.[3:0] V_{CELL} UVLO. This bit along with fault bits 0x10.6 OVF and 0x10.5 UVF allow the MCU to differentiate between an OV and OVLO, or a UV and UVLO.

7.2.1.6 0x10.10 STF

The Self Test Fault bit is set if the VPACK or VSS OW, or Oscillator test fails during the Self Test Loop (System Scan Sequence). This fault triggers a transition to LP Mode.

The bit is set to 0 when the device resets provided that the condition is cleared.

7.2.1.7 0x10.8 COMMTO

The Communication Timeout bit is set to 1 when the device has not received a valid serial communication from the MCU within the communication timeout period (0x80.[14:13] Communication TO). A communication timeout fault forces the device to transition to LP Mode.

The bit is set to 0 when the device resets or when a valid serial communication had been received. A valid serial communication is when the SDA line is pulled low by the MCU while the SCL line is high.

7.2.1.8 0x10.7 DCVF

The Delta Cell Voltage Fault bit is set to 1 when the minimum cell voltage subtracted from the maximum cell voltage is greater than the 0x82.[15:12] DV_{CELL} OV threshold. The test is performed in the normal loop of the system scan. A threshold violation causes the device to transition to LP Mode if bit 0x80.8 AutoSCAN En is set. The Power FET Fault Response lists the FET behavior versus faults.

In IDLE Mode, the device does not control the FETs or change Modes for a DCVF.

The DCVF bit is cleared when the device resets or when the Min/Max Cell difference falls below the threshold.

7.2.1.9 0x10.6 OVF

The Overvoltage Fault bit is set when at least one cell voltage measurement exceeds an OV threshold. For each system scan, the device compares the maximum cell voltage to the cell OV (0x81.[15:9] V_{CELL} OV) and OVLO (0x81.[3:0] V_{CELL} OVLO) thresholds. The test is performed in the normal loop of the system scan. The bit setting is the OR'd result of the two comparisons. The device may change Modes depending on the comparison that failed. An OVLO failure takes precedence over an OV failure. The Power FET Fault Response lists the FET behavior versus a set fault.

The OVF fault has a recovery threshold (0x81.[6:4] V_{CELL} OV Hysteresis) that enables the device to clear the fault after the cell voltages drop below the setting. See Recovery Threshold for details.

The RAA489220 does not disable the FETs for an OVF in IDLE Mode (page 17).

The OVF bit is cleared when the device resets or when the maximum cell reading measures below both thresholds.

A OVF asserts the $\overline{ALERT}$ pin and the bit is latched until a command read of the fault and status registers is received. More information about the $\overline{ALERT}$ pin and fault and status bit interactions is discussed on page 56.

7.2.1.10 0x10.5 UVF

The Undervoltage Fault bit is set when at least one cell voltage measurement falls below a UV threshold. For each system scan, the device compares the minimum cell voltage to the cell UV (0x82.[11:8] V_{CELL} UV) and UVLO (0x82.[3:0] V_{CELL} UVLO) thresholds. The test is performed in the normal loop of the system scan. The bit setting is the OR'd result of the two comparisons. The device may change Modes depending on the comparison that failed. An UVLO failure takes precedence over an UV failure. The Power FET Fault Response lists the FET behavior versus a set fault.

The UVF fault has a recovery threshold (0x82.[6:4] V_{CELL} UV Hysteresis) that enables the device to clear the fault after the cell voltages rises above the setting. See Recovery Threshold for details.

The RAA489220 does not disable the FETs for an UVF in IDLE Mode (page 17).

The UVF bit is cleared when the device resets or when the minimum cell reading measures above both thresholds.

A UVF asserts the $\overline{ALERT}$ pin and the bit is latched until a command read of the fault and status registers is received. More information about the $\overline{ALERT}$ pin and fault and status bit interactions is discussed on page 56.

7.2.1.11 0x10.4 OTF

The Over-Temperature Fault bit is set when the voltage reading of either thermistor is below the OT threshold(s). The device design assumes an NTC (Negative temperature coefficient) thermistor on the THERM pin. Table 30 lists example threshold settings represented as pin voltages, ADC codes, and temperature.

The device compares the THERM pin voltage readings to the DOT (0x83.[13:11] DOT) and COT (0x83.[5:3] COT) thresholds for each system scan. The comparison is performed in the THERM loop of the system scan (System Scan Sequence).

If the device detects a discharge current (0x11.1 DCHRGI), the DOT threshold is used. If a charge current is detected (0x11.0 CHRGI), the COT threshold is used. A DOT failure takes precedence over a COT failure. The device may change modes depending on the comparison that failed. Power FET Fault Response lists the FET behavior versus a set fault.

The COT recovery threshold is a fixed hysteresis of approximately 5°C below the COT Threshold. The DOT threshold has no hysteresis.

The RAA489220 does not disable the FETs for an OTF in IDLE Mode (page 17).

The OTF bit is cleared when the device resets or when the thermistor voltage rises above the violated threshold.

An OTF asserts the $\overline{\text{ALERT}}$ pin and the bit is latched until a command read of the fault and status registers is received. More information about the $\overline{\text{ALERT}}$ pin and fault and status bit interactions is discussed on page 56.

7.2.1.12 0x10.3 UTF

The Under-Temperature Fault bit is set when the voltage reading of either thermistor is above the UT threshold(s). The device design assumes an NTC (Negative temperature coefficient) thermistor on the THERM pin. Table 30 lists example threshold settings represented as pin voltages, ADC codes, and temperature.

The device compares the THERM pin voltage readings to the DUT (0x83.[10:8] DUT) and CUT (0x83.[2:0] CUT) thresholds for each system scan. The comparison is performed in the THERM loop of the system scan (System Scan Sequence).

If the device detects a discharge current (0x11.1 DCHRGI), the DUT threshold is used. If a charge current is detected (0x11.0 CHRGI), the CUT threshold is used. A DUT failure takes precedence over a CUT failure. The device may change modes depending on the comparison that failed. The Power FET Fault Response lists the FET behavior versus a set fault.

The CUT recovery threshold is a fixed hysteresis of approximately 5°C above the CUT Threshold. The DUT threshold has no hysteresis.

The RAA489220 does not disable the FETs for a UTF in IDLE Mode (page 17).

The UTF bit is cleared when the device resets or when the thermistor voltage drops below the violated threshold.

An UTF asserts the $\overline{\text{ALERT}}$ pin and the bit is latched until a command read of the fault and status registers is received. More information about the $\overline{\text{ALERT}}$ pin and fault and status bit interactions is discussed on page 56.

7.2.1.13 0x10.2 SCF

The Short-Circuit Fault bit reports the result of the analog OR'd short-circuit comparisons for both discharge (DCSP - CSN) and charge (CCSP-CSN) sense resistors. If the discharge voltage exceeds the SCC Threshold (0x84.[14:12] SCC) for the SCC Delay time (0x83.[15:14] SCC Delay), the SCF bit is set to 1. A charge current that results in a charge voltage that is less than SCC Threshold for SCC Delay time sets the bit to 1.

An SCF disables the FETs and transitions the device to LOW POWER Mode.

The bit clears if the device is reset and the condition is no longer present.

7.2.1.14 0x10.1 DOCF

The Discharge Overcurrent Fault bit reports the result of the discharge overcurrent digital comparison. If the I_{PACK} discharge (DCSP-CSN) measurement result is above the DOC threshold (0x84.[11:6] DOC) for the DOC delay time (0x84.15 DOC/COC Delay), bit DOCF is set to 1. The test is performed in the normal loop of the system scan (System Scan Sequence).

A DOCF disables the FETs and transitions the device to LOW POWER Mode if detected during AutoSCAN.

The device does not change modes for a DOCF while in IDLE Mode. The master controls the power FETs and mode transitions while in IDLE.

The bit clears when the device resets, when the measurement reads below the DOC threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

7.2.1.15 0x10.0 COCF

The Charge Overcurrent Fault bit reports the result of the charge overcurrent digital comparison. If the I_{PACK} charge (CCSP-CSN) measurement result is below the COC threshold (0x84.[5:0] COC) for the COC delay time (0x84.15 DOC/COC Delay), bit COCF is set to 1. The test is performed in the normal loop of the system scan (System Scan Sequence).

A COCF disables the CFET and transitions the device to LOW POWER Mode if detected during AutoSCAN.

The device does not change modes for a COCF while in IDLE Mode. The master controls the power FETs and mode transitions while in IDLE.

The bit clears when the device resets, when the measurement reads above the COC threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

7.2.2 0x11 Masks and Status

IMPORTANT: If a mask bit (or bits) are cleared to connect a status change to the $\overline{\text{ALERT}}$ pin, the relevant status bit(s) becomes latched. In this case, the status register must be read to clear the bit and release the $\overline{\text{ALERT}}$ pin. See bit descriptions that follow for more information.

Table 13. 0x11 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x11.[15:8] **RW**	BUSY Mask	HVGPIO Mask	V/IEOC Mask	RSV	CH/LD PRESI Mask	RSV	RSV	V3P3OK	FF
0x11.[7:0] **RO**	BUSY	VTEMP Status	VEOC	IEOC	CH PRESI	LD PRESI	DCHRGI	CHRGI	00

7.2.2.1 0x11.15 Busy Mask

The Busy Mask bit connects the Busy bit (0x41.15 Busy) status to the $\overline{\text{ALERT}}$ pin by asserting the pin to VSS when the device is making measurements. A mask bit setting of 0 connects the Busy bit status to the pin. A mask bit setting of 1 (default) disables this connection. The Busy bit it only operational in SCAN and IDLE Modes.

A mask bit setting of 0 and the Busy bit value transitioning from 0 to 1 results in the $\overline{\text{ALERT}}$ pin asserted to VSS until the master reads the status register. When the read has occurred, the $\overline{\text{ALERT}}$ pin returns to a high impedance state.

When the $\overline{\text{ALERT}}$ pin is released, the Busy bit is allowed to change states freely.

The Busy bit can change states freely if the Busy Mask bit is set to 1.

7.2.2.2 0x11.14 HVGPIO Mask

The HVGPIO Mask bit connects the OVLO, UVLO, STF, OWF, and VTMPF status bits to the HVGPIO pin by asserting the pin to VSS when the status bit is set if this mask bit is set to 0. A setting of 1 (default) masks the faults and the pin state is unaffected.

7.2.2.3 0x11.13 V/IEOC Mask

The VEOC/IEOC Mask bit connects the status of the VEOC (0x11.5 VEOC) and IEOC (0x11.4 IEOC) bits to the $\overline{\text{ALERT}}$ pin if set to 0. A mask bit setting of 1 (default) disables this connection.

With the mask bit setting of 0, a VEOC or IEOC bit transitioning from 0 to 1 results in the $\overline{\text{ALERT}}$ pin being asserted to VSS until the master reads the status from the device. When the read has occurred, the status bit(s) is cleared and the $\overline{\text{ALERT}}$ pin returns to a high-impedance state.

The VEOC and IEOC bits can change states freely for a VEOC/IEOC Mask bit setting of 1.

7.2.2.4 0x11.12 RSV

Set this bit to 1 when writing the register and ignore it on read-back.

7.2.2.5 0x11.11 CH/LD PRESI Mask

The Charger Present and Load Present Mask bit connects the status of the CH PRESI (0x11.3 CH PRESI) and LD PRESI (0x11.2 LD PRESI) bits to the $\overline{\text{ALERT}}$ pin if set to 0. A mask bit setting of 1 (default) disables this connection.

With the mask bit setting of 0, a CH or LD PRES bit transitioning from 0 to 1 results in the $\overline{\text{ALERT}}$ pin being asserted to VSS until the master reads the status from the device. When the read has occurred, the status bit(s) is cleared and the $\overline{\text{ALERT}}$ pin returns to a high impedance state.

The Charger Present and Load Present bits can change states freely for a Charger Present and Load Present Mask bit setting of 1.

7.2.2.6 0x11.[10:9] RSV

Set these bits to 1 when writing the register and ignore it on read-back.

7.2.2.7 0x11.8 V3P3OK

The V3P3 OK bit is set to 1 when the pin voltage falls within the normal range, or set to 0 if high or low. The voltage is monitored by an analog comparator when the device is in IDLE or SCAN Mode. The device takes no automatic action based on this bit. The normal range is defined by PG_{V3P3_UV} and PG_{V3P3_OV}.

7.2.2.8 0x11.7 Busy

The Busy bit reports whether the device is busy measuring parameters or executing the Self Test Loop while the device is in SCAN Mode. The bit is set to 1 when the device is busy, 0 indicates that device is idle.

The bit signal can be connected to the $\overline{\text{ALERT}}$ pin by way of the bit 0x11.15 Busy Mask. The bit is latched when the Busy Mask bit is set to 0.

7.2.2.9 0x11.6 VTEMP Status

The VTEMP Status bit reports when the VTEMP pin output is enabled for measuring THERM1/2. If the bit 0x42.15 VTEMP EN is set to 1, the VTEMP Status bit does not track the status of the VTEMP output.

7.2.2.10 0x11.5 VEOC

The Voltage End-of-Charge bit is active when the device is charging (0x11.0 CHRGI). The bit is set to 1 when the maximum cell voltage is above the VEOC threshold but lower than the OV threshold. The VEOC threshold is the same as the overvoltage recovery voltage (OV Hysteresis subtracted from OV Threshold). The VEOC bit is an indicator intended to inform the charger to switch from constant current to constant voltage.

After reading all cell voltages within a battery pack, the VEOC bit is set to 1 when the maximum cell voltage is above the VEOC threshold. The VEOC bit is set to 0 when the maximum cell voltage reading is below the threshold or when the device exits LP Mode.

When the VEOC bit transitions from a 0 to 1, the IEOC threshold is not compared to the current reading until 10ms after the VEOC transition has occurred. The time allows for the charger to change from constant current to constant voltage.

The status of the VEOC bit can be connected to the $\overline{\text{ALERT}}$ pin with the VEOC/IEOC Mask bit (0x11.13 V/IEOC Mask). A Mask bit setting of 0 latches the VEOC bit after a bit transition from 0 to 1.

7.2.2.11 0x11.4 IEOC

The Current End-of-Charge status bit becomes active after the VEOC Status bit sets during charging (the maximum cell voltage is above the VEOC threshold but lower than OV threshold). The device has to be charging (0x11.0 CHRGI) for the IEOC detection function to be active. When the charger has switched to constant voltage sourcing, the pack current tappers as the sum of the cell voltages approaches the pack voltage applied from the charger. When the charge current drops below the threshold 0x81.[8:7] IEOC, the IEOC bit transitions from 0 to 1, indicating that the battery is full.

For a series power FET configuration (0x82.7 CPWR = 0), if the IEOC bit sets, both power FETs turn OFF and the device transitions to LP Mode. For a parallel power FET configuration (CPWR = 0), only LCFET is turned OFF.

The IEOC bit is set to 0 when VEOC is set to 0. The VEOC bit is cleared when the maximum cell voltage reading is below the VEOC threshold or when the device exits LP Mode.

The device starts comparing the current-sense resistor voltage to the IEOC Threshold 10ms after the VEOC bit has transitions from 0 to 1. The time allows the charger to switch from constant current to constant voltage.

The status of the bit can be connected to the $\overline{\text{ALERT}}$ pin with the VEOC/IEOC Mask bit. A Mask bit setting of 0 latches the IEOC bit after it transitions from 0 to 1.

7.2.2.12 0x11.3 CH PRESI

The Charge Present status bit is set to 1 when the voltage at the CHMON pin falls below the threshold V_{CHTHR}. The bit is not latched if the LD/CH PRESI Mask bit is set to 1. A CH PRESI bit transition from 0 to 1 wakes the device from LP Mode (edge triggered). The device begins monitoring 100ms after LCFET turns OFF. See CHMON Pin for more about the charger detection circuit.

If the LD/CH PRESI Mask bit is set to 0, the CH PRESI bit is latched until the master reads the Fault and Status register. The latched bit results in the $\overline{\text{ALERT}}$ pin asserting until the status register read.

Typically, the CHMON Pin connects to the negative charger terminal. However, alternative circuits can be used to wake up the part.

7.2.2.13 0x11.2 LD PRESI

The Load Present Indicator bit is set to 1 when the voltage at the LDMON pin is pulled above the VPACK - LDMON Threshold (V_{LDThr}) by an attached load. The bit is not latched unless the LD/CH PRESI mask bit is set to 0. A bit transition from 0 to 1 exits the LP Mode. The device monitors for a rising edge at the pin, which results in a rising edge for the bit. The device monitors for an edge 100ms after LDFET turns OFF. See LDMON Pin for more about the load detect circuit.

If the LD/CH PRESI Mask bit is set to 0, the LD PRESI bit is latched until the master reads the Fault and Status register. The latched bit results in the $\overline{\text{ALERT}}$ pin asserting until the status register read.

The LDMON Pin should connect to the negative terminal of the load.

7.2.2.14 0x11.1 DCHRGI

The Discharge Current Indicator bit sets if charge is being removed from the battery pack. If the current voltage measurement is greater than approximately 600µV (page 9), the DCHRGI bit is set to 1.

The DCHRGI bit is set when there are two consecutive readings greater than the DCHRGI threshold. The bit is set to 0 when a single I_{PACK} measurement falls below the DCHRGI threshold. This bit is not latched.

Some fault responses are gated by DCHRGI bit status and the CPWR bit setting. The Power FET Fault Response lists the FET behavior versus faults.

7.2.2.15 0x11.0 CHRGI

The Charge Current Indicator bit sets if charge is being added to the battery pack. If the current voltage measurement is less than approximately -600µV (I_{CHRGI}), the CHRGI bit is set to 1.

The CHRGI bit is set when there are two consecutive readings below the CHRGI threshold. The bit is set to 0 when a single I_{PACK} measurement rises above the CHRGI threshold. This bit is not latched.

Some fault responses are gated by CHRGI bit status and the CPWR bit setting. The Power FET Fault Response lists the FET behavior versus faults.

7.2.3 0x40 System Config 1

Table 14. 0x40 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x40.[15:8] **RO**	RSV	RSV	RSV	RSV	HVGPIO Status	ALERT Status	LDFET Status	LCFET Status	00
0x40.[7:0] **RW**	Soft Reset	Clear All Faults	GO2LPM	RSV	HVGPIO Assert	ALERT Assert	LDFET Enable	LCFET Enable	00

7.2.3.1 0x40.11 HVGPIO Status

The read only HVGPIO pin Status bit indicates the status of the HVGPIO pin. A 1 indicates the pin is pulled high. A 0 indicates the pin voltage is less than the V_{IL}voltage (page 12).

7.2.3.2 0x40.10 ALERT Status

The read only $\overline{ALERT}$ pin Status bit indicates the status of the $\overline{ALERT}$ pin while in operation. A 0 indicates the pin is pulled high. A 1 indicates the pin voltage is less than the V_{IL}voltage (page 12) and an ALERT condition exists.

7.2.3.3 0x40.9 LDFET Status

The read only LDFET pin Status bit indicates the status of the low-side DFET pin voltage while in operation. This bit is a read only bit. A 1 indicates that the pin voltage is above $LxFET_{VIL}$ (page 11). A 0 indicates that the pin voltage is below the VIL threshold

7.2.3.4 0x40.8 LCFET Status

The read only LCFET pin Status bit indicates the status of the low-side CFET pin voltage while in operation. This bit is a read only bit. A 1 indicates that the pin voltage is above $LxFET_{VIL}$ (page 11). A 0 indicates that the pin voltage is below the VIL threshold

7.2.3.5 0x40.7 Soft Reset

Setting the Soft Reset bit to 1 forces the state machine to jump to the Reset State, which resets all register values to the factory defaults, including data registers. The device then proceeds through the Power Up State before turning ON the FETs as it enters IDLE Mode. The bit action is equivalent to a hard reset or a power-on reset (POR) event. All counters and state machines are set to their default states. This bit is cleared when the registers are set to the factory defaults. The default bit setting is 0.

7.2.3.6 0x40.6 Clear All Faults

Write a 1 to the Clear All Faults bit to clear all faults, status bits, and counters. Other register settings are maintained with this command. On completion, the bit is set to 0 (default).

The analog compared faults do not clear while the condition that sets them is present. Use this bit to reset the no current counter and other fault counters when exiting LOW POWER Mode.

7.2.3.7 0x40.5 Go2LPM

Write a 1 to the Go to LOW POWER Mode bit to force the RAA489220 to transition to LOW POWER Mode. This bit function only executes when the device is in either IDLE or SCAN Mode. The default bit setting is 0.

7.2.3.8 0x40.3 HVGPIO Pin Assert

Writing a 1 to this bit asserts the HVGPIO pin to the VSS pin. An internal open-drain NMOS is activated providing a low-impedance connection between the HVGPIO pin and VSS pin. Writing a 0 to this bit, turns OFF the NMOS leaving the HVGPIO pin in a high impedance state. The default setting of this pin is 0.

7.2.3.9 0x40.2 $\overline{\text{ALERT}}$ Pin Assert

Writing a 1 to this bit asserts the pin to the VSS pin. A internal NMOS is activated providing a low impedance connection between the $\overline{\text{ALERT}}$ and VSS pins. Writing a 0 to this bit turns OFF the NMOS leaving the $\overline{\text{ALERT}}$ pin in a high impedance state. The default setting of this pin is 0.

7.2.3.10 0x40.1 LDFET En

The LDFET Enable bit turns ON and OFF the low-side power DFET. Write a 1 to enable the device's internal current source to turn on the LDFET. A 0 (default) indicates that the current source is OFF and the pin is in a high-impedance state. This bit should only be written in IDLE Mode, do not change during AutoSCAN (0x80.8 AutoSCAN En).

7.2.3.11 0x40.0 LCFET En

The LCFET Enable bit turns ON and OFF the low-side power CFET. Write a 1 to enable the device's internal current source to turn on the LCFET. A 0 (default) indicates that the current source is OFF and the pin is in a high-impedance state. This bit should only be written in IDLE Mode, do not change during AutoSCAN (0x80.8 AutoSCAN En).

7.2.4 0x41 Measure Select

Table 15. 0x41 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x41.[15:8] **RO**	Busy	RSV	RSV	RSV	RSV	RSV	RSV	RSV	00
0x41.[7:0] **R/W**	Trigger Measurement	RSV	RSV	Measurement Selection					00

7.2.4.1 0x41.15 Busy

The read only Busy measuring bit indicates the status of the measurement that has been triggered by the trigger measurement bit, or measurement status during AutoSCAN (see 0x80.8 AutoSCAN En). A 1 indicates that the device is performing a measurement.

7.2.4.2 0x41.7 Trigger Measurement

Write a 1 to this bit to trigger the measurement(s) selected with the Measurement Selection bits while in IDLE Mode. This bit automatically clears to 0 (default) after the measurement has completed. The bit is only active while in IDLE Mode.

All measurements are compared to their respective thresholds, but the device does not change Modes, turn OFF the power FET(s), or assert the $\overline{\text{ALERT}}$ pin when a fault is detected. The MCU is expected to check the results of triggered measurements in IDLE Mode and react accordingly. There are three exceptions:

- If the device does not receive communication from the MCU within the setting of 0x80.[14:13] Communication TO, the power FETs turn OFF and the device transitions to LP Mode.
- If an analog fault occurs, the device turns OFF the power FETs and the device transitions to LP Mode.
- If the measurement selection is Single System Scan, the $\overline{\text{ALERT}}$ pin asserts on a fault detection.

The $\overline{\text{ALERT}}$ pin is asserted for faults that result in the device transitioning to LOW POWER Mode. See Power FET Fault Response for details.

Faults are set based on the number of consecutive threshold violations. The fault count threshold is the same as the fault count threshold used during AutoSCAN (0x80.8 AutoSCAN En).

7.2.4.3 0x41.[4:0] Measurement Selection

The Measurement Selection bits determine the action the device executes when the Trigger Measurement bit is set to 1. All measurement registers are updated following triggered measurements. Table 16 lists the actions the device can perform. The default setting for these bits is 0. The measured value is stored in the Thermistor 2 data register unless stated otherwise. Only Single System Scans are compared to fault thresholds, single triggered measurements do not detect faults or assert the $\overline{\text{ALERT}}$ pin.

Table 16. Measurement Selection Table

0x41.4	0x41.3	0x41.2	0x41.1	0x41.0	Measurement	Description
0	0	0	0	0	Single System Scan	One Complete System Scan with Self Test and Thermistor Measurements. All measurement registers, fault and current flow counters are updated
0	0	0	0	1	VTEMP	Measures the pin voltage at the VTEMP pin. The VTEMP En bit has to be set to 1 before measuring the pin.
0	0	0	1	0	V3P3	Measures the pin voltage at the V3P3 pin.
0	0	0	1	1	V2P5	Measures the pin voltage at the V2P5 pin.
0	0	1	0	0	VBG2	Measures the voltage at the VBG2 pin.
0	0	1	0	1	Internal Temp	Measures the voltage at the Internal temperature sensor.
0	0	1	1	0	THERM1	Measures the voltage at the THERM1 Pin. Use the bit 0x42.15 VTEMP EN to turn ON VTEMP before triggering this measurement.
0	0	1	1	1	THERM 2	Measures the voltage at the THERM2 Pin. Use the bit 0x42.15 VTEMP EN to turn ON VTEMP before triggering this measurement.
0	1	0	0	0	VPACK	Measure VPACK. Delta VCell, Cell Min and Cell Max registers are unchanged.
0	1	0	0	1	VCell 1	Measure VCell1, DVCell, Cell Min and Cell Max registers are unchanged.
0	1	0	1	0	VCell 2	Measure VCell2, DVCell, Cell Min and Cell Max registers are unchanged.
--	--	--	--	--	------	----- Meas VCell XX ----.
1	0	0	1	0	VCell 10	Measure VCell10, DVCell, Cell Min, and Cell Max registers are unchanged.
--	--	--	--	--	------	----- RESERVED DO NOT PROGRAM----.
1	0	1	1	0	IPACK (D)	Measure the voltage between DCSP and CSN pins.
1	0	1	1	1	IPACK (C)	Measure the voltage between CCSP and CSN pins.

7.2.5 0x42 System Config 2

Table 17. 0x42 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x42.[15:8]	VTEMP EN	Self Test En	LP Reg	RSV	RSV	RSV	Isrce VC10	Isrce VC9	40
0x42.[7:0]	Isrce VC8	Isrce VC7	Isrce VC6	Isrce VC5	Isrce VC4	Isrce VC3	Isrce VC2	Isrce VC1	00

7.2.5.1 0x42.15 VTEMP EN

The VTEMP Enable bit turns ON or OFF the VTEMP output. the default setting of 0 turns OFF the output while a setting of 1 turns it on. This bit is only functional in IDLE Mode.

In SCAN Mode, the device automatically controls the VTEMP output for continuous (0x80.8 AutoSCAN En) and Single System Scans. The state machine turns ON and OFF the VTEMP output while executing the THERM and Self Test Loops (System Scan Sequence) in system scan. The state machine does not change the state of this bit while in this Mode.

Triggered measurements of the thermistor voltages executed from IDLE Mode using Table 16 do not automatically enable the VTEMP output. The VTEMP EN bit must be set before the trigger and should be cleared following its completion.

7.2.5.2 0x42.14 Self Test En

The Self Test Enable bit setting of 1 (default) includes the Self Test Loop tests during the system scan sequence (System Scan Sequence). A setting of 0 bypasses Self Test during the system scan sequence.

7.2.5.3 0x42.13 LP Regulator

The LP Regulator bit sets regulator operation while in LOW POWER Mode. A setting of 1 enables the strong regulator in LP Mode. The power-good comparators are enabled when the strong regulator is used. The current consumption of the device is more while this regulator is enabled. A setting of 0 (default) enables the weak regulator while in LP Mode reducing current consumption. Power consumption during and device state on exit from LP Mode is also dependent on bit 0x80.7 Sleep En.

For the lowest power consumption, the device should use the settings Sleep En = 0 and LP Reg = 0. The register contents are not retained with these settings. The device wakes up on a RESET, POR, I^2C transaction, charge, or load detect.

7.2.5.4 0x42.[9:0] ISRC VCn

Setting this bit to 1 turns on the current source (page 11) that connects between the VC pin and VSS. The default setting for these bits is 0.

7.2.6 0x80 System Config 3

Registers 0x80-0x84 require the use of a key sequence before writing them is permitted, see Write to Protected Registers 0x80-0x84.

Table 18. 0x80 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x80.[15:8]	OW Enable	Communication Timeout		Scan Delay		Fault Delay		AutoSCAN En	EA
0x80.[7:0]	Sleep En	Product ID							A0

7.2.6.1 0x80.15 Open Wire En

An Open-Wire Enable bit setting of 1 (default) includes an open-wire test for cell connections while executing the Self Test Loop (Figure 18) within the system scan. An open-wire test can be executed while in IDLE Mode by triggering the Single System Scan (Table 16) with this bit previously set to 1.

7.2.6.2 0x80.[14:13] Communication TO

The Communication Timeout bits set the maximum time between MCU communications with the RAA489220 before a timeout fault (0x10.8 COMMTO) forces a transition to LP Mode. If the SDA pin does not make high-to-low transition while the SCL pin is high within the selected period of time, the device transitions to LOW POWER Mode.

When the MCU asserts the SDA pin low while the SCL pin is high, the communication timer resets to 0. Table 19 lists the selectable times.

Table 19. Comm TO Selections

D[14:13]	Timeout Time (s)
00	OFF
01	0.1
10	1
11	5

7.2.6.3 0x80.[12:11] Scan Delay

The Scan Delay bits control the time delay between continuous system scans (0x80.8 AutoSCAN En). Scan Delay is only functional while the device is in AutoSCAN in SCAN Mode.

Table 20 lists the available and default delays.

Table 20. Scan Delay Selections

D[12:11]	Timeout Time (s)
00	0
01	0.1
10	0.5
11	1

7.2.6.4 0x80.[10:9] Fault Delay

The Fault Delay bits set the time delay between AutoSCANs if a fault is detected. It replaces the Scan Delay time between continuous system scans. If the fault remains (determined by the relevant fault thresholds) after the delay has timed out, the related fault bit sets. Fault Delay is only operable when the device is in AutoSCAN. With a setting of 00, this feature is disabled and the Scan Delay value remains in effect.

See Table 4 and Table 5 for the faults that use this setting. Table 21 lists the available delay settings.

Table 21. Fault Delay Selections

D[10:9]	Timeout Time (s)
00	OFF
01	0.1
10	1
11	5

7.2.6.5 0x80.8 AutoSCAN En

An AutoSCAN Enable bit setting of 0 (default) transitions the state machine to IDLE Mode after a triggered measurement is completed. For a bit setting of 1, the state machine stays in SCAN Mode after the system scan has completed and the state machine transitions back to the start of Scan state where another system scan is performed. An AutoSCAN En bit setting of 1 places the device in a continuous scan loop until a fault is detected or the bit value is changed to 0 by the MCU.

7.2.6.6 0x80.7 Sleep En

A Sleep Enable bit setting of 1 (default) before a transition to LOW POWER Mode allows the device to retain the register settings if bit 0x42.13 LP Regulator is also set to 1. A Sleep Enable bit setting of 0 does not retain the register settings in LP Mode, the defaults are loaded on wake up.

7.2.6.7 0x80.[6:0] Product ID

This is the configuration specific product ID for the device.

PRODUCT (RAA489xxx)	Description	Product ID (HEX)
RAA489220	Prototype	0x00
RAA489220	Standard Product	0x20

7.2.7 0x81 OV and EOC Thresholds

Table 22. 0x81 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x81.[15:8]	V_{CELL} OV Threshold							IEOC	CC
0x81.[7:0]	IEOC	OV Hysteresis			V_{CELL} OVLO Threshold				2D

7.2.7.1 0x81.[15:9] V_{CELL} OV

Each V_{CELL} measurement is compared to overvoltage limits. The overvoltage threshold detector alerts the system to discontinue charging at the selected voltage during charge. The threshold detector is a digital comparator that requires an ADC V_{CELL} measurement to compare. If this threshold is exceeded, fault bit 0x10.6 OVF is set to 1.

The setting ranges from 3.23V to 4.5V with a 10mV step size and a default of 4.25V.

7.2.7.2 0x81.[8:7] IEOC

The Current End-of-Charge Threshold register sets the minimum charge current by setting the threshold voltage of a digital comparator for undercurrent detection. Bit 0x11.4 IEOC is set to indicate an end-of-charge condition when the charge current decreases to the point at which the voltage across the current-sense resistor is less than this threshold setting. The comparator is enabled ~10ms after bit VEOC transitions from low to high.

Table 23. IEOC Selections

D[8:7]	IEOC ADC Code	Typical IEOC Voltage
00	0x0133	0.65mV
01	0x0136	0.7mV
10	0x014C	1mV
11	0x01E4	3mV

7.2.7.3 0x81.[6:4] V_{CELL} OV Hysteresis

The V_{CELL} OV Hysteresis setting determines the cell voltage required to recover from and clear a V_{CELL} OV Fault (0x10.6 OVF). The recovery voltage is the setting of this register subtracted from 0x81.[15:9] V_{CELL} OV.

The setting ranges from 25mV to 400mV with a variable step size and a default of 100mV.

Table 24. OV Hysteresis Selections

3-Bit Setting	V_{CELL} OV Hysteresis
000	25mV
001	50mV
010	100mV
011	200mV
100	250mV
101	300mV
110	350mV
111	400mV

7.2.7.4 0x81.[3:0] V_{CELL} OVLO

Each V_{CELL} measurement is compared to overvoltage limits. During charge, the overvoltage threshold detector alerts the system to discontinue charging at the selected voltage. The threshold detector is a digital comparator that requires an ADC V_{CELL} measurement to compare. If this threshold is exceeded, fault bits 0x10.6 OVF and 0x10.11 LOF are set to 1.

The setting ranges from 3V to 4.5V with a 100mV step size and a default of 4.3V.

7.2.8 0x82 DV_{CELL}OV, UV Thresholds

Table 25. 0x82 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x82.[15:8]	DV_{CELL} OV Threshold				V_{CELL} UV Threshold				0D
0x82.[7:0]	CPWR	V_{CELL} UV Hysteresis			V_{CELL} UVLO Threshold				25

7.2.8.1 0x82.[15:12] DV_{CELL} OV

The Delta V_{CELL} Overvoltage register sets the threshold for a digital compare of the maximum difference between cell voltages. The detection is used to maintain cell voltage readings within a predetermined voltage range. A DV_{CELL} OV threshold violation sets the fault 0x10.7 DCVF when the difference between maximum and minimum cell voltages (see Measurement Reads) is greater than the threshold.

The setting ranges from 0.5V to 2V with a 100mV step size and a default of 0.5V.

7.2.8.2 0x82.[11:8] V_{CELL} UV

Each V_{CELL} measurement is compared to undervoltage limits. During discharge, the undervoltage threshold detector alerts the system to discontinue discharge at the selected voltage. The threshold detector is a digital comparator that requires an ADC V_{CELL} measurement to compare. If this threshold is exceeded, fault bit 0x10.5 UVF is set to 1.

The setting ranges from 1.5V to 3V with a 100mV step size and a default of 2.7V.

7.2.8.3 0x82.7 CPWR

The Configure Power FET bit changes the power FET response versus the fault signaled. A bit setting of 0 (default) is for series power FET configurations. The power FETs are dependent on the CHRGI and DCHRGI bit status with this setting. A bit setting of 1 is for parallel power FET configuration.

The power FET automatic response versus fault is found in Power FET Fault Response.

7.2.8.4 0x82.[6:4] V_{CELL} UV Hysteresis

The V_{CELL} UV Hysteresis setting determines the cell voltage required to recover from and clear a V_{CELL} UV Fault (0x10.5 UVF). The recovery voltage is the setting of this register added to 0x82.[11:8] V_{CELL} UV.

The setting ranges from 100mV to 800mV with a 100mV step size and a default of 300mV.

7.2.8.5 0x82.[3:0] V_{CELL} UVLO

Each V_{CELL} measurement is compared to undervoltage limits. During discharge, the undervoltage threshold detector alerts the system to discontinue discharge at the selected voltage. The threshold detector is a digital comparator that requires an ADC V_{CELL} measurement to compare. If this threshold is exceeded, fault bits 0x10.5 UVF and 0x10.11 LOF are set to 1.

The setting ranges from 1.5V to 3V with a 100mV step size and a default of 2.0V.

7.2.9 0x83 SCC, OT/UT Thresholds

See section Setting Thermistor Thresholds on how to calculate the OT/UT thresholds. See Fault Detection and Recovery and Power FET Fault Response for a detailed descriptions of the relationship between fault thresholds, delays, and device reactions.

Table 26. 0x83 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x83.[15:8]	SCC Delay		DOT			DUT			98
0x83.[7:0]	Therm Enable		COT			CUT			B4

7.2.9.1 0x83.[15:14] SCC Delay

The Short-Circuit Current Delay register sets the delay time for short-circuit current detection. If the short-circuit current remains, determined by threshold 0x84.[14:12] SCC, after the delay has timed out the related fault bit sets (see 0x10.2 SCF).

Table 27. SCC Delay

D[15:14]	Delay
00	Off
01	0.1ms
10	1ms
11	10ms

7.2.9.2 0x83.[13:11] DOT

The Discharge Over-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is discharging (0x11.1 DCHRGI is set). The RAA489220 assumes NTC thermistors are in use, which means that if the thermistor voltage is less than this threshold fault bit 0x10.4 OTF is set.

The selectable thresholds are listed in Table 29 with the default setting highlighted.

7.2.9.3 0x83.[10:8] DUT

The Discharge Under-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is discharging (0x11.1 DCHRGI is set). The RAA489220 assumes NTC thermistors are in use, which means that if the thermistor voltage is greater than this threshold fault bit 0x10.4 OTF is set.

The selectable thresholds are listed in Table 29 with the default setting highlighted.

7.2.9.4 0x83.[7:6] Thermistor Enable

The Thermistor Enable bits selects the number of thermistors to measure and compare. The bit selections are listed in Table 28

Table 28. Thermistor Enable Selection

Thermistor Enable Bits: D[7:6]		Action
0	0	OFF (no measurements)
0	1	THERM1
1	0	THERM1 and THERM2
1	1	RSV

VTEMP does not turn ON for a bit selection OFF (00b) in Table 28. For all other selections, the VTEMP regulator turns ON 18ms (page 9) before measuring the pin(s) during either AutoSCAN or a Triggered Single System Scan. Triggered measurements of the thermistor voltages alone requires the user to first enable the VTEMP output, see 0x42.15 VTEMP EN.

7.2.9.5 0x83.[5:3] COT

The Charge Over-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is charging (0x11.0 CHRGI is set). The RAA489220 assumes NTC thermistors are in use, which means that if the thermistor voltage is less than this threshold fault bit 0x10.4 OTF is set.

COT has a recovery hysteresis of ~5°C if the recommended circuit is used and it is dependent on the selected threshold.

7.2.9.6 0x83.[2:0] CUT

The Charge Under-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is charging (0x11.0 CHRGI is set). The RAA489220 assumes NTC thermistors are in use which means that if the thermistor voltage is greater than this threshold fault bit 0x10.4 OTF is set.

CUT has a recovery hysteresis of ~5°C if the recommended circuit is used and it is dependent on the selected threshold.

7.2.9.7 Setting Thermistor Thresholds

The Thermistor Threshold register settings represent voltages.

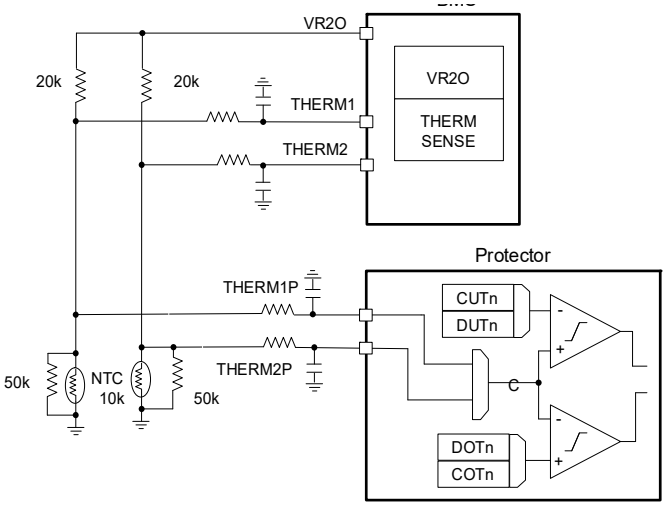


Figure 19. Thermistor Circuit Configuration

Before the device performing a thermistor measurement during either AutoSCAN or a Triggered Single System Scan, the VTEMP output is turned on ~18ms before the ADC measures the THERM1 voltage. The time allows the voltage at the THERM pin to settle before measuring. The settling time at the THERM pin is dependent on the pin capacitance. Figure 19 illustrates the recommended thermistor circuit connection.

The selectable thermistor voltage thresholds are listed in Table 29 with the defaults highlighted.

Table 29. Thermistor Thresholds

3-bit Setting	COT (V)	DOT (V)	CUT (V)	DUT (V)
000	0.678	0.222	1.622	1.622
001	0.59	0.194	1.526	1.526
010	0.518	0.17	1.422	1.422

Table 29. Thermistor Thresholds (Cont.)

3-bit Setting	COT (V)	DOT (V)	CUT (V)	DUT (V)
011	0.45	0.15	1.314	1.314
100	0.39	0.13	1.198	1.198
101	0.338	0.114	1.086	1.086
110	0.294	0.098	0.974	0.974
111	0.258	0.086	0.866	0.866

These thresholds are listed in terms of temperature for an example thermistor with a B Factor of 3435 in Table 30. This table lists the temperature threshold, the corresponding ADC code and pin voltage for all selectable (COT, CUT, DOT, DUT) and hysteresis thresholds.

Table 30. Example Thermistor Thresholds

Thermistor Temperature (C)	ADC code (HEX)	Therm Pin Voltage (mV)
100	1B0	96
95	1C8	108
90	1E4	122
85	205	138
80	22A	157
75	255	178
70	286	203
65	2C0	232
60	303	265
55	350	303
50	3A8	348
45	40E	399
40	483	458
35	508	524
30	59E	599
25	645	683
20	6FD	775
15	7C6	875
10	89B	981
5	97B	1094
0	A5E	1208
-5	B41	1321
-10	C1D	1431
-15	CEC	1534
-20	DA9	1629

7.2.10 0x84 Current Thresholds

See Fault Detection and Recovery and Power FET Fault Response for a detailed descriptions of the relationship between fault thresholds, delays, and device reactions.

Table 31. 0x84 Register Definition

Register	Bit Function								Default (Hex)
	15/7 (MSB)	14/6	13/5	12/4	11/3	10/2	9/1	8/0 (LSB)	
0x84.[15:8]	OC Delay	SCC Threshold			DOC Threshold				CC
0x84.[7:0]	DOC Threshold		COC Threshold						71

7.2.10.1 0x84.15 DOC/COC Delay

The Discharge/Charge Overcurrent Delay register sets the delay time for overcurrent detection. If the overcurrent remains (determined by the DOC/COC thresholds) after the delay has timed out, the related fault bit sets (see 0x10.1 DOCF and 0x10.0 COCF).

With the default setting of 1, the delay is set to 0x80.[10:9] Fault Delay; if 0, 0x80.[12:11] Scan Delay is selected.

7.2.10.2 0x84.[14:12] SCC

The Short-Circuit Current threshold register sets the short-circuit threshold voltage of the analog comparator for Discharge current. The Charge path short-circuit threshold comparator has a typical (fixed) threshold of ~200mV.

If the voltage across the current-sense resistor (see DCSP, CCSP, and CSN Pins) is more negative than this threshold for more than 0x83.[15:14] SCC Delay, fault bit 0x10.2 SCF is set.

When a short-circuit event is detected, the device automatically disables both the CFET and DFET.
IMPORTANT: When the FETs are disabled as a result of a short-circuit event, the FET Status bits 0x40.9 LDFET Status and 0x40.8 LCFET Status bits are not cleared.

Table 32. SCC Threshold

D[14:12]	Threshold
000	Reserved
001	25mV
010	50mV
011	100mV
100	200mV

7.2.10.3 0x84.[11:6] DOC

The Discharge Overcurrent threshold register sets the overcurrent threshold of a digital comparator. If the voltage across the current-sense resistor (DCSP, CCSP, and CSN Pins exceeds this threshold for more than 0x84.15 DOC/COC Delay discharge), fault bit 0x10.1 DOCF is set.

The setting ranges from 1mV to 51mV with a step size of 1mV and a default of 50mV. Setting above 51mV disables DOC detection.

7.2.10.4 0x84.[5:0] COC

The Charge Overcurrent threshold register sets the overcurrent threshold of a digital comparator. If the voltage across the current-sense resistor (DCSP, CCSP, and CSN Pins exceeds this threshold for more than 0x84.15 DOC/COC Delay discharge), fault bit 0x10.0 COCF is set.

The setting ranges from 1mV to 51mV with a step size of 1mV and a default of 50mV. Setting above 51mV is undefined and should be prevented.

8. I²C Serial Interface

The device includes a digital interface for users to configure the device operation and monitor parameters. The device is available to communicate to anytime the chip is not being reset. The device supports an I²C SMBus serial interface.

This device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master. The device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the device operates as the slave device in all applications.

The master sends command codes to perform block reads. The device does not support random sequential reads. A command code read is a block read with the starting register address and the number of bytes to read back digitally encoded into the device. Command codes support register read backs with and without CRC.

8.1 I²C Slave Address

The device can be can be used with any I²C host device. Each device must have its own unique serial address. The device supports packet error checking. Packet error checking is enabled by a separate slave address.

The slaves address for both CRC and non CRC packages are listed in Table 33.

Table 33. I²C Address Values

	Address (7-Bit Binary)
Packets without CRC	0010 010
Packets with CRC	1010 110

8.2 Communication Packet Format

The device communicates with a master that is complaint with the I²C protocol. The device processes read and write requests as word (2 byte) widths. A write action requires 2 bytes (word) of data to change the individual bits within the register. The minimum data width for a read command is two bytes.The device support command codes (see Command Codes) in place of sequential reads.

The ordering of the bytes is compliant to a Little Endian standard. The Little Endian has the 1st data byte containing data Bits 7 through 0 of the data byte word. The second data byte contain data Bits 15 through 8. The most significant bit within the byte is data Bit 7 for the first byte and data Bit 15 for the second byte. The least significant bit for each byte is data Bit 0 for the 1st bit and data Bit 8 for the second bit. The device processes the packet in byte widths. Reading a 0x8008 from a register has the device to sending the data byte 0x08 as the first byte and 0x80 as the second byte (overall 0x0880). Similar to reading, the write byte is ordered in the same manor. A register value of 0x12FE is sent to the device as 0xFE12. It is responsibility of the master to reverse the order of the bytes. Figure 21 illustrates the order of the data bytes for a read command. Figure 20 illustrates the order of the data bytes for a write command. See I²C Slave Address for more information on communicating to the device.

8.3 Cyclical Redundancy Check (CRC)

The device has a CRC (cyclical redundancy check) for securer communication between master and slave. The CRC code is a byte in length. The equation of the CRC is $X^8+X^2+X^1+1$. The CRC equation has a minimum Hamming Distance of 4 for payloads up to 247 bits. **Note:** If a NACK occurs during a CRC-enabled transmission, the CRC engine of the RAA489220 resets.

For Write commands, the register of the device is changed when the transmitted CRC byte by the master is the same in value as the CRC byte calculated by the slave (the device). When the two CRC bytes agree, the slave transmits an acknowledge bit (ACK) to the master. If the byte values do not agree, a NACK is transmitted is set.

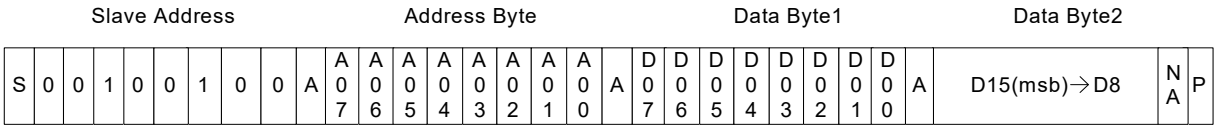


Figure 20. I²C Write Data Format

For Read commands, the slave sends CRC byte(s) as part of the read packet. It is the responsibility of the master to check the CRC byte versus the calculated CRC byte of the master. As part of the Read command, the master writes several bytes to indicate a Read command and to indicate which register value to reading from. For a read, the slave sends the master a CRC byte with the calculated value for the two slave address bytes, the address byte and the read word. Figure 27 and Figure 25, shows the read and write formats with a CRC byte.

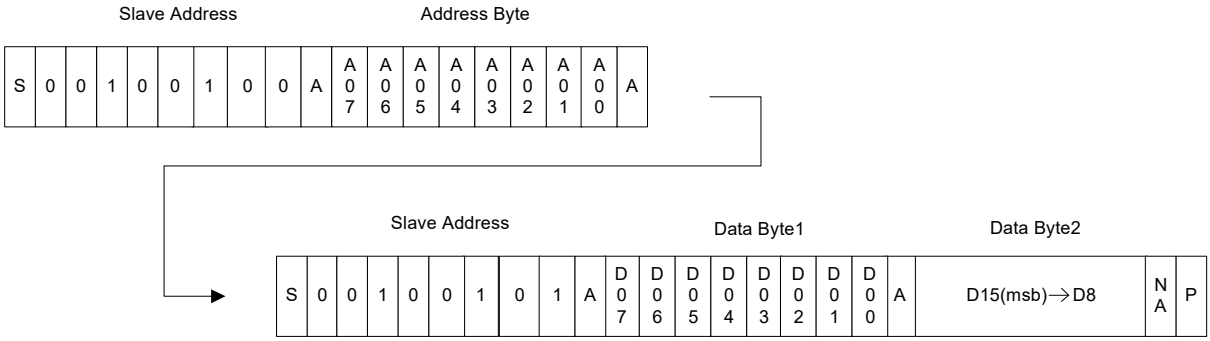


Figure 21. I²C Read Data Format

8.4 Protocol Conventions

The logic state on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 22). At power-up, the SDA pin is in the input Mode.

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 22). A START condition is ignored during the power-up sequence.

All I²C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH (see Figure 22). A STOP condition at the end of a Read operation, or at the end of a Write operation returns the I²C state machine to its initial state where it waits for the next START.

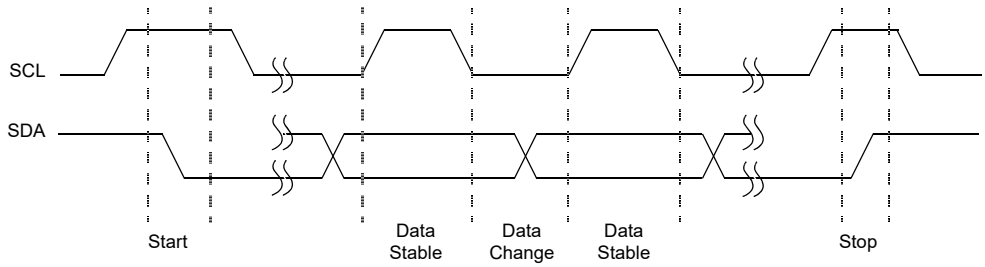


Figure 22. Valid Data Changes, Start, and Stop Conditions

An Acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 23). The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte and responds again after a successful receipt of the Register Address Byte. The device responds with an ACK after receiving each data byte of a write operation. The device indicates that the maximum number bytes have been received for a write packet by sending a NACK to the master. The master then sends a Stop bit to terminate the packet.

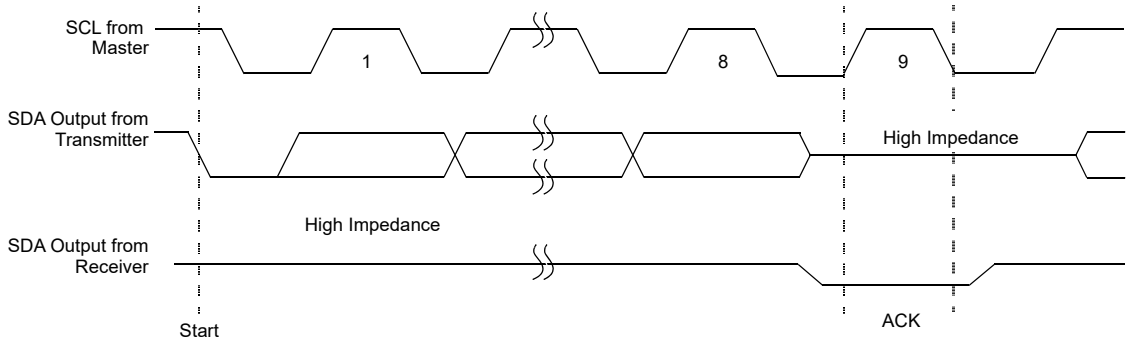


Figure 23. Acknowledge Response from Receiver

For a read packet, the device sends an ACK after each byte sent by the master. The master sends an ACK bit following every byte transmitted by the device. The master sends a NACK bit after the final read back byte. The slave then sends a Stop bit to terminate the packet.

The last bit of the Slave Address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a 1, a Read operation is selected. A 0 selects a Write operation (see Figure 24).

After loading the entire Slave Address byte from the SDA bus, the device compares it with the internal Slave Address. When a correct compare occurs, the device outputs an acknowledge on the SDA line.

8.4.1 Write Operation

A Write operation requires a START condition, followed by a Slave Address byte, a Register Address byte, a word of Data, and a STOP condition (see Figure 24). The slave device responds with an ACK after successfully receiving each of the four bytes. The content of the word of Data is transferred to the device register at the SCL pin rising edge during the ACK and a successful comparison of the master's CRC byte versus the internally calculated CRC byte.

8.4.2 Write to Protected Registers 0x80-0x84

The write protected registers 0x80 through 0x84 have defaults set at the factory, but can be written by the MCU when unlocked for the write operation. First, Renesas recommends writing 0x0000 to register 0x6F to reset the unlock engine. Next, the following three codes must be written to register 0x6F in order: 0x6F9C, 0x70A5, and 0x48E1. Keep in mind the device expects data in LSB – MSB format. When registers 0x80-0x84 have been modified, Renesas recommends writing a 0x0000 to register 0x6F to reset the lock to avoid unintentional modification of these settings.

The keys must be in sequence, and any new writes of other values lockout the write function. This added protection prevents inadvertent writes that could change protection thresholds or configured device operation.

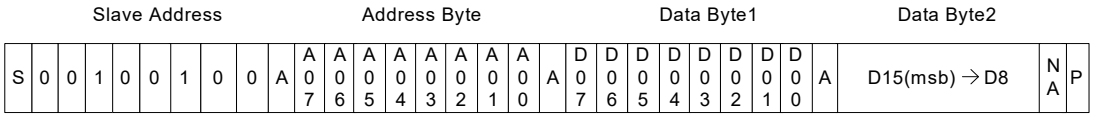


Figure 24. I²C Write Format

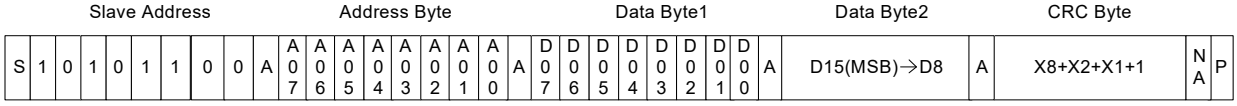


Figure 25. I²C Write Format with CRC

8.4.3 Read Operation

A Read operation consists of a 3-byte sequence, followed by one word of Data (see Figure 26). The master initiates the read operation by sending the following sequence of bits: a START bit, the Slave Address byte with the R/W bit set to 0, a Register Address byte, a second START bit, and a second Slave Address byte with the same seven MSBs but with the R/W bit set to 1. After each of the four bytes, the device responds with an ACK. The device transmits the word of Data followed by a CRC byte (if enabled) for as long as the master responds with an ACK. The ACK bit occurs on the rising edge of the SCL pin for every 8-bits transmitted. The master terminates the Read operation by issuing a NACK, and then a STOP condition.

The Data words received from the slave are from the memory location indicated by an internal pointer. This initial value of the pointer is determined by the address byte in the Read operation instruction, and it increments by one during transmission of each word of Data.

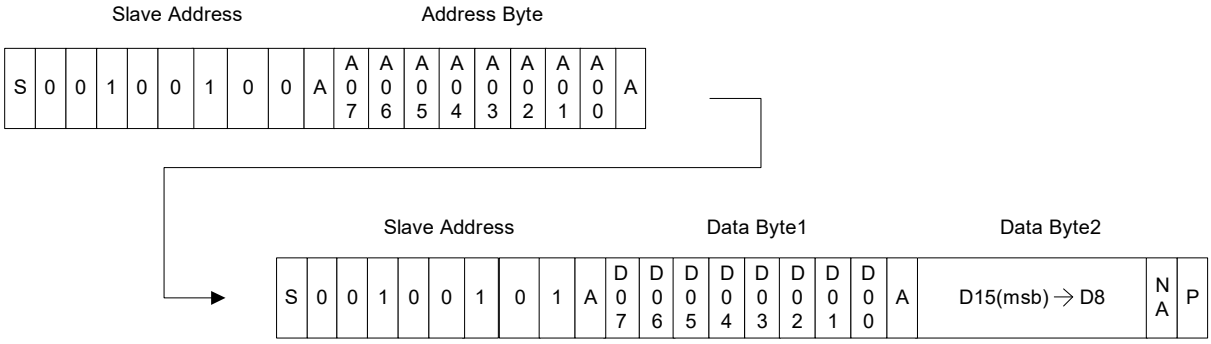


Figure 26. I²C Read Format

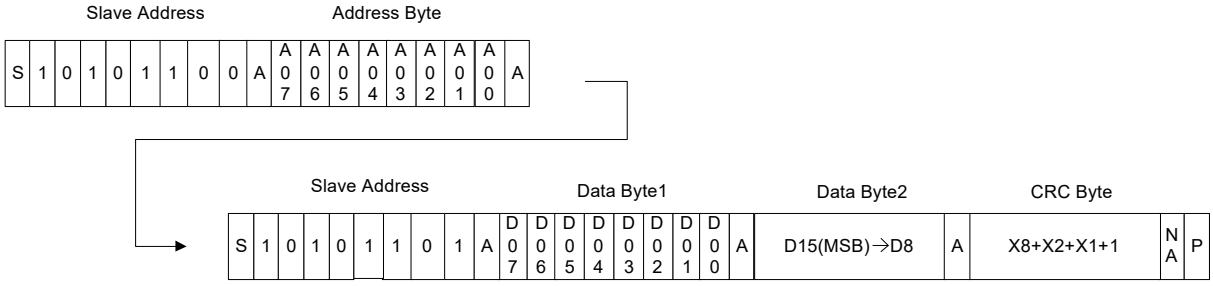


Figure 27. I²C Read Format with CRC

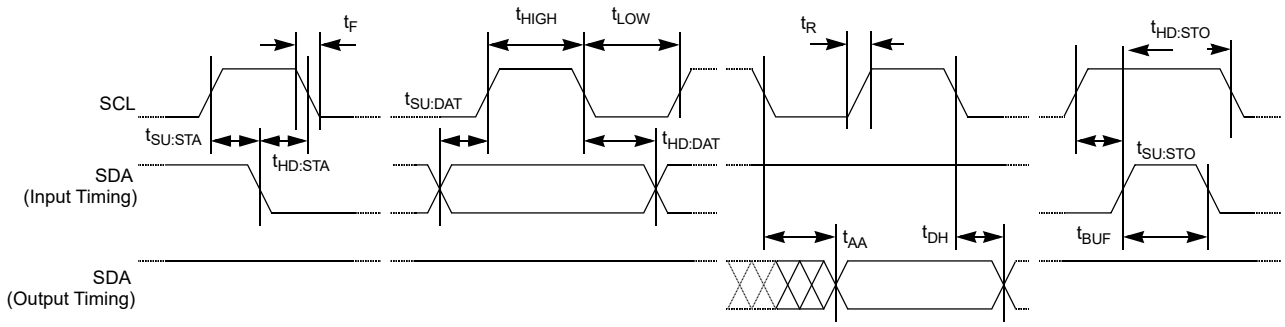


Figure 28. I²C Timing

8.4.4 Command Codes

Command codes are block reads that have the starting read register address and the number of bytes to read back digitally encoded into the device. Table 34 defines each command code and the registers that are read back. The use of command codes is faster than individually reading each register.

A Fault and Status command received by the device while the $\overline{\text{ALERT}}$ pin is sticky results in the $\overline{\text{ALERT}}$ pin able to change state freely. See LDFET Pin for more information on how the $\overline{\text{ALERT}}$ pin interacts with the Fault and Status command code.

Table 34. Command Codes and Read Times

Reg Addr (Hex)	Register Name	Start Addr (Hex)	End Addr (Hex)	Num Of bytes	Read Time (100kbs) (ms)	Registers Read Back
C1	Fault and Status	10	11	3+4	0.84	Read Fault and Status
C2	Read Measurements	00	06	3+14	1.74	VPACK, V_{Cell_max}, V_{Cell_min}, THERM1, THERM2, $I_{discharge}$ and I_{charge}
C3	I_{PACK}	05	06	3+4	0.84	$I_{discharge}$ and I_{charge}

Figure 29 and Figure 30 are the packet formats for command codes. The command codes support CRC. The CRC byte value is calculated from the value of each register word read back, the two slave addresses and the command code. The calculation of the CRC is processed from the first slave address byte to the final byte that is read back.

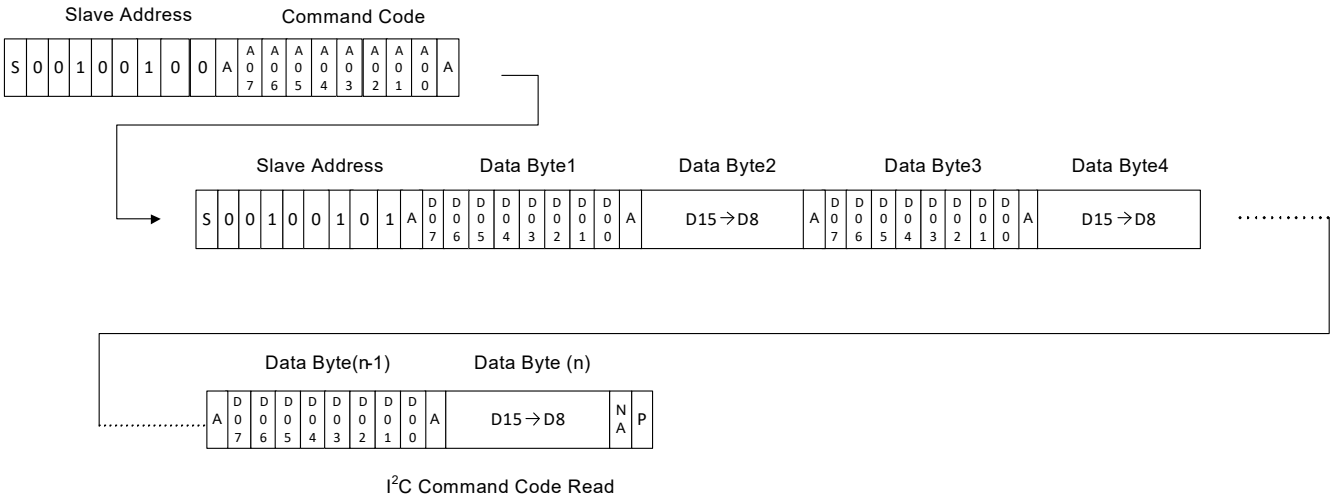


Figure 29. I²C Command Code Read Format

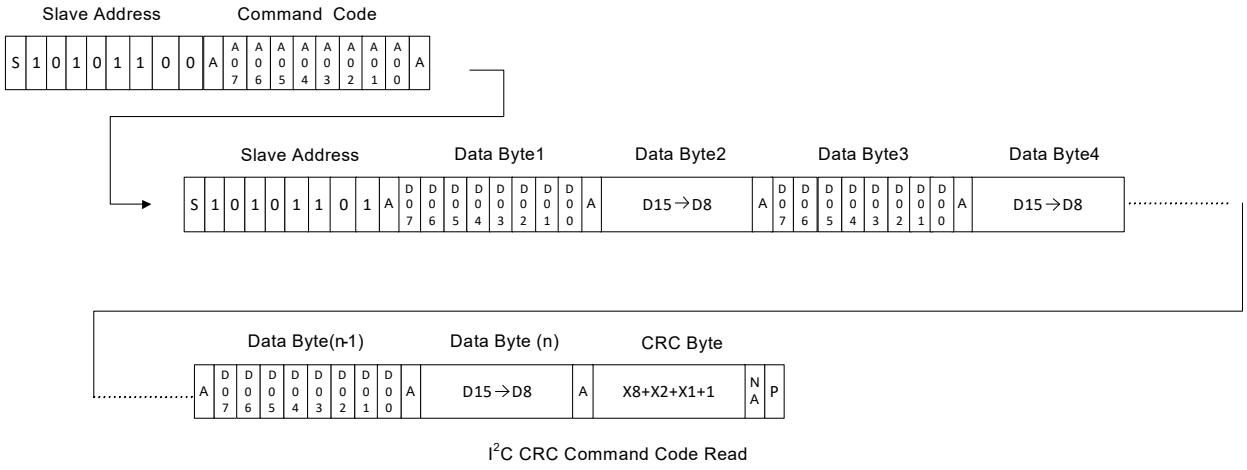


Figure 30. I²C Command Code Read Format with CRC

9. Pins

9.1 VCn Pins

The VCn pins are the voltage sense inputs of the device that are connected in pairs to differentially measure each cell voltage. Positive pin VC_n and negative pin VC_{n-1} are connected to the ADC through a multiplexer. Each voltage sense input uses an external filter to protect against battery voltage transients. The basic input filter structure provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. Place any vias in line to the signal inputs so that the inductance of these forms a low-pass filter with the grounded capacitors.

The filtered battery cell voltages internally connects to the cell voltage monitoring system. The monitoring system contains a multiplexer to select a specific input, and an analog to digital converter.

Figure 31 illustrates a typical V_{CELL} filter connection for the device. The differential capacitance (C_{Diff}) should be 0.1µF. The isolation resistance (R_{ISO}) should be 1kΩ. Using values greater than what is recommend can result in measurement accuracy errors or open connection test faults, lesser values could reduce Hot Plug tolerance.

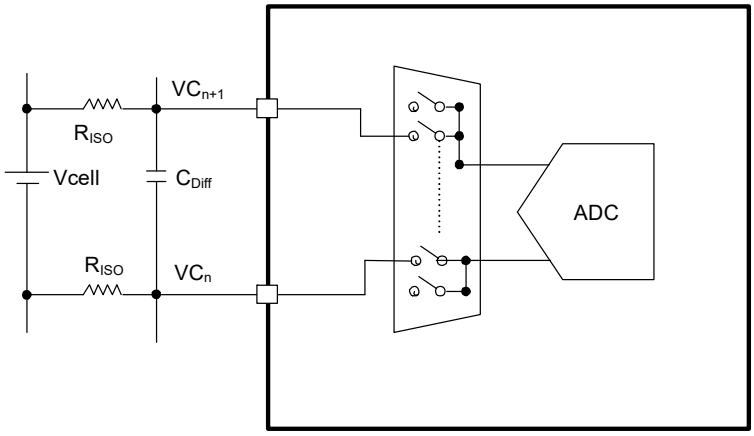


Figure 31. Voltage Sense Pin Connections

9.1.1 Open Wire on VCn Pins

The device performs an open-wire test by turning ON a 275µA current source reference to VSS for each active VCn pin simultaneously. A VCn pin is active depending on the number of series cells the device is configured for. The current source on time is 10ms. After 7ms from turning ON the pin current, the device performs a VCell scan to measure the cell voltages of the pack while current is being drawn from the pin. The cells are measured starting at cell 1 and proceeding to the top cell of the pack. If a cell reading measures below 0.6V (0x058), an internal flag is set. The open-wire test has to fail two times consecutively before the OWF bit is set 1. The open-wire test is performed in the Self Test Loop of the system scan. The open wire only reports if any of the cell open-wire tests fail. To specifically find the open-wire pin that failed, use the VC pin current register (0x43) to individually turn ON the pin current source and perform a VCell/VPACK read. Below is a simplified current schematic for the open-wire (Cells) functionality.

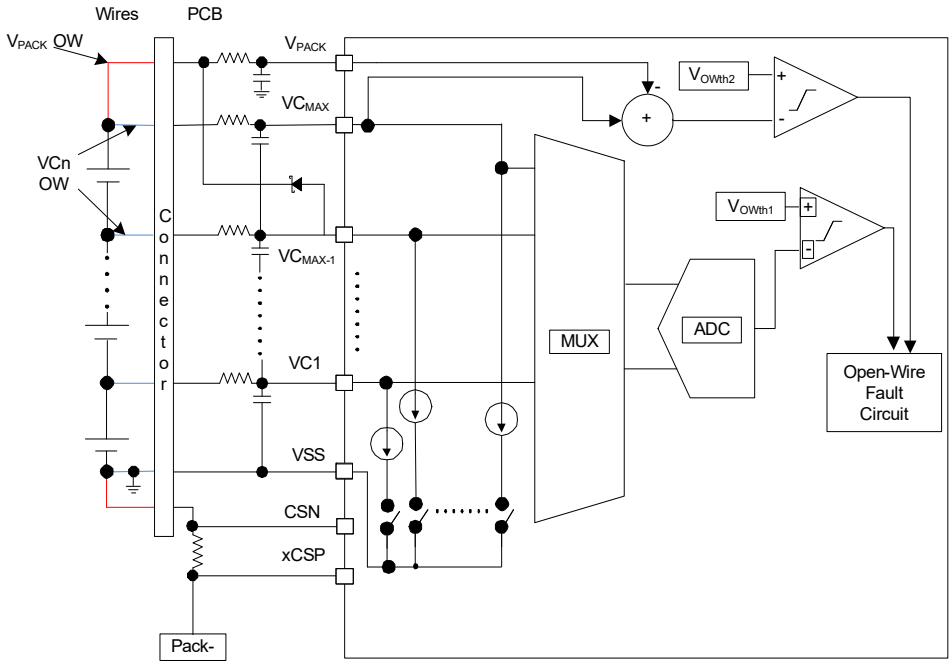


Figure 32. Simplified Open-Wire Cell Circuitry

9.2 VPACK Pin

The VPACK pin is the main power connection to the device. Connect a 10µF bypass cap to ground at the pin (Figure 32). The filter time constant for the VPACK pin should match the VCn pin filters.

9.3 HVGPIO Pin

The HVGPIO pin is a high voltage general purpose input output pin. Internally, the HVGPIO pin is connected to an open-drain NMOS, and the source is tied to VSS. When the control bit is enabled (0x40.3 HVGPIO Pin Assert), the NMOS makes a low-impedance path to VSS; otherwise, it is a high impedance. The pin state is monitored to indicate its status with bit 0x40.11 HVGPIO Status.

This pin can be used for fuse blowing to drive an LED or as an input when using an MCU. See the example fuse connection in Figure 1. Mask bit 0x11.14 HVGPIO Mask connects the pin state to specific faults.

9.4 V3P3 Regulator and GATE Pins

The device has an internal regulator that uses an external power transistor to provide regulated voltages for its internal circuits. The output of this regulator also powers other system circuitry, including the microcontroller.

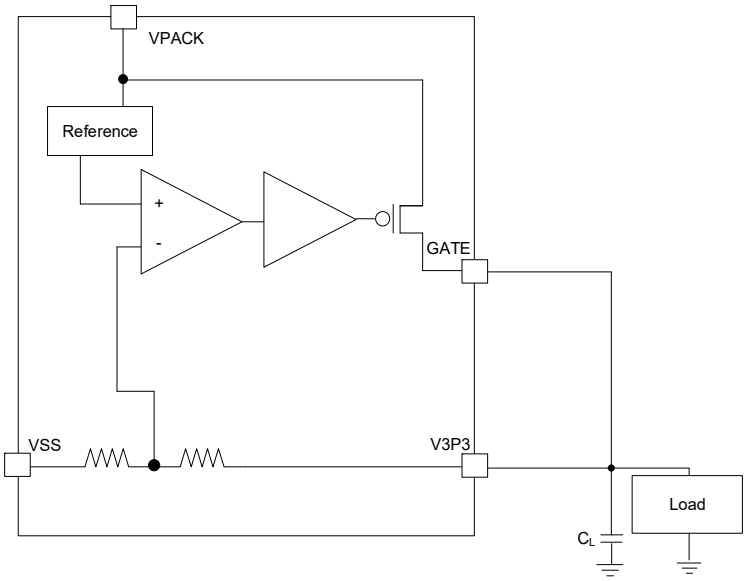


Figure 33. External Power Supply Components

9.4.1 V3P3 Pin

The V3P3 pin is the analog 3.3V power supply input and is the analog feedback node for the regulator control circuit and internal analog supply. Connect a 2.2µF bypass capacitor from V3P3 to the analog ground (AGND) pin.

9.4.2 GATE Pin

The GATE Pin drives the analog 3.3V pin power.

9.5 V2P5 Pin

The V2P5 pin is the internal 2.5V digital power supply. The V2P5 power is derived from the V3P3 pin. External connections must be limited to a decoupling capacitor to DGND. This pin is for internal use only. Do not load or drive this pin from an external source. Connect a 1µF to 10µF capacitor to the digital ground (DGND) pin.

9.6 DGND Pin

DGND is the digital ground reference pin for the device. It must have a solid connection to the digital ground plane. If separate digital and analog ground planes are used, they should be connected together at the VSS pin.

9.7 $\overline{\text{ALERT}}$ Pin

The $\overline{\text{ALERT}}$ pin is an active low open-drain digital output pin that indicates either a fault or status bit change has occurred. A pull-up of >4.7kΩ to V3P3 or the MCU supply is necessary. Any fault that turns OFF both power FETs forces a transition to LP Mode 100ms after asserting the $\overline{\text{ALERT}}$ pin low. The time delay allows the MCU to read the fault and status registers before entering LP Mode. This pin is a high impedance while in LP Mode.

If more than one fault or status bit is asserted before reading the Fault and Status registers, the $\overline{\text{ALERT}}$ pin is released and re-asserted after the first read. The device requires the Fault and Status registers to be read a second time before releasing the $\overline{\text{ALERT}}$ pin, which is specific to cases with more than one fault/status bit assertion (0x81 OV and EOC Thresholds and 0x81 OV and EOC Thresholds).

Figure 34 shows timing diagrams for different Fault or Status bit sequencing scenarios. Figure 34(A) shows an example of two fault or status changes before a read. In this case, an OV detection sets OVF then the OV clears before a read. Each OVF and OV clearing causes a separate assertion of the $\overline{\text{ALERT}}$ pin. Figure 34(B) is an example of single persistent fault or status bit change, each followed a read that releases ALERT.

All fault and status bits that are connected to the $\overline{\text{ALERT}}$ pin are logically OR'd. A Status bit that has a masked bit that is enabled prevents the bit connection to the $\overline{\text{ALERT}}$ pin.

Reading the Fault and Status registers individually does not release the $\overline{\text{ALERT}}$ pin, both must be read sequentially. A sequential read without starting at the fault register (0x10) does not release the $\overline{\text{ALERT}}$ pin.

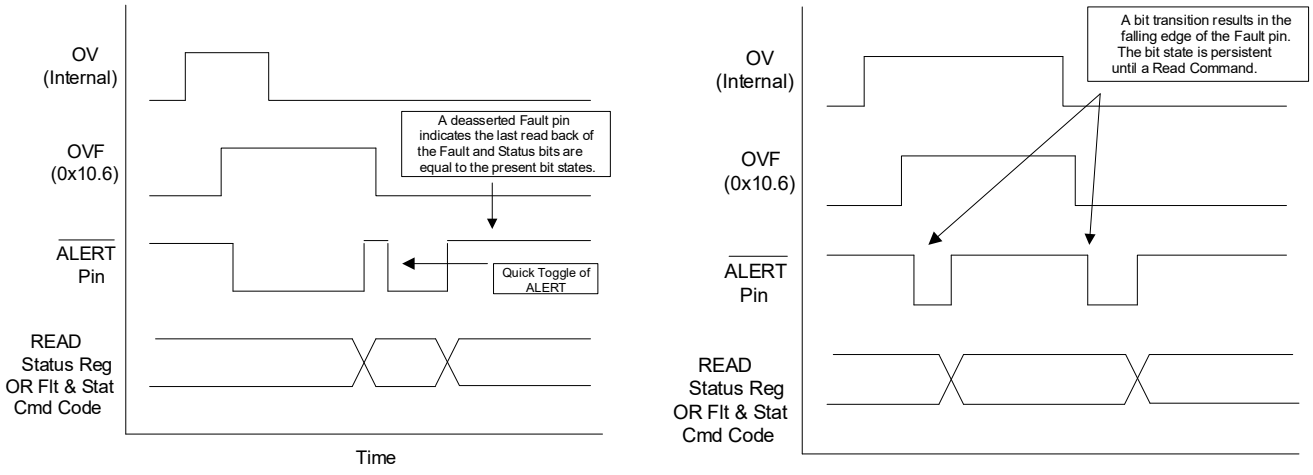


Figure 34. Fault Timing Diagrams

9.8 SCL Pin

The SCL pin is the communications clock pin driven by the master for I^2C communications protocol. Connect an optional minimum 4.7kΩ valued resistor from the pin to V3P3 ensuring it is pulled high in LP Mode so that the wakeup with communication works properly. If the MCU has a push-pull output and ensures this is high, the resistor can be omitted to save power.

9.9 SDA Pin

The SDA pin is the serial data pin for bidirectional communications between master and slave for the I^2C communications protocols. It is driven by the master for sending a slave address byte for write commands. In this mode, the device pin is an open drain. The pin is driven by the slave for data reads. Connect a minimum 4.7kΩ valued resistor from the pin to V3P3.

9.10 VTEMP and THERM Pins

THERM pins are analog voltage inputs that connect to thermistor circuitry. These pins are optimized to work with external NTC thermistors to monitor the temperature of the battery pack. The thermistors are biased by the VTEMP output, as shown in Figure 35.

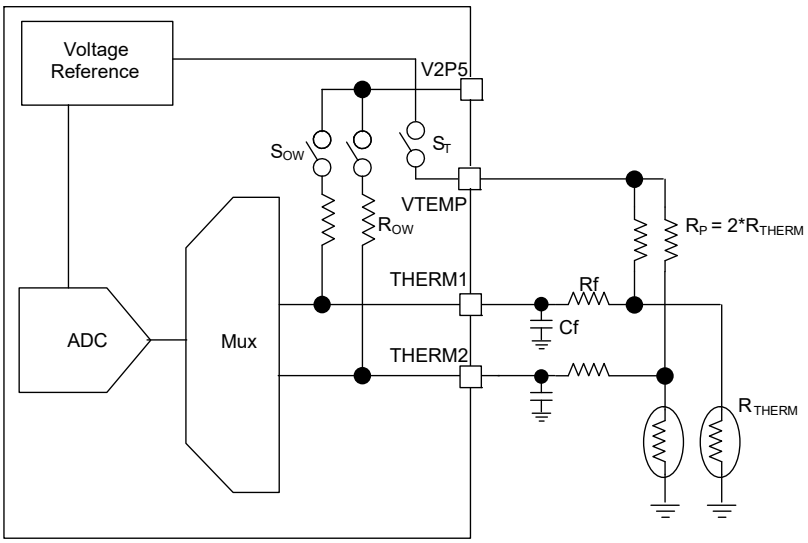


Figure 35. Thermistor Pin Configuration

The Thermistor inputs are sampled as part of the system scan sequence (Figure 18). Before measuring the thermistors, the internal switch S_T is closed, connecting the two pull-up resistors R_P through the VTEMP pin to the reference voltage. This sets up a pair of voltage dividers consisting of R_P and R_{THERM}. The voltage between these resistors is a function of the temperature (R_{THERM}). From the thermistor, optional low-pass filters consisting of Rf and Cf connects to each THERM pin. Each of these pins is then measured in sequence relative to VSS. Switches S_{OW} are used only for an open-wire test as part of the Self Test Loop.

9.10.1 Hard RESET

A hard reset is initiated by connecting the THERM2 pin above the reset threshold voltage RST_{VTHERM} for t_{RESET} time. The Reset voltage threshold is defined with respect to (above) the voltage on the V2P5 pin. A switch with terminals connecting the THERM2 and the V3P3 pin is used on the evaluation boards. The Reset state is exited ~2ms after the voltage (falling edge) on THERM2 pin drops below ~2.6V.

9.10.2 Thermistor Pins Open-Wire Test

The Thermistor pins are tested for open wires in the Self Test Loop of the system scan. If the measured result exceeds threshold 0x0FD7 for two consecutive tests, the device sets bit 0x10.12 VTMPF to 1. The thermistor divider network must be chosen to remain below the open-wire threshold over the range of operation.

9.11 LDMON Pin

The Load Monitor pin detects a voltage above the VPACK - V_{LDTHR} (page 11) threshold. This pin is intended to be connected to the negative terminal of the load for load detection. A 1M internal pull-down resistor biases the voltage on the pin below the threshold.

The pin state is available for read back as bit 0x11.2 LD PRESI. A LD PRESI bit value of 1 indicates the voltage is above threshold VPACK - V_{LDTHR}.

The device monitors for a rising edge, except for the 100ms period following shutoff of LDFET. The device exits LP Mode on detection of the rising edge of the pin voltage.

9.12 CHMON Pin

The Charge Monitor pin detects the falling edge of the node voltage when below threshold V_{CHTHR} (page 11). This pin is intended to be connected to the negative terminal of the charger to allow for charger detection. A 1M internal pull-down resistor biases the voltage on the pin if left open to below the threshold.

The pin state is available for read back as bit 0x11.3 CH PRESI. A CH PRESI bit value of 1 indicates the voltage is below threshold V_{CHTHR}.

The device monitors for a falling edge of the pin and a rising edge of the CH PRESI bit, except for the 100ms period following shutoff of LCFET. The device exits LP Mode on detection of the falling edge of the pin voltage (rising edge of the CH PRESI bit).

9.13 LCFET Pin

The low-side charge FET pin controls the low-side power FET (0x40.0 LCFET En). When enabled, the pin drives the NMOS gate high ($LxFET_{GV}$) to turn it ON. The pin is tied internally to VSS through a 2.5k resistor for 500µs then becomes high-impedance (see R_{LCFET_OFF}) when shut off or a relevant fault is detected.

9.14 LDFET Pin

The low-side discharge FET pin controls the low-side power FET (0x40.1 LDFET En). When enabled, the pin drives the NMOS gate high ($LxFET_{GV}$) to turn it ON. When a relevant fault is detected, the pin is tied internally to VSS through a 2.5k resistor.

9.15 DCSP, CCSP, and CSN Pins

Current is monitored by measuring the differential voltage across a current-sense resistor connected between the CCSP or DCSP and CSN pins as shown in Figure 36. The current-sense circuit individually monitors charge and discharge currents. Both charge (CCSP-CSN) and discharge (DCSP-CSN) currents are measured every system scan. Current measurements are interlaced with the other measurements during the system scan.

The Charge Current Sense Positive (CCSP) pin is connected to the CHARGE- terminal for split current sense (0x82.7 CPWR = 1) applications. The CCSP pin is connected to the source pin of the LDFET for shared current sense (CPWR = 0) applications.

The Discharge Current Sense Positive (DCSP) pin is connected to the source of the DFET.

The Current Sense Negative (CSN) pin is connected to BAT- (VSS and ground), the most negative voltage of the pack.

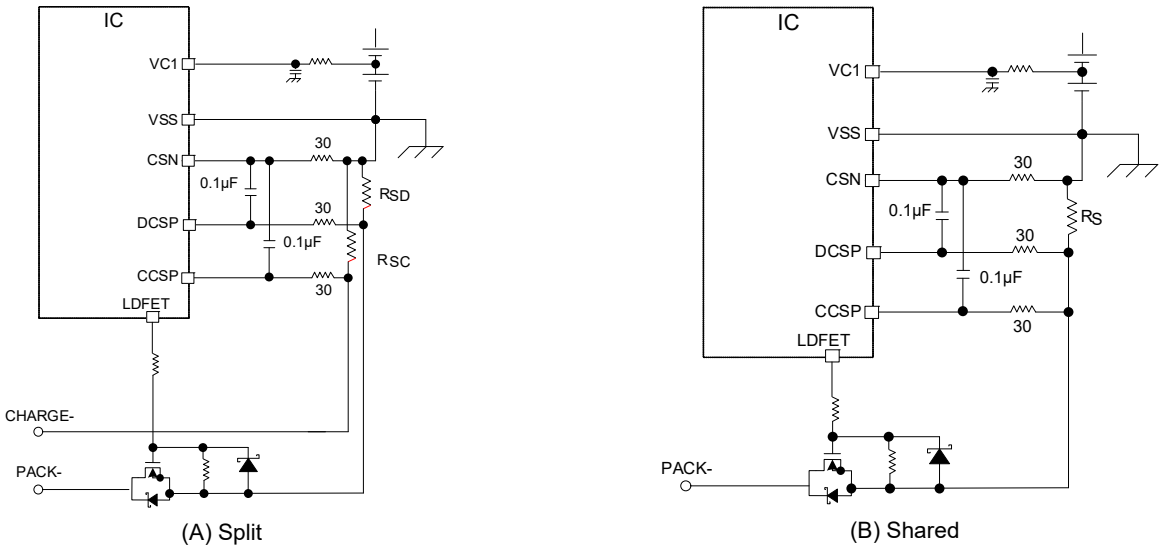


Figure 36. Current Sense

Recommended component values for the current monitor circuitry are shown in Figure 36. The 30Ω resistor is chosen to filter system noise and to minimize measurement errors.

The value of the current-sense resistor is application specific and must be determined based on peak and nominal load currents, charge current, and end-of-charge current detection (0x11.4 IEOC).

Renesas does not recommend operating at the extreme limits of the inputs. In an application, care should be taken to guard-band against additional noise and transients that can cause current levels to reach or exceed the maximum voltages.

9.16 VSS Pin

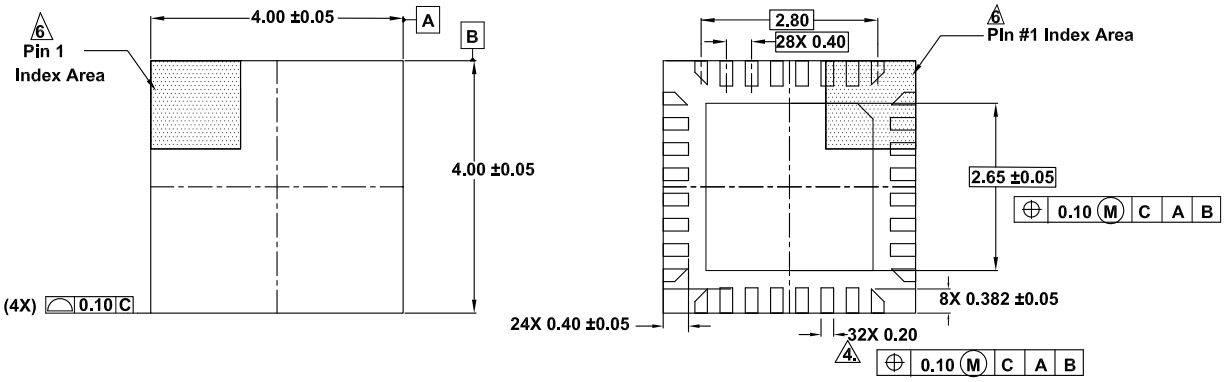
VSS is the analog ground pin. It must have a solid connection to the ground plane(s). The digital and analog ground planes should connect together as close to the VSS pin as possible. Never connect the exposed pad to any other signal other than VSS. Multiple vias are recommended for good thermal conductivity. The PCB footprint should always have an EPAD landing. Soldering to the EPAD also provides mechanical stability.

10. Package Outline Drawing

For the most recent package outline drawing, see L32.4x4C.

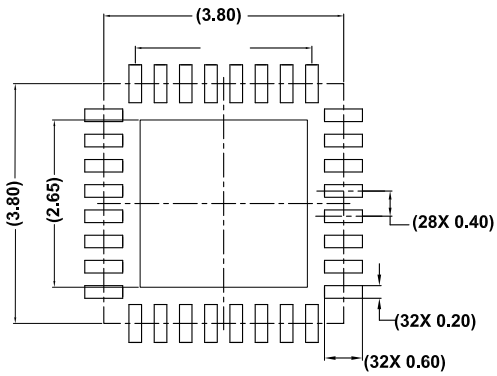
L32.4x4C

32 Lead Quad Flat No-Lead Plastic Package (QFN)
Rev 2, 4/2022

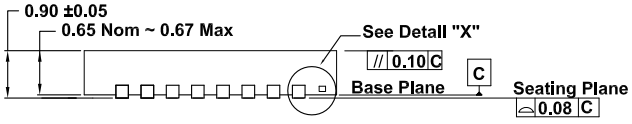


Top View

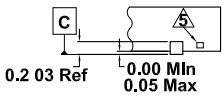
Bottom View



Typical Recommended Land Pattern



Side View



Detail "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

11. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA489220AGNP#HA5	489220 AGNP	32 LD 4x4 QFN	L32.4x4C	Reel, 6k	-40 to +85°C
RAA489220AGNP#MA5				Reel, 1k	
RAA489220AGNP#AA5				Tray	
RTKA489220DK0000BU	Evaluation Kit				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA489220 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 35. Key Differences Between Family of Parts

Part Number	Cells Supported		Pack Voltage (Op V)		Cell Bal.	I_{PACK} Sense	Fuel Gauge	Charge/ Discharge FET		Supply Current (A)		Stand Alone	Int. MCU	Int. ADC	Daisy Chain
	Min	Max	Min	Max				Ctrl	Loc.	Norm.	Sleep				
RAA489220	4	10	6	44	No	Low Side	No	Yes	Low Side	110µ	2µ	Yes	No	12b	No
RAJ240310	3	10	8	50	Both	Low Side	Yes	Yes	Low Side	50µ	1µ	Yes	Yes	15b/ 18b	No
RAJ240100	3	10	4	50	Both	Low Side	Yes	Yes	High Side	50µ	1µ	Yes	Yes	15b/ 18b	No
RAJ240090	3	8	4	50	Both	Low Side	Yes	Yes	High Side	50µ	1µ	Yes	Yes	15b/ 18b	No
RAJ240080	2	5	4	28	Both	Low Side	Yes	Yes	High Side	50µ	1µ	Yes	Yes	15b/ 18b	No
ISL94216	4	16	12	55	Both	Low Side	No	Yes	Both [1]	200µ	10u	No	No	16b	No
ISL94212	6	12	6	60	Ext.	No	No	No	N/A	3.31m	12µ	No	No	14b	Yes
ISL94208	4	6	8	27	Both	Low Side	No	Yes	Low Side	850µ	2µ	No	No	No	No
ISL94202	3	8	4	36	Ext.	High Side	No	Yes	High Side	348µ	13µ	Yes	No	14b	No

1. GPIO can be configured to support low side C/DFETs.

12. Revision History

Revision	Date	Description
1.00	Jul 27, 2022	Initial release.