RAA808013

2.7V to 5.5V Input, 3A Synchronous Buck Regulator

The RAA808013 is a 3A synchronous buck regulator with an input range of 2.7V to 5.5V. It provides an easy-to-use, high-efficiency low BOM count solution for a variety of applications.

The RAA808013 integrates both high-side and low-side MOSFETs and features a PFM mode for improved efficiency at light loads.

The RAA808013 adopts Constant On-Time (COT) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The part switches at a default frequency of 1.5MHz.

The RAA808013 can switch between constant on-time control and constant off-time control smoothly and can also switch between constant off-time control and 100% Duty Cycle smoothly with V_{IN} voltage changing.

With the wide VIN range and reduced BOM, the part provides an easy-to-implement design solution for a variety of applications while giving superior performance. It provides a robust design for high voltage industrial applications and an efficient solution for battery-powered applications.

The part is available in a small TSOT23-6 plastic package with an operation junction temperature range of -40°C to +125°C.

Features

- 2.7V to 5.5V operating input range
- 3A output current
- Output adjustable from 0.6V
- 100% duty cycle in dropout
- 77mΩ and 42mΩ internal power MOSFET switches
- High switching frequency (1.5MHz)
- EN for power sequencing
- Internal soft-start
- Cycle-by-cycle overcurrent protection (7 times)
- OCP and SCP with hiccup mode
- Input undervoltage lockout (UVLO)
- Over-temperature protection
- Small TSOT23-6 package

Applications

- Low-voltage, high-density power system
- Point-of-load regulation for high-performance DSPs, FPGAs, ASICs, and microprocessors
- Broadband, networking, and optical
- Communications infrastructure
- Portable instruments and battery-powered devices
- Solid-state drives (SSD)
- Industrial and medical equipment
- Gaming, DTV, and set-top boxes

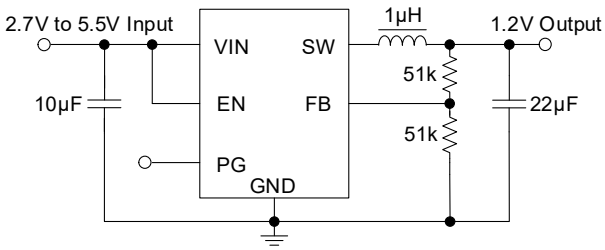


Figure 1. Typical Application

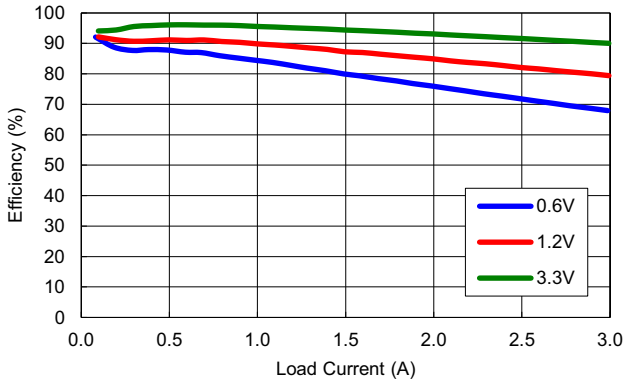


Figure 2. Efficiency vs Load, L = 1.0µH, V_{IN} = 5V

Contents

1. Overview

1.1 Typical Application Circuits

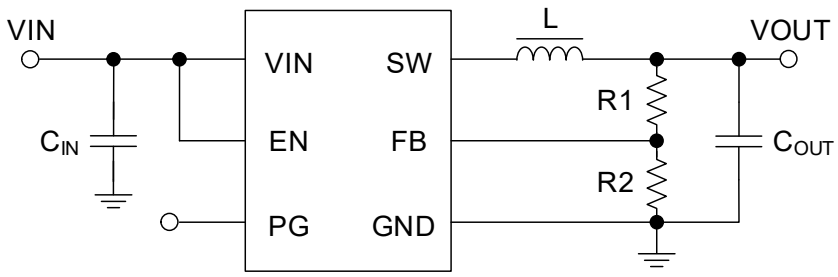


Figure 3. External Default Parameter Selection

Table 1. External Component Selection

V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_1 (kΩ)	R_2 (kΩ)
0.6	1	22x2	0	51
	2.2	22		
1.0	1	22x2	34	51
	2.2	22		
1.2	1	22	51	51
	2.2	10		
1.8	1	22	102	51
	2.2	10		
2.5	1	22	162	51
	2.2	10		
3.3	1	22	229	51
	2.2	10		

1.2 Block Diagram

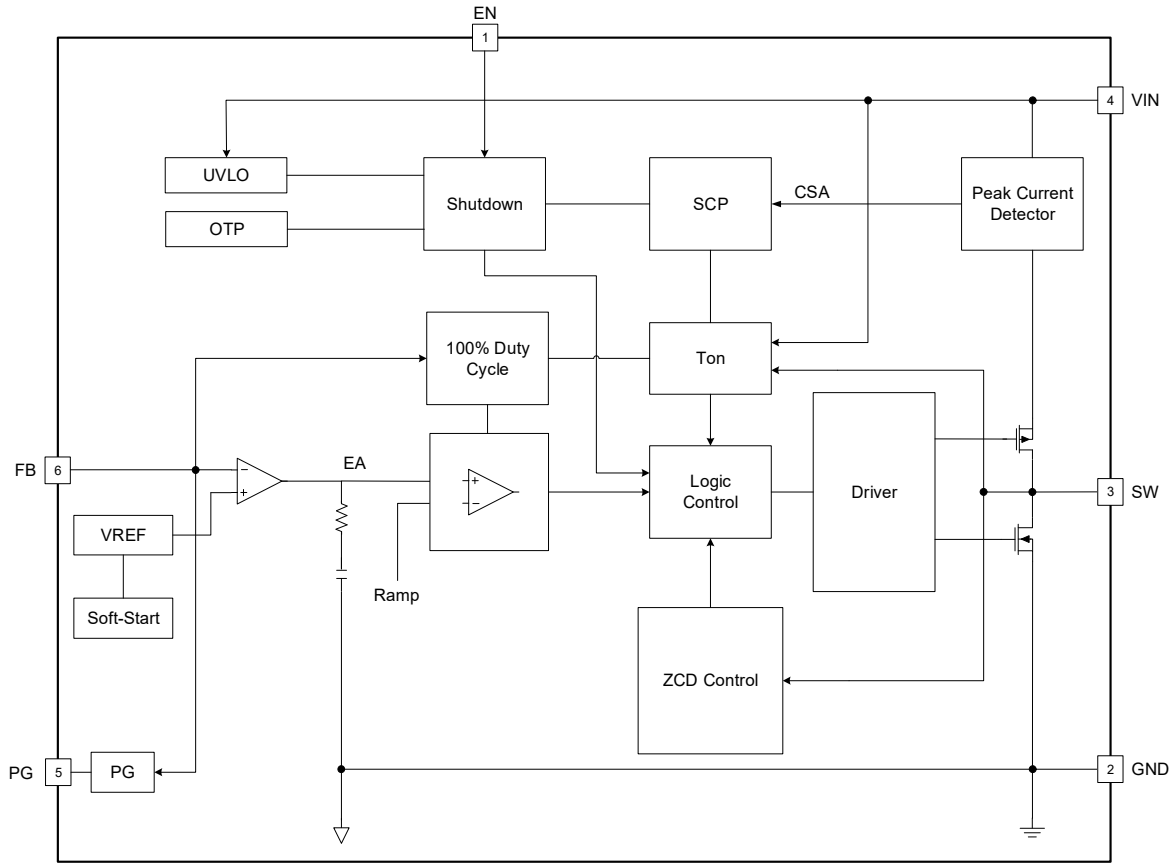
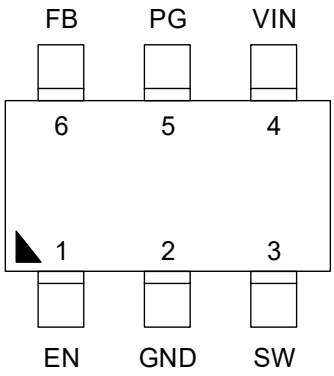


Figure 4. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



TOP View

2.2 Pin Descriptions

Pin Name	Number	Description
EN	1	Enable control input.
GND	2	Ground pin.
SW	3	Switch Node.
VIN	4	Supply voltage. The IC operates from a +2.7V to +5.5V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
PG	5	Power-good indicator. The output of this pin is an open-drain with an external pull-up resistor. PG is in high-impedance when FB is higher than the typical 0.54V. Otherwise, it is pulled low.
FB	6	Feedback pin, 0.6V ±3.5% across temperature range of -40 to 125°C.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN to GND	-0.3	+6	V
SW to GND (DC)	-0.3	V_{IN} + 0.3	V
SW to GND (20ns)	-4	+7	V
EN to GND	-0.3	V_{IN} + 0.3	V
FB to GND	-0.3	V_{IN} + 0.3	V
PG to GND	-0.3	V_{IN} + 0.3	V
VOUT to GND (DC)	-0.3	V_{IN} + 0.3	V

3.2 ESD Ratings

ESD Rating	Value	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
TSOT23-6 Package	112	45

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Ambient Temperature Range	-40	+125	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	2.7	5.5	V
Ambient Temperature	-40	+125	°C
Output Voltage, V_{OUT}	0.6	5.5	V

3.5 Electrical Specifications

Typical operating conditions at 25°C, V_{IN} = 5V, T_J = -40 to +125 °C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +125°C)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Supply Voltage						
V_{IN} Voltage Range	V_{IN}		**2.7**		**5.5**	V
Undervoltage Lockout Threshold Rising	V_{INUV_rise}				**2.65**	V
Undervoltage Lockout Threshold Hysteresis	V_{INUV_hys}			60		mV
V_{IN} Quiescent Supply Current	I_Q			52	**67**	µA
V_{IN} Shutdown Supply Current	I_{SD}	V_{EN} = 0V, V_{IN} = 5V, T_J = 25°C[2]			1	µA
Feedback Voltage						
Feedback Voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 5.5V, T_J = 25°C	0.588	0.6	0.612	V
		T_J = -40°C to +125°C	**-3.5**		**3.5**	%
Feedback Current	I_{FB_leak}	V_{FB} = 0.6V		10		nA
Soft-Start						
Internal Soft-Start Ramp Time	t_{SS}			0.8		ms
Internal MOSFET						
PFET Switch On-Resistance	r_{DSON_P}	V_{IN} = 5V, I_{RMS} = 0.3A, T_J = 25°C		77		mΩ
NFET Switch On-Resistance	r_{DSON_N}			42		mΩ
SWITCHING						
Nominal Switching Frequency	F_S			1.5		MHz
On-Time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		160		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		222		ns
Minimum Off-Time	t_{OFF_MIN}	T_J = -40°C to +125°C		130		ns
Minimum On-Time[3]	t_{ON_MIN}	T_J = -40°C to +125°C		120		ns
Power-Good						
PG Threshold - VFB Rising				90		%
PG Threshold - VFB Falling				85		%
Power-Good Sink Current Capability	V_{PG_L}	I_{SINK} = 1mA, T_J = 25°C			0.4	V
PG Internal Pull-Up Resistor	R_{PG}	V_{EN} = V_{IN}=2.7V, V_{FB} = 0.6V		500		kΩ
Enable Voltage						
Input Threshold		Falling Edge, Logic Low			**0.4**	V
		Rising Edge, Logic High	**1.2**			V
EN Logic Input Leakage Current		V_{EN} = 2V		1		µA
		V_{EN} = 0V		0		µA

Typical operating conditions at 25°C, V_{IN} = 5V, T_J = -40 to +125 °C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +125°C)** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Fault Protection						
Peak Current Limited	I_{peak}		**3.7**[4]	4.6		A
Hiccup Time				3.6		ms
Zero Cross Threshold	I_{ZCD}			50		mA
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		160		°C
	T_{HYS}	Hysteresis		15		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Test Condition: V_{IN} = 5V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
3. Minimum On-Time required to maintain loop stability.
4. Compliance to limits is assured by design.

4. Typical Performance Graphs

4.1 Buck Efficiency Curves

L=1µH, C_{out}=22µF, T_A = +25°C

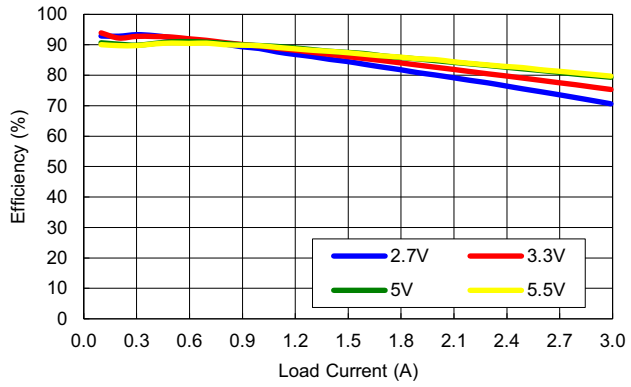


Figure 5. Efficiency vs Load, V_{OUT} = 1.2V

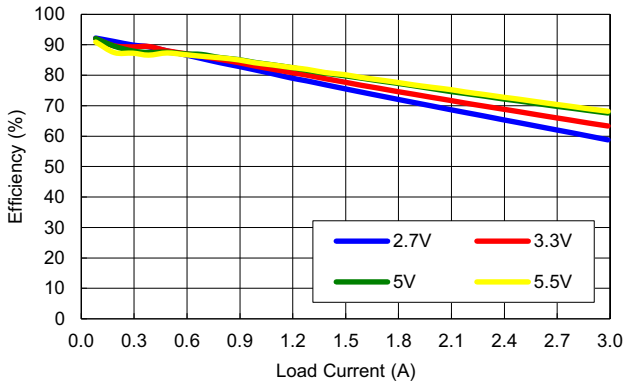


Figure 6. Efficiency vs Load, V_{OUT} = 0.6V

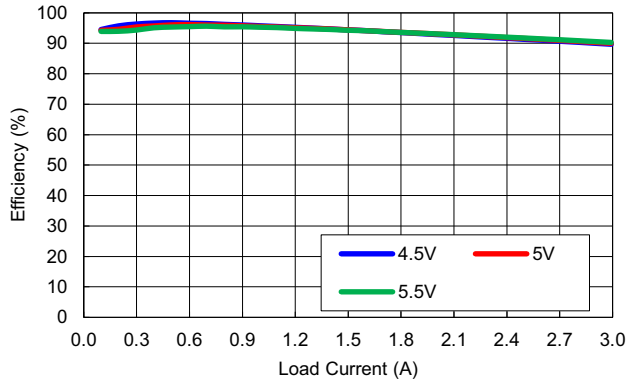


Figure 7. Efficiency vs Load, V_{OUT} = 3.3V

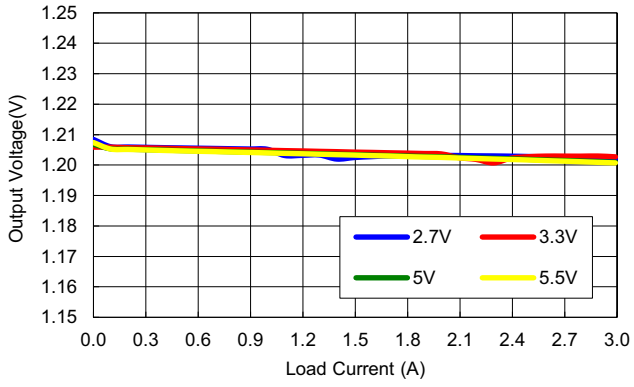


Figure 8. V_{OUT} Regulation vs Load, V_{OUT} = 1.2V

L=1µH, C_{out}=22µF, T_A = +25°C (Cont.)

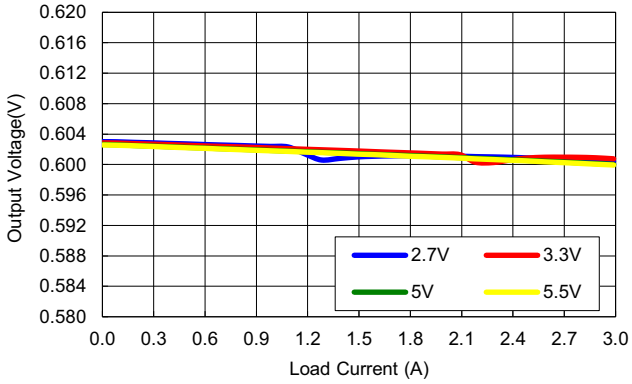


Figure 9. V_{OUT} Regulation vs Load, V_{OUT} = 0.6V

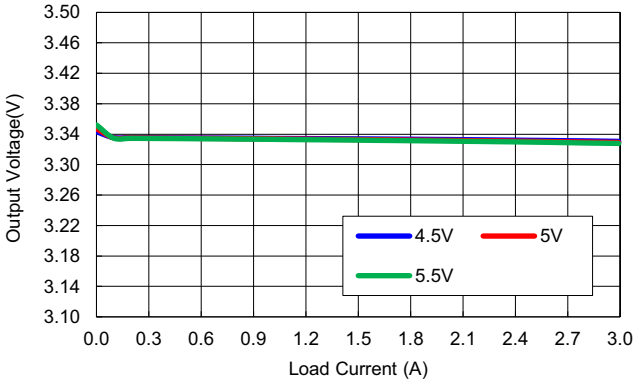


Figure 10. V_{OUT} Regulation vs Load, V_{OUT} = 3.3V

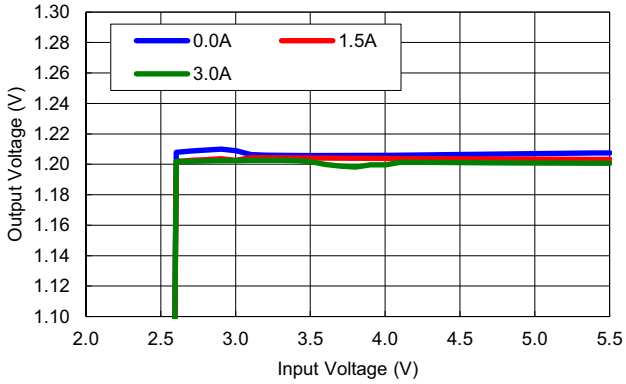


Figure 11. Line Regulation, V_{OUT} = 1.2V

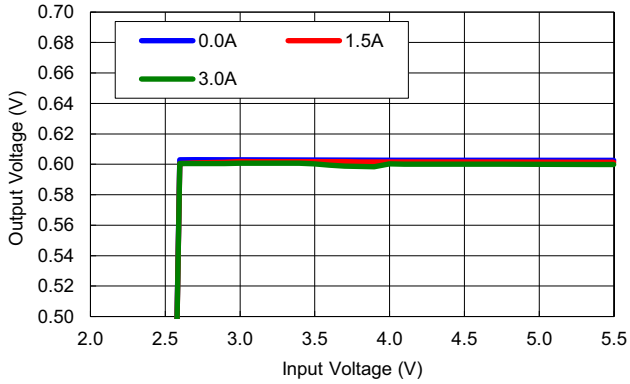


Figure 12. Line Regulation, V_{OUT} = 0.6V

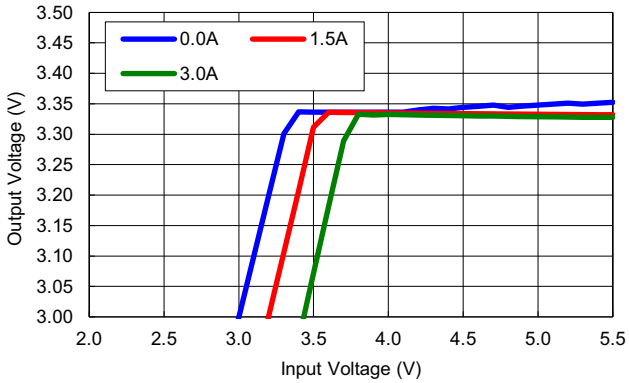


Figure 13. Line Regulation, V_{OUT} = 3.3V

4.2 Buck Measurements

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C

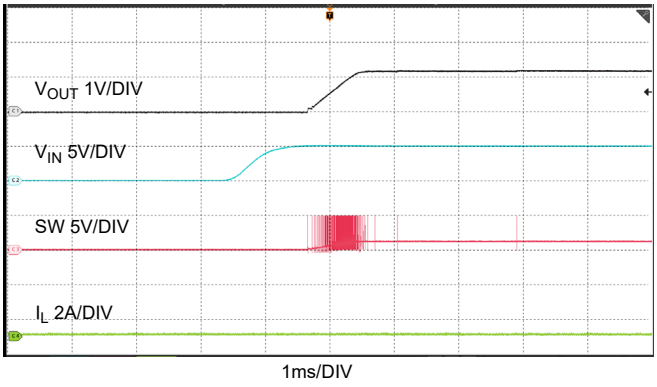


Figure 14. Startup at 0A

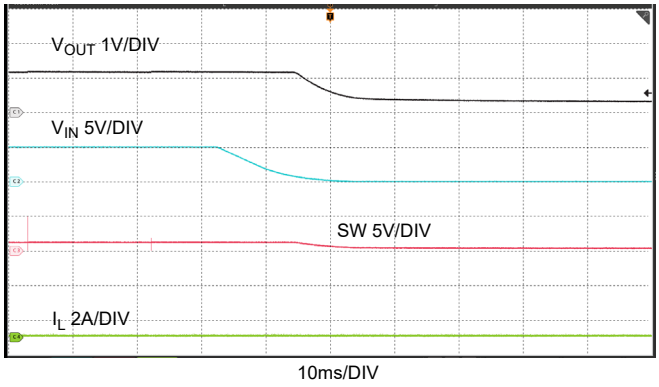


Figure 15. Shutdown at 0A

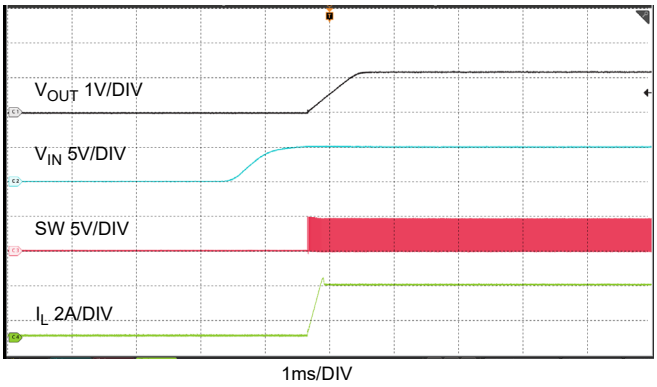


Figure 16. Startup at 3A

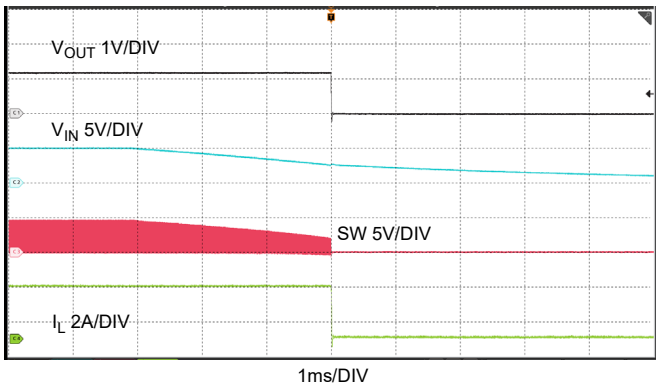


Figure 17. Shutdown at 3A

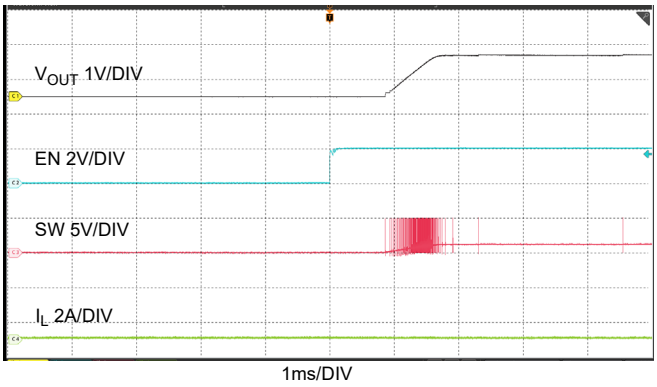


Figure 18. EN On at 0A

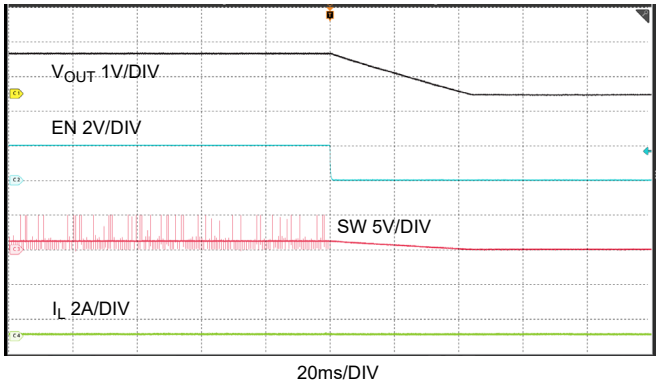


Figure 19. EN Off at 0A

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

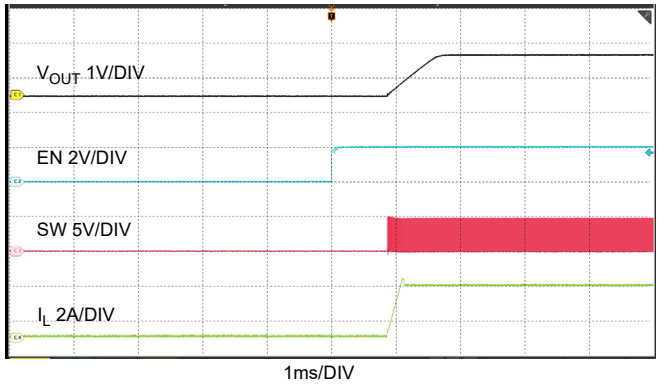


Figure 20. EN On at 3A

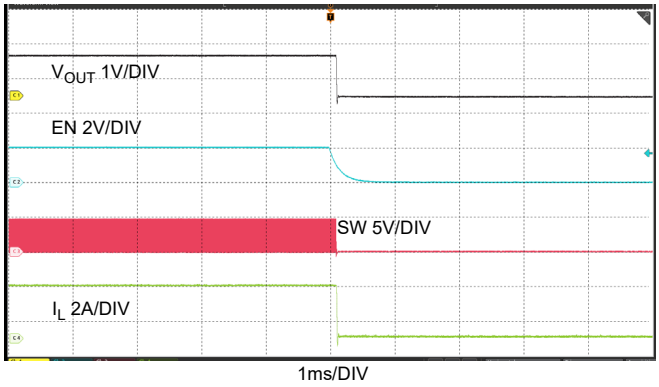


Figure 21. EN Off at 3A

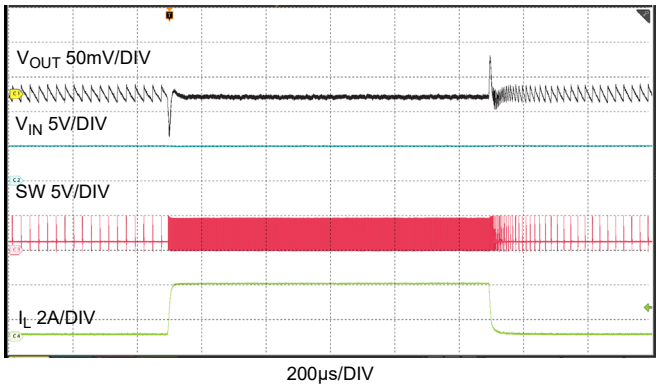


Figure 22. Load Transition, 0A->3A

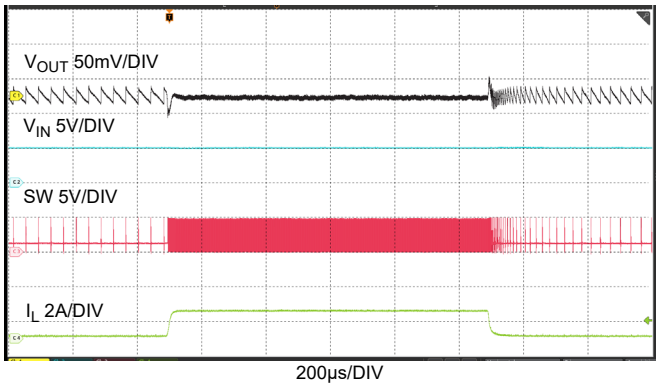


Figure 23. Load Transition, 0A->1.5A

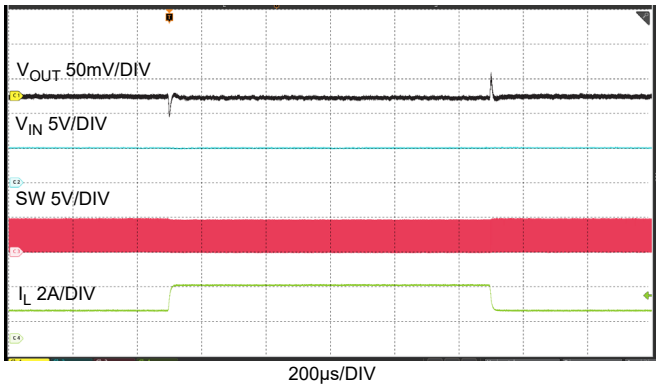


Figure 24. Load Transition, 1.5A->3A

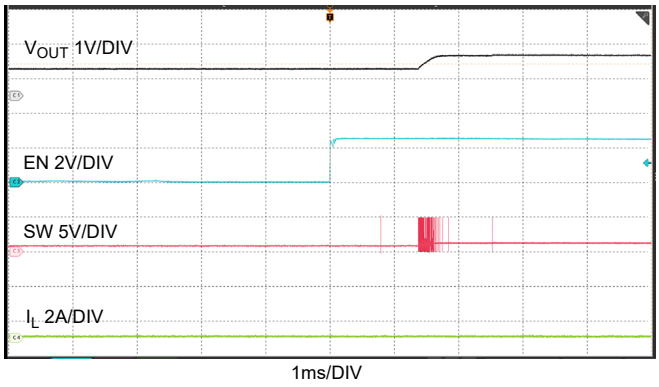


Figure 25. Pre-Bias On, No Load

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

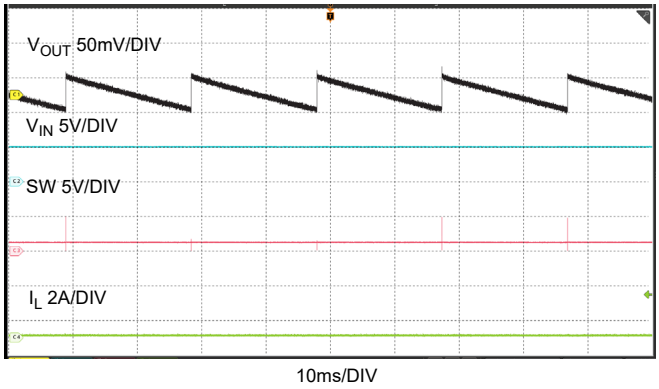


Figure 26. Steady State at 0A

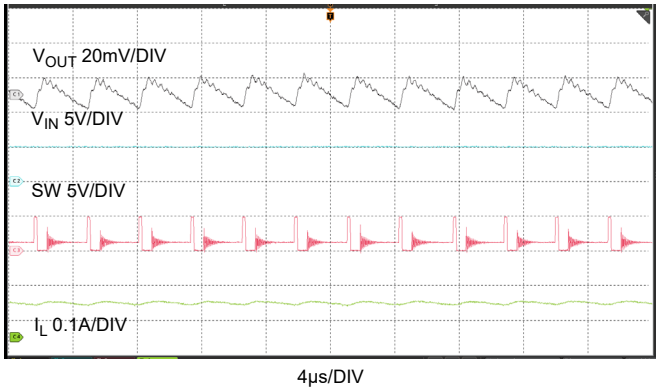


Figure 27. Steady State at 0.1A

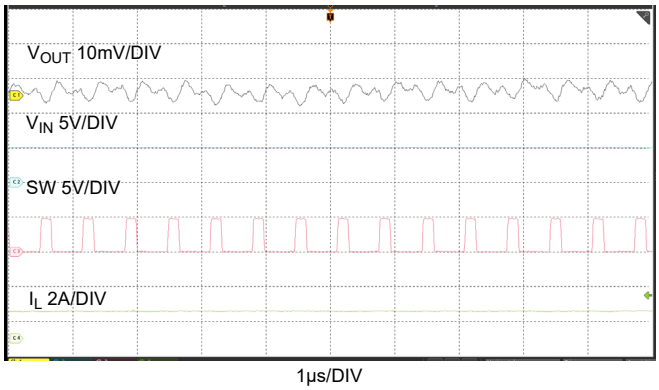


Figure 28. Steady State at 1.5A

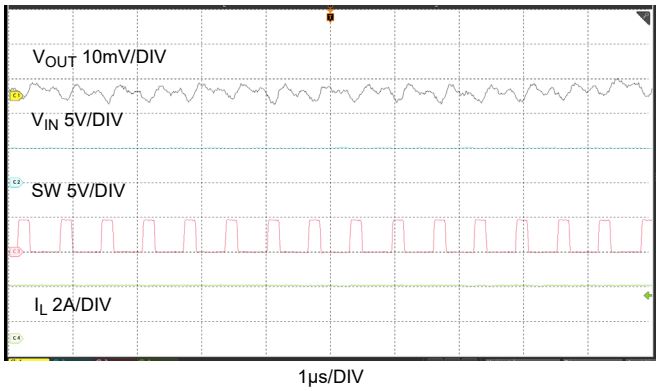


Figure 29. Steady State at 3A

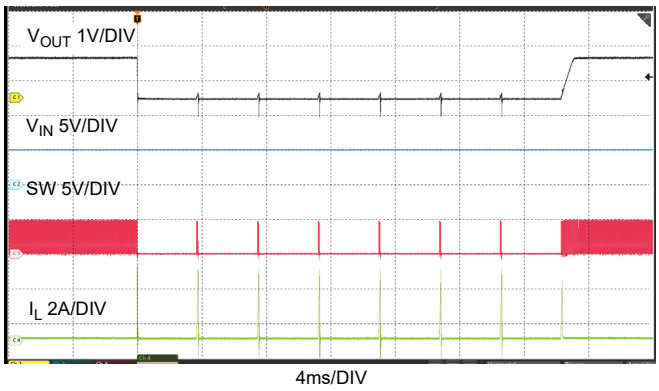


Figure 30. Hiccup with Output Short, No Load

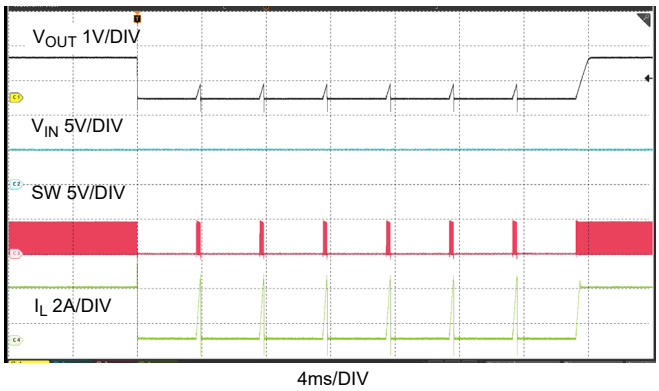


Figure 31. Hiccup with Output Short, Full Load

5. Functional Description

The RAA808013 is the low voltage buck regulator capable of running at 100% duty cycle. It can output 3A current continuously from a 2.7V to 5.5V input voltage with excellent load and line regulation. The Protection includes input UVP, cycle-by-cycle peak current limit, hiccup mode OCP and OTP. The constant on-time control scheme provides a fast response for dynamic load and high efficiency for a light load.

Comparied to the traditional COT, RAA808013 offers a nearly constant frequency by input voltage feed-forward and output voltage feedback. It can keep the frequency at 1.5MHz (typical) across the full input and output voltage range. It can run in DCM by using a zero-cross detector circuit to achieve high efficiency at light load. Also, in sleep mode, it can achieve significantly low standby power loss.

The chip can run in constant off-time mode when V_{IN} is close to V_{OUT}. It can keep the V_{OUT} in the regulation even if V_{IN} is close to V_{OUT}. The 100% duty cycle can be achieved when V_{OUT} equals V_{IN}.

5.1 Soft-Start

When V_{IN} reaches 2.65V and EN is high, the PWM starts up with an internal soft-start cap being charged by an internal current source after a short time delay. The soft-start time is 800µs. The delay time of EN/Power-on to soft-start is 750µs. Figure 32 shows the startup sequence diagram. RAA808013 supports pre-bias start-up.

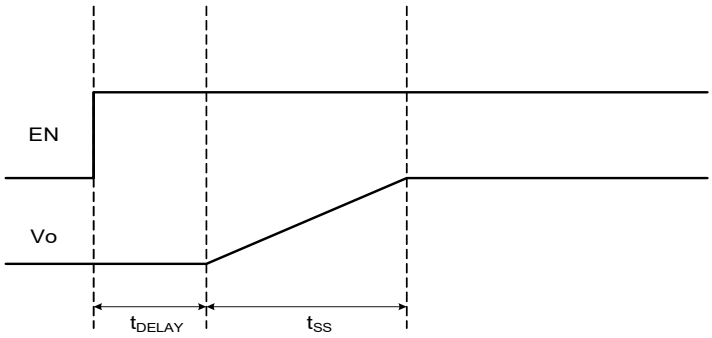


Figure 32. Startup Sequence

5.2 Constant On-Time Operation

RAA808013 operates in a constant on-time mode in most light load to full load, regulating the output voltage with the constant on-time operation. With V_{IN} feed-forward and V_{OUT} feedback, the switching frequency in this mode is almost constant.

5.3 100% Duty Cycle

When the input voltage is lower than the output set point, the high-side MOSFET stays on to keep the output voltage equal to the input voltage.

5.4 Light-Load Operation

When the load is light, with the valley of inductor current dropping to below zero, the RAA808013 switches to DCM mode.

When the load is light enough, the RAA808013 enters into PFM Sleep mode. In the sleep mode, off-time increases, and some unnecessary circuits are disabled for power saving. Figure 33 shows the DCM operation. The IC enters the DCM mode of operation when eight consecutive cycles of inductor current crossing zero are detected.

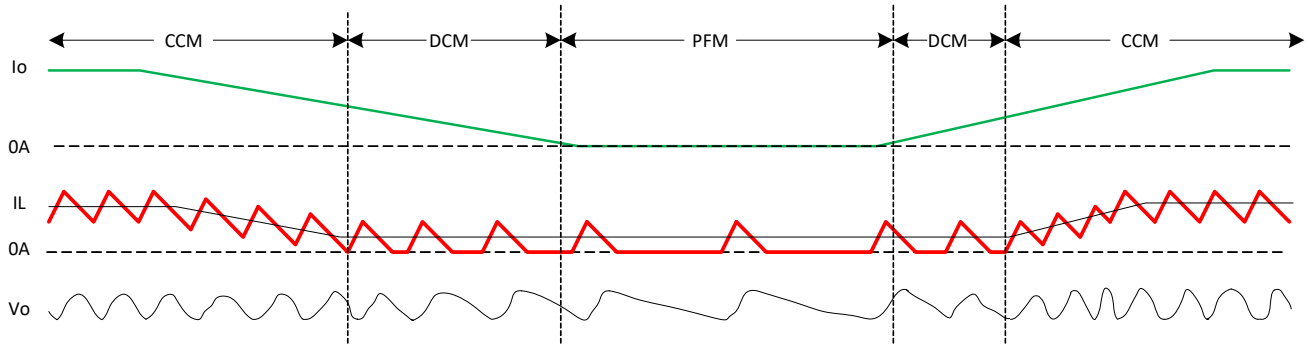


Figure 33. DCM Mode Operation Waveforms

5.5 Undervoltage Protection (UVLO)

The UVLO continuously monitors the VCC voltage to ensure the device works properly. When the VCC is high enough to reach the UVLO high threshold voltage, the regulator starts up or pre-biases to its regulated output voltage. If VCC decreases to its low threshold voltage, the device shuts down.

5.6 Power-Good

PG is the open-drain output of a comparator that continuously monitors the buck regulator output voltage through the FB pin. PG is actively held low when EN is low and during the soft-start period. After the soft-start period completes, PG becomes high-impedance provided the FB pin is higher than the threshold specified in Power-Good. Should FB be lower than 85% of the setpoint 0.6V, PG is pulled low until FB returns. Over-temperature faults also force PG low until the fault condition is cleared by an attempt to soft start.

5.7 Enable Operation

The EN turn-on threshold is 1.2V max. As a result, this pin must not be left floating and should be tied to VIN if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use an open collector or open-drain outputs to control the EN pin.

5.8 Protection Features

5.8.1 Cycle-by-Cycle Peak Current Limit

The RAA808013 has a 4.6A current limit for the high-side FET (HS-FET). When the HS-FET hits its current limit, it shuts down immediately until the next cycle, preventing the inductor current from rising and possibly damaging the components.

5.8.2 HICCUP OCP

RAA808013 operates in Hiccup mode after seven continuous current limit cycles. Hiccup time is 3.6ms. See Figure 34.

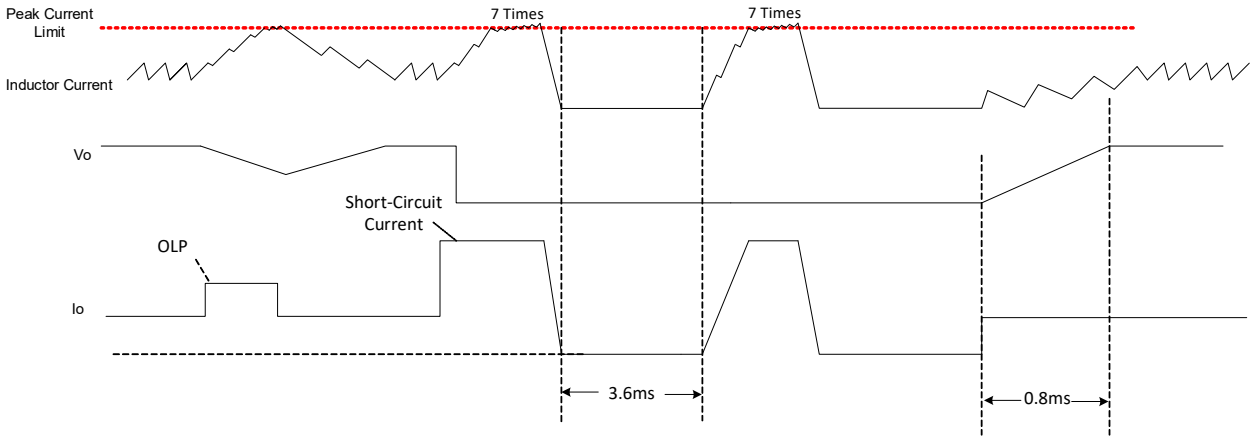


Figure 34. OCP and SCP Protection

5.8.3 Over-Temperature Protection

Over-temperature protection limits maximum junction temperature in the RAA808013. When the junction temperature (T_J) exceeds 160°C, both FETs are turned off, and the controller waits for the temperature to decrease by approximately 15°C. During this time, PG is pulled low. When the temperature is within an acceptable range, the controller initiates a normal soft-start sequence. For continuous operation, the 125°C junction temperature rating should not be exceeded.

6. Application Guidelines

6.1 Output Voltage Setting

The regulator output voltage is easily programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; see Figure 35.

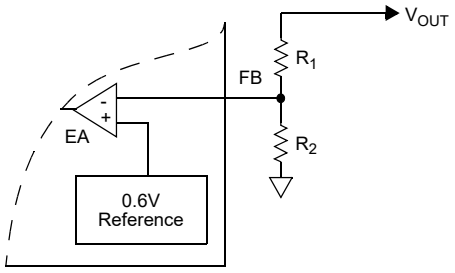


Figure 35. External Resistor Divider

The output voltage programming resistor, R_2, depends on the value chosen for the feedback resistor, R_1, and the required output voltage, V_{OUT}, of the regulator. Equation 1 describes the relationship between V_{OUT} and resistor values.

(EQ. 1) $$R_2 = \frac{R_1 \times 0.6V}{V_{OUT} - 0.6V}$$

If the required output voltage is 0.6V, R_2 is left unpopulated and R_1 is 0Ω.

6.2 Output Inductor Selection

The inductor value determines the ripple current of the converter. Choosing an inductor current requires a somewhat arbitrary choice of ripple current. A reasonable starting point is 30% of the total load current. The inductor value is then calculated using Equation 2:

(EQ. 2) $$L = \frac{V_{IN} - V_{OUT}}{FS \times \Delta I} \times \frac{V_{OUT}}{V_{IN}}$$

Increasing the value of inductance reduces the ripple current and therefore, the ripple voltage. However, the larger inductance value can reduce the response time of the converter to a load transient. The current rating of the inductor should be such that it does not saturate in overcurrent conditions. For typical RAA808013 applications, the inductor value generally lies at 1µH or 2.2µH.

6.3 Output Capacitor Selection

An output capacitor is required to reduce output voltage ripple. The control loop allows the use of low ESR ceramic capacitors enabling a small solution size on the PC board. Electrolytic and polymer capacitors can also be used.

Although ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the capacitor datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published; however, an assumption of ~20% further reduction generally suffices. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. However, ceramic capacitors are a good choice in many applications because of their reliability and extremely low ESR.

Equation 3 (where ΔI is the peak-to-peak ripple current of the inductor, f_{SW} is the switching frequency, C_{OUT} is the output capacitor, ESR is the equivalent series resistance of the output capacitor, ESL is the equivalent series inductance of the output capacitor, and L is the output filter inductance) allows the calculation of the required capacitance to meet the required ripple voltage level. Additional capacitance can be used.

(EQ. 3) $$V_{OUTripple} = \left(\frac{\Delta I}{8 \times f_{SW} \times C_{OUT}} + \Delta I \times ESR + \frac{ESL \times V_{IN}}{L} \right)$$

Note: This is only a simple engineering algorithm to calculate the output ripple voltage because the phase of ripple voltage generated by the capacitor charging is different from that generated by the ripple current on ESR.

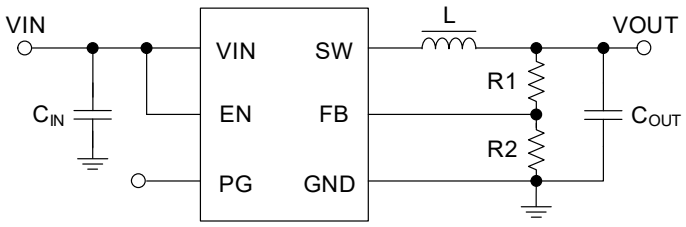


Figure 36. Application Circuit

7. Layout Considerations

Proper layout of the power converter minimizes EMI and noise and ensures first pass success of the design. PCB layouts are provided in multiple formats on the Renesas website. In addition, Figure 37 makes clear the important points in the PCB layout. In reality, the PCB layout of the RAA808013 is quite simple.

- A multi-layer printed circuit board with a GND plane is recommended. Figure 37 shows the connections of the critical components in the converter. *Note:* Capacitors C_{IN} and C_{OUT} could each represent multiple physical capacitors. The most critical connections are to tie the PGND pin to the package GND pad. This connection of the GND pad to the system plane ensures a low-impedance path for all return current, and an excellent thermal path to dissipate heat. With this connection made, place the high frequency MLCC input capacitor near the VIN pin and use vias directly at the capacitor pad to tie the capacitor to the system GND plane.
- Place a 1µF MLCC near the VCC pin and directly connect its return with a via to the system GND plane.
- Place the feedback divider close to the FB pin and do not route any feedback components near SW.

A component placement example is shown in Figure 37.

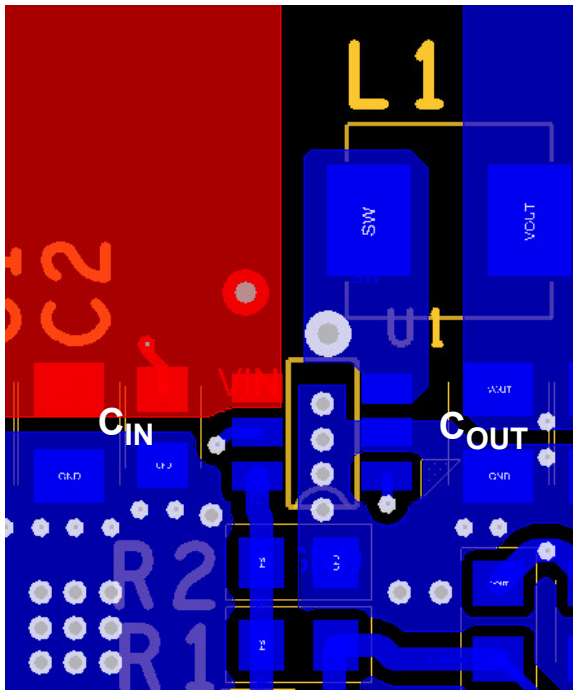


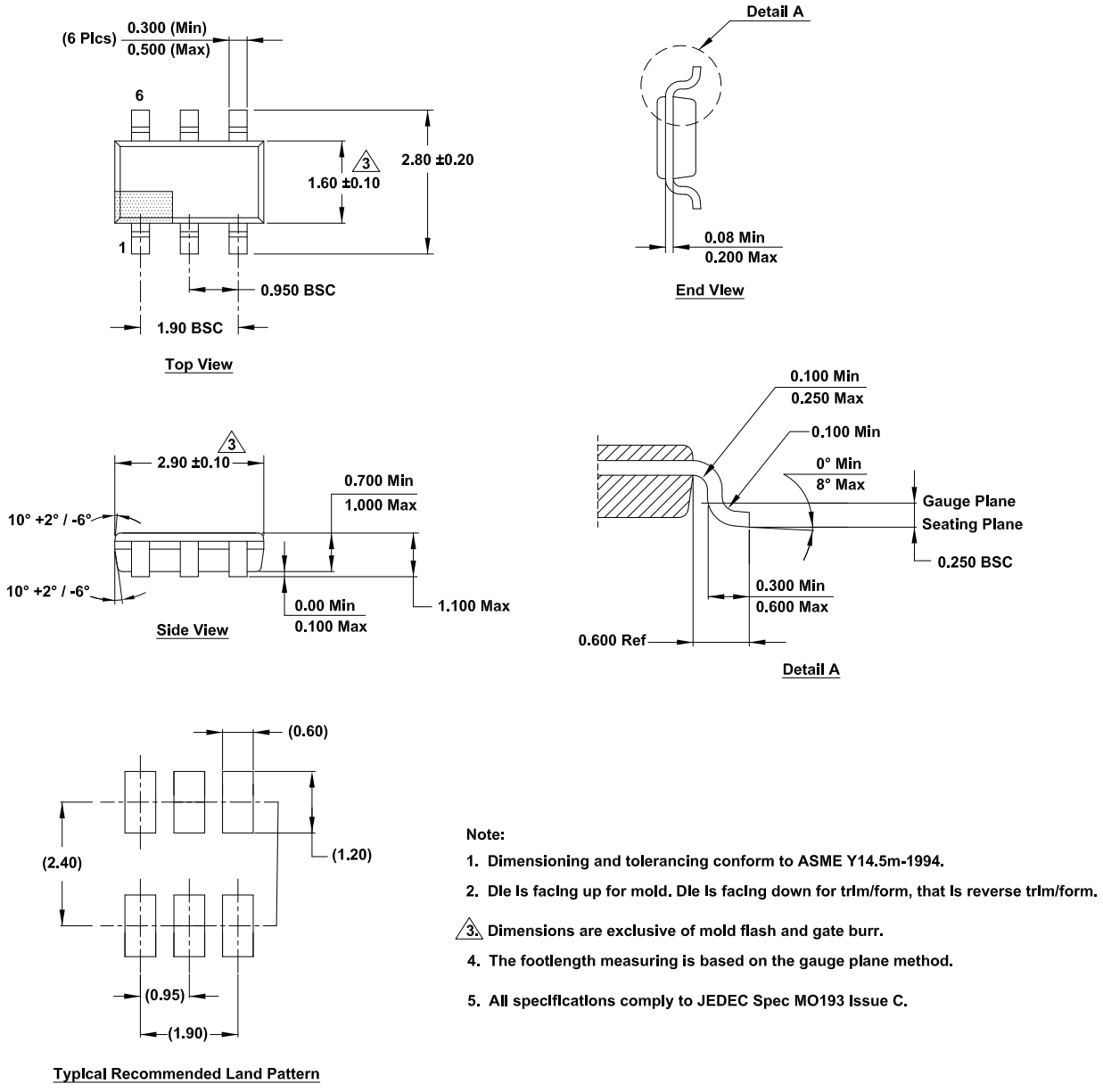
Figure 37. Printed Circuit Board Example Component Placement

8. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

P6.064C

6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20



Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

9. Ordering Information

Part Number[1][2]	Part Marking[3]	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RAA808013GP3#JA0	813	6 Ld TSOT23	P6.064C	Reel, 3k	-40 to +125°C
RTKA808013DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA808013 device page. For more information about MSL, see TB363.
3. The part marking is located on the bottom of the part.
4. See TB347 for details about reel specifications.

10. Revision History

Rev.	Date	Description
1.00	Aug 19, 2022	Initial release