RAA808015A

2.7V to 5.5V Input, 5A Synchronous Buck Regulator

The RAA808015A is a 5A synchronous buck regulator with an input range of 2.7V to 5.5V. It provides an easy-to-use, high-efficiency low BOM count solution for a variety of applications.

The RAA808015A integrates both high-side and low-side MOSFETs and features a PFM mode for improved efficiency at light loads.

The RAA808015A adopts Constant On-Time (COT) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The part switches at a default frequency of 1.8MHz.

The RAA808015A can switch between constant on-time control and constant off-time control smoothly and can also switch between constant off-time control and 100% duty cycle smoothly with V_{IN} voltage changing.

With the wide VIN range and reduced BOM, the part provides an easy-to-implement design solution for a variety of applications while giving superior performance. It provides a robust design for low voltage industrial applications in addition to an efficient solution for battery powered applications.

The part is available in a small Pb-free 2mmx2.5mm QFN plastic package with an operation junction temperature range of -40°C to +125°C.

Features

- 2.7V to 5.5V operating input range
- 5A output current
- Output adjustable from 0.6V
- 100% duty cycle in dropout
- 20mΩ and 16mΩ internal power MOSFET switches
- High switching frequency (1.8MHz)
- EN for Power Sequencing
- Fixed Soft Start time
- Cycle-by-cycle overcurrent protection (3 times)
- OCP and SCP with Hiccup mode
- Input undervoltage lockout (UVLO)
- Over-temperature protection
- Small QFN 2x2.5 package

Applications

- Low-voltage, high-density power system
- Point-of-load regulation for high-performance DSPs, FPGAs, ASICs, and microprocessors
- Broadband, networking, and optical
- Communications infrastructure
- Gaming, DTV, and set-top boxes

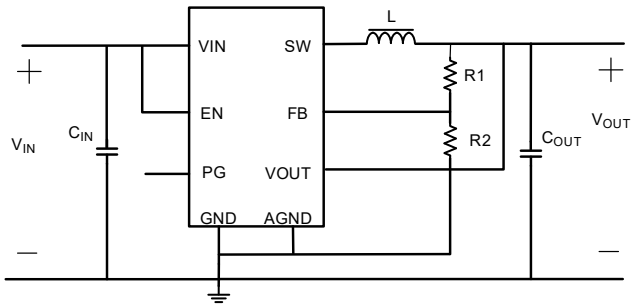


Figure 1. Typical Application

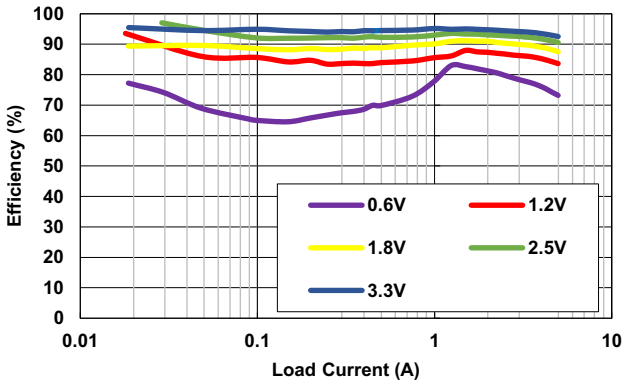


Figure 2. Efficiency vs Load, PFM, L = 0.47µH, V_{IN} = 5V

Contents

1. Overview

1.1 Typical Application Circuits

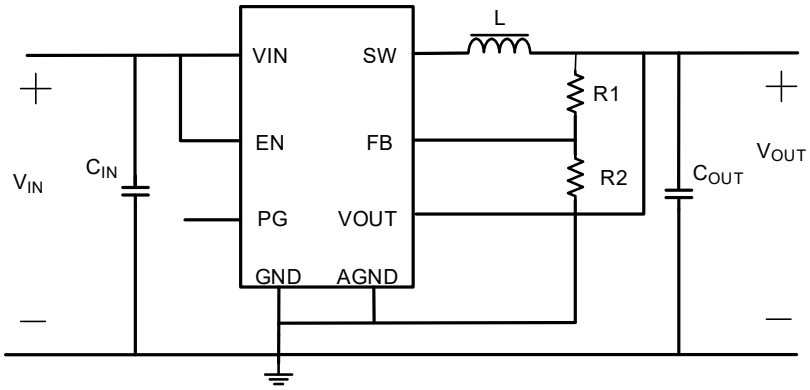


Figure 3. External Default Parameter Selection

Table 1. External Component Selection

V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_1 (kΩ)	R_2 (kΩ)
0.6	0.47	2×22	0	300[1]
1	0.47	2×22	200	300
1.2	0.47	2×22	200	200
1.8	0.47	2×22	200	100
2.5	0.47	2×22	200	63.2
3.3	0.47	2×22	200	44.2

1. If the required output voltage is 0.6V, R_2 should be smaller than 500kΩ.

1.2 Block Diagram

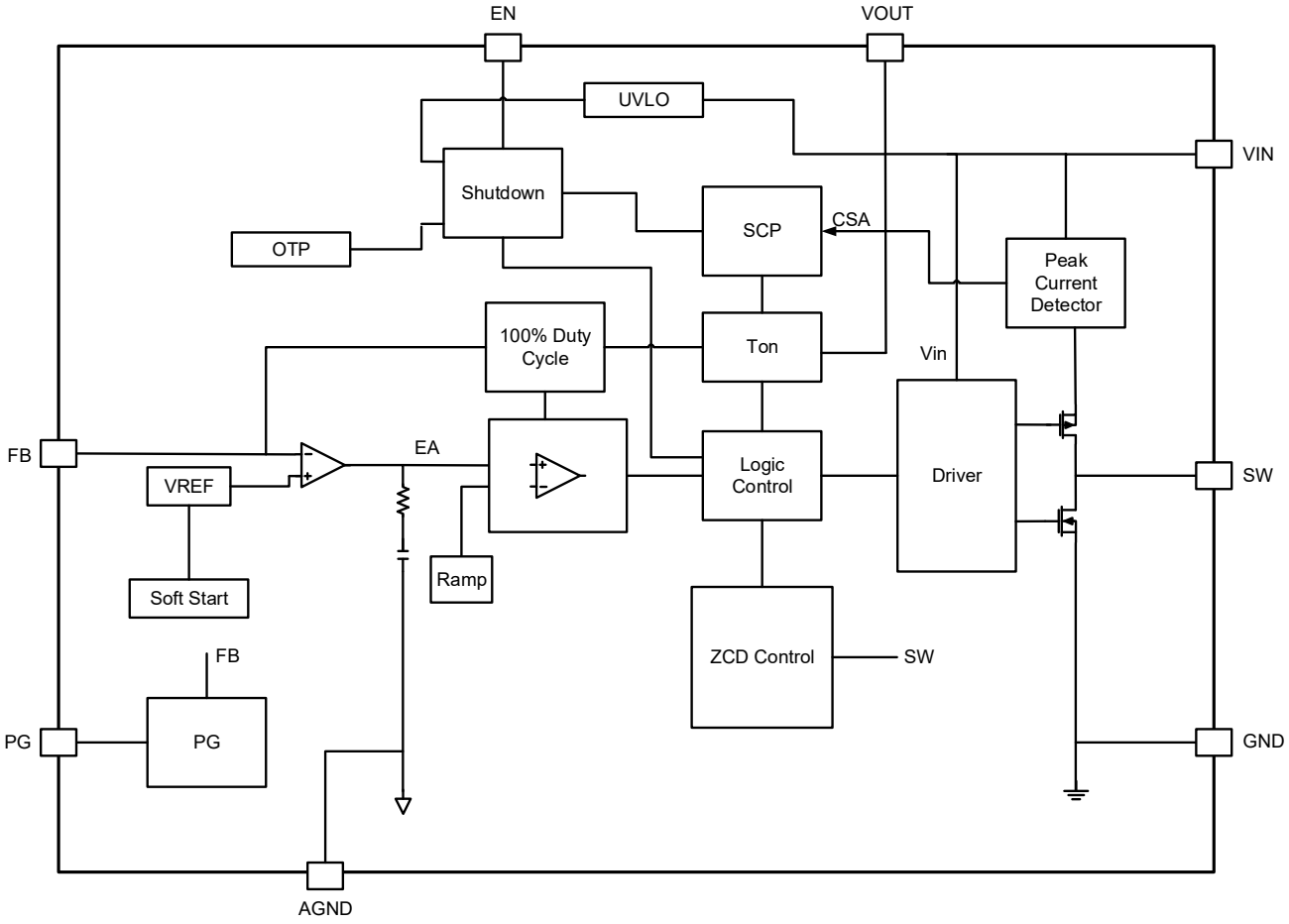
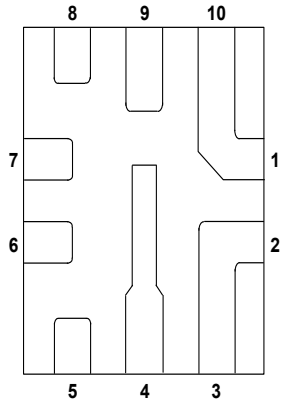


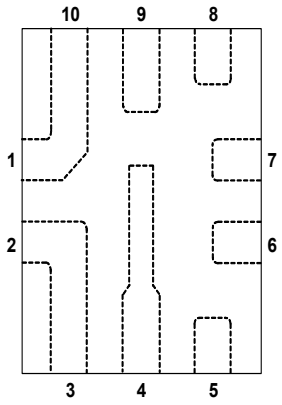
Figure 4. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Bottom View



Top View

2.2 Pin Descriptions

Pin Name	Number	Description
SW	1, 10	Switch Node.
GND	2, 3	Power ground.
VIN	4	Supply voltage. The IC operates from a +2.7V to +5.5V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
PG	5	Power-good indicator. The output of this pin is an open-drain with internal pull-up resistor to VIN. PG is in high impedance when FB is higher than the typical 0.54V. Otherwise, it is pulled low.
EN	6	Enable control input.
AGND	7	Analog ground. Provides the ground return path for control circuitry and internal reference.
FB	8	Feedback pin, 0.6V ±3.5% across temperature range of -40 to 125°C.
VOUT	9	Output voltage sense input.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN to GND	-0.3	+6	V
SW to GND (DC)	-0.3	VIN + 0.3	V
SW to GND (10ns)	-4	+7.5	V
EN to GND	-0.3	VIN + 0.3	V
FB to GND	-0.3	VIN + 0.3	V
PG to GND	-0.3	VIN + 0.3	V
VOUT to GND (DC)	-0.3	VIN + 0.3	V

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
10 Ld QFN 2×2.5 Package	58.1	3.9

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Ambient Temperature Range	-40	+125	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	2.7	5.5	V
Ambient Temperature	-40	+125	°C
Output Voltage, V_{OUT}	0.6	3.3	V

3.5 Electrical Specifications

Typical operating conditions at 25°C, V_{IN} = 5V, T_J = -40 to +125 °C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +125°C)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Supply Voltage						
V_{IN} Voltage Range	V_{IN}		**2.7**		**5.5**	V
Undervoltage Lockout Threshold - Rising	V_{INUV_rise}				**2.65**	V
Undervoltage Lockout Threshold - Hysteresis	V_{INUV_hys}			60		mV
V_{IN} Quiescent Supply Current	I_Q			55	70	µA
V_{IN} Shutdown Supply Current	I_{SD}	V_{EN} = 0V, V_{IN} = 5V, T_J = 25°C [2]			1	µA
Feedback Voltage						
Feedback Voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 5.5V, T_J = 25°C	0.588	0.6	0.612	V
		T_J = -40°C to +125°C	**-3.5**		**3.5**	%
Feedback Current	I_{FB_leak}	V_{FB} = 0.6V		10		nA
Soft-Start						
Internal Soft-Start Ramp Time	t_{SS}	V_{OUT} rising from 0V to 100%		800		us
Internal MOSFET						
PFET Switch On-Resistance	r_{DSON_P}	V_{IN} = 5V, I_{RMS} = 0.8A, T_J = 25°C		20		mΩ
NFET Switch On-Resistance	r_{DSON_N}			16		mΩ
Switching						
Nominal Switching Frequency	F_S	V_{IN} = 5V, V_{OUT} = 1.2V		1.8		MHz
On-Time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		133		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		185		ns
Minimum Off-Time	t_{OFF_min}	T_J = -40°C to +125°C		100		ns
Minimum On-Time	t_{ON_min}	T_J = -40°C to +125°C		110		ns
Power-Good						
PG Threshold - VFB Rising				90		%
PG Threshold - VFB Falling				85		%
Power-Good Sink Current Capability	V_{PG_L}	I_{SINK} = 1mA, T_J = 25°C			0.4	V
PG Internal Pull-Up Resistor	R_{PG}			500		kΩ
Enable Voltage						
Input Threshold		Falling Edge, Logic Low, I_Q < 5µA			**0.4**	V
		Rising Edge, Logic High	**1.2**			V
EN Logic Input Leakage Current		V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Fault Protection						
Peak Current Limited[3]	I_{peak}		6.4	7.8		A
Hiccup Time				3.6		ms
Zero Cross Threshold	I_{ZCD}			120		mA

Typical operating conditions at 25°C, V_{IN} = 5V, T_J = -40 to +125 °C, unless otherwise specified. **Boldface limits apply across the operating temperature range (-40°C to +125°C)** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		160		°C
	T_{HYS}	Hysteresis		15		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Test Condition: V_{IN} = 5V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
3. Compliance to limits is established by design.

4. Typical Performance Curves

4.1 Efficiency Curves

T_A = +25°C

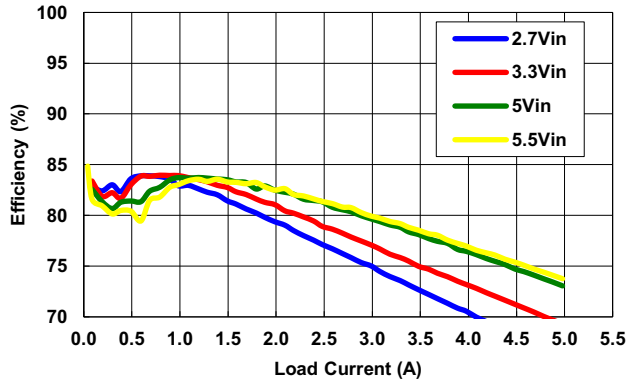


Figure 5. Efficiency vs Load, V_{OUT} = 0.6V, L = 0.47µH

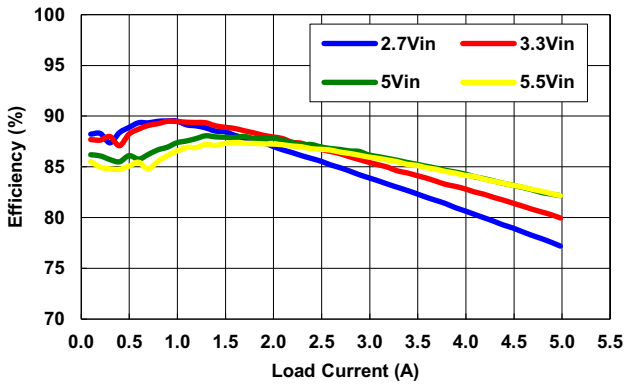


Figure 6. Efficiency vs Load, V_{OUT} = 1.2V, L = 0.47µH

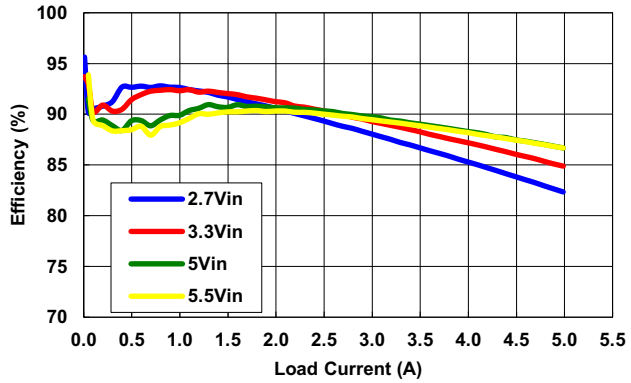


Figure 7. Efficiency vs Load, V_{OUT} = 1.8V, L = 0.47µH

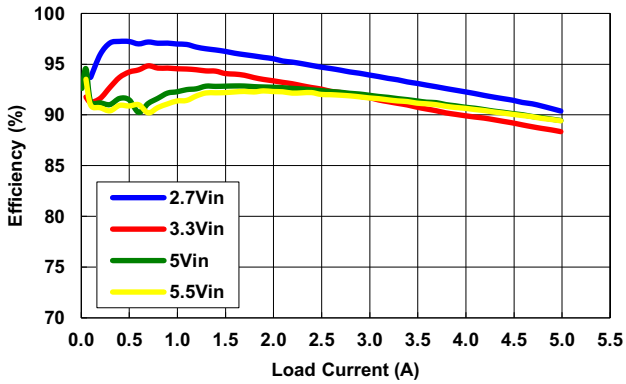


Figure 8. Efficiency vs Load, V_{OUT} = 2.5V, L = 0.47µH

T_A = +25°C (Cont.)

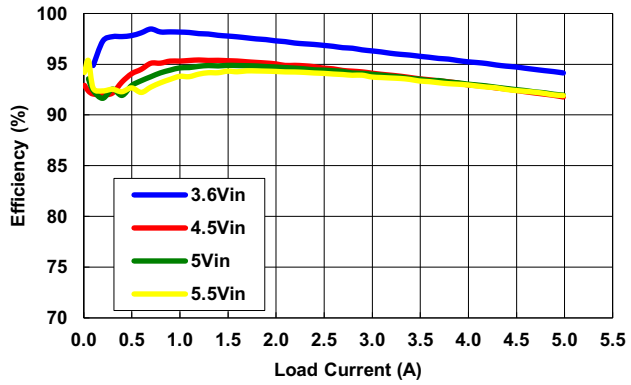


Figure 9. Efficiency vs Load, V_{OUT} = 3.3V, L = 0.47µH

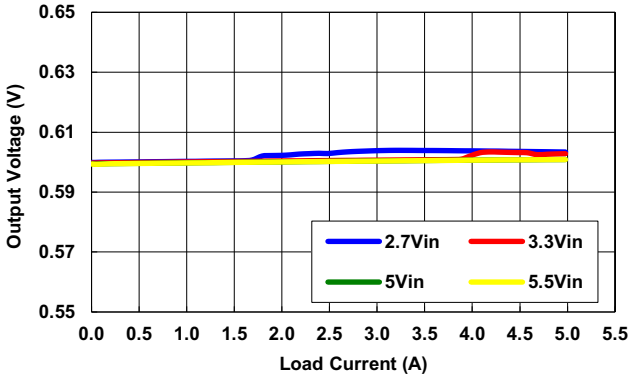


Figure 10. V_{OUT} Regulation vs Load, V_{OUT} = 0.6V

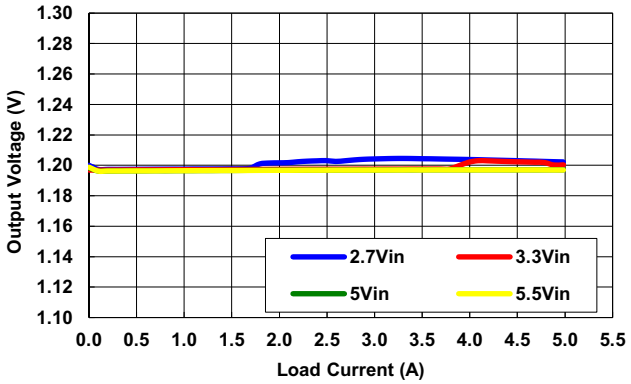


Figure 11. V_{OUT} Regulation vs Load, V_{OUT} = 1.2V

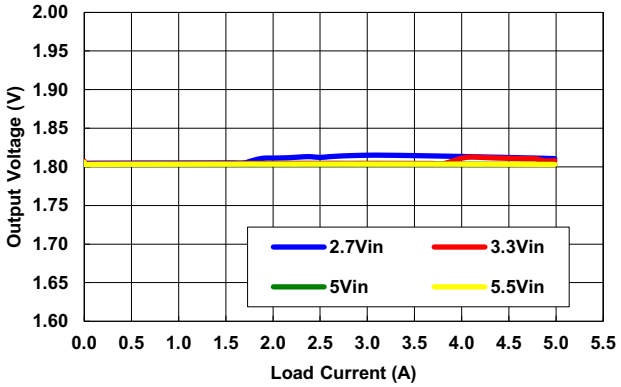


Figure 12. V_{OUT} Regulation vs Load, V_{OUT} = 1.8V

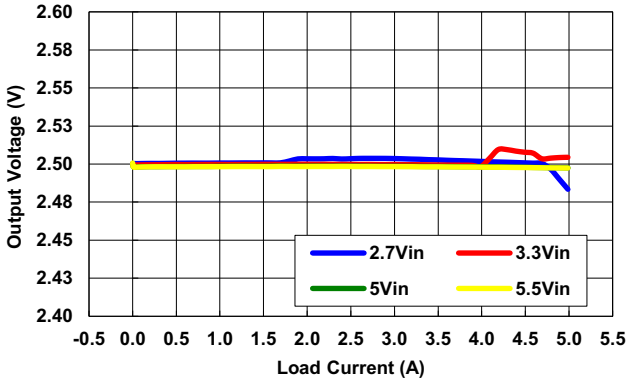


Figure 13. V_{OUT} Regulation vs Load, V_{OUT} = 2.5V

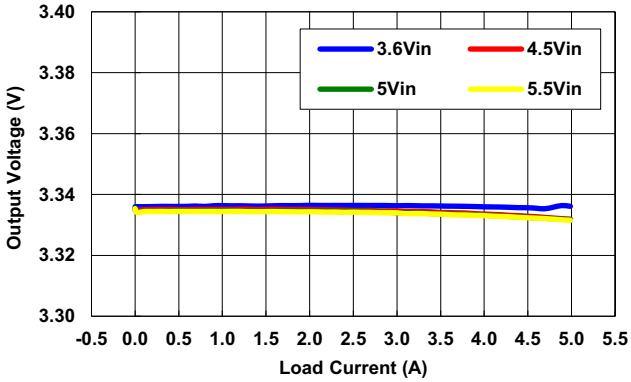


Figure 14. V_{OUT} Regulation vs Load, V_{OUT} = 3.3V

T_A = +25°C (Cont.)

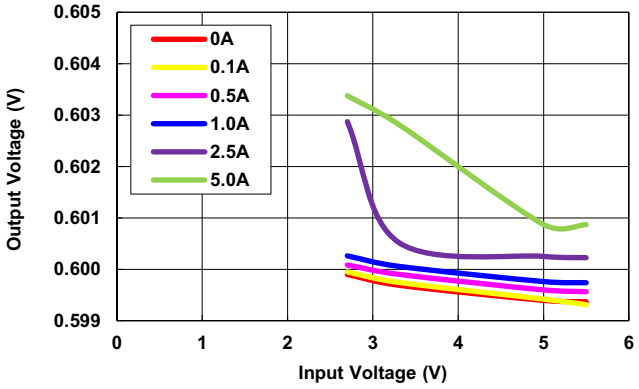


Figure 15. Line Regulation, V_{OUT} = 0.6V

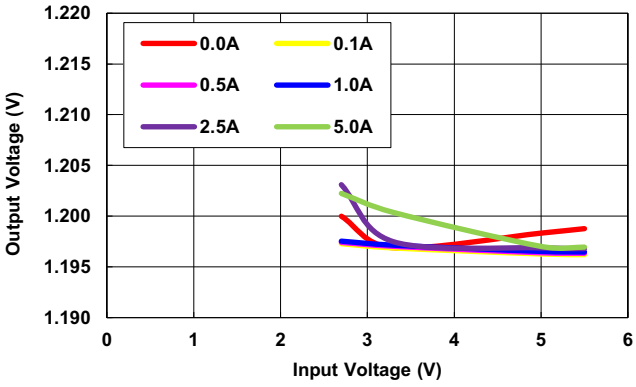


Figure 16. Line Regulation, V_{OUT} = 1.2V

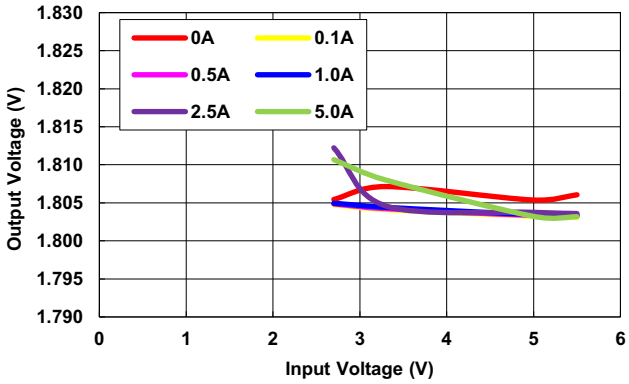


Figure 17. Line Regulation, V_{OUT} = 1.8V

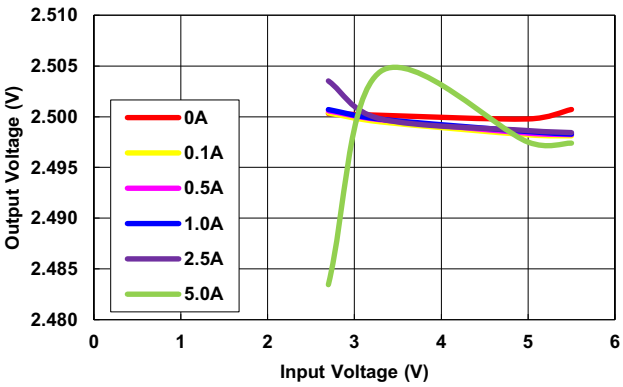


Figure 18. Line Regulation, V_{OUT} = 2.5V

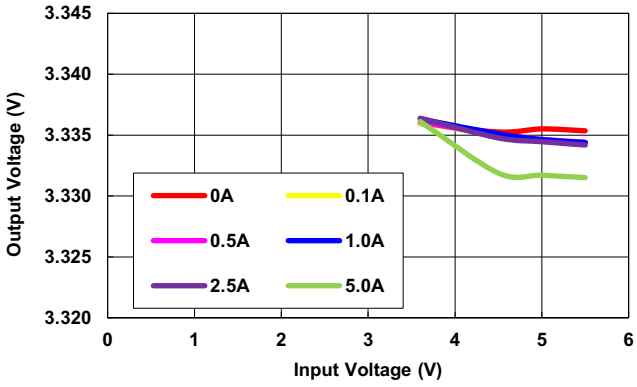


Figure 19. Line Regulation, V_{OUT} = 3.3V

4.2 Buck Measurements

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C

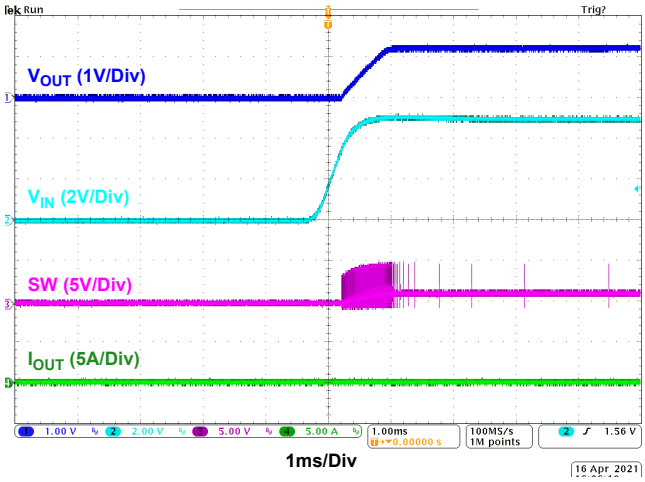


Figure 20. Startup at No Load

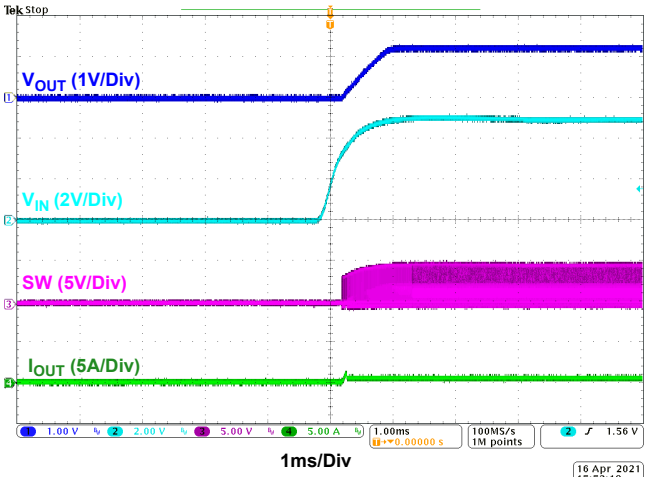


Figure 21. Startup at 0.5A Load

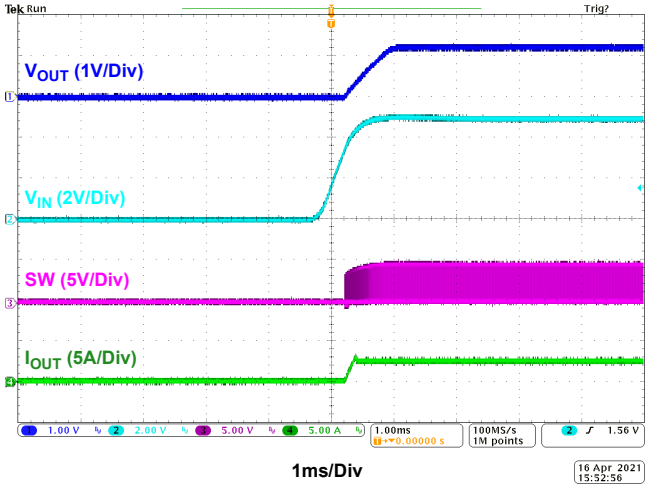


Figure 22. Startup at Half Load

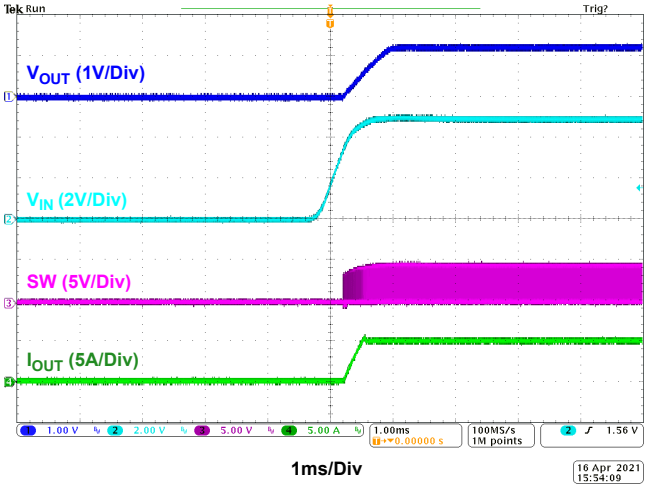


Figure 23. Startup at Full Load

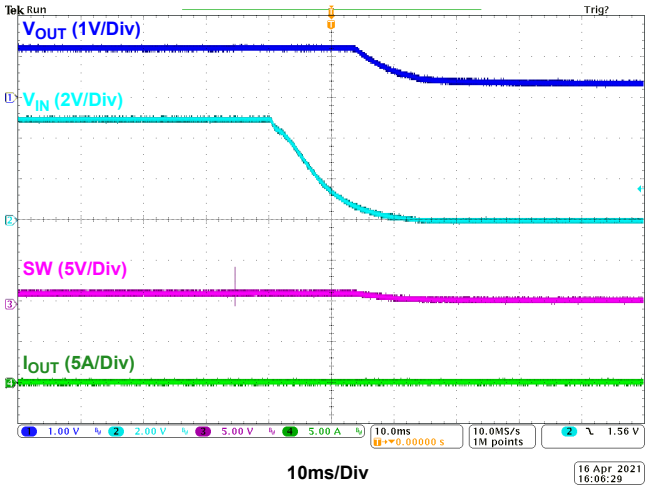


Figure 24. Shutdown at No Load

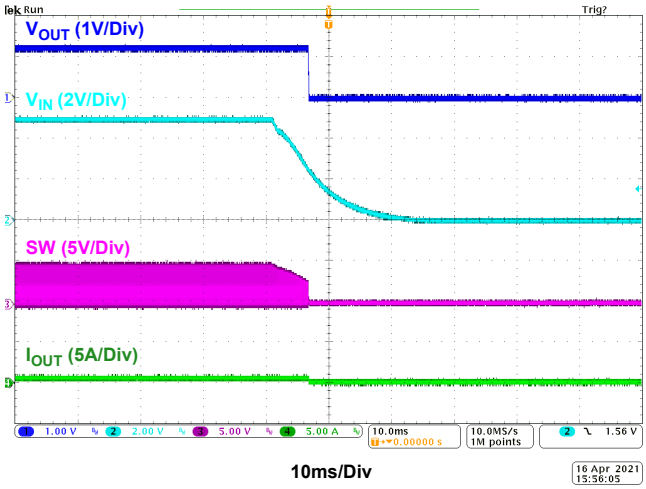


Figure 25. Shutdown at 0.5A LO

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

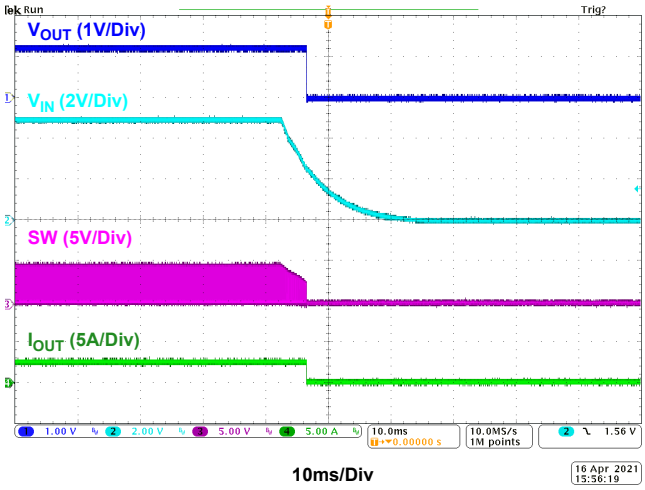


Figure 26. Shutdown at Half Load

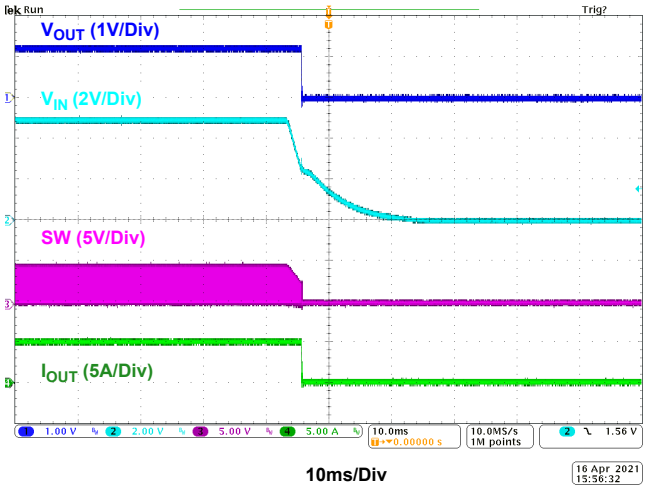


Figure 27. Shutdown at Full Load

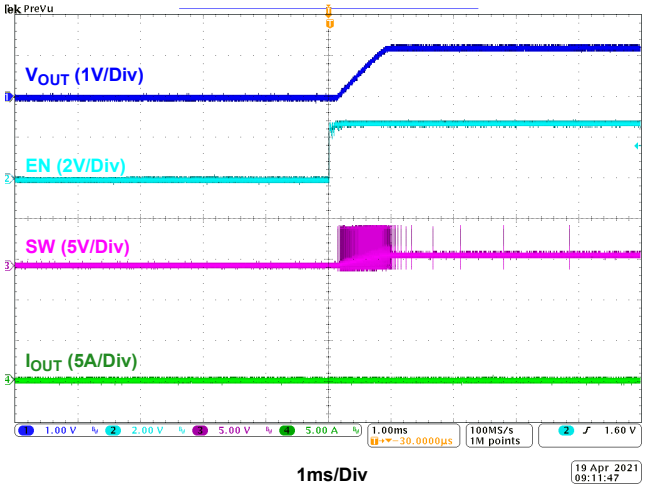


Figure 28. EN On at No Load

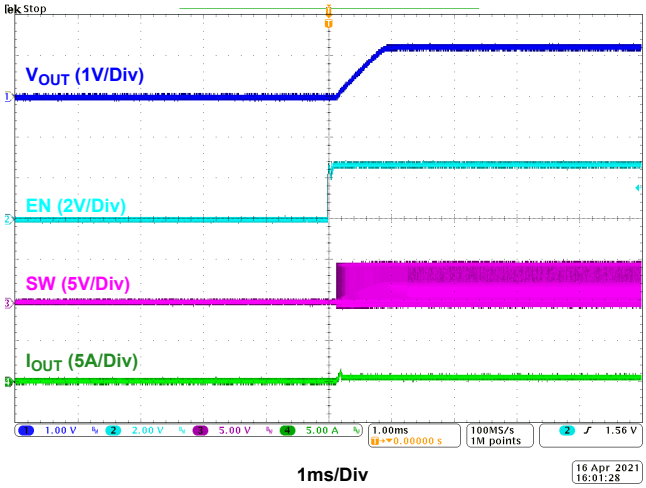


Figure 29. EN On at 0.5A Load

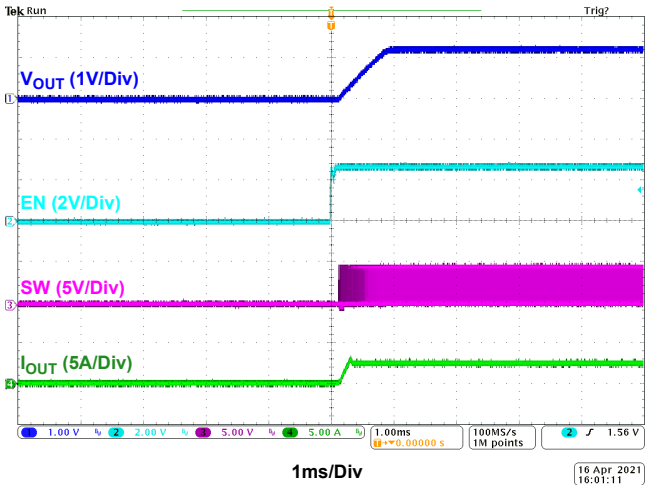


Figure 30. EN On at Half Load

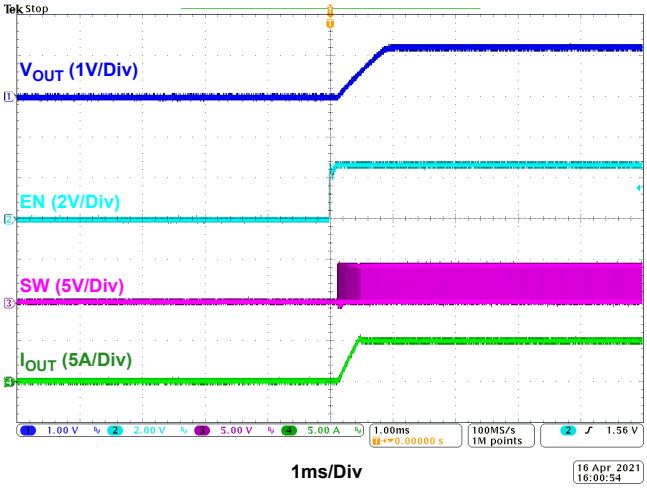


Figure 31. EN On at Full Load

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

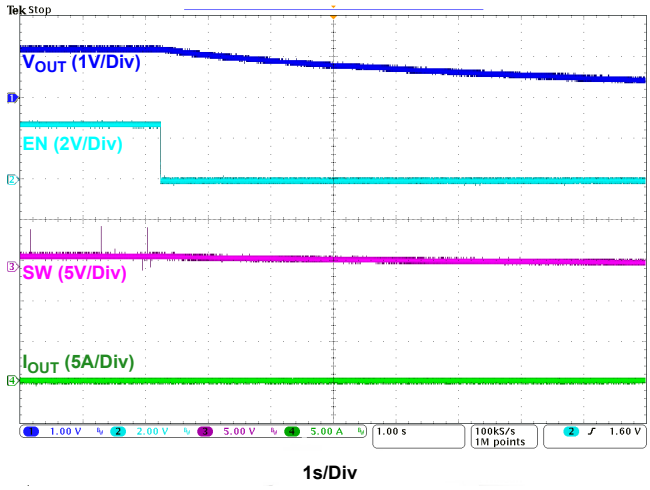


Figure 32. EN Off at No Load

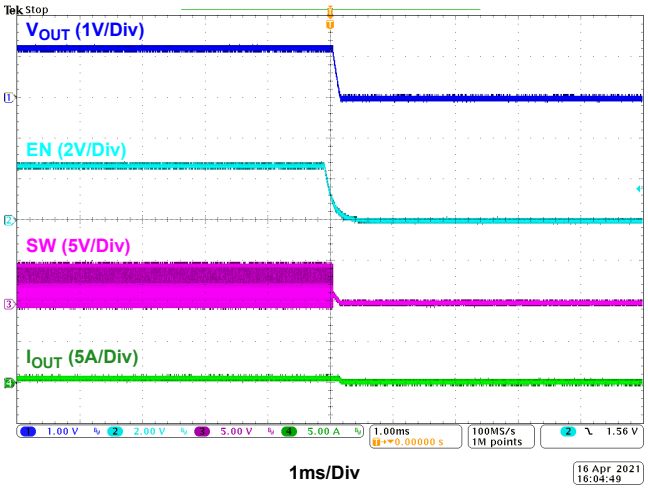


Figure 33. EN Off at 0.5A Load

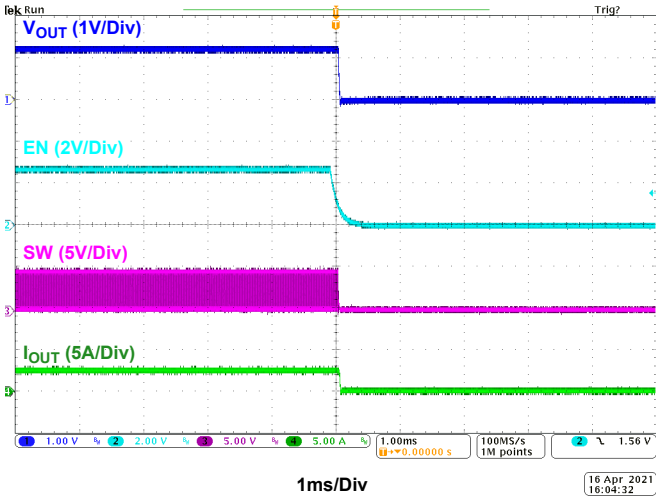


Figure 34. EN Off at Half Load

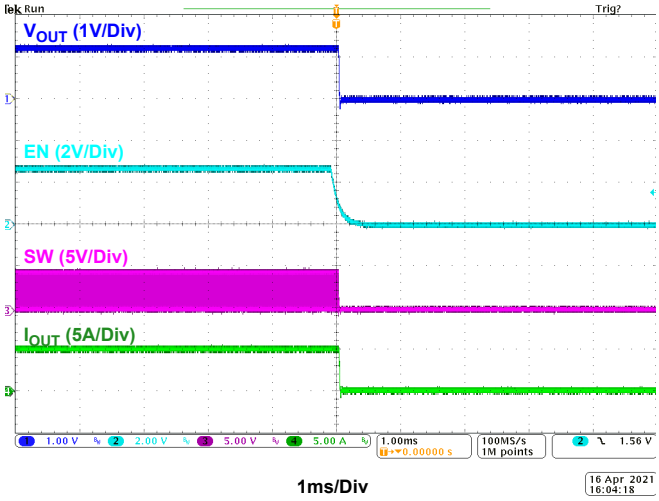


Figure 35. EN Off at Full Load

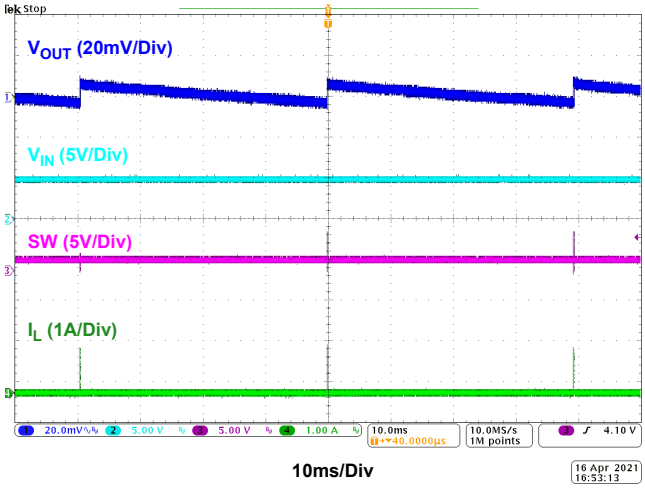


Figure 36. Steady State at No Load

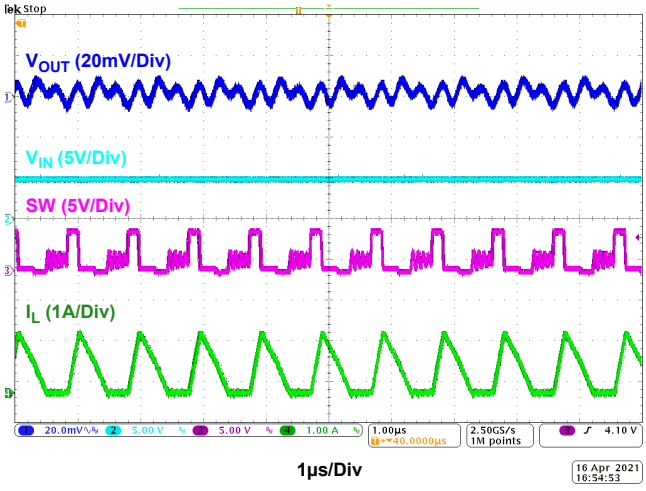


Figure 37. Steady State at 0.5A Load

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

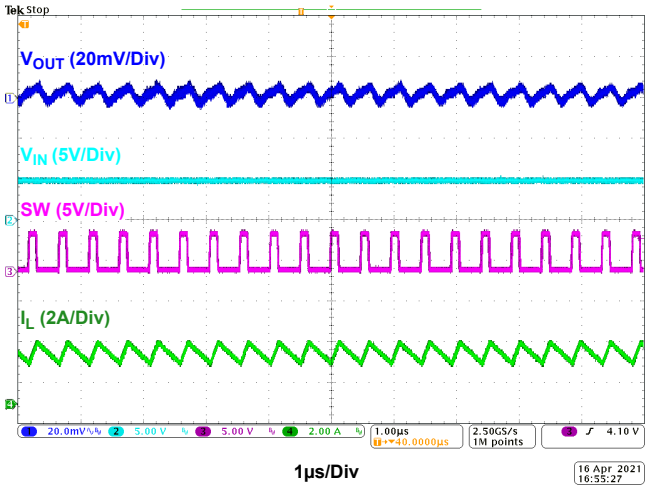


Figure 38. Steady State at Half Load

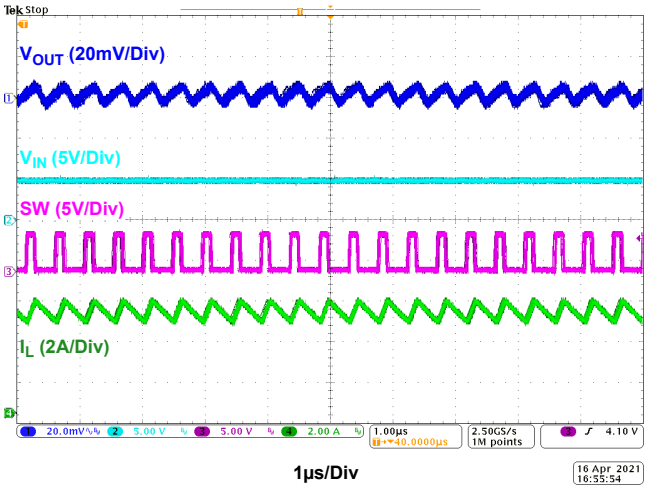


Figure 39. Steady State at Full Load

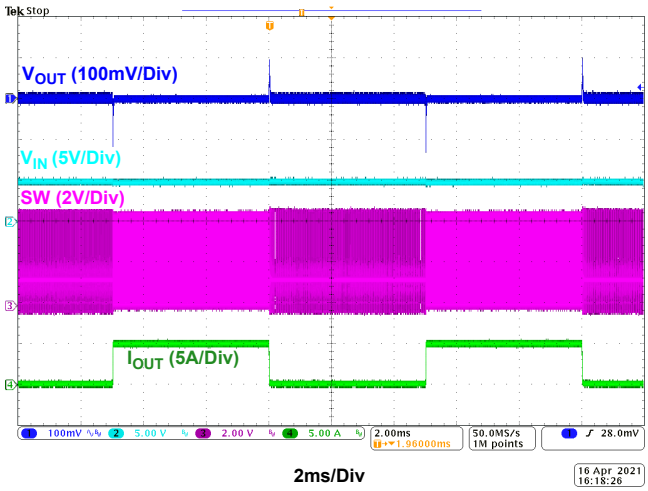


Figure 40. Load Transient 0A-5A

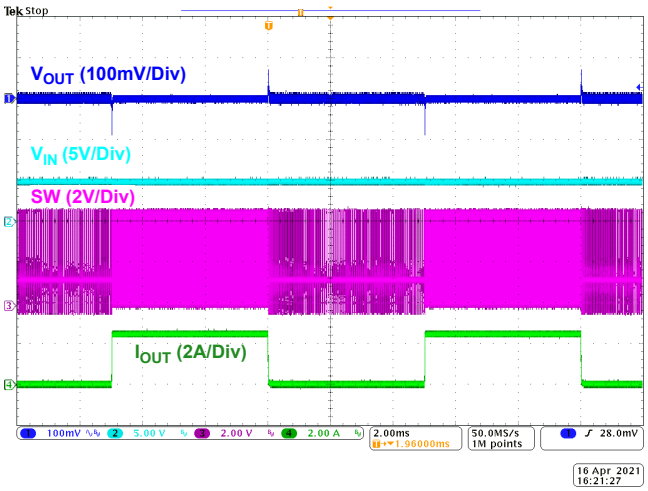


Figure 41. Load Transient 0A-2.5A

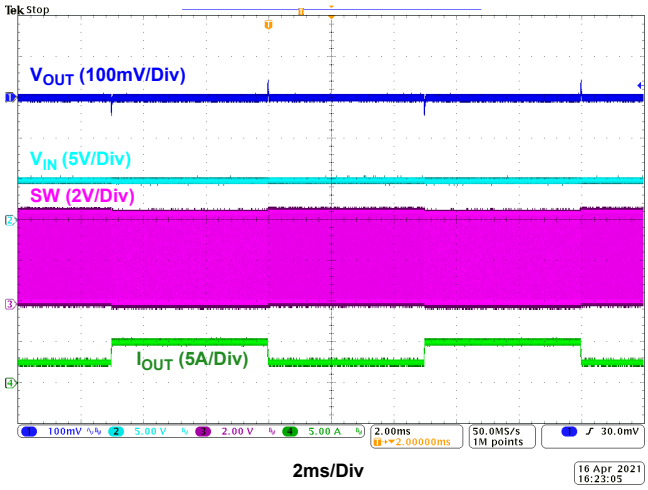


Figure 42. Load Transient 2.5A-5A

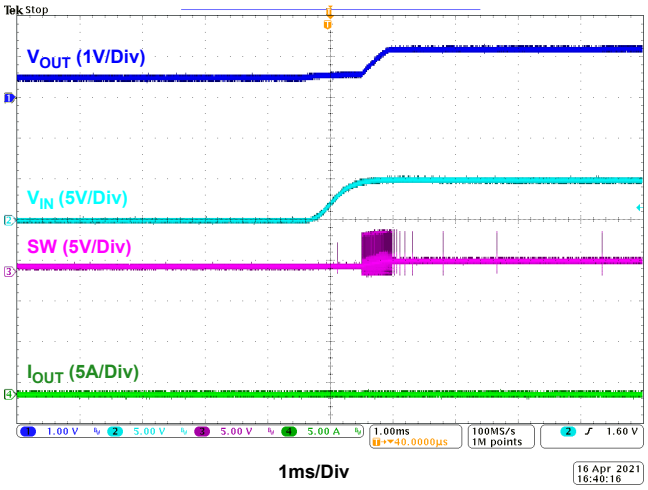


Figure 43. Pre-Bias Startup, Vpre = 0.5V

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C (Cont.)

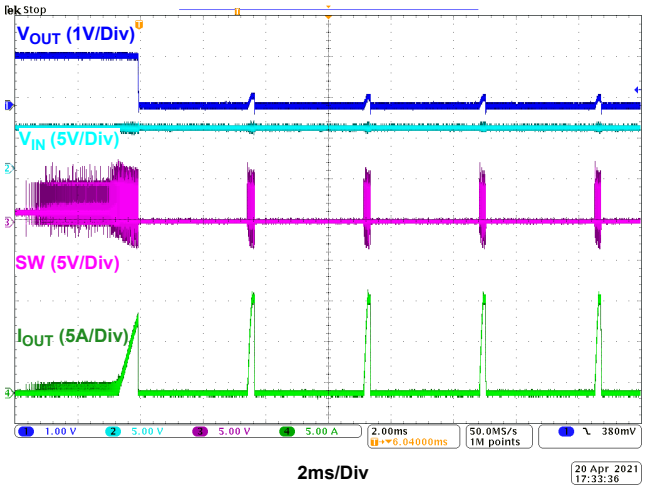


Figure 44. Hiccup with Output Short, No Load

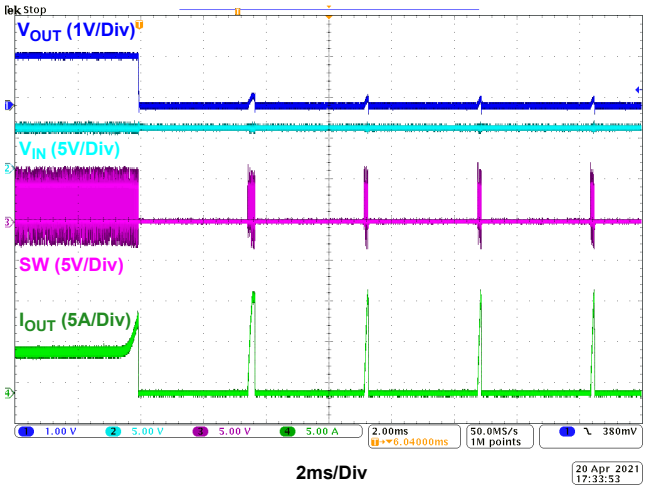


Figure 45. Hiccup with Output Short, Full Load

5. Functional Description

The RAA808015A is the low voltage buck regulator capable of running at 100% duty cycle. It can output 5A current continuous from a 2.7V to 5.5V input voltage with excellent load and line regulation. The protection includes input UVP, cycle-by-cycle peak current limit, hiccup mode OCP, and OTP. The constant on-time control scheme provides fast response for dynamic load and high-efficiency for light load.

Comparing to the traditional COT, RAA808015A offers a nearly constant frequency by input voltage feedforward and output voltage feedback. It can keep the frequency at 1.8MHz(typical) across the full input and output voltage range. The RAA808015A can run in DCM by zero cross detector circuit to achieve high efficiency at light load. Also, it can achieve low standby power loss.

The chip can run in constant off-time mode when V_{IN} is close to V_{OUT}. It can keep the V_{OUT} in the regulation even if V_{IN} is close to V_{OUT}. The 100% duty cycle can be achieved when V_{OUT} is equal to V_{IN}.

5.1 Soft-Start

When V_{IN} reaches 2.65V and EN is high, the PWM starts up with an internal soft-start cap being charged by an internal current source. The soft-start time is 800µs and pre-bias start-up is supported.

5.2 Constant On-Time Operation

RAA808015A operates in constant on-time mode in most light load to full load, regulating the output voltage with constant on time operation. With the V_{IN} feedforward and V_{OUT} feedback, the switching frequency in this mode is almost constant.

5.3 100% Duty Cycle

When the input voltage is lower than the output set point, the high-side MOSFET (HS-FET) stays on to keep the output voltage equal to the input voltage.

5.4 Light-Load Operation

When the load is light and the valley of the inductor current drops below zero, the RAA808015A switches to DCM mode.

When the load is light enough, the RAA808015A enters into PFM Sleep mode. In the Sleep mode, off-time increases, and some unnecessary circuits are disabled for power saving. Figure 46 shows the DCM operation. The IC enters the DCM mode of operation when the inductor current crossing zero is detected.

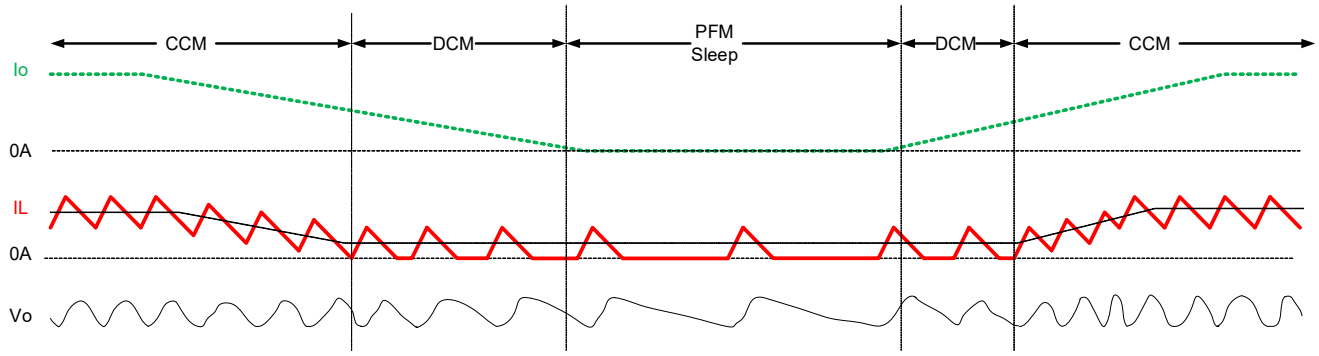


Figure 46. DCM Mode Operation Waveforms

5.5 Undervoltage Protection (UVLO)

The UVLO continuously monitors the VCC voltage to make sure the device works properly. When the VCC is high enough to reach the UVLO high threshold voltage, the regulator starts up or pre-bias to its regulated output voltage. When the VCC decreases to its low threshold voltage, the device shuts down.

5.6 Power-Good

PG is the open-drain output of a comparator with an internal 500kΩ pull-up resistor that continuously monitors the buck regulator output voltage using the FB pin. PG is actively held low when EN is low and during the soft-start period. After the soft-start period completes, PG becomes high impedance provided the FB pin is higher than the threshold specified in Power-Good in the Electrical Specifications table. Should FB be lower than 85% of the set point of 0.6V, PG is pulled low until FB returns. Over-temperature faults also force PG low until the fault condition is cleared by an attempt to soft-start.

5.7 Enable Operation

The EN turn on threshold is 1.2V max. As a result, this pin must not be left floating and should be tied to VIN if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open-drain outputs to control the EN pin.

5.8 Protection Features

5.8.1 Cycle-by-Cycle Peak Current Limit

The RAA808015A has a typical 7.8A current limit for the HS-FET. When the HS-FET hits its current limit, it shuts down immediately until the next cycle. This prevents the inductor current from rising and possibly damaging the components.

5.8.2 HICCUP OCP

RAA808015A operates in Hiccup mode after three continuous current limit cycles. Hiccup time is 3.6ms. See Figure 47.

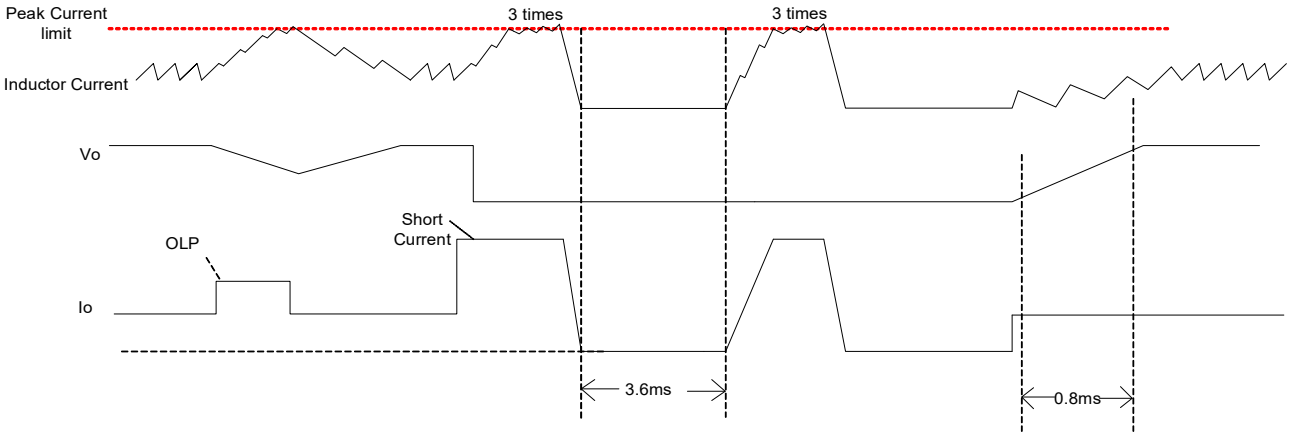


Figure 47. OCP and SCP Protection

5.8.3 Over-Temperature Protection

Over-temperature protection limits maximum junction temperature in the RAA808015A. When junction temperature (T_J) exceeds 160°C, both FETs are turned off and the controller waits for temperature to decrease by approximately 15°C. During this time, PG is pulled low. When the temperature is within an acceptable range, the controller initiates a normal soft-start sequence. For continuous operation, the 125°C junction temperature rating should not be exceeded.

6. Application Information

6.1 Output Voltage Setting

The regulator output voltage is easily programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; see Figure 48.

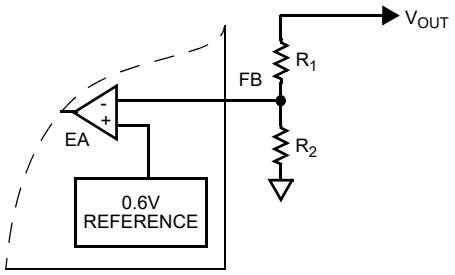


Figure 48. External Resistor Divider

The output voltage programming resistor, R_2, depends on the value chosen for the feedback resistor, R_1, and the desired output voltage, V_{OUT}, of the regulator. Equation 1 describes the relationship between V_{OUT} and resistor values.

(EQ. 1) $$R_2 = \frac{R_1 \times 0.6V}{V_{OUT} - 0.6V}$$

If the required output voltage is 0.6V, R_2 shoul be smaller than 500kΩ and R_1 is 0Ω.

6.2 Output Inductor Selection

The inductor value determines the ripple current of the inductor. Choosing an inductor value requires a somewhat arbitrary choice of ripple current. A reasonable starting point is 30% of total load current. The inductor value is then calculated using Equation 2:

(EQ. 2) $$L = \frac{V_{IN} - V_{OUT}}{FS \times \Delta I} \times \frac{V_{OUT}}{V_{IN}}$$

Increasing the value of inductance reduces the ripple current and therefore, the ripple voltage. However, the larger inductance value can reduce the response time of the converter to a load transient. The inductor current rating should be such that it does not saturate in overcurrent conditions. For typical RAA808015A applications, inductor values are typically 0.47µH.

6.3 Output Capacitor Selection

An output capacitor is required to reduce the output ripple voltage. The control loop allows the use of low ESR ceramic capacitors enabling small solution size on the PC board. Electrolytic and polymer capacitors can also be used.

Although ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the datasheets to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published; however, an assumption of ~20% further reduction generally suffices. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. However, ceramic capacitors are a good choice in many applications because of their reliability and extremely low ESR.

Equation 3 allows the calculation of the required capacitance to meet the required ripple voltage level. Additional capacitance can be used.

(EQ. 3) $$V_{OUTripple} = \left(\frac{\Delta I}{8 \times f_{SW} \times C_{OUT}} + \Delta I \times ESR\right)$$

In Equation 3, ΔI is the peak-to-peak ripple current of the inductor, f_{SW} is the switching frequency, C_{OUT} is the output capacitor, ESR is the equivalent series resistance of the output capacitor. **Note:** This is only a simple engineering algorithm to calculate the output ripple voltage because the phase of ripple voltage generated by the capacitor charging is different from that generated by the ripple current on ESR.

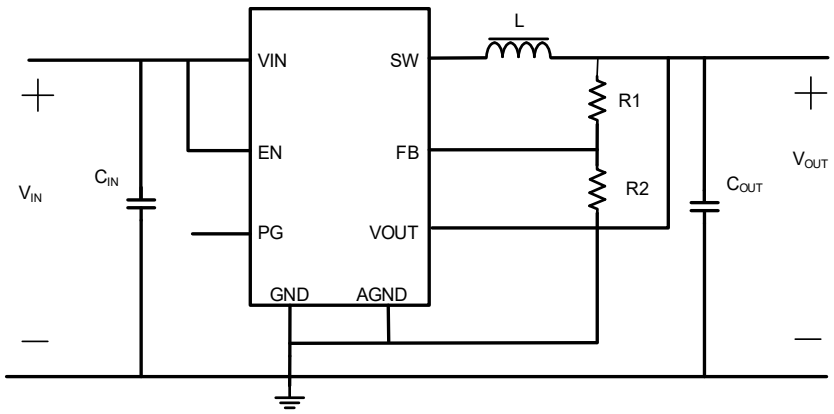


Figure 49. Application Circuit

7. Layout Considerations

Proper layout of the power converter minimizes EMI and noise and insure first pass success of the design. PCB layouts are provided in multiple formats on the Renesas web site. In addition, Figure 50 makes clear the important points in PCB layout. In reality, PCB layout of the RAA808015A is quite simple.

- A multi-layer printed circuit board with GND plane is recommended. Figure 50 shows the connections of the critical components in the converter. **Note:** Capacitors on the input and output can each represent multiple physical capacitors. The most critical connections are to tie the PGND pin to the package GND pad. This connection of the GND pad to GND plane insures a low-impedance path for all return current, and an excellent thermal path to dissipate heat. With this connection made, place the high-frequency MLCC input capacitor near the VIN pin and use vias directly at the capacitor pad to tie the capacitor to the GND plane.
- The AGND and PGND pin connection should be as short as possible.
- Place the feedback divider close to the FB pin and do not route any feedback components near PHASE.

An example component placement is shown in Figure 50

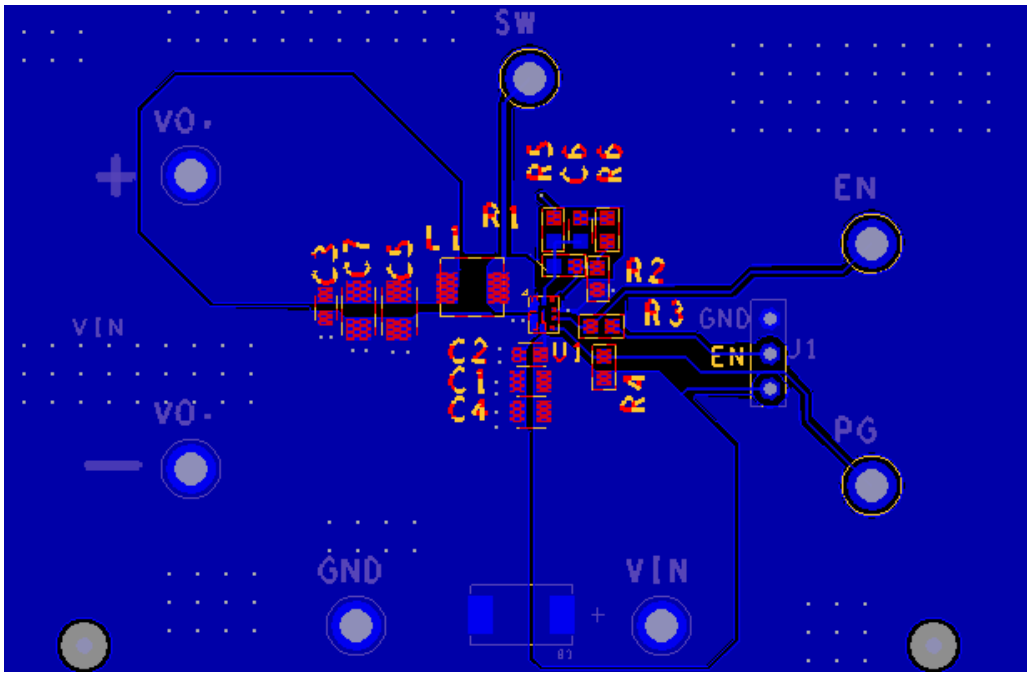


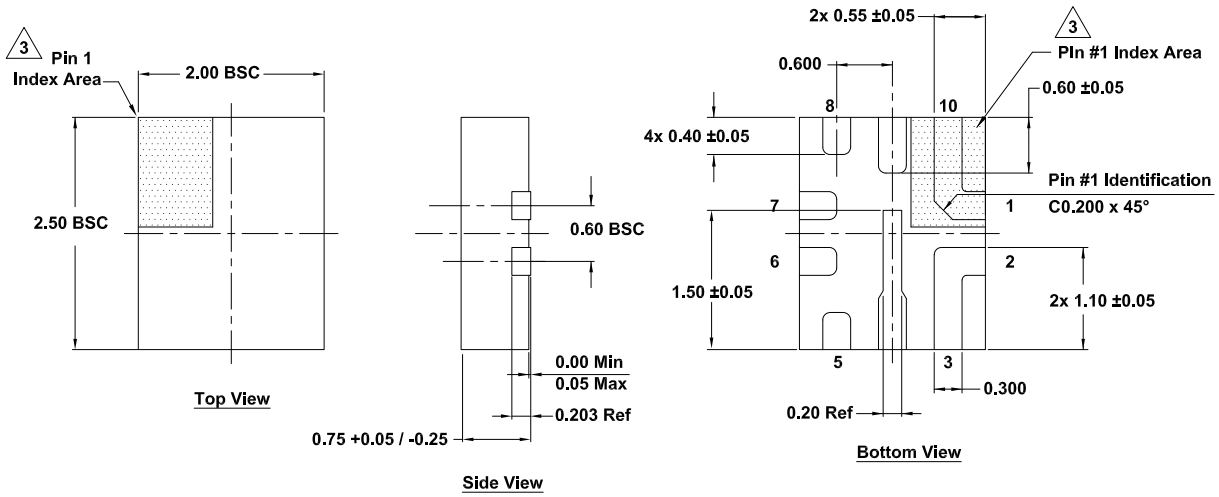
Figure 50. Printed Circuit Board Example Component Placement

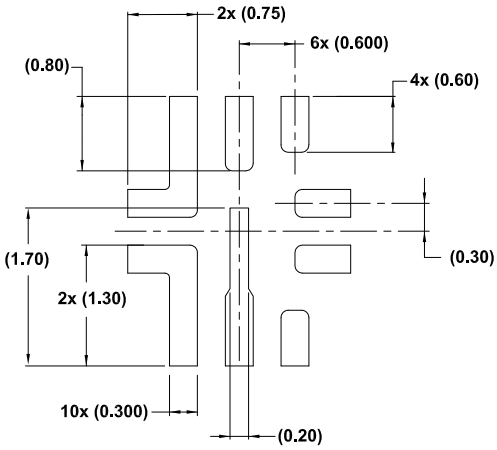
8. Package Outline Drawings

For the most recent package outline drawing, see L10.2x2.5.

L10.2x2.5

10 Lead 2x2.5 Flip Chip Quad Flat No-Lead Package (FCQFN)
Rev 0, 7/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.
4. Unless otherwise specified, tolerance: Decimal ±0.05

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA808015AGNP#HA0	85A	10 Lead 2x2.5 Flip-Chip QFN	L10.2x2.5	Reel, 6k	-40 to +125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA808015A device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.02	Jul 22, 2022	Updated 3.5 Electrical Specifications: Internal MOSFET, Power-Good, and Enable Voltage.
1.01	Jul 15, 2022	Updated Figures 4, 10, 11, 12, 13, and 14. Updated SW to GND (10ns) maximum spec changed 7V to 7.5V. Added IQ maximum spec. Added test condition to t_{SS} and F_S specs. For V_{PG_L} spec, removed Typical and added maximum. Updated test condition for the PG Internal Pull-Up Resistor and Input Threshold specifications.
1.00	May 26, 2022	Initial release