RC22514A

FemtoClock®2 Sub-100fs Frequency Synthesizer

The RC22514A is a small, low-power timing device designed to be placed immediately adjacent to a PHY, switch, ASIC or FPGA that requires several reference clocks with jitter performance less than 100fs (max). The device can act as a frequency synthesizer to locally generate the reference clock or as a DCO for frequency margining or OTN clock applications.

The RC22514A is a member of Renesas' high-performance FemtoClock2 family.

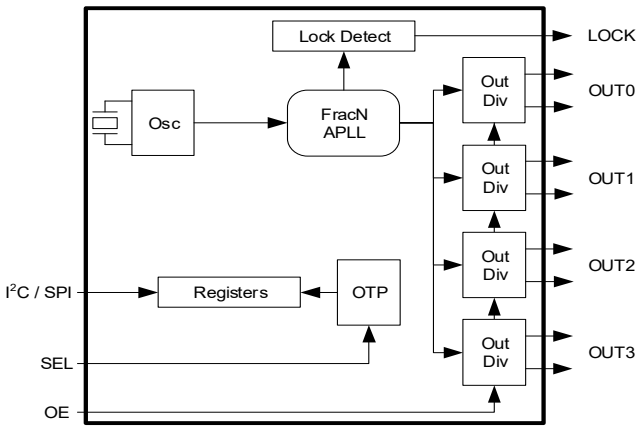
Applications

- Reference clock generator for 100Gbps / 400Gbps PHYs or switches
- Adjustable OTN clock reference for OTU3 / OTU4 mappers
- Reference clock for programmable FiberOptic Modules

Features

- Jitter below 100fs RMS maximum (10kHz to 20MHz)
- PLL core consists of fractional-feedback Analog PLL (APLL)
  - Operates from an integrated 78.125MHz crystal
  - APLL frequency independent of input / crystal frequency
  - Operates as a frequency synthesizer or Digitally Controlled Oscillator (DCO)
  - DCO has tuning granularity of < 1ppb
- Programmable status output
- 4 differential / 8 LVCMOS outputs
  - Any frequency from 10MHz to 1GHz (180MHz for LVCMOS)
  - Programmable output buffer supports HCSL (DC-coupled), LVDS/LVPECL/CML (AC-coupled) or two LVCMOS
  - Differential output swing is selectable: 400mV to 800mV
  - Output Enable input with programmable effect
- Supports up to 1MHz I^2C or up to 20MHz SPI serial processor port
- Can configure itself automatically after reset via internal customer-definable One-Time Programmable (OTP) memory with up to four different configurations
- 4 × 4 mm 28-VFQFPN package

Block Diagram



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1. About this Document

1.1 Document Conventions

This document uses the following conventions.

1.1.1 Signal Notation

Signals are either active low or active high. An active-low signal has an active state of logic 0 (or the lower voltage level) and is denoted by a lowercase n prefix. An active-high signal has an active state of logic 1 (or the higher voltage level) and is not denoted by a special character. The following table illustrates the signal naming convention.

Table 1. Signal Naming Convention

State	Signal Naming
Active low	nNAME
Active high	NAME

1.1.2 Object Size Notation

- A byte is an 8-bit object.
- A half-word (hword) is a 16-bit object.
- A word is a 32-bit object.
- A double-word (dword) is a 64-bit object.

1.1.3 Numeric Notation

- Hexadecimal numbers are denoted by the prefix 0x (for example, 0x04).
- Binary numbers are denoted by the prefix 0b (for example, 0b010).
- Register blocks that have multiple iterations are denoted by [x:y] in their names; where x is first instance, and y is the last instance. For example, BLOCK[0:1] with a base address of 0x10 += 0x08 indicates there are two iterations of the registers defined for BLOCK, with instance 0 at a base address of 0x10 and instance 1 at a base address of 0x18.

1.1.4 Endianness

RC22514A uses little-endian notation.

The Least Significant Bit (LSB) in a data object is numbered with 0, and the Most Significant Bit (MSB) is numbered with the width of the object minus 1. For example, the LSB index of a word is 0 and the MSB is 31.

The least significant byte of a multi-byte register field is located at the base address of the register and subsequent bytes up to the most significant byte are located at increasing byte addresses. For example, given a half-word located at address 0x42, the least significant byte (bits 7:0) can be accessed at address 0x42, and the most significant byte (bits 15:8) can be accessed at address 0x43.

Some multi-byte register fields are updated atomically, where the values written to the lower order bytes are buffered but not applied to the internal logic until the most significant bits are written, which then triggers the entire new register field value to be applied to the internal logic at once. Atomic registers fields are noted in the description.

When a multi-byte register field is non-atomic (the default if not noted otherwise), the value written to any byte of the field is immediately applied to the internal logic.

2. Pin Information

2.1 Pin Assignments

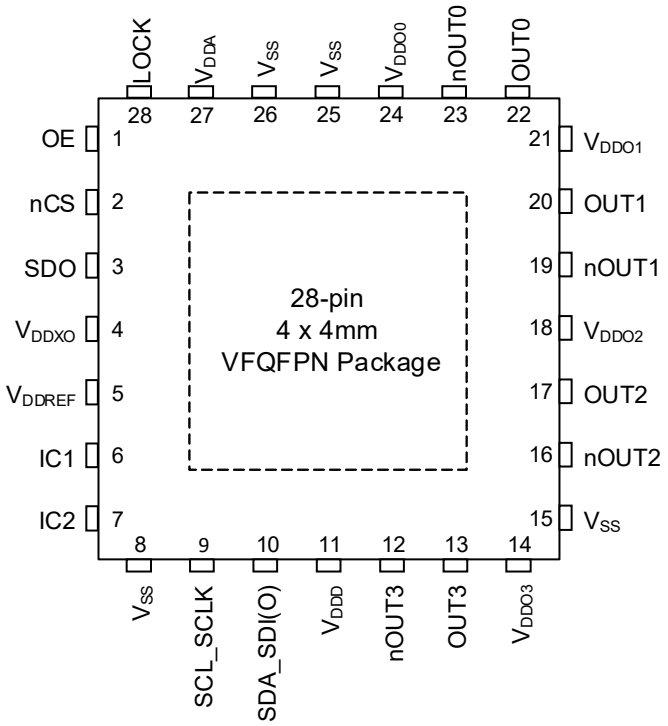


Figure 1. Pin Assignments – Top View

2.2 Pin Descriptions

Table 2. Pin Descriptions

Number	Name	Type		Description
1	OE	I	Optional Pullup/ Pulldown	Output Enable signal for all clock outputs when oe_sel is set to 0. Polarity, pull-up enable and pull-down enable are controlled by the oe_pol, oe_pu, and oe_pd register fields, respectively.
2	nCS	I		I^2C Mode: Unused SPI Mode: Chip Select
3	SDO	O		I^2C Mode: Unused SPI Mode: Data Out (4-wire) and Unused (3-wire)
4	V_{DDXO}	Power		Oscillator supply. 1.8V supported.
5	V_{DDREF}	Power		Reference input supply. 1.8V supported.
6	IC1	I		Internal Connect: Leave unconnected or tie to a test point.
7	IC2	I		Internal Connect: Leave unconnected or tie to a test point.
8	V_{SS}	Power		Negative supply voltage. Connect to same supply as the EPAD.
9	SCL_SCLK	I	Optional Pull-up	I^2C Mode: I^2C interface bi-directional clock. SPI Mode: Serial Clock The pull-up enable is controlled by the scl_pu register field.
10	SDA_SDI(O)	I/O	Optional Pull-up	I^2C Mode: I^2C interface bi-directional data in open-drain mode. SPI Mode: Serial Data In and Out (3-wire)/Serial Data In (4-wire) The pull-up enable is controlled by the sda_pu register field.
11	V_{DDD}	Power		Core digital function supply. 1.8V or 3.3V supported. Note that the digital power consumption is increased when operating above 1.8V (for information, see Power Considerations). OE, nCS. SDO, SCL_SCLK, and SDA_SDI(O) are referenced to this voltage.

Table 2. Pin Descriptions (Cont.)

Number	Name	Type		Description
12	nOUT3	O		Output Clock 3 negative.
13	OUT3	O		Output Clock 3 positive.
14	V_{DDO3}	Power		Supply voltage for output pair OUT3 and nOUT3. 1.8V supported. This pin can be left unconnected if clock output 3 is unused and the corresponding out_pd bit is set to 1.
15	V_{SS}	Power		Negative supply voltage. Connect to same supply as the Epad.
16	nOUT2	O		Output Clock 2 negative.
17	OUT2	O		Output Clock 2 positive.
18	V_{DDO2}	Power		Supply voltage for output pair OUT2 and nOUT2. 1.8V supported. This pin can be left unconnected if clock output 2 is unused and the corresponding out_pd bit is set to 1.
19	nOUT1	O		Output Clock 1 negative.
20	OUT1	O		Output Clock 1 positive.
21	V_{DDO1}	Power		Supply voltage for output pair OUT1 and nOUT1. 1.8V supported. This pin can be left unconnected if clock output 1 is unused and the corresponding out_pd bit is set to 1.
22	OUT0	O		Output Clock 0 positive.
23	nOUT0	O		Output Clock 0 negative.
24	V_{DDO0}	Power		Supply voltage for output pair OUT0 and nOUT0. 1.8V supported. This pin can be left unconnected if clock output 0 is unused and the corresponding out_pd bit is set to 1.
25, 26	V_{SS}	Power		Negative supply voltage. Connect to same supply as the Epad.
27	V_{DDA}	Power		Analog function supply for core analog functions. 1.8V supported. LOCK is referenced to this voltage.
28	LOCK	O	See description	PLL lock status or other status as selected by lock_sel. Polarity, pull-up enable and pull-down enable are controlled by the lock_pol, lock_pu, and lock_pd register fields, respectively.
EPAD	V_{SS}	Power		Negative supply voltage. Epad must be connected before any positive supply voltage is applied.

Table 3. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE		-	1.6	-	pF
		SCL_SCLK		-	8	-	pF
		SDA_SDI(O)		-	160	-	pF
R_{PULLUP}	Input Pull-Up Resistor	OE		51	54	57	kΩ
		nCS		51	53	57	kΩ
		SCL_SCLK		51	54	57	kΩ
		SDA_SDI(O)		51	54	57	kΩ
	Output Pull-Up Resistor	LOCK		51	54	57	kΩ
		SDO		51	53	57	kΩ
$R_{PULLDOWN}$	Input Pull-Down Resistor	OE					kΩ
	Output Pull-Down Resistor	LOCK		51	54	57	kΩ
		SDO		51	53	57	kΩ
R_{OUT}[1]	Output Impedance	LOCK	V_{DDA} = 1.89V	30	43	70	Ω
		SDA_SDI(O)	V_{DDD} = 1.89V	48	49	50	Ω
		SDO		30	43	70	Ω

[1] Output impedance for the clock outputs are provided in Table 19.

3. Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC22514A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
V_{DD33}	3.3V power supplies	V_{DDD}	-0.5	3.63	V
V_{DD18}	1.8V power supplies	V_{DDREF}, V_{DDXO}, V_{DDA}, V_{DDO3}, V_{DDO2}, V_{DDO1}, V_{DDO0}	-0.5	1.98	V
V_{IN}	Voltage on any input		-0.5	3.63	V
I_O	Output Current - Continuous	OUT0/1/2/3	-	30	mA
		LOCK, SDA_SDI(O), SDO	-	25	mA
	Output Current - Surge	OUT0/1/2/3	-	60	mA
		LOCK, SDA_SDI(O), SDO	-	50	mA
T_{JMAX}	Maximum Junction Temperature		-	150	°C
T_S	Storage temperature		-65	150	°C
-	ESD - Human Body Model		-	2000	V
-	ESD - Charged Device Model		-	500	V

3.2 Recommended Operating Conditions

Table 5. Recommended Operating Conditions[1][2]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction temperature	-	-	125	°C
T_A	Ambient air temperature	-40	-	85	°C
V_{DDREF}	Supply Voltage for Input Clock Buffers and Dividers	1.71	1.8	1.89	V
V_{DDXO}	Supply Voltage for Crystal Oscillator	1.71	1.8	1.89	V
V_{DDA}	Supply Voltage for Analog Core	1.71	1.8	1.89	V
V_{DDD}	Supply Voltage for Digital Core[3]	1.71	1.8/3.3	3.465	V
V_{DDOx}[4]	Supply Voltage for Output Clock Driver and Divider[5]	1.71	1.8	1.89	V
t_{PU}	Power Up Time for V_{DDx} - for all supply voltages to reach minimum specified voltage (power ramps must be monotonic)[6]	0.05	-	5	ms

[1] It is your responsibility to ensure that device junction temperature remains below the maximum allowed.

[2] All conditions in this table must be met to ensure device functionality.

[3] Supports 1.8V ±5% or 3.3V ±5% operation, not a continuous range.

[4] V_{DDOx} represents any of V_{DDO3}, V_{DDO2}, V_{DDO1}, or V_{DDO0}.

[5] Currents for the outputs are shown in Table 12 as appropriate for the mode the individual output is operating in.

[6] This implies all supply rails must reach their minimum voltage within maximum T_{PU}.

3.3 Reference Clock Phase Jitter and Phase Noise

Table 6. Output Phase Jitter Characteristics[1][2]

Symbol	Parameter		Test Condition		Typical	Maximum	Unit
tjit(Φ)	Phase Jitter, RMS (Random)[3]		10kHz to 20MHz 78.125MHz Crystal[4]; Synthesizer Mode	106.25MHz	78	100	fs
				125MHz	73	100	fs
				156.25MHz	72	100	fs
				212.5MHz	71	100	fs
				312.5MHz	67	100	fs
Φ_{SSB}(100k)	Single Sideband Phase Noise	100kHz	156.25MHz input, Clock Generator Mode; All outputs enabled at 156.25MHz		-148	-	dBc/Hz
Φ_{SSB}(1M)		1MHz			-153	-	dBc/Hz
Φ_{SSB}(10M)		10MHz			-165	-	dBc/Hz
Φ_{SSB}(30M)		≥30MHz			-167	-	dBc/Hz

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.

[4] APLL at 10.625GHz to allow for outputting common ETH/FC frequencies.

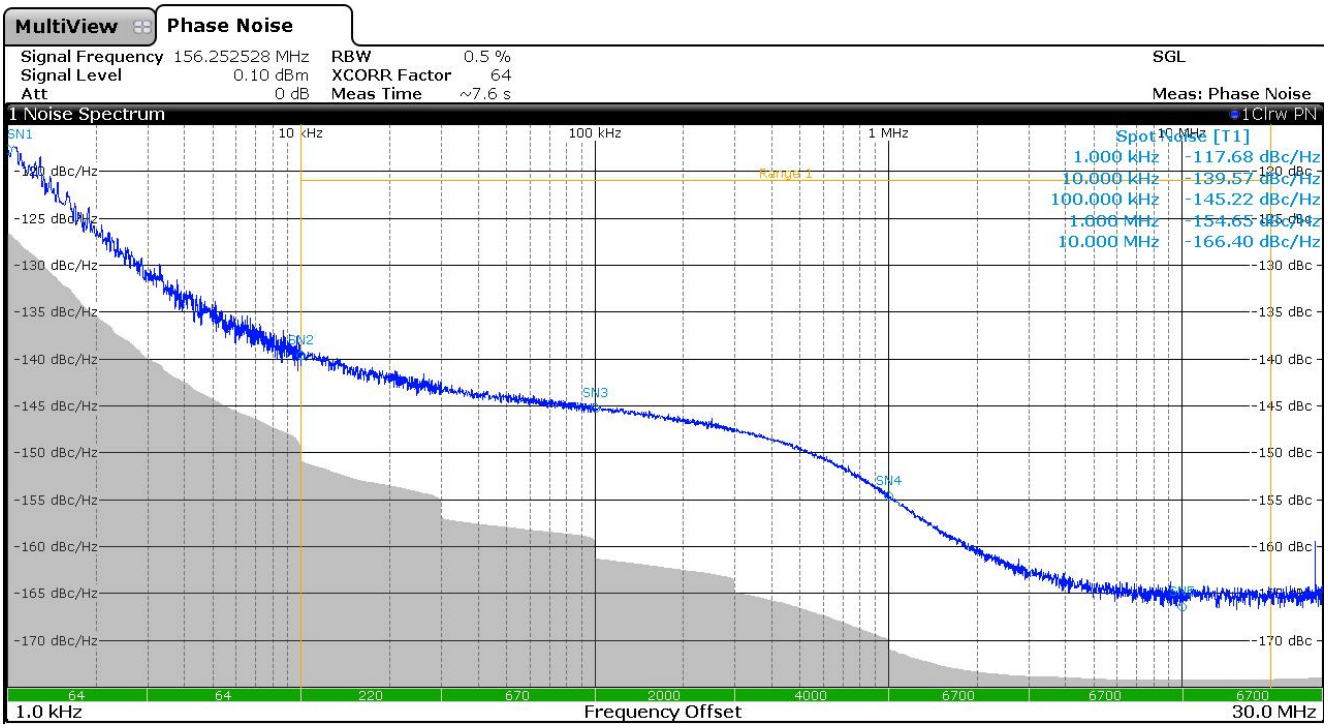


Figure 2. 156.25MHz Output Phase Noise - Integer Synthesizer Mode

Table 7. PCI Express Jitter Specifications[1][2]

Symbol	Parameter	Test Conditions	Typical	PCIe Industry Specification	Unit
$t_{jphPCIeG1-CC}$	PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen 1 (2.5 GT/s)[3][4]	0.836	86	ps (p-p)
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Lo Band (5.0 GT/s)[3][4]	0.014	3	ps (RMS)
		PCIe Gen 2 Hi Band (5.0 GT/s)[3][4]	0.055	3.1	ps (RMS)
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (8.0 GT/s)[3][4]	0.022	1	ps (RMS)
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (16.0 GT/s)[3][4][5]	0.029	0.5	ps (RMS)
$t_{jphPCIeG5-CC}$		PCIe Gen 5 (32.0 GT/s)[3][4][6]	0.008	0.15	ps (RMS)

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 5.0, Revision 1.0*. For the exact measurement setup, see the Test Loads section of the datasheet. The worst case results for each data rate are summarized in this table.

[4] Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a Real-Time Oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to a peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[5] In channel simulations to account for additional noise in a real system, 0.7ps RMS must be used.

[6] In channel simulations to account for additional noise in a real system, 0.25ps RMS must be used.

3.4 AC Electrical Characteristics

Table 8. Input Frequency Characteristics[1]

Symbol	Parameter		Test Condition	Minimum	Maximum	Unit
f_{SCLK}	Serial Port Clock SCL_SCLK	I^2C Operation	Slave Mode	100	1200	kHz
		SPI Operation	Slave Mode	0.1	20	MHz

[1] V_{DDXO} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C

Table 9. PLL Characteristics[1][2]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
f_{VCO}	Analog PLL VCO Operating Frequency			9.7	-	10.7	GHz
Δf_{OUT}	Output frequency tuning resolution		DCO Mode	$[2^{-40} \times 1e12] = 0.91$			ppt
f_{PFD}	Analog Phase/Frequency Detector (PFD) Operating Frequency		Integer VCO feedback	50	-	312.5	MHz
f_{MON}	Reference Monitor Operating Frequency	CLKMON0/1		-	-	33	MHz
		CLKMON2		-	-	312.5	MHz
$t_{startup}$	Start-up Time[3]	Internal OTP Start-up	Synthesizer mode	-	7	10	ms

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Measured from when all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.

Table 10. Output Frequency Characteristics[1][2]

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	Differential Output			10	-	1000	MHz
		LVCMOS Output			10	-	180	MHz
t_{SK}	Output to Output Skew[3][4]	Differential[5]	Any two outputs		-	40	45	ps
		LVCMOS[6]	Any OUTx to any other OUTx or any nOUTx to any other nOUTx		-	80	90	ps
			OUTx to nOUTx of the same output pair, configured in-phase		-	80	90	ps
Δt_{SK}	Temperature Variation[7] Output-Output				-	-	1	ps/°C
Δt_{PD}	Input to Output Delay Variation Differential[5]		Any mode		-	-	±200	ps
t_R / t_F	Output Rise and Fall Times 20% to 80%	Differential Output[8]	HCSL Mode	SWING[9] = Any	-	-	120	ps
			LVDS Mode	SWING[10] = Any	-	-	180	ps
		LVCMOS Output[11]	V_{DDOx} = 1.8V ±5%		-	-	800	ps
odc	Output Duty Cycle	Differential Output	$f_{OUT} \leq f_{VCO}$ / N; N = 10, 12, …		48	50	52	%
			$f_{OUT} \leq f_{VCO}$ / N; N = 39, 41, …		48	50	52	%
			$f_{OUT} \leq f_{VCO}$ / N; N = 11, 13, …37		45	50	55	%
		LVCMOS	Any frequency		45	50	55	%
ΔF/F	Frequency Stability (Free-run)		Over 10 years. Inclusive of 25ºC tolerance, operating temperature range, input voltage change, load change, aging, shock, and vibration.		-50		50	PPM

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.

[4] This parameter is defined in accordance with JEDEC Standard 65.

[5] Measured at the differential cross points.

[6] Measured at V_{DDOx} / 2.

[7] This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.

[8] Measured with outputs terminated with 50Ω to GND.

[9] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[10] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

[11] Measured with outputs terminated with 50Ω to V_{DDOx} / 2.

Table 11. Power Supply Noise Rejection[1][2]

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection[3][4]	f_{NOISE} ≤1MHz	V_{DDOx} = 1.8V[5]	-105	-94	-	dBc
			V_{DDXO} = 1.8V	-95	-87	-	dBc
		f_{NOISE} ≤100kHz	V_{DDREF} = 1.8V	-95	-86	-	dBc
			V_{DDD} = 1.8V	-140	-114	-	dBc
		100kHz <f_{NOISE} ≤600kHz	V_{DDREF} = 1.8V	-140	-109	-	dBc
			V_{DDD} = 1.8V	-100	-96	-	dBc
		600kHz <f_{NOISE} ≤1MHz	V_{DDREF} = 1.8V	-155	-143	-	dBc
			V_{DDD} = 1.8V	-105	-99	-	dBc

[1] V_{DDXO} = V_{DDREF} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] 50mV peak-to-peak sine-wave noise signal injected on indicated power supply pin(s).

[4] Noise spur amplitude measured relative to 156.25MHz carrier.

[5] Excluding V_{DDOx} of the output being measured.

3.5 DC Electrical Characteristics

Table 12. Power Supply DC Characteristics - Supply Current[1][2][3]

Symbol	Parameter	Test Condition		Current Consumption		Unit
				Typ	Max	
I_{DDREF}	Supply Current for V_{DDREF}[4]	1.8V LVCMOS input		8	13	mA
		HCSL input (P_N_Diff_Sel = 0, en_HCSL = 1)		10		mA
		LVDS input (P_N_Diff_Sel = 1, en_LVDS = 1)		11		mA
		AC-coupled differential input		5.5		mA
I_{DDXO}	Supply Current for V_{DDXO}	V_{DDXO} = 1.89V		5.5	10	mA
I_{DDA}	Supply Current for V_{DDA}	V_{DDA} = 1.89V		129	150	mA
I_{DDD}	Supply Current for V_{DDD}	V_{DDD} = 1.89V		25	30	mA
		V_{DDD} = 3.465V		26		mA
I_{DDOx}[5]	Supply Current for V_{DDOx}[6][7]	HCSL Mode	SWING[8] = 200mV	31	50	mA
			SWING = 250mV	32		mA
			SWING = 300mV	33		mA
			SWING = 350mV	34		mA
			SWING = 400mV	35		mA
			SWING = 450mV	36		mA
			SWING = 500mV	37		mA
			SWING = 550mV	39		mA
			SWING = 600mV	40		mA
			SWING = 650mV	41		mA
			SWING = 700mV	42		mA
			SWING = 750mV	43		mA
			SWING = 800mV	44		mA
			SWING = 850mV	45		mA
			SWING = 875mV	45		mA
			SWING = 900mV	46		mA
		LVDS Mode	AMP[9] = 350mV	30	40	mA
			AMP = 400mV	31		mA
		Output Disabled		28	50	mA
		Output Hi-Z		26	30	mA
		LVCMOS Mode	In phase	34	45	mA
			Opposite phase	34		mA
			nOUTx Disabled	31	40	mA
			OUTx Disabled	31		mA

[1] Output current consumption is not affected by any of the core device power supply voltage levels.

[2] Internal dynamic switching current at maximum f_{OUT} is included.

[3] V_{SS} = 0V, T_A = -40°C to 85°C.

[4] Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.

[5] I_{DDOx} denotes the current consumed by each V_{DDOx} supply.

[6] V_{DDOx} = 1.89V.

[7] Measured with outputs unloaded.

[8] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[9] Refers to the output voltage (amplitude) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

Table 13. LVCMOS Status and Control Signal DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DDD} = 3.3V ±5%	2	-	V_{DDD} + 0.3	V
		V_{DDD} = 1.8V ±5%	0.65 × V_{DDD}	-	V_{DDD} + 0.3	
V_{IL}	Input Low Voltage	V_{DDD} = 3.3V ±5%	-0.3	-	0.8	V
		V_{DDD} = 1.8V ±5%	-0.3	-	0.35 × V_{DDD}	
I_{IH}	Input High Current	V_{IN} = V_{DDD} = V_{DDD} (max)	-	-	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V, V_{DDD} = V_{DDD} (max)	-75	-	-	µA
V_{OH}	Output High Voltage	V_{DDD} = 3.3V ±5% or 1.8V ±5% I_{OH} = -100µA	V_{DDD} - 0.2	-	-	V
		(LOCK Signal Only) V_{DDA} = 1.8V ±5% I_{OH} = -100µA	V_{DDA} - 0.2	-	-	V
V_{OL}	Output Low Voltage	V_{DDD} = 3.3V ±5% or 1.8V ±5% V_{DDA} = 1.8V ±5% I_{OL} = 100µA	-	-	0.2	V

[1] 3.3V characteristics in accordance with JESD8C-01, 1.8V characteristics in accordance with JESD8-7A.

[2] V_{SS} = 0V, T_A = -40°C to 85°C.

[3] Input specifications see signals SCL_SCLK, SDA_SDI(O), OE, nCS. Output specifications see signals LOCK, SDO, SDA_SDI(O) (3-wire SPI).

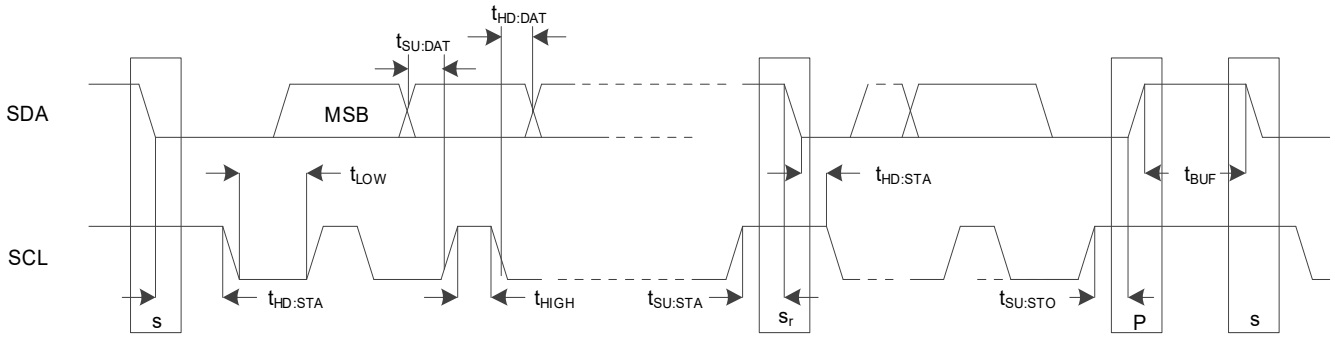


Figure 3. I²C Slave Timing Diagram

Table 14. I²C Slave Timing[1]

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD:STA}$	Hold time (repeated) START condition	4000	-	600	-	260	-	ns
t_{LOW}	LOW period of the SCL clock	4700	-	1300	-	500	-	ns
t_{HIGH}	HIGH period of the SCL clock	4000	-	600	-	260	-	ns
$t_{SU:STA}$	Set-up time for a repeated START condition	4700	-	600	-	260	-	ns
$t_{HD:DAT}$	Data hold time[2]	0[3]	-[4]	0[3]	-[4]	0	-	ns
$t_{SU:DAT}$	Data set-up time	250	-	100[5]	-	50	-	ns
$t_{SU:STO}$	Set-up time for STOP condition	4000	-	600	-	260	-	ns
t_{BUF}	Bus free time between a STOP and START condition	4700	-	1300	-	500	-	ns

[1] All values referred to V_{IH} (minimum) and V_{IL} (maximum) levels (see Table 13).

[2] $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, and applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] The maximum $t_{HD:DAT}$ could be 3.45µs and 0.9µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[5] A Fast mode I²C-bus device can be used in a Standard mode I²C-bus system, but the requirement $t_{SU:DAT}$ 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Table 15. I²C-Bus Characteristics

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	-	120	ns
t_f	Fall time of both SDA and SCL signals[1][2][3][4]	-	300	20 × (V_{DDD} / 5.5 V)	300	20 × (V_{DDD} / 5.5 V)[5]	120[4]	ns
C_D	Capacitive load for device on bus	-	5	-	5	-	5	pF

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[2] If mixed with Hs-mode devices, faster fall times are allowed.

[3] The maximum t_f for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_f is specified at 250ns, allowing series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[4] In Fast Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[5] Necessary to be backwards compatible to Fast mode.

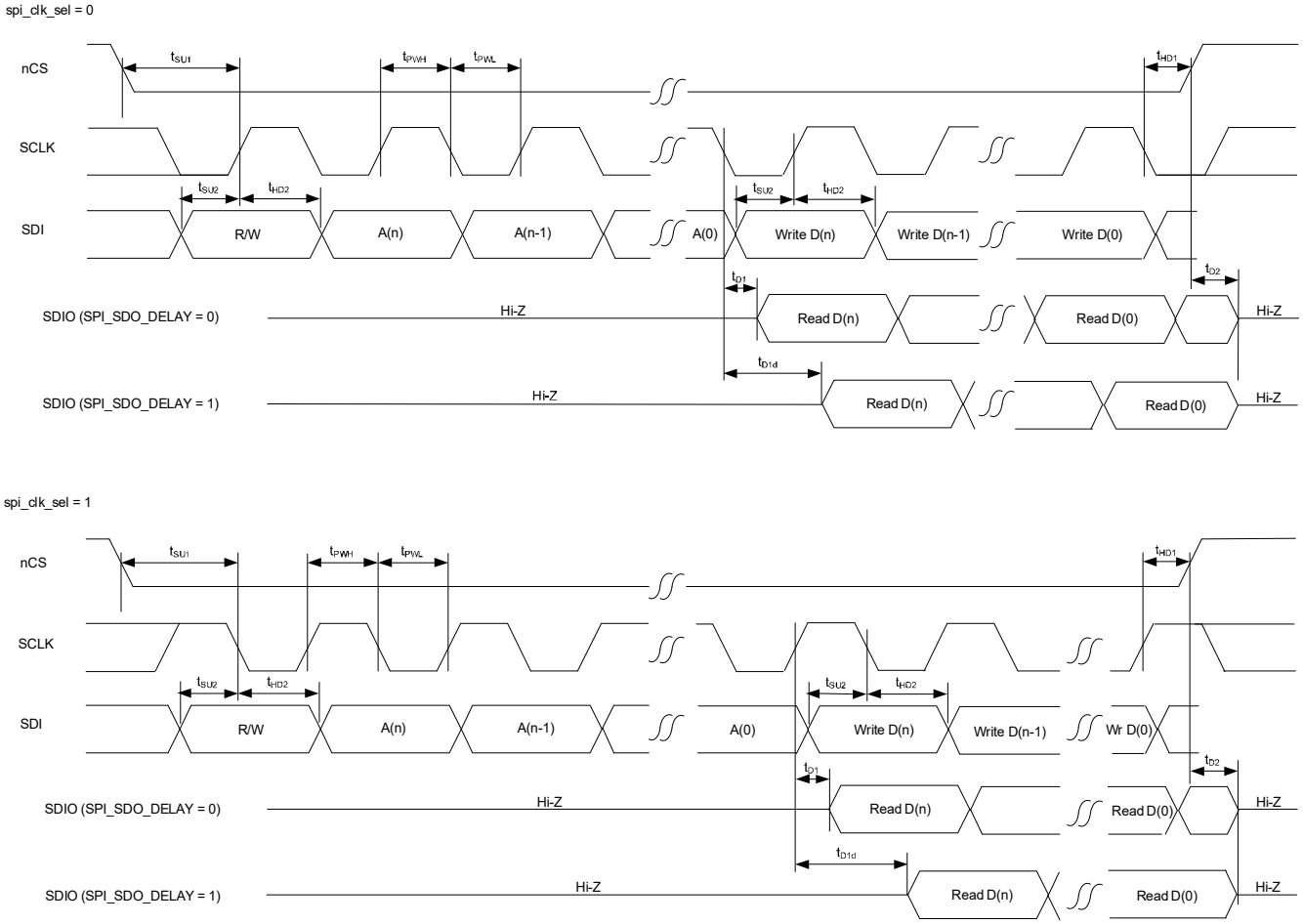


Figure 4. SPI Timing Diagram

Table 16. SPI Slave Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	-	-	20	MHz
t_{PWH}	SCLK Pulse Width High	25	-	-	ns
t_{PWL}	SCLK Pulse Width Low	25	-	-	ns
t_{SU1}	nCS Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{SU2}	SDIO Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD2}	SDIO Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{D1}	Read Data Valid Time from SCLK rising or falling edge with no data delay added	4	5.6	-	ns
t_{D1d}	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing[1]	t_{D1} + half SCLK period	-	-	ns
t_{D2}	SDIO Read Data Hi-Z Time from CS High[2]	-	10	-	ns

[1] Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.

[2] This is the time until the RC22514A releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

Table 17. Differential Clock Input DC Characteristics[1]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
$V_{I(PP)}$	Peak-to-Peak Voltage[2][3][4]		0.15	-	1.2	V
V_{CMR}	Common Mode Input Voltage[2][4][5][6]	PMOS input buffer (HCSL, P_N_Diff_Sel = 0)	VI(PP) / 2	0.35	V_{DDREF} - 1.2	V
		NMOS input buffer (LVDS, P_N_Diff_Sel = 1)	0.7	1.2	V_{DDREF} - (VI(PP) / 2)	V

[1] V_{DDREF} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] V^{IL} should not be less than -0.3V.

[3] V_{PP} is the single-ended amplitude of the input signal. The differential specification is 2*V_{PP}.

[4] V_{DDREF} = 1.8V ±5%. Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.

[5] Common-mode voltage is defined as the cross-point.

[6] Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection. For example, when supplying an LVDS input signal that is referenced to a 2.5V supply at its source, the V_{DDREF} supply must also be 2.5V nominal voltage.

Table 18. Differential Clock Output DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
V_{OUT}	Absolute Voltage on HCSL output	[4]		-125[5]	-	1150[6]	mV
V_{CROSS}	Absolute Voltage Output Crossing	HCSL Mode[7]		350	-	500	mV
ΔV_{CROSS}	Total Variation on HCSL output crossing over all edges[8]	[9]		-	30	100	mV
V_{OVS}[10]	Output Voltage Swing	HCSL Mode	SWING = 200mV[11]	195	-	250	mV
			SWING = 250mV	245	-	315	mV
			SWING = 300mV	295	-	380	mV
			SWING = 350mV	345	-	450	mV
			SWING = 400mV	395	-	520	mV
			SWING = 450mV	445	-	585	mV
			SWING = 500mV	495	-	645	mV
			SWING = 550mV	545	-	725	mV
			SWING = 600mV	595	-	780	mV
			SWING = 650mV	645	-	820	mV
			SWING = 700mV	685	-	855	mV
			SWING = 750mV	725	-	880	mV
			SWING = 800mV	755	-	915	mV
			SWING = 850mV	785	-	960	mV
			SWING = 875mV	810	-	1005	mV
			SWING = 900mV	825	-	1045	mV
		LVDS Mode	AMP = 350mV[12]	350	-	460	mV
			AMP = 400mV	365	-	500	mV

Table 18. Differential Clock Output DC Characteristics[1][2][3] (Cont.)

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
V_{CMR}	Output Common Mode Voltage	LVDS Mode[13]	CENTER = 700mV[14]	650	-	750	mV
			CENTER = 800mV	750	-	850	mV
			CENTER = 900mV	800	-	950	mV
			CENTER = 1000mV	900	-	1050	mV

[1] V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Terminated with 100Ω across OUTx and nOUTx.

[3] OUTx refers to any of the output pairs OUT3/nOUT3, OUT2/nOUT2, OUT1/nOUT1 or OUT0/nOUT0.

[4] Measurement taken from single-ended waveform.

[5] Defined as the minimum instantaneous voltage including undershoot.

[6] Defined as the maximum instantaneous voltage including overshoot.

[7] Terminated with 50Ω to GND on each of OUTx and nOUTx.

[8] Defined as the total variation of all crossing voltages of rising OUTx and falling nOUTx, This is the maximum allowed variance for any particular system.

[9] Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[10] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.

[11] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[12] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

[13] Terminated with 100Ω across OUTx and nOUTx.

[14] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output using the ODRV_MODE_CNFG Register.out_lvds_cm_voltage field for each output.

Table 19. LVCMOS Clock Output DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{DDOx} = ±100µA	V_{DDOx} - 0.2	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
Z_{OUT}	Output Impedance		41	51	67	Ω

[1] V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Applies to any of OUT3, nOUT3, OUT2, nOUT2, OUT1, nOUT1, nOUT0, or OUT0.

[3] Output voltages compliant with JESD8-7A, Normal Range.

4. Applications Information

4.1 Power Considerations

For power and current consumption calculations, see the Renesas Timing Commander tool.

4.2 Recommendations for Unused Input and Output Pins

4.2.1 LVCMOS Control Pins

LVCMOS control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

4.2.2 LVCMOS Outputs

Any LVCMOS output must be left floating if unused. There should be no trace attached. Set the mode of the output buffer to a high-impedance state to avoid any noise being generated.

4.2.3 Differential Outputs

All unused differential outputs must be left floating. Renesas recommends that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

4.3 Clock Input Interface

The RC22514A provides a programmable input buffer for reference clock inputs, as shown in Figure 5. This programmable buffer allows most standard signaling protocols to be supported with no need for external termination components at the receiver end of the transmission line.

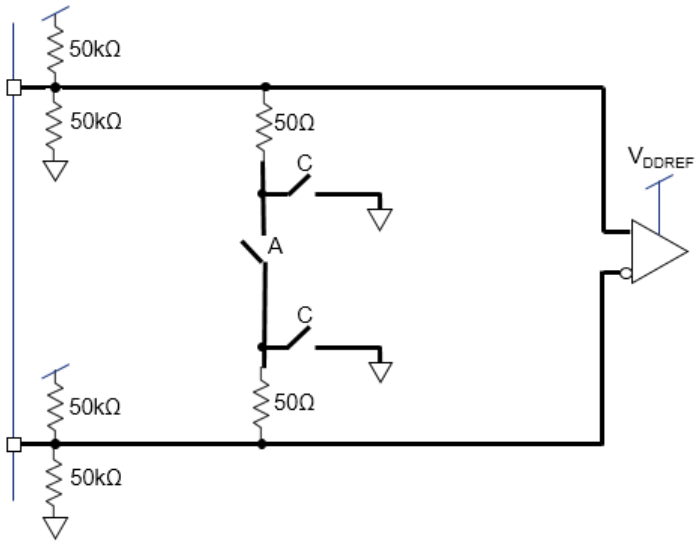


Figure 5. Programmable Input Buffer Logical Diagram

By making appropriate register selections, the switches labeled A and C in Figure 5 can be closed as shown in Table 20 to support the indicated protocols. With the switches closed as indicated, the input buffer behaves as shown in Figure 6 for the various input reference signal protocols.

Note: HCSL is sometimes used in an 85Ω transmission line environment and this input buffer supports that with no external terminations needed. However, this is not expected to be used often in RC22514A applications.

Table 20. Input Buffer Programming Options for Specific Signaling Protocols

Input Signaling Protocol	Register Setting	Switches Closed	V_{DDREF} Voltage Required
LVDS	REF_CLK_IN_CNFG Register.en_LVDS	A	1.8V
HCSL	REF_CLK_IN_CNFG Register.en_HCSL	C	1.8V[1]
1.8V LVCMOS	REF_CLK_IN_CNFG Register.CMOS_Sel	-	1.8V
Externally AC-coupled LVCMOS[2]	REF_CLK_IN_CNFG Register.en_selfbias_cmos	-	1.8V
Externally AC-coupled[2]	REF_CLK_IN_CNFG Register.en_dc_bias	-	1.8V

[1] Only a 1.8V V_{DDREF} is supported. If a higher VDD is used by the transmitter, then External AC-coupling must be used.

[2] In this mode of operation, AC-coupling capacitors must isolate the voltage level of the transmitter from the receiver. The signal must be properly termination on the transmitter side of the AC-coupling capacitors. No terminations are needed between the AC-coupling capacitors and the RC22514A.

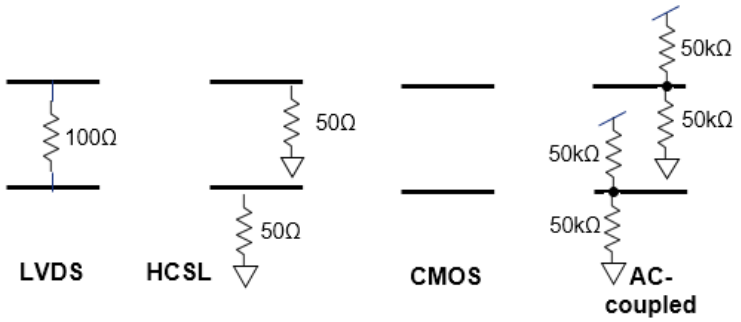


Figure 6. Input Buffer Behavior by Protocol

4.4 Differential Output Termination

The RC22514A provides a programmable output buffer for clock outputs. This buffer allows most standard signaling protocols to be supported with no need for external termination components at the transmitter side of the transmission line.

Note: Many receivers of the type expected to be used with a high-performance device like RC22514A are equipped with internal terminations that can include trace termination, voltage biasing, and even AC-coupling in some cases. Consult with the receiver specifications to determine if any or all of the following indicated external components are needed.

4.4.1 Direct-Coupled HCSL Termination

For HCSL differential protocol, the following termination scheme is recommended (see Figure 7). A typical HCSL design uses a 50Ω resistor to ground at the receiver. The RC22514A supports source termination (see Figure 7), with an internal 50Ω resistor to ground at the transmitter. This is enabled by setting ODRV_MODE_CNFG Register.out_hcsl_term_en.

For alternate termination schemes, see HCSL Terminations in *Quick Guide - Output Terminations (AN-953)* located on the RC22514A product page, or contact Renesas for support.

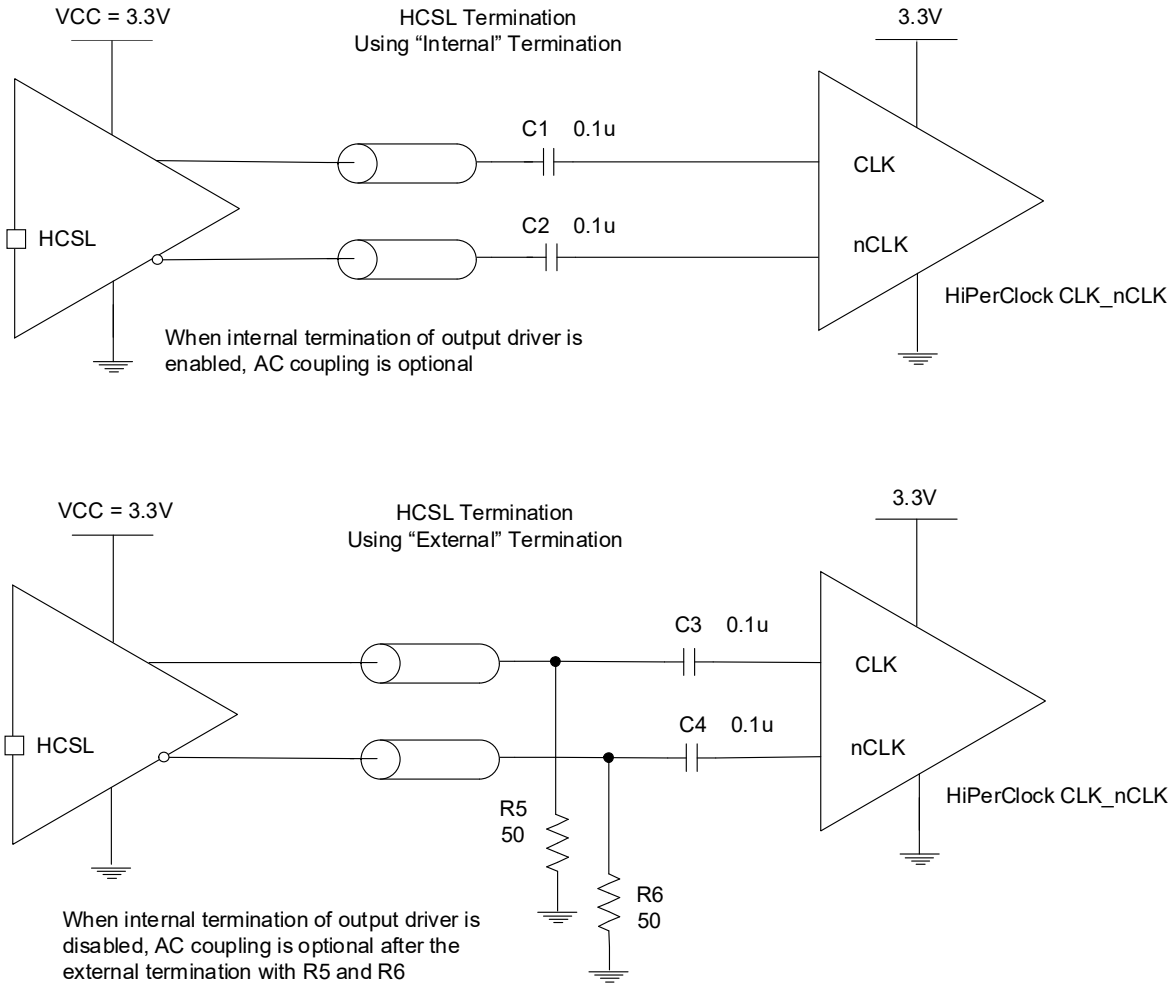


Figure 7. Standard HCSL Termination

4.4.2 Direct-Coupled LVDS Termination

For LVDS differential protocol, the following termination scheme is recommended (see Figure 8). The recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. To avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

For alternate termination schemes, see LVDS Terminations in *Quick Guide - Output Terminations (AN-953)* located on the RC22514A product page, or contact Renesas for support.

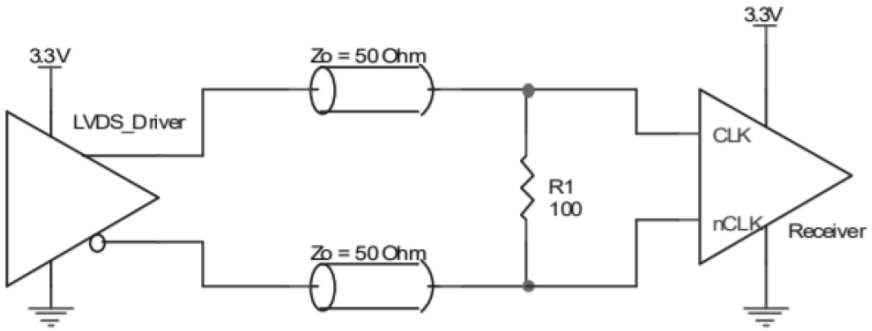


Figure 8. Standard LVDS Termination

4.4.3 AC-Coupled Differential Termination

For any other type of differential protocol, AC-coupling should be used as shown in Figure 9, which assumes a 100Ω differential transmission-line environment. The RC22514A should be programmed in HCSL mode when using AC-coupling, with an appropriate voltage swing selection for the receiver being driven. The device supports a wide range of programmable voltage swing options.

No terminations are needed between the RC22514A and the AC-coupling capacitors. Select the resistors on the receiver side of the AC-coupling capacitors to provide an appropriate voltage bias for the particular receiver. Consult receiver specifications for details. Finally, a 100Ω resistor across the differential pair, located near the receiver attenuates or prevents reflections that may corrupt the clock signal integrity.

It may also be useful to consult *Quick Guide - Output Terminations (AN-953)* located on the RC22514A product page, or contact Renesas for support.

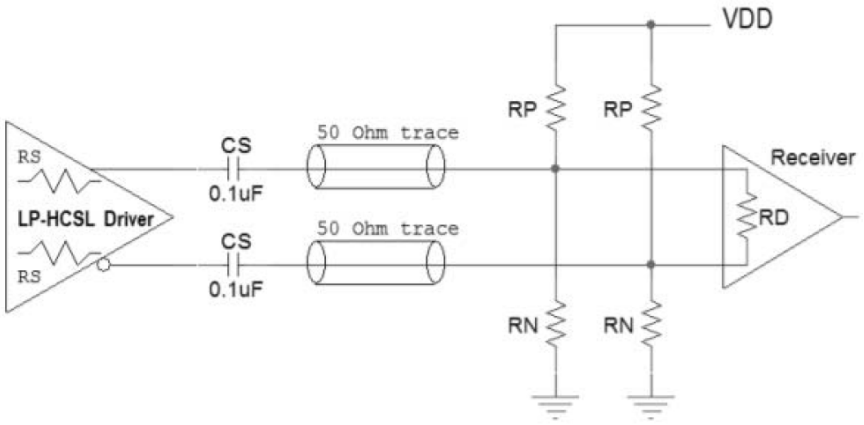


Figure 9. AC-Coupling Termination

5. Architecture

The RC22514A detailed block diagram is shown in Figure 10. Blocks are described in the following chapter. The crystal shown is internal to the package and so the ability to over-drive it is not supported in RC22514A.

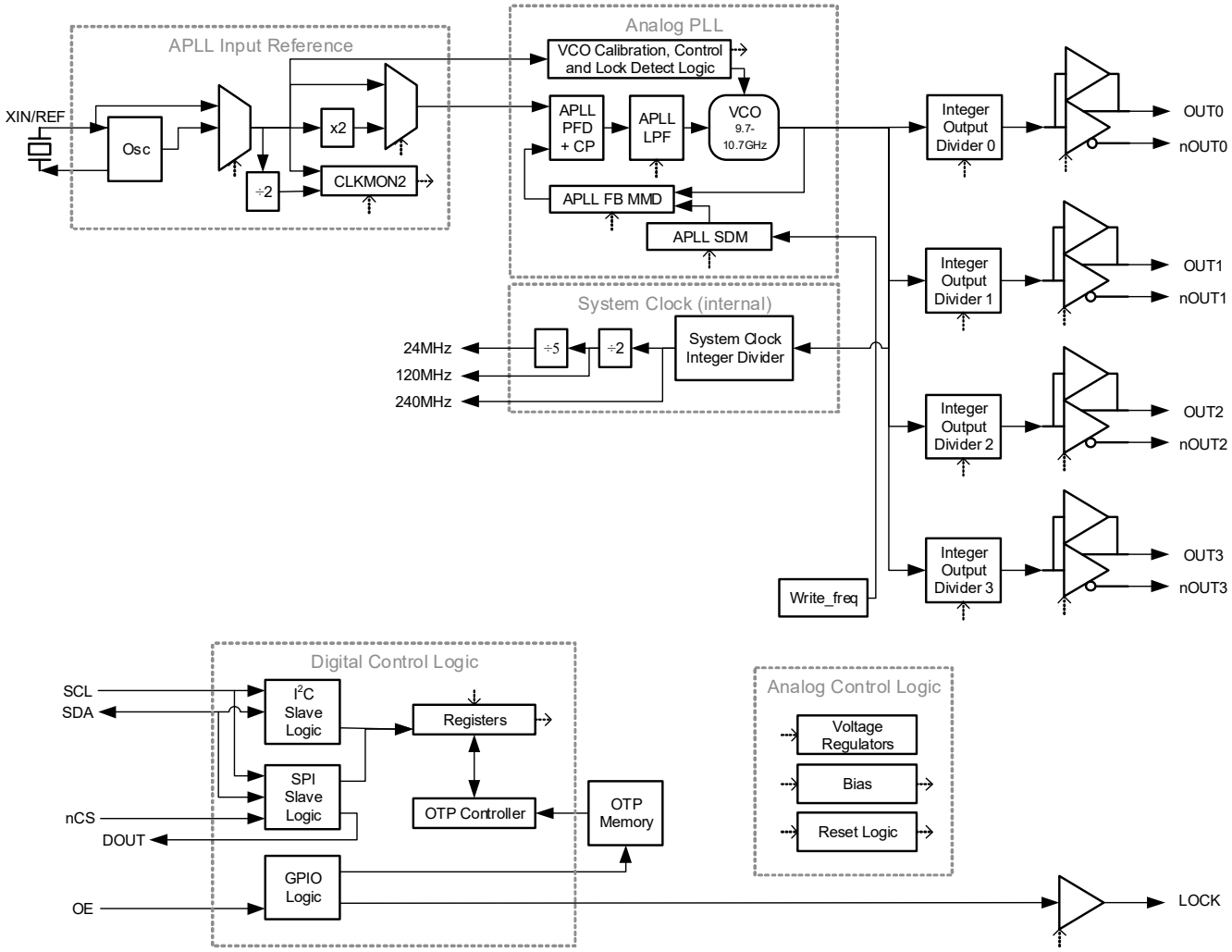


Figure 10. Detailed Block Diagram

5.1 Modes of Operation

5.1.1 Frequency Synthesizer/Digitally Controlled Oscillator (DCO)

When operating as a frequency synthesizer or DCO, the device receives its clock input from a crystal in the same package as the RC22514A die. The clock is multiplied-up internally to a high frequency using a fractional-feedback Analog PLL (APLL) that can generate a wide range of frequencies that are unrelated to the crystal frequency. The APLL frequency in turn is used by integer output dividers to generate several output frequencies that are related to each other, but unrelated to the crystal frequency.

In DCO mode, a frequency control word is passed directly from an external processor or FPGA to the fractional APLL. The frequency control word (specifying ppm offset) is written to the write_freq register. This value is scaled according to the APLL feedback divide ratio and then applied to the feedback divider.

A fixed frequency offset can be programmed to compensate for the initial frequency offset of the crystal, if known. This can be programmed in the OTP configuration during final test.

In these modes, the reference clock inputs are unused.

6. Blocks

6.1 Device Reset Logic

The Reset Logic holds all internal logic in reset from the initial ramping of the power supply pins until the on-chip voltage regulators have stabilized. After that it controls the sequence of bringing the individual logic blocks out of reset. For information, see Power-up Sequence.

6.1.1 Bias Calibration

The bias circuits provide precision reference voltages needed by other internal circuits. During the Power-up Sequence these undergo a calibration process. Completion of the calibration process sets bias_cal_done. If in the unlikely event there is an issue, it sets bias_cal_fail, and the startup sequence continues. You can read these bits using the serial port to confirm that the bias calibration succeeded. If bias calibration fails, contact Renesas for assistance.

6.2 Crystal Oscillator

The crystal oscillator (XO) supports a fundamental-mode parallel-resonant crystal that is integrated into the package.

6.3 Analog Phase Lock Loop

The Analog Phase Lock Loop (APLL) consists of a frequency doubler, a Phase-Frequency Detector (PFD), a Loop Filter (LPF), a Voltage-Controlled Oscillator (VCO), and a feedback divider. Renesas recommends using Renesas' Timing Commander software to provide optimized register setting recommendations for the APLL.

6.3.1 Frequency Doubler

The reference clock frequency is doubled using the frequency doubler before entering into the PFD, enabled by the en_doubler register bit.

6.3.2 APLL Loop Filter (LPF)

The LPF is a lead-lag filter with the topology shown in Figure 11. This circuit accepts the current from the PFD/CP circuit and provides the filtered control voltage to adjust the frequency of the VCO.

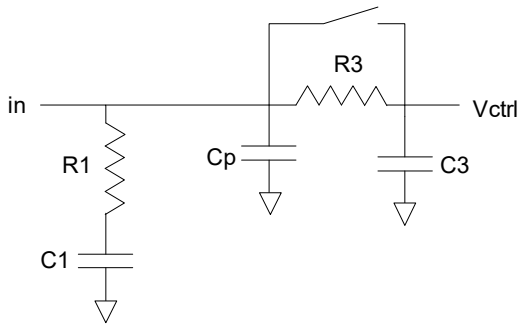


Figure 11. APLL LPF Topology

C1 has a fixed nominal capacitance of 1100 pF. The values of R1, Cp, R3, and C3 can be adjusted using the cnf_LPF_res, cnf_LPF_cp, cnf_LPF_R3, and cnf_LPF_C3 register fields, respectively. The switch bypassing the third pole is controlled by byp_p3, and can be enabled only when the APLL feedback divider is set to an integer value. All loop filter components are internal to the device.

The default effective bandwidth (BW) of the APLL is 365kHz.

6.3.3 Voltage-Controlled Oscillator (VCO)

The VCO is a quad-core LC VCO with a tunable frequency range of 9.7GHz to 10.7GHz across PVT. There is temperature compensation to allow the VCO frequency to remain stable across the operating temperature range regardless of the temperature at which calibration was performed.

6.3.4 APLL Feedback Divider

The APLL Feedback divider consists of two parts. The Multi-Modulus Divider (MMD) performs the actual division of the VCO frequency down to the nominal frequency needed to match the PFD input reference frequency (from frequency doubler). The MMD contains a number of integer divide ratios that are switched between under control of the Sigma-Delta Modulator (SDM) block. This allows a fractional divide ratio to be achieved while also providing noise shaping to minimize the spurs that switching would otherwise cause. The divide ratio is configured using the apll_fb_div_frac and apll_fb_div_int register fields.The fractional portion of the divide ratio is a 27-bit integer representing the numerator of an M/N fraction. The denominator is fixed at 2^{27}. It is recommended that fractions close to 0, 1, or 1/2 be avoided for best phase noise performance.

6.3.5 APLL Lock Detector

The analog lock detector indicates whether the APLL is locked to a input reference. The current lock status can be read in the apll_lock_sts register bit or reflected on one of the general purpose output pins (see GPIOs). The falling edge of the lock status sets the apll_lol event bit. This bit remains set until cleared by the user.

The lck_detect_ref_sel register field must be programmed according to the input reference frequency range.

6.3.6 Direct DCO Control

When the APLL is in Synthesizer mode, a frequency offset can be programmed using the write_freq register field. The frequency adjustment's LSB resolution is 2^{-40}, which translates to approximately 0.91ppt. An offset to compensate for the initial frequency offset of the internal crystal is pre-programmed by Renesas at the factory in xtal_trim.

6.4 Reference Clock Outputs

6.4.1 Integer Output Divider (IOD)

There are four independent integer output dividers (IOD0/1/2/3), corresponding to the four differential output clocks, which divide the VCO frequency to the desired output frequency. The integer divide ratio is programmed in the outdiv_ratio register field.

When operating in differential mode, the output clocks support a continuous frequency range from 1MHz to 1000MHz. When operating in LVCMOS mode, the output clocks support a continuous frequency range from 1MHz to 180MHz.

The output clock disable (from the OE pin or out_dis; for details, see Clock Output Driver) acts synchronously to avoid glitches or runt pulses when disabling or enabling the output.

The maximum skew between any outputs configured for the same output type is shown in Table 10. This is achieved by:

- The output dividers are automatically synchronized after the PLL is configured on startup, and can be manually synchronized by writing the divider_sync register bit following reconfiguration. The output clocks are interrupted for 50µs to 300µs during synchronization, depending on the APLL re-lock time. On power-up, this interruption is hidden because the output drivers are not enabled until after it is complete. However on a manual synchronization command, this interruption is visible if the outputs are enabled.
- The delay in the clock fanout from the VCO to each divider is balanced to minimize output-output skew.

6.4.2 Clock Output Driver

There are four independent differential clock output drivers supporting receiver-only termination schemes using termination values of 100Ω across OUTx and nOUTx. The output type (HCSL, LVDS, or LVCMOS) is selected by

the out_mode register field. The output swing level is selected by the out_cnf_hcsl_swing or out_cnf_lvds_amp register field depending on the output type. In HCSL mode, internal termination of 50Ω resistor to ground on both of OUTx and nOUTx can be enabled as configured by out_hcsl_term_en. In CMOS mode, one or both of OUTx and nOUTx can be active as configured by out_cmos_mode.

When output x is disabled, OUTx and nOUTx are held low by default. The disabled state can be set to low/high or tristate by setting the out_dis_state register field. When output x is enabled, OUTx and nOUTx operate normally.

If a clock output is unused, the corresponding out_pd register bit can be set to 1 to power down the output driver logic and tristate the outputs. While powered down, the output cannot be enabled and its output enable is ignored. If a clock output is never used, it can be powered down and the corresponding V_{DDOx} pin can be left unconnected.

6.4.3 Output Enable Control

During the Power-up Sequence, the clock output drivers are powered down (OUTx and nOUTx are tri-stated) until the power supplies have stabilized. Then the output drivers are powered up in the default disabled state (OUTx and nOUTx are both held low).

After the OTP configuration load completes, the clock output drivers can be held disabled until the APLL locks according to the out_startup setting:

- Clock output drivers are disabled until APLL lock asserts
- Clock output drivers are enabled immediately

The APLL lock status no longer affects the clock output drivers, regardless of the out_startup setting.

After startup, the clock output drivers are then user-controllable using output enable control. When the oe_sel register bit is set to 1, each clock's output can be independently disabled by setting the corresponding out_dis register bit to 1, and enabled by setting out_dis to 0. When the oe_sel register bit is set to 0, de-assertion of the OE input pin disables all powered-up clock output drivers. Assertion of OE enables the powered-up clock output drivers that are not disabled by their corresponding out_dis register bits. For more information on polarity and pull-up/pull-down control, see Output Enable.

6.5 Reference Monitors

There is one reference monitor core for each reference. The monitor core consists of a short-term (Loss Of Signal) monitor.

- The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least 8 times that of the measuring clock period. The measuring clock period for the LOS monitor is the system clock.

There are short-term clock monitors on the crystal clock input (LOSMON2). The implementation structure of the monitors are the same but with different configuration settings.

The LOS monitors nominal value should be programmed as follows:

- LOS monitor – sys_clk_2x / ref clock, where ref clock should be at least 8x less than sys_clk_2x for best results.

6.5.1 Comparator

All monitors have both reject and accept threshold values that are all programmable in CSRs (los_nom_num, los_acc_margin, los_rej_margin). The nominal value is compared with the nominal value +/- accept_margin or reject_margin.

When the counter value exceeds the reject threshold, the internal "failure counter" increments, and the internal "good counter" value resets it to 0. When the counter value is within the accept threshold, the "failure counter" resets to 0 and the "good counter" increments.

When the "good counter" reaches los_good_times for the LOS monitor, or the value of 1 for the Activity monitor, the monitor's status (los_sts) get cleared, indicating a valid reference.

When the “failure counter” reaches los_fail_times for the LOS monitor, or the value of 1 for the Activity monitor, the monitor’s status (los_sts) get set, indicating an out-of-spec reference.

6.5.2 Alarm and Interrupt

The combinational OR of the LOS monitor’s los_sts are used to qualify/disqualify the reference, unless masked by los_fail_mask bits.

When the status (los_sts) changes from valid to invalid, the corresponding los_evt bit gets set and can be cleared only by a CSR write, unless the underlying failing condition is still there, in which case the write does not take effect.

6.6 OTP

The RC22514A supports four user-definable, non-volatile start-up configurations stored in an internal OTP (one-time programmable) memory. Each configuration is capable of storing values for all write-able configuration registers. The configuration is selected by the values of the Configuration Select Pins latched at power-up. The serial interfaces are inactive until all register values specified in the selected configuration are written.

6.7 Serial Interfaces

I2C or SPI operation is selected by the ssi_enable register field which defaults to I2C mode. The serial interfaces are inactive until the OTP load completes during the power-up sequence.

6.7.1 Paging

You can choose to operate the serial port providing the full offset address within each burst, or to operate in a paged mode where part of the address offset is provided in each transaction and another part comes from an internal page register in each serial port. Figure 12 shows how page register and offset bytes from each serial transaction interact to address a register within the RC22514A.

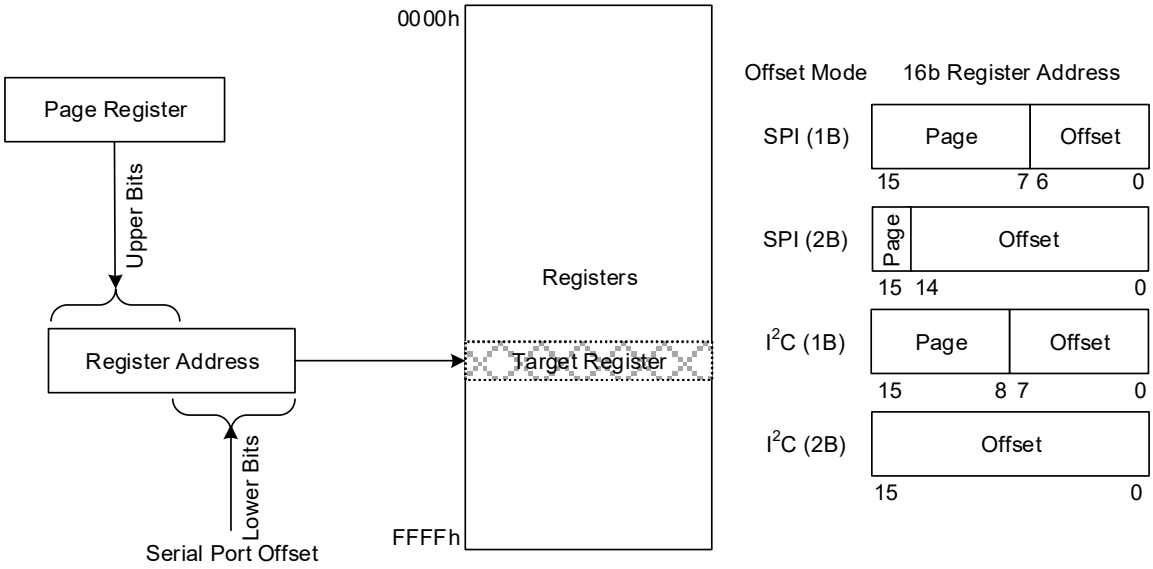


Figure 12. Register Addressing Modes Using Serial Port

6.7.2 I2C Slave

The I2C slave protocol of the RC22514A complies with the I2C specification, version UM10204 Rev.6 – 4 April 2014. In the following description, SCL refers to the SCL_SCLK pin and SDA refers to the SDA_SDI(O) pin.

Figure 13 shows the sequence of states on the I2C SDA signal for the supported modes of operation.

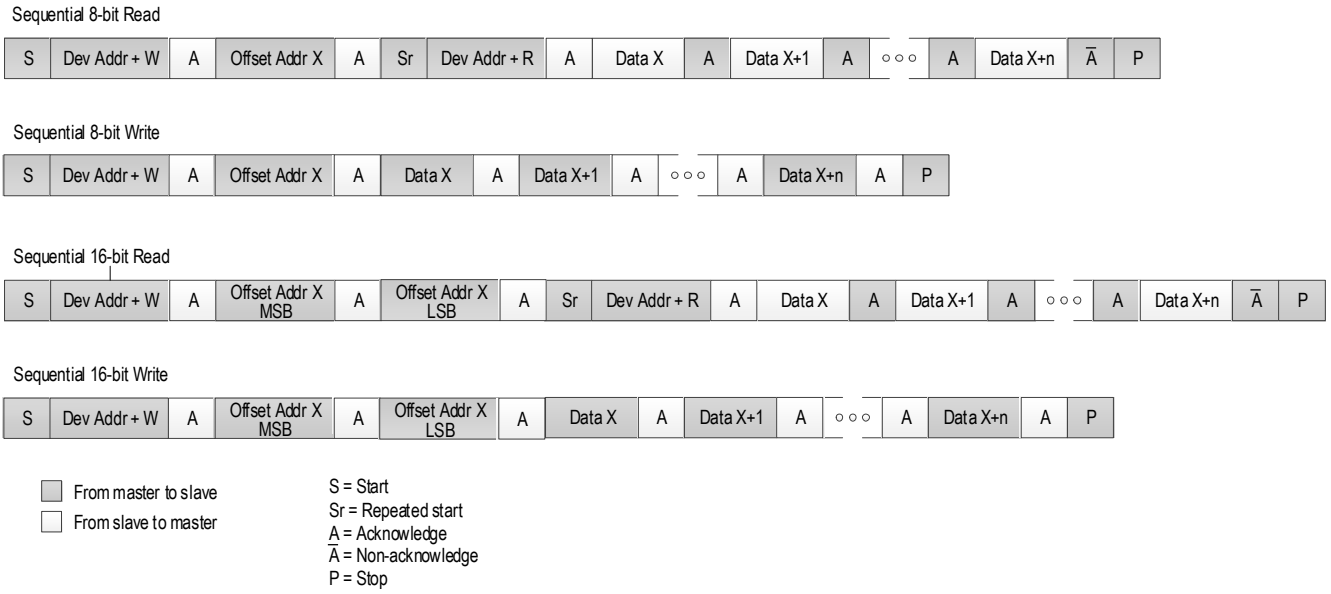


Figure 13. I²C Slave Sequencing

The Dev Addr shown in the figure represents the I²C bus address that the device responds to. This 7-bit value in the i2c_addr register field defaults to 0x09 if not programmed using the OTP load, or controlled through pins, as per Table 21.

The selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be configured using the ssi_addr_size register field. These offsets are used in conjunction with the page register to access registers internal to the device (see Figure 12). Because the I²C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8 bits of the register offset address come from the Offset Addr byte and the upper 8 bits come from the page register. The page register can be accessed at any time using an offset byte value of 0xFC. This 4-byte register must be written in a single-burst write transaction.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes.

Note: I²C burst mode operation is recommended to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I²C burst access. Bursts can be of greater length if required but must not extend beyond the end of the register page (Offset Addr 0xFF in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

Figure 3 and Table 14 show the detailed timing on the interface. 100kHz (Standard mode), 400kHz (Fast mode), and 1MHz (Fast mode Plus) operation are supported. The output slew rate is set according to the speed selected by the i2c_speed register field.

The I²C interface operating at 1MHz supports a DCO update rate of approximately 16k updates per second.

6.7.2.1 I2C 1-byte (1B) Addressing Example

RC22514A I²C 7-bit I²C address is 0x09 with LSB = R/W

Example write 0x8003 to register 0x20:

```
12* FC 00 00 00 00      #Set Page Register, *I2C Address is left-shifted one bit.
12 20 03 80             #Write data 0x8003 to 0x20
```

Example read from register 0x168

```
12* FC 00 01 00 00      #Set Page Register, *I2C Address is left-shifted one bit.
12 68                   #Set I2C pointer to 0x168, I2C instruction should use "No Stop".
13 <read back data>     #Send address with Read bit set.
```

6.7.2.2 I2C 2-byte (2B) Addressing Example

RC22514A I^2C 7-bit I^2C address is 0x09 with LSB = R/W

Example write 0x8003 to register 0x20:

```
12 00 20 03 80          #Write data 0x8003 to 0x0020
```

Example read from register 0x168:

```
12 01 68                #Set I2C pointer to 0x0168, * I2C instruction should use "No Stop".
13 <read back data>     #Send address with Read bit set.
```

6.7.3 SPI Slave

In the following description, nCS refers to the nCS pin, SCLK refers to the SCL_SCLK pin, SDI SDIO refer to the SDA_SDI(O) pin, and SDO refers to the SDO pin.

The RC22514A supports 4-wire or 3-wire SPI operation as a selectable protocol on the serial port. The 3-wire or 4-wire mode is selected by the spi_3wire register bit. In 4-wire mode, there are separate data in (to the RC22514A) and data out signals (SDI and SDO respectively). In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal.

When reading, a configurable number of dummy bytes can be read before the requested data byte(s) as controlled by the spi_dummy_en and spi_dummy_size register fields. When the SPI clock is faster than the system clock frequency divided by 4, at least 1 dummy byte must be enabled. Writes do not use dummy bytes.

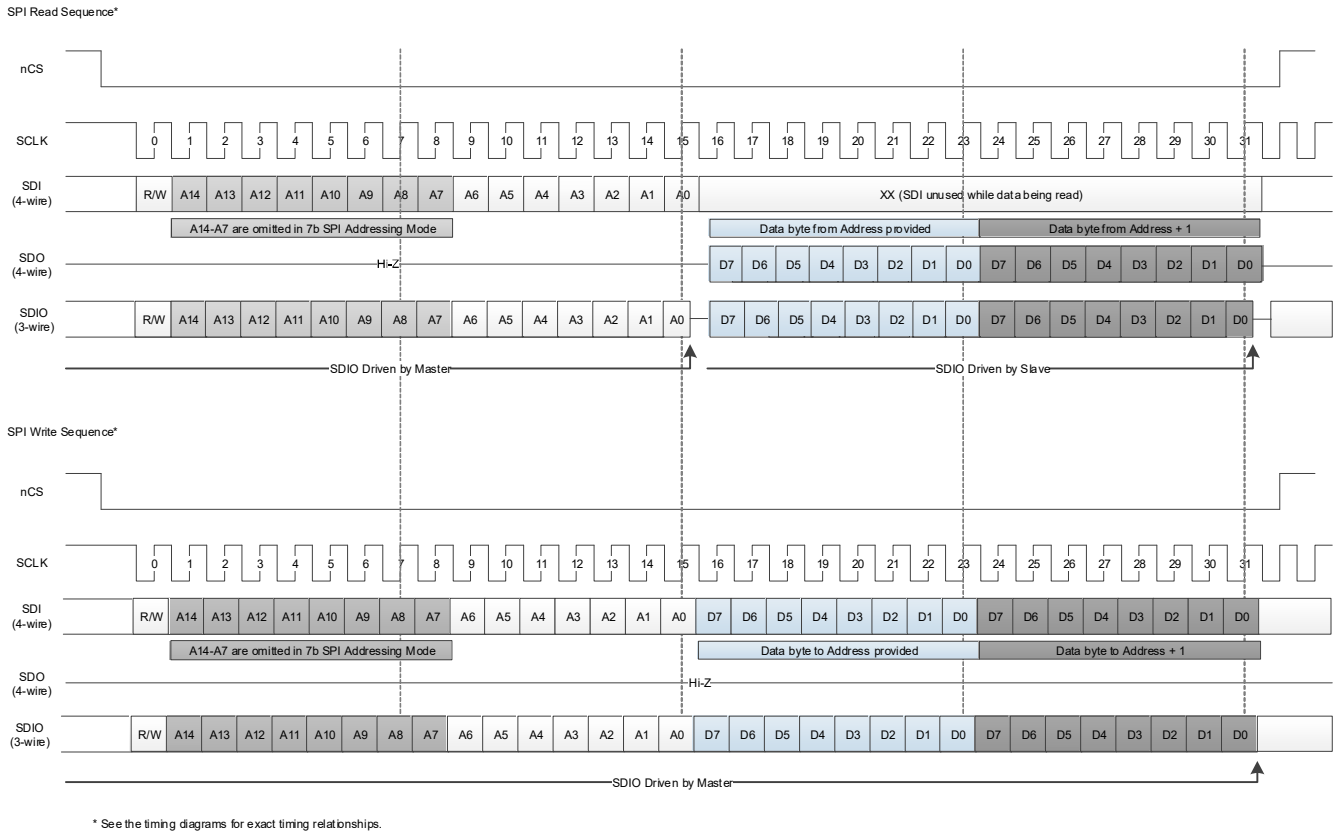


Figure 14. SPI Sequencing

Figure 14 shows the sequencing of address and data on the serial port in both 3-wire and 4-wire SPI mode.4-wire SPI mode is the default. The R/W bit is high for read cycles and low for write cycles. The read sequence is shown without dummy bytes (spi_dummy_en set to 0). If 1 dummy byte were enabled, then the data bits labeled Data byte from Address provided would be zero, the data bits labeled Data byte from Address + 1 would become Data byte from Address provided, and they would be followed by another 8 bits containing Data byte from Address + 1.

SPI operation can be configured for the following settings through register fields:

- 1-byte (1B) or 2-byte (2B) offset addressing (ssi_addr_size) (see Figure 12)
- In 1B operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed using an Offset Address of 0x7C with a 4-byte burst access.
- In 2B operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and the upper 1-bit is fixed to b'0.
- Data sampling on falling or rising edge of SCLK (spi_clk_sel)
- Output (read) data positioning relative to active SCLK edge (spi_del_out)

Note: SPI burst mode operation is recommended to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts can be of greater length if desired but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

SPI timing is shown in Figure 4 and Table 16.

The SPI interface operating at 20MHz supports a DCO update rate of approximately 400k updates per second.

6.7.3.1 SPI 1-byte (1B) Addressing Example

Example write "50" to register 0xE4:

```
7C 80 00 00 00          #Set Page register
64* 50                  #*MSB is 0 for write transactions
```

Example read from 0x24:

```
7C 00 00 00 00          #Set Page register
A4* 00                  #*MSB is set, so this is a read command
```

6.7.3.2 SPI 2-byte (2B) Addressing Example

Example write "50" to register 0x124

```
01* 24 50               #*MSB is 0 for write transactions
```

Example read from 0xE4:

```
80* E4 00               #*MSB is set, so this is a read command
```

6.8 GPIOs

6.8.1 Lock Status

The LOCK output pin reflects one of these conditions as selected by the lock_sel register field:

- APLL lock
- Reference #0 loss-of-signal
- Crystal loss-of-signal
- Reference #0 activity monitor status
- Reference #0 ref_invalid status
- Device Interrupt (Refer to the device_int_sts register bit)
- Device ready (OTP load is complete and the serial port is active)
- Logic low
- Logic high

The polarity of LOCK is controlled by the lock_pol register bit. Internal pull-up resistors can be enabled by setting the lock_pu and the and pull-down resistors by enabling the lock_pd register bits. The output can be tri-stated by setting the lock_hiz register bit. LOCK can be configured as an open-drain output by setting the lock_od register bit.

The LOCK output driver is disabled until the OTP configuration load completes, allowing it to function as one of the Configuration Select Pins.

6.8.2 Serial Data Out

When the serial port is configured for SPI 4-wire mode, the SDO pin is the data out. When the serial port is configured for either I^2C mode or SPI 3-wire mode, the SDO pin reflects one of the following conditions as selected by the sdo_sel register field:

- APLL lock
- Reference #0 loss-of-signal
- Crystal loss-of-signal
- Reference #0 activity monitor status
- Reference #0 ref_invalid status
- Device Interrupt (Refer to the device_int_sts register bit)
- Device ready (OTP load is complete and the serial port is active)
- Logic low
- Logic high

The polarity of SDO is controlled by the sdo_pol register bit. Internal pull-up resistors can be enabled by setting the sdo_pu register bits and the pull-down resistors can be enabled by setting the sdo_pd register bits. The output can be tri-stated by setting the sdo_hiz register bit. SDO can be configured as an open-drain output by setting the sdo_od register bit.

In SPI 4-wire mode, the sdo_pol, sdo_pu, sdo_pd, sdo_hiz, and sdo_od register bits must be set to 0 (the default reset value).

The SDO output driver is disabled until the OTP configuration load completes, allowing it to function as one of the Configuration Select Pins.

6.8.3 Output Enable

After the clock output drivers become user controllable during the startup sequence, the OE input pin controls the output enable of the output drivers if appropriately configured (for details, see Output Enable Control).

The polarity of the OE input is controlled by the oe_pol register bit. Internal pull-up resistors can be enabled by setting the oe_pu register bits and the pull-down resistors can be enabled by setting the oe_pd register bits.

The OE input also can function as one of the Configuration Select Pins.

6.9 Power-up Sequence

There are no power-up/down sequencing requirements on the power supply pins, or between the power supply pins and input signals. There are no external reset sequencing requirements.

After VCO calibration, the output dividers and APLL feedback divider are synchronized. The VCO output clock is gated, the divider resets are de-asserted, and the VCO output clock is ungated. Each divider outputs a rising edge on the first cycle of the VCO clock.

After the APLL locks (generally within 200us), the reference clock monitors are enabled.

In synthesizer/DCO mode, the enabled output drivers are set to normal operation and the output clocks begin to toggle. The power-up sequence is complete.

Setting the divider_sync register bit triggers the divider synchronization sequence and waits for the APLL to relock. The output drivers are disabled during this time.

Setting the apll_reinit bit restarts the power-up sequence from the VCO calibration step. The output drivers are disabled and are re-enabled after the APLL locks as in the regular power-up sequence.

6.9.1 Configuration Select Pins

When the power-on-reset de-assets, the logic level of the following pins are latched into the gpio_at_startup register field:

- LOCK
- OE
- SDA_SDI(O)
- SDO
- nCS

A 2-bit index of the OTP user configuration is selected according to the config_sel register field (this field is intended to be written in the OTP Common Configuration), which determines the OTP user configuration to use. The config_sel register also determines how the lower two bits of the I²C address (according to the i2c_addr register field) are selected, if applicable.

Table 21. OTP and I²C Address User Configuration Selection

config_sel[3:0]	Configuration Index [1]	Configuration Index [0]	I²C Address [1]	I²C Address [0]
0x0	0	0	i2c_addr[1]	i2c_addr[0]
0x1	0	1	i2c_addr[1]	i2c_addr[0]
0x2	1	0	i2c_addr[1]	i2c_addr[0]
0x3	1	1	i2c_addr[1]	i2c_addr[0]
0x4 (default)	OE	LOCK	nCS	SDO
0x5	SDO	LOCK	nCS	OE
0x6	SDO	OE	nCS	LOCK
0x7	SDA_SDI(O)	SCL_SCLK	i2c_addr[1]	i2c_addr[0]
0x8	nCS	LOCK	SDO	OE
0x9	nCS	OE	SDO	LOCK
0xA	nCS	SDO	OE	LOCK
0xB	nCS	SDA_SDI(O)	SDO	LOCK
0xC	nCS	SCL_SCLK	OE	SDA_SDI(O)
0xD	nCS	SDA_SDI(O)	OE	SCL_SCLK
0xE	SDA_SDI(O)	LOCK	OE	nCS
0xF	SDA_SDI(O)	SDO	OE	LOCK

The LOCK, SDA_SDI(O), SDO, nCS, and OE levels at power-up can be selected by connecting pull-up or pull-down resistors on the board. When I²C mode is selected, SCL_SCLK and SDA_SDI(O) must have a pull-up resistor and should not be used for OTP configuration or I²C address selection.

If only two pin selectable user configurations are required, any one of the five inputs can be used as the select by programming two pairs of user configurations to use the same blocks, such that the value of the uncontrolled input pin is irrelevant. For example, to use only the LOCK pin, config_sel can be set to 0x8 with user configurations 0 and 2 programmed equivalently and user configurations 1 and 3 programmed equivalently.

6.9.2 Divider Synchronization

The output dividers must be synchronized with each other to align the output clocks to the common multiple of their divide ratios. If the APLL reference is the crystal, synchronizing the APLL feedback divider is not necessary but causes the APLL to lose lock and re-lock.

6.9.2.1 Divider Synchronization Procedure

The Divider Sync Procedure is illustrated in Figure 15.

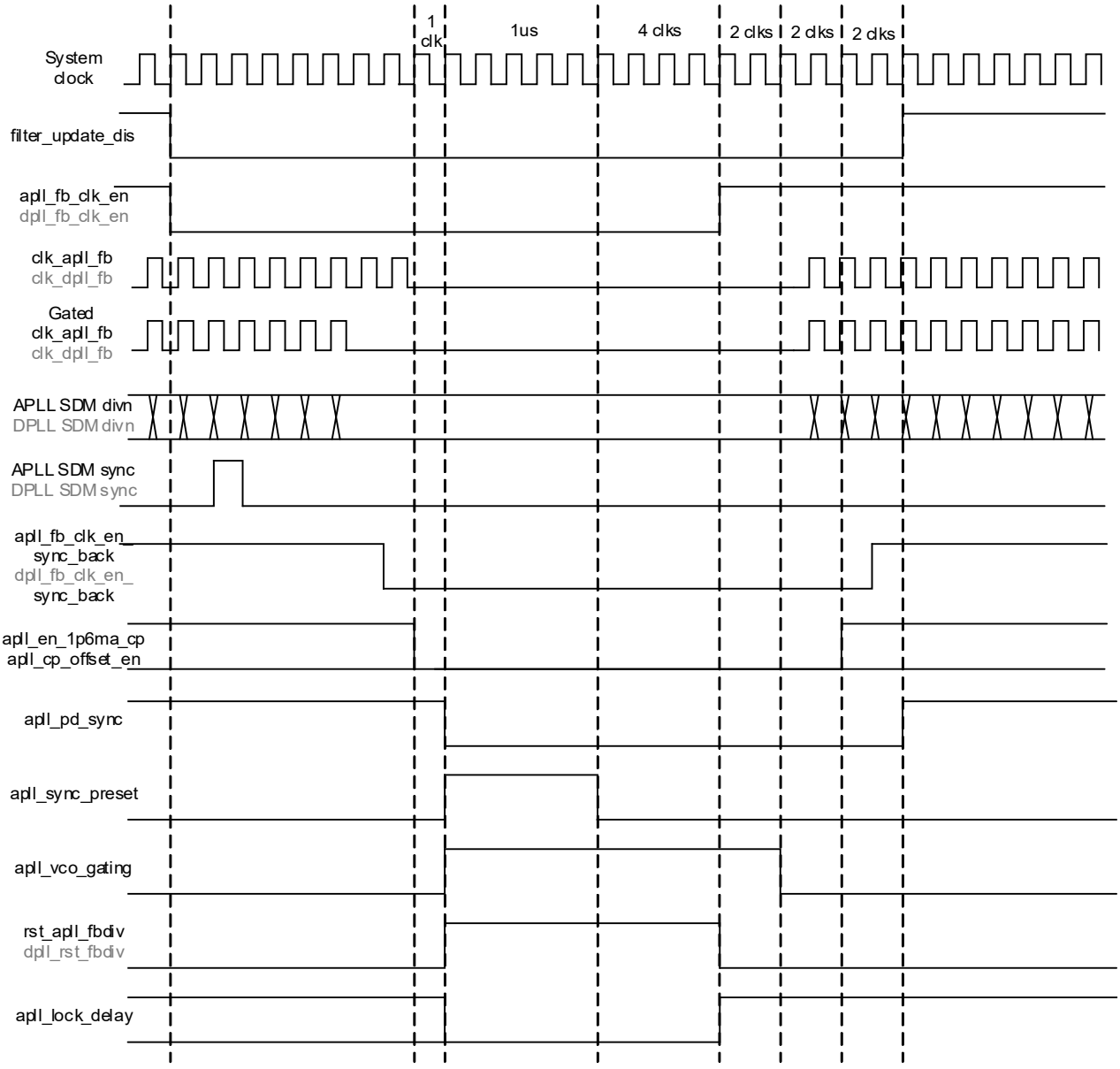


Figure 15. Divider Synchronization Procedure

6.9.3 Maximum PLL Lock Times

When operating in clock synthesizer mode, the maximum start-up and APLL lock time is 10ms. This is measured from the last voltage rail achieving nominal limits to the output clock being stable (no locking transients, no clock interruptions).

7. Register Organization

7.1 Register Block Offsets

Table 22. Register Block Offset

Block Offsets	Block Name	Register Block Address Table Links	Register Block Description
0x00	GLOBAL	Global Block Register Offsets	GLOBAL Registers
0x20	INT	Interrupt Block Register Offsets	INT Registers
0x30	Rsvd	Reserved	-
0x40	Rsvd	Reserved	-
0x50	LOSMON[2]	LOS Monitor Block Register Offsets	LOSMON Registers[1]
0x60	Rsvd	Reserved	-
0x80	Rsvd	Reserved	-
0xA0	MISC	MISC Block Register Offsets	-
0xE0	Rsvd	Reserved	-
0xF0	SYSDIV	System Clock Divider Block Register Offsets	SYSDIV Registers
0xF4	BIAS	Bias Block Register Offsets	BIAS Registers
0xF8	XO	Crystal Block Register Offsets	XO Registers
0x100	OUT[0]	Clock Output Block Register Offsets	OUT Registers
0x108	OUT[1]	Clock Output Block Register Offsets	OUT Registers[1]
0x110	OUT[2]	Clock Output Block Register Offsets	OUT Registers[1]
0x118	OUT[3]	Clock Output Block Register Offsets	OUT Registers[1]
0x120	REF[0]	Clock Reference Addresses	REF Registers
0x124	Rsvd	Reserved	-
0x130	GPIO	GPIO Block Register Offsets	GPIO Registers
0x140	SSI	SSI Block Register Offsets	SSI Registers
0x150	APLL	APLL Block Register Offsets	APLL Registers
0x190	INP	Clock Input Block Register Offsets	INP Registers
0x1D0	Rsvd	Reserved	-

[1] Register block functionality is the same, so the description is not duplicated.

7.2 Register Block Address Maps

7.2.1 Global Register Block Address Map

The Global Register block has a base address of 0x00. The addresses shown in Table 23 are offsets starting from this base address.

Table 23. Global Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	VENDOR_ID Register	Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.
0x02	hword	DEVICE_ID Register	Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.
0x04	hword	DEVICE_REV Register	Device revision identification information. Address map for this block of registers: Global Block Register Offsets.
0x06	hword	DEVICE_PGM Register	Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.
0x08	byte	DEVICE_CNFG Register	Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.
0x0A	byte	DEV_RESET Register	Device reset commands. Address map for this block of registers: Global Block Register Offsets.
0x0C	hword	SW_RESET Register	Software reset command. Address map for this block of registers: Global Block Register Offsets.
0x0E	hword	CLOCK_GATE Register	Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas if further details are needed.
0x10	byte	DEVICE_STS Register	Device status. Address map for this block of registers: Global Block Register Offsets.

7.2.2 Interrupt Register Block Address Map

The Interrupt block has a base address of 0x20. The addresses shown below are offsets starting from this base address.

Table 24. Interrupt Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	INT_EN Register	Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.
0x02	hword	INT_STS Register	Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

7.2.3 Loss of Signal Monitor Register Block Address Map

The LOS Monitor 2 block has a base address of 0x50. The addresses shown below are offsets starting from this base address. Note that before reprogramming a Loss of Signal Monitor block, the corresponding losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

Table 25. LOS Monitor Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	LOSMON_STS Register	LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x01	byte	LOSMON_EVENT Register	LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x02	byte	LOSMON_QUAL Register	LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x04	hword	LOSMON_WINDOW Register	LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x08	word	LOSMON_THRESH Register	LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x0C	word	LOSMON_NOMINAL Register	LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

7.2.4 MISC Register Block Address Map

The Misc block has a base address of 0xA0. The addresses shown below are offsets starting from this base address.

Table 26. MISC Block Register Offsets

Offset	Size	Register Name	Register Description
0x00~2		Reserved	Reserved
0x03	byte	MISC_TRIM_OFFSET Register	Crystal trim offset. Address map for this block of registers: MISC Block Register Offsets.
0x04~27		Reserved	Reserved
0x28	word	MISC_WRITE_FREQ Register	Write Frequency command. Address map for this block of registers: MISC Block Register Offsets.

7.2.5 System Clock Divider Register Block Address Map

The System Clock Divider block has a base address of 0xF0. The addresses shown below are offsets starting from this base address.

Table 27. System Clock Divider Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SYS_DIV_INT Register	System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

7.2.6 Bias Register Block Address Map

The Bias block has a base address of 0xF4. The addresses shown below are offsets starting from this base address.

Table 28. Bias Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	Reserved	Reserved
0x02	hword	BIAS_STS Register	Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

7.2.7 Crystal Register Block Address Map

The Crystal block has a base address of 0xF8. The addresses shown below are offsets starting from this base address.

Table 29. Crystal Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	XO_CNFG Register	Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets. For information on how to set up this interface, see Differential Output Termination.

7.2.8 Clock Output Register Block Address Map

The Clock Output 0 block has a base address of 0x100.
The Clock Output 1 block has a base address of 0x108.
The Clock Output 2 block has a base address of 0x110.
The Clock Output 3 block has a base address of 0x118.
The addresses shown below are offsets starting from this base address.

Table 30. Clock Output Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	OD_CNFG Register	Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.
0x02	byte	ODRV_EN Register	Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.
0x03	byte	ODRV_MODE_CNFG Register	Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.
0x04	byte	ODRV_AMP_CNFG Register	Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

7.2.9 Clock Reference Register Block Address Map

The Clock Reference Register block has a base address of 0x120. The addresses shown below are offsets starting from this base address

Table 31. Clock Reference Addresses

Offset	Size	Register Name	Register Description
0x00	word	PREDIV_CNFG Register	Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

7.2.10 GPIO Register Block Address Map

The GPIO Register block has a base address of 0x130. The addresses shown below are offsets starting from this base address.

Table 32. GPIO Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	OE_CNFG Register	Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.
0x01	byte	IO_CNFG Register	Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.
0x02	hword	LOCK_CNFG Register	Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.
0x04	hword	SDO_CNFG Register	SDO pin configuration control. Address map for this block of registers: GPIO Block Register Offsets.
0x06	byte	Reserved	Reserved
0x07	byte	STARTUP_STS Register	Start-up status. Address map for this block of registers: GPIO Block Register Offsets.
0x08	byte	GPIO_STS Register	GPIO status. Address map for this block of registers: GPIO Block Register Offsets.
0x0C	word	SCRATCH0 Register	Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

7.2.11 SSI Register Block Address Map

The SSI Register block has a base address of 0x140. The addresses shown below are offsets starting from this base address.

Table 33. SSI Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SPI_CNFG Register	SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x01	byte	I2C_FLTR_CNFG Register	I^2C mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x02	byte	I2C_TIMING_CNFG Register	I^2C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.
0x03	byte	I2C_ADDR_CNFG Register	I^2C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.
0x04	byte	SSI_GLOBAL_CNFG Register	Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

7.2.12 APLL Register Block Address Map

The Analog PLL block has a base address of 0x150. The addresses shown below are offsets starting from this base address.

Table 34. APLL Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	APLL_FB_DIV_FRAC Register	APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.
0x04	hword	APLL_FB_DIV_INT Register	APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.
0x06	byte	APLL_FB_SDM_CNFG Register	APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.
0x07	byte	APLL_CNFG Register	APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.
0x08	hword	Reserved	Reserved
0x0A	byte	LPF_CNFG Register	APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.
0x0B	byte	LPF_3RD_CNFG Register	APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.
0x0C	byte	Reserved	Reserved
0x0D	byte	Reserved	Reserved
0x0E	byte	Reserved	Reserved
0x0F	byte	Reserved	Reserved
0x10	byte	Reserved	Reserved
0x12	hword	Reserved	Reserved
0x14	hword	APLL_LOCK_CNFG Register	APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.
0x16	byte	APLL_LOCK_THRSH Register	APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.
0x17	byte	VCO_CAL_STS Register	APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.
0x18	byte	APLL_STS Register	APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.
0x19	byte	APLL_EVENT Register	APLL Event status. Address map for this block of registers: APLL Block Register Offsets.
0x1A	byte	APLL_LOL_CNT Register	APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

7.2.13 Clock Input Register Block Address Map

The Clock Input block has a base address of 0x190. The addresses shown below are offsets starting from this base address.

Table 35. Clock Input Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	REF_CLK_IN_CNFG Register	Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

8. Register Descriptions

8.1 GLOBAL Registers

8.1.1 VENDOR_ID Register

Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default	Description
15:12	dev_id_type	RO	0x1	Device ID Block Type. A value of 0x1 indicates that this register is followed by a 16-bit Device ID register, a 16-bit Device Revision register, and a 16-bit Device Programming register.
11	reserved	RO	0x0	reserved.
10:0	vendor_id	RO	0x33	Vendor ID. Renesas JTAG ID.

8.1.2 DEVICE_ID Register

Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	device_id	RW	0x304A	Device ID. For default value refer to the Product Id in Table 42.

8.1.3 DEVICE_REV Register

Device revision identification information. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	Reserved
12:8	font_id	RO	0x2	Font ID. Font ID to distinguish die variants. Decode as follows: • 0x0 = Font 0 (Font 0) • 0x1 = Font 1 (Font 1) • 0x2 = Font 2 (Font 2)
7:4	ana_rev	RO	0x3	Hardware analog revision. Decode as follows: • 0x1 = First revision (TV) • 0x2 = Second revision (RevA) • 0x3 = Third revision (RevB)
3:0	dig_rev	RO	0x2	Hardware digital revision. Decode as follows: • 0x1 = First revision (TV) • 0x2 = Second revision (RevA/B)

8.1.4 DEVICE_PGM Register

Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	dash_code	RW	0x0	Dash code. Decimal value assigned by Renesas to identify the user configuration loaded in OTP at the factory. This field is writeable and is configured from the OTP common configuration programmed at the factory. • 0x0 = No user configurations are programmed at the factory

8.1.5 DEVICE_CNFG Register

Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	digldo_cnf	RW	0x0	Digital LDO voltage select. Selects the digital LDO voltage level. This setting is intended for test purposes only. • 0x0 = 1.25V • 0x1 = 1.32V
6:4	xo_delay	RW	0x0	Crystal Startup Delay. Selects the wait time for the internal crystal oscillator circuit during the startup sequence. The default setting of 1ms should be sufficient for all crystals. This setting is intended for debug purposes only. • 0x0 = 1 ms • 0x1 = 2.5 ms • 0x2 = 5 ms • 0x3 = 7.5 ms • 0x4 = 10 ms • 0x5 = 0.5 ms • 0x6 = 15 ms • 0x7 = reserved
3:0	config_sel	RW	0x4	User Configuration Select. Controls the selection of the user configuration stored in OTP to read on start-up (for details, see OTP and I2C Address User Configuration Selection).

8.1.6 DEV_RESET Register

Device reset commands. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	input_div_global_setb	RW	0x1	Input Dividers Common Set. When cleared, both input dividers get held in set mode (bit is active low). This allows to set and release both dividers at roughly the same time.
4	out_global_oe	RW	0x1	Output Global OE. This bit allows manual CSR control of the output OE.
3:2	reserved	RO	0x0	reserved.
1	divider_sync	RW	0x0	Divider synchronization. Writing this bit to 1 synchronizes the Output Dividers. The output clocks are squelched for approximately 10µs. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.

Bit Field	Field Name	Type	Default Value	Description
0	apll_reinit	RW	0x0	APLL Reinitialization. Writing this bit to 1 restarts the startup sequence from the VCO calibration step, including divider synchronization. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.

8.1.7 SW_RESET Register

Software reset command. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	reserved	RW	0x0	reserved
10:9	reserved	RO	0x0	reserved.
8	bias_cal_sw_rst	RW	0x0	Bias Cal Software reset. The bias calibration logic is held in reset while this bit is set to 1.
7:4	reserved	RO	0x0	reserved.
3	losmon2_sw_rst	RW	0x0	LOSMON2 Software reset. The Loss-of-signal Monitor 2, which monitors the crystal input, is held in reset while this bit is set to 1.
2:1	reserved	RO	0x0	reserved.
0	otp_sw_rst	RW	0x0	OTP Software reset. The OTP logic is held in reset while this bit is set to 1.

8.1.8 CLOCK_GATE Register

Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas if further details are needed.

Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	dig_cg	RW	0x0	Digital Logic Clock Gate. All digital clocks that do not have separate clock gating control bits in this register are gated while this bit is set to 1. Because this gates the register bus clock, no further register access is possible through the serial port. The device must be power cycled to recover. This bit is intended for test purposes only (shut down all digital logic during analog characterization or debug).
10:9	reserved	RO	0x0	reserved.
8	reserved	RW	0x0	reserved
7	reserved	RO	0x0	reserved.
6	reserved	RW	0x0	reserved
5:4	reserved	RO	0x0	reserved.
3	losmon2_cg	RW	0x0	LOSMON2 Clock Gate. The Loss-of-signal Monitor 2 is clock gated while this bit is set to 1.
2:1	reserved	RO	0x0	reserved.
0	reserved	RW	0x0	reserved.

8.1.9 DEVICE_STS Register

Device status. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	startup_seq_sts	RO	0x0	Startup Sequence Status. Status related to the startup sequence. This field is intended for debug purposes only. bit [0] = Bias calibration timeout (2ms) bit [1] = OTP load timeout (10ms) bit [2] = APLL lock timeout (2ms)
4	osc_fallback	RO	0x0	Power-on-Reset Ring Oscillator Fallback. Set to 1 if the system clock divider output does not begin toggling during the startup sequence and the reset controller muxes the ring oscillator clock onto the system clock instead.
3	device_ready	RO	0x0	Device Ready. Set to 1 when the OTP load completes during the startup sequence.
2	reserved	RO	0x0	reserved.
1:0	config_loaded	RO	0x0	User Configuration Loaded. Indicates the user configuration loaded from OTP on start-up. Note that the common configuration is always loaded in addition to any user configurations are loaded.

8.2 INT Registers

8.2.1 INT_EN Register

Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_en	RW	0x0	Device interrupt enable. Overall device interrupt enable. When this field is set to 1, the device interrupt is asserted while device_int_sts is 1.
14:12	reserved	RO	0x0	reserved.
11:9	reserved	RW	0x0	reserved.
8:7	reserved	RO	0x0	reserved.
6	los2_int_en	RW	0x0	XTAL Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los2_int_sts bit contributes to the device interrupt.
5:4	reserved	RO	0x0	reserved.
3:0	reserved	RO	0x0	reserved.

8.2.2 INT_STS Register

Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_sts	RO	0x0	Device interrupt status. Overall device interrupt status. This bit is the OR of all the other interrupt status bits in this register after masking by their respective interrupt enable bits in INT_EN Register. This bit is masked by device_int_en. The resulting signal is output on the LOCK pin when lock_sel selects the device interrupt.
14:9	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
8:7	reserved	RO	0x0	reserved.
6	los2_int_sts	RO	0x0	XTAL Monitor Loss-of-Signal interrupt status Mirrors the los_evt event bit
5:0	reserved	RO	0x0	reserved.

8.3 LOSMON Registers

Before reprogramming a Loss of Signal Monitor block, the corresponding losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

8.3.1 LOSMON_STS Register

LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	ref_invalid	RO	0x1	Reference Clock Invalid status. Indicates whether this reference clock is currently considered to be invalid. This occurs if the clock is disqualified by one or more of the Loss-of-Signal and Activity monitors. • 0x0 = Clock is valid • 0x1 = Clock is invalid
0	los_sts	RO	0x1	Loss-of-Signal status. Current value of the LOS status from the clock monitor: • 0x0 = Clock meets the monitoring criteria • 0x1 = Loss-of-signal detected

8.3.2 LOSMON_EVENT Register

LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	los_evt	RW1C	0x1	Loss-of-Signal Event status. Set while the clock monitor asserts LOS. This bit cannot be cleared by software while the LOS condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. • 0x0 = Loss-of-signal not detected since the last time the bit was cleared • 0x1 = Loss-of-signal detected since the last time the bit was cleared

8.3.3 LOSMON_QUAL Register

LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	los_good_times	RW	0x0	LOS Monitor Qualification Count If this number of consecutive accepted clock LOS monitoring windows occur without a rejected window, then the clock is qualified and los_sts is set to 0. A value of 0 is the same as using the value 1.
3:0	los_fail_times	RW	0x0	LOS Monitor Disqualification Count If this number of rejected clock LOS monitoring windows occur without qualifying the clock, then the clock is disqualified and los_sts is set to 1. A value of 0 is the same as using the value 1.

8.3.4 LOSMON_WINDOW Register

LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:8	reserved	RO	0x0	reserved.
7:3	los_div_ratio	RW	0x0	LOS Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by los_div_ratio is less than 1/8 of the system clock frequency to achieve 25% accuracy. One period of the divided clock is the monitoring window duration. A value of 0 or 1 means divide by 1. The value 0x1F is not supported.
2:1	reserved	RO	0x0	reserved.
0	los_fail_mask	RW	0x0	LOS Monitor Failure Mask Masks the LOS monitor status los_sts contribution to ref_invalid. • 0 = los_sts contributes to ref_invalid • 1 = los_sts does not contribute to ref_invalid

8.3.5 LOSMON_THRESH Register

LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:16	los_acc_margin	RW	0x0	LOS Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within los_nom_num ± los_acc_margin.
15:13	reserved	RO	0x0	reserved.
12:0	los_rej_margin	RW	0x0	LOS Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of los_nom_num ± los_rej_margin.

8.3.6 LOSMON_NOMINAL Register

LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:13	reserved	RO	0x0	reserved.
12:0	los_nom_num	RW	0x0	LOS Monitor Nominal Cycle Count Sets the expected number of system clock periods within one monitor window. Set to 0x0 to disable the LOS monitor. Disabling the monitor causes the los_sts to get asserted, therefore the los_fail_mask should also be set when this field is written to 0x0.

8.4 MISC Registers

8.4.1 MISC_TRIM_OFFSET Register

Crystal trim offset. Address map for this block of registers: MISC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	xtal_trim	RW	0x0	Crystal Trim Offset. Crystal fractional frequency offset compensation. This is an 8-bit 2's complement value. Resolution = 2^{-20} ≈ 1 ppm, Range = ±2^{-13} ≈ ±122 ppm.

8.4.2 MISC_WRITE_FREQ Register

Write Frequency command. Address map for this block of registers: MISC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:0	write_freq	RW	0x0	Write Frequency. Frequency control word for synthesizer/DCO mode. This is a 29-bit 2's complement value. The units are 2^{-40} * 1e6 [ppm]. This provides a maximum setting of ±244ppm. An update to this multi-byte register only takes effect when the most significant byte (bits [28:24]) are written.

8.5 SYSDIV Registers

8.5.1 SYS_DIV_INT Register

System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
4:0	sys_div_int	RW	0xC	System Clock Divide Integer. The system clock divide integer value must be set to produce a system frequency between 180MHz and 333MHz, divided down from the APLL VCO frequency divided by 4. The frequency picked has side effects on various calculations done in other blocks (LOSMON Registers). Normally expected to be between 210MHz and 240MHz. The minimum valid value for this field is10 and the maximum is 15.

8.6 BIAS Registers

8.6.1 BIAS_STS Register

Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:9	reserved	RO	0x0	reserved.
8	bias_cal_in	RO	0x0	Bias Calibration comparator value. Raw bias_cal_in value.
7:5	cnf_bias_cal_eff	RO	0x0	Bias Calibration effective configuration value. Indicates the configuration value selected as sent to the bias control circuit. Valid when bias_cal_done is set to 1.
4:2	cnf_bias_cal	RO	0x0	Bias Calibration configuration value. Indicates the configuration value selected by the bias calibration logic. Valid when bias_cal_done is set to 1.
1	bias_cal_fail	RO	0x0	Bias Calibration failed. Indicates whether bias calibration completed successfully. Valid when bias_cal_done is set to 1. • 0x0 = Bias calibration succeeded • 0x1 = Bias calibration failed
0	bias_cal_done	RO	0x0	Bias Calibration done. Indicates whether bias calibration is running: • 0x0 = Bias calibration is in progress • 0x1 = Bias calibration is completed

8.7 XO Registers

8.7.1 XO_CNFG Register

Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets. For information on how to set up this interface, see Differential Output Termination.

Bit Field	Field Name	Type	Default Value	Description
31:19	Reserved	RO	0x0	reserved.
18:17	xo_cfg_res	RW	0x0	reserved. Not used.
16	en_ldo_xo	RW	0x1	XO LDO Enable. When set, enables the XO LDO.

Bit Field	Field Name	Type	Default Value	Description
15:14	en_gain	RW	0x1	XO gain boosting control. Selects the number of gain boosting amplifiers enabled during startup. • 0x0 = Gain boosting amplifiers are disabled • 0x1 = One parallel amplifier is enabled • 0x2 = Two parallel amplifiers are enabled • 0x3 = All three parallel amplifiers are enabled
13:8	Reserved	RW	0x1F	reserved.
7:6	Reserved	RW	0x0	reserved.
5:0	Reserved	RW	0x1F	reserved.

8.8 OUT Registers

8.8.1 OD_CNFG Register

Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	en_ldo_od	RW	0x1	Output Divider LDO Enable. When set, enables the corresponding output divider LDO.
14	reserved	RO	0x0	reserved.
13:0	outdiv_ratio	RW	0x69	Output Divider ratio. Output divider ratio. The minimum divide value is 10 (decimal).

8.8.2 ODRV_EN Register

Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:2	out_dis_state	RW	0x0	Output Driver disabled state. Controls the state of OUTx/nOUTx when the output driver is disabled. • 0x0 = Held Low/Low (except LVDS mode is held Low/High) • 0x1 = Held Low/High • 0x2 = Held Hi-Z/Hi-Z • 0x3 = Normal operation (not held static). This is intended for debug purposes only.
1	out_dis	RW	0x0	Output Driver disable. Forces the Output Driver to be disabled (for details, see Output Enable Control). • 0 = Output Driver is enabled if not disabled by other means • 1 = Output Driver is disabled
0	out_pd	RW	0x0	Output Driver power down. Powers down the Output Driver. When powered down, OUTx/nOUTx are tri-stated and the output enable control is ignored. • 0 = Output Driver is powered up and can be enabled/disabled • 1 = Output Driver is powered down

8.8.3 ODRV_MODE_CNFG Register

Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_cmos_mode	RW	0x1	Output Driver CMOS mode. Controls how OUTx and nOUTx are driven when CMOS mode is selected. • 0x0 = OUTx, nOUTx are driven with the same phase • 0x1 = OUTx, nOUTx are driven with the opposite phase • 0x2 = Only OUTx is driven. nOUTx is held low. • 0x3 = Only nOUTx is driven. OUTx is held low.
5:4	out_lvds_cm_voltage	RW	0x2	Output Driver LVDS common mode voltage control. Controls the common mode voltage of the output driver when LVDS mode is selected. • 0x0 = 700mV • 0x1 = 800mV • 0x2 = 900mV • 0x3 = 1000mV
3	out_hcsl_term_en	RW	0x1	Output Driver HCSL termination enable. Controls the internal HCSL termination. • 0x0 = Internal HCSL termination is disabled. An external termination resistor to ground is required. • 0x1 = Internal HCSL termination is enabled, providing an internal 50ohm resistor to ground.
2	en_out_bias	RW	0x1	Output Driver Bias Enable. When set, enables the output driver bias circuit.
1:0	out_mode	RW	0x0	Output Driver type. Selects the output driver type. • 0x0 = HCSL • 0x1 = reserved • 0x2 = LVDS • 0x3 = CMOS

8.8.4 ODRV_AMP_CNFG Register

Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	out_cnf_hcsl_swing	RW	0xB	Output Driver HCSL amplitude control. Controls the amplitude of the output driver when CML mode is selected. Each value provides a 50mV increment. • 0x0 = 200mV • 0x1 = 250mV • 0x2 = 300mV • 0x3 = 350mV • 0x4 = 400mV • 0x5 = 450mV • 0x6 = 500mV • 0x7 = 550mV • 0x8 = 600mV • 0x9 = 650mV • 0xA = 700mV • 0xB = 750mV • 0xC = 800mV • 0xD = 850mV • 0xE = 875mV • 0xF = 900mV
3	out_cnf_lvds_amp	RW	0x0	Output Driver LVDS amplitude control. Controls the amplitude of the output driver when LVDS mode is selected. • 0 = 350mV • 1 = 400mV
2:0	reserved	RW	0x4	reserved.

8.9 REF Registers

8.9.1 PREDIV_CNFG Register

Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

Use the Renesas Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
31:25	reserved	RO	0x0	reserved.
24:23	reserved	RO	0x0	reserved.
22	input_div_setb	RW	0x1	Input Divider Set When cleared, the corresponding input divider gets held in set mode (bit is active low).
21	enb_input_div	RW	0x0	Input Divider Enable When cleared, enables the corresponding input divider (active low).
20:0	reserved	RO	0x0	reserved.

8.10 GPIO Registers

8.10.1 OE_CNFG Register

Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	oe_pd	RW	0x0	OE Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the OE pin.
4	oe_pu	RW	0x1	OE Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the OE pin.
3	oe_pol	RW	0x0	OE Input Polarity. Controls the active polarity of the OE input pin when oe_sel is set to 0. • 0x0 = Active high (1 = enable outputs, 0 = disable outputs) • 0x1 = Active low (0 = enable outputs, 1 = disable outputs)
2:1	reserved	RO	0x0	reserved.
0	oe_sel	RW	0x0	OE Select. Selects whether the OE input pin can control the output enable of the clock output drivers: • 0x0 = The OE input disables the clock output drivers when deasserted. • 0x1 = The OE input does not affect the clock output drivers.

8.10.2 IO_CNFG Register

Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_startup	RW	0x0	Output Disable on startup until PLL locks. Controls whether the clock output drivers are disabled until the APLL locks during the startup sequence. • 0x0 = Clock output drivers are disabled until APLL lock asserts • 0x2 = Clock output drivers are not disabled by APLL lock status • 0x1, 0x3 = Reserved
5:4	pp_drv	RW	0x2	Push-Pull Drive Strength • Applies to pads LOCK, SDO, and SDA_SDI(O) (for 3-wire SPI only) when configured for push-pull mode. Drive strength increases as this setting increases.
3:2	od_drv	RW	0x3	Open-Drain Drive Strength • Applies to pads LOCK and SDO when configured for open-drain mode. Drive strength increases as this setting increases.
1	sda_pu	RW	0x1	SDA Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SDA_SDI(O) pin.
0	scl_pu	RW	0x1	SCL Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SCL_SCLK pin.

8.10.3 LOCK_CNFG Register

Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	reserved.
12	lock_od	RW	0x0	LOCK Open-drain enable. Set to 1 to configure the LOCK pin as an open-drain output. When lock_pol is set to 0, LOCK is driven low when the value to output is 0 and LOCK is open-drain when the value to output is 1. When lock_pol is set to 1, LOCK is driven low when the value to output is 1 and LOCK is open-drain when the value to output is 0.
11	lock_hiz	RW	0x0	LOCK Tristate Enable. Set to 1 to place the LOCK pin in a high-impedance state.
10	lock_pd	RW	0x0	LOCK Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the LOCK pin. This should not be used when lock_od is set to 1.
9	lock_pu	RW	0x1	LOCK Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the LOCK pin. Note that this internal pull-up is weak, so an external pull-up, tied to the V_{DDA} voltage rail is recommended when lock_od is set to 1.
8	lock_pol	RW	0x0	LOCK Output Polarity. Selects the polarity of the signal driven on the LOCK pin. When set to active high, the true value of the signal is driven. When set to active low, the inverse of the signal is driven. For example, when lock_sel selects APLL lock, and lock_pol is set to active high, LOCK drives high when the APLL is locked, and drives low when the APLL is unlocked. When lock_pol is set to active low, LOCK drives low when the APLL is locked, and drives high when the APLL is unlocked. This setting is ignored when lock_sel is set to 0x1F. • 0x0 = Active high • 0x1 = Active low
7:5	reserved	RO	0x0	reserved.
4:0	lock_sel	RW	0x0	LOCK Output Mode Select. Selects the status/clock to output on the LOCK pin: • 0x0 = APLL lock (apll_lock_sts) • 0x4 = Crystal loss-of-signal (LOSMON2 los_sts) • 0x9 = Device Interrupt (device_int_sts & device_int_en) • 0xA = Device ready (startup sequence completed) • 0x1D: Logic low • 0x1E: Logic high • Others: reserved

8.10.4 SDO_CNFG Register

SDO pin configuration control. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	reserved.
12	sdo_od	RW	0x0	SDO Open-drain enable. Set to 1 to configure the SDO pin as an open-drain output. When sdo_pol is set to 0, SDO is pulled low when the value to output is 0 and LOCK is open-drain when the value to output is 1. When sdo_pol is set to 1, SDO is pulled low when the value to output is 1 and LOCK is open-drain when the value to output is 0.

Bit Field	Field Name	Type	Default Value	Description
11	sdo_hiz	RW	0x0	SDO Tristate Enable. Set to 1 to tristate the SDO pin.
10	sdo_pd	RW	0x0	SDO Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the SDO pin.
9	sdo_pu	RW	0x1	SDO Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SDO pin.
8	sdo_pol	RW	0x0	SDO Output Polarity. • 0x0 = Active high (1 = locked, 0 = not locked) • 0x1 = Active low (0 = locked, 1 = not locked)
7:4	reserved	RO	0x0	reserved.
3:0	sdo_sel	RW	0x0	SDO Output Select. Selects the status/clock to output on the SDO pin when the serial port is in either I2C mode or SPI 3-wire mode. In SPI 4-wire mode, SDO is the SPI data out. • 0x0 = APLL lock (apll_lock_sts) • 0x4 = Crystal loss-of-signal (LOSMON2 los_sts) • 0x9 = Device Interrupt (device_int_sts & device_int_en) • 0xA = Device ready (startup sequence completed) • 0xD = Logic low • 0xE = Logic high • others = reserved

8.10.5 STARTUP_STS Register

Start-up status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	bond_id	RO	0x0	Bond ID value. Value of bond id die pad.
6	reserved	RO	0x0	Reserved
5:0	gpio_at_startup	RO	0x0	GPIO startup value. Value of pins latched at startup. bit [0] = LOCK bit [1] = SDA_SDI(O) bit [2] = SCL_SCLK bit [3] = SDO bit [4] = OE bit [5] = nCS

8.10.6 GPIO_STS Register

GPIO status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	lock_o	RO	0x0	LOCK Output value. Reflects the value driven on the LOCK pin when lock_sel is set to 0x0 through 0x4. This bit reads as 0 when lock_sel is set to any other value.
0	oe_i	RO	0x0	OE Input value. Reflects the value input on the OE pin when oe_sel is set to 0. This bit reads as 0 when oe_sel is set to 1.

8.10.7 SCRATCH0 Register

Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:0	scratch0	RW	0x0	Scratch register. This value can be stored in OTP on a per-configuration basis. It is not used by the device hardware for any purpose. Users can set this to any value.

8.11 SSI Registers

The acronym SSI refers to items that are generic to the Slave Serial Interface in any mode of operation. SPI or I^2C is used for features and functions that are specific to those operating modes.

8.11.1 SPI_CNFG Register

SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:5	spi_dummy_size	RW	0x1	SPI dummy read byte count. Number of dummy bytes shifted out before the read data when spi_dummy_en is 1. • 0x0 = reserved • 0x1 = 1 byte • 0x2 = 2 bytes • 0x3 = 3 bytes
4	spi_dummy_en	RW	0x0	SPI dummy read byte enable. Enables insertion of dummy read bytes. • 0x0 = Read data is immediately available (no dummy bytes) • 0x1 = spi_dummy_size number of bytes are shifted out before the read data
3	spi_del_out	RW	0x0	SDO driving edge selection. Selects the clock edge that drives SDO. • 0x0 = SDO is driven on opposite SCLK edge than the sampling edge • 0x1 = SDO is delayed one half cycle of SCLK
2	reserved	RO	0x0	reserved.
1	spi_clk_sel	RW	0x0	SDI sampling edge selection. Selects the clock edge that samples SDI. • 0x0 = SDI is sampled on rising SCLK edge • 0x1 = SDI is sampled on falling SCLK edge
0	spi_3wire	RW	0x1	Select SPI 3-wire mode. Selects 3-wire or 4-wire mode. • 0x0 = Normal 4-wire SPI • 0x1 = 3-wire SPI. Data is received and transmitted on SDA_SDI(O)

8.11.2 I2C_FLTR_CNFG Register

I2C mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5:4	i2c_speed	RW	0x0	I2C speed selection. Selects the operating speed of the I2C interface. Only the output driver slew rate is affected by this setting (higher setting means higher drive strength). The I2C master must provide the appropriate SCL frequency and other timing requirements according to the selected speed. • 0x0 = 1.8V Standard mode (100 kHz) or 3.3V Standard (100kHz) and Fast mode (400kHz) • 0x1 = 1.8V Fast mode (400 kHz) • 0x2 = reserved • 0x3 = 1.8V and 3.3V Fast mode plus (1 MHz)
3:0	i2c_spike_fltr	RW	0x1	I2C digital spike filter duration. Controls the duration of the digital spike filters on the SCL and SDA inputs, specified in number of system clock cycles. 0 disables filtering.

8.11.3 I2C_TIMING_CNFG Register

I2C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	i2c_sda_high_hold	RW	0x4	I2C/SMBus transmit one bit delay. Delays transmission of 1 value by 8x this number of system clock cycles.
3:0	i2c_sda_low_hold	RW	0x4	I2C/SMBus transmit zero bit delay. Delays transmission of 0 value by8x this number of system clock cycles.

8.11.4 I2C_ADDR_CNFG Register

I2C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:0	i2c_addr	RW	0x09	I2C device address. Sets I2C device address that the SSI acknowledges and accepts accesses on. Bits[1:0] are set by OTP only and can be overridden by pins as per Table 21.

8.11.5 SSI_GLOBAL_CNFG Register

Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	ssi_addr_size	RW	0x0	SSI address size. When 0 the SSI expects 1-byte CSR addresses; when 1 the SSI expects 2-byte CSR addresses. Upper address bits are taken from the SSI's page register to create a full 32-bit CSR address. • 0x0 = 1-byte address • 0x1 = 2-byte address

Bit Field	Field Name	Type	Default Value	Description
1:0	ssi_enable	RW	0x1	SSI mode. Selects the serial port mode: • 0x0 = SSI is disabled • 0x1 = SSI is in I2C mode • 0x2 = SSI is in SPI mode • 0x3 = Reserved

8.12 APLL Registers

8.12.1 APLL_FB_DIV_FRAC Register

APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:27	reserved	RO	0x0	reserved.
26:0	apll_fb_div_frac	RW	0x0	APLL Feedback Divider Fraction Numerator. APLL feedback divider numerator value. The denominator is a fixed value of 2^{27}. This register is atomic. When the most significant byte (bits [31:24]) is written, the new value is applied to the APLL.

8.12.2 APLL_FB_DIV_INT Register

APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9:0	apll_fb_div_int	RW	0x6C	APLL Feedback Divider Integer. APLL feedback divider integer value. This register is atomic. When the most significant byte (bits [15:8]) is written, the new value is applied to the APLL.

8.12.3 APLL_FB_SDM_CNFG Register

APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	apll_fb_dither_en	RW	0x0	APLL Feedback SDM Dither Enable. Dither enable for the SDM controlling the APLL feedback divider. • 0x0 = dither disabled • 0x1 = dither enabled
4	apll_fb_dither_ns	RW	0x0	APLL Feedback SDM Dither Noise shaping. Dither noise shaping enable for the SDM controlling the APLL feedback divider. • 0x0 = dither not shaped • 0x1 = dither shaped

Bit Field	Field Name	Type	Default Value	Description
3:2	apll_fb_dither_gain	RW	0x0	APLL Feedback SDM Dither Gain. Gain control for the SDM controlling the APLL feedback divider. • 0x0 = LSB • 0x1 = 2*LSB • 0x2 = 4*LSB • 0x3 = 8*LSB
1:0	apll_fb_sdm_order	RW	0x3	APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the APLL. • 0x0 = Integer • 0x1 = 1st order • 0x2 = 2nd order • 0x3 = 3rd order

8.12.4 APLL_CNFG Register

APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	en_doubler	RW	0x1	Frequency doubler enable. Enables the frequency doubler. • 0 = Disable • 1 = Enable

8.12.5 LPF_CNFG Register

APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.

See to APLL Loop Filter (LPF) for details. Use the Renesas Timing Commander Software to provide optimal setting recommendations for a specific device configuration.

Bit Field	Field Name	Type	Default Value	Description
7	apll_vco_filter_byp	RW	0x0	VCO current source filter bypass. • 0 = Filter active • 1 = Filter bypassed
6:4	cnf_LPF_cp	RW	0x7	Loop filter pole capacitor setting. • 0x0 = 33.3pF • 0x1 = 36pF • 0x2 = 38.7pF • 0x3 = 41.4pF • 0x4 = 44.1pF • 0x5 = 46.8pF • 0x6 = 49.5pF • 0x7 = 52.2pF

Bit Field	Field Name	Type	Default Value	Description
3:0	cnf_LPF_res	RW	0x6	Loop filter resistor setting. • 0x0 = 0Ohm • 0x1 = 400Ohm • 0x2 = 800Ohm • 0x3 = 1.2kOhm • 0x4 = 1.6kOhm • 0x5 = 2kOhm • 0x6 = 2.4kOhm • 0x7 = 2.8kOhm • 0x8 = 3.2kOhm • 0x9 = 3.6kOhm • 0xA = 4kOhm • 0xB = 4.4kOhm • 0xC = 4.8kOhm • 0xD = 5.2kOhm • 0xE = 5.6kOhm • 0xF = 6kOhm

8.12.6 LPF_3RD_CNFG Register

APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	byp_p3	RW	0x0	Bypass 3rd pole. This bit can only be set to 1 when operating with an integer feedback divider. • 0 = 3rd pole active • 1 = 3rd pole bypassed
6:4	cnf_LPF_R3	RW	0x3	Loop filter 3rd pole resistor setting. • 0x0 = 0Ohm • 0x1 = 800Ohm • 0x2 = 1.6kOhm • 0x3 = 2.4kOhm • 0x4 = 3.2kOhm • 0x5 = 4kOhm • 0x6 = 4.8kOhm • 0x7 = 5.6kOhm
3	reserved	RO	0x0	reserved.
2:0	cnf_LPF_C3	RW	0x7	Loop filter 3rd pole capacitor setting. • 0x0 = 2pF • 0x1 = 3pF • 0x2 = 4pF • 0x3 = 5pF • 0x4 = 6pF • 0x5 = 7pF • 0x6 = 8pF • 0x7 = 9pF

8.12.7 APLL_LOCK_CNFG Register

APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	use_raw_lock	RW	0x0	APLL Lock Status Select to Pin. When set, the raw selected lock (precision or original) is sent to the GPIO status pin (LOCK or SDO)
8	apll_precision_lock_en	RW	0x1	APLL Precision Lock Detector Enable. When set, enables the lock detector using the ranges controlled by apll_th_refl and apll_th_refh.
7:6	apll_lock_timer	RW	0x2	APLL Lock Timer. Controls the digital debounce interval for the lock indication for the APLL. This duration is a function of the system clock cycles. • 0x0 = 0us • 0x1 = 570 cycles of the system clock • 0x2 = 5700 cycles of the system clock • 0x3 = 57000 cycles of the system clock.
5	sel_1time_lock	RW	0x0	One time lock select. Controls whether lock detection occurs once or continuously. • 0x0 = Real-time lock. • 0x1 = One-time lock. When the lock signal asserts, it remains asserted even if the APLL loses lock.
4	lck_detect_cal_byp	RW	0x0	Lock detect during calibration enable. Selects when the lock detector is enabled. • 0x0 = Lock detector is enabled after VCO calibration completes • 0x1 = Lock detector is enabled during and after VCO calibration
3	lck_byp	RW	0x0	Lock detector disable. • 0x0 = Lock detector is enabled according to lck_detect_cal_byp and sel_1time_lock • 0x1 = Lock detector is disabled and the lock signal is asserted
2:0	lck_detect_ref_sel	RW	0x0	Analog Lock Detect RC filter resistor Selects the filter resistor. C=5pF. • 0x0 = 7.5kΩ • 0x1 = 15kΩ • 0x2 = 23kΩ • 0x3 = 30kΩ • 0x4 = 37.5kΩ • 0x5 = 45kΩ • 0x6 = 53kΩ • 0x7 = 60kΩ

8.12.8 APLL_LOCK_THRSH Register

APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	apll_th_refh	RW	0x8	APLL Precision Lock High Threshold. Controls the high threshold voltage of the precision lock detector. The threshold is approximately 750mV + 20mV * apll_th_refh. The default is around 900mV.
3:0	apll_th_refl	RW	0x8	APLL Precision Lock Low Threshold. Controls the low threshold voltage of the precision lock detector. The threshold is approximately 50mV + 18mV * apll_th_refl. The default is around 200mV.

8.12.9 VCO_CAL_STS Register

APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	vco_cal_fail	RO	0x0	VCO Calibration failed. Indicates whether VCO calibration completed successfully. Valid when vco_cal_done is set to 1. • 0x0 = VCO calibration succeeded • 0x1 = VCO calibration failed
6	vco_cal_done	RO	0x0	VCO Calibration done. Indicates whether VCO calibration is running: • 0x0 = VCO calibration is in progress • 0x1 = VCO calibration is completed
5:0	vco_cap	RO	0x0	VCO Calibration frequency band. Indicates the frequency band selected by the VCO calibration logic. Valid when vco_cal_done is set to 1.

8.12.10 APLL_STS Register

APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_sts	RO	0x0	APLL rail high real-time status. When high, indicates that the APLL is railed high.
1	apll_rail_low_sts	RO	0x0	APLL rail low real-time status. When high, indicates that the APLL is railed low.
0	apll_lock_sts	RO	0x0	APLL lock real-time status. Indicates if the APLL is locked to its reference. • 0x0 = unlocked • 0x1 = locked

8.12.11 APLL_EVENT Register

APLL Event status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_evt	RW1C	0x0	APLL Rail High event. Set to 1 when the APLL lock detects a rail high status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
1	apll_rail_low_evt	RW1C	0x0	APLL Rail Low event. Set to 1 when the APLL lock detects a rail low status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
0	apll_lol	RW1C	0x0	APLL Loss-of-lock event. Set to 1 when the APLL lock status transitions from locked to unlocked. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.

8.12.12 APLL_LOL_CNT Register

APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:0	apll_lol_cnt	RW	0x0	APLL Loss-of-Lock Counter. This counter increments each time the APLL lock status de-asserts, and saturates at 0xF. It is cleared by writing it to 0x0, and can be preset by writing the desired value. Preset can be used either as a debug tool or to cause a threshold alarm to happen sooner because the alarm threshold is not configurable.

8.13 INP Registers

8.13.1 REF_CLK_IN_CNFG Register

Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

Use the Renesas Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	en_LVDS	RW	0x0	Reference Clock LVDS Enable. Enables compatible termination when the reference clock input signal is LVDS. • 0 = LVDS input termination is disabled • 1 = LVDS input termination is enabled
8	en_HCSL	RW	0x0	Reference Clock HCSL Enable. Enables compatible termination when the reference clock input signal is HCSL. • 0 = HCSL input termination is disabled • 1 = HCSL input termination is enabled
7	en_ldo_ib	RW	0x1	Reference Clock Input Pad LDO enable. When set, enables the input buffer LDO.

Bit Field	Field Name	Type	Default Value	Description
6	en_selfbias_cmos	RW	0x0	Reference Clock Input Pad internal self-bias enable. When the single-ended reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. • 0x0 = Internal self-bias is disabled (input signal is DC-coupled) • 0x1 = Internal self-bias is enabled (input signal is AC-coupled)
5:4	en_term	RW	0x0	Unused. No defined function. Reserved for future use.
3	en_dc_bias	RW	0x0	Reference Clock Input Pad internal DC bias enable. When the differential reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. • 0 = Internal DC bias is disabled (input signal is DC-coupled) • 1 = Internal DC bias is enabled (input signal is AC-coupled)
2	en_inbuff	RW	0x0	Reference Clock Input Pad enable. The reference clock input pad must be enabled in Clock Generator mode and should be left disabled in synthesizer/DCO mode. • 0 = Input pad is disabled • 1 = Input pad is enabled
1	CMOS_Sel	RW	0x0	Reference Clock Input Pad CMOS/differential select. Configures the reference clock input pad for a single-ended CMOS or differential input signal. • 0 = Differential input is selected • 1 = CMOS input is selected
0	P_N_Diff_Sel	RW	0x0	Reference Clock Input Pad PMOS/NMOS select. Configures the reference clock input pad according to the common mode voltage of the provided input signal. • 0 = PMOS input pair is enabled (low common mode voltage) • 1 = NMOS input pair is enabled (higher common mode voltage)

9. Package Information

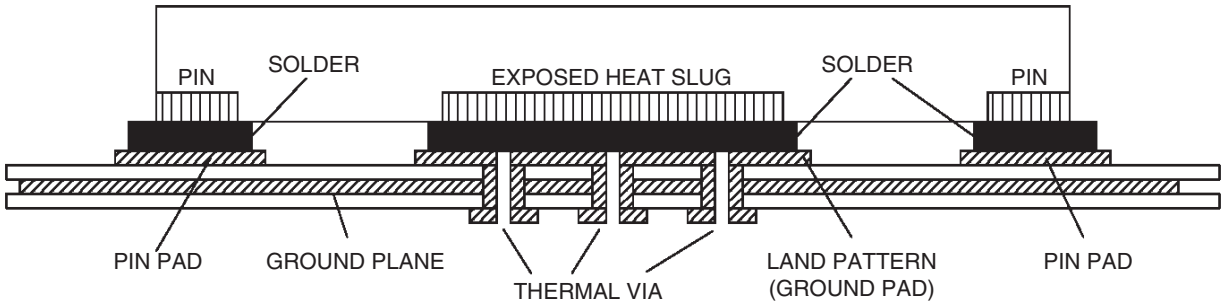
9.1 ePad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 16*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13 mils (0.30 to 0.33 mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

Figure 16. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)



9.2 Thermal Characteristics

Table 36. Thermal Characteristics

Symbol	Parameter		Value	Unit
θ_{JA}	Theta J_A. Junction to Ambient Air Thermal Coefficient[a][b]	0 m/s air flow	49.6	°C/W
		1 m/s air flow	46.6	°C/W
		2 m/s air flow	43.9	°C/W
		3 m/s air flow	42.8	°C/W
θ_{JB}	Theta J_B. Junction to Board Thermal Coefficient[a][c]		9.7	°C/W
θ_{JC}	Theta J_C. Junction to Device Case Thermal Coefficient[a]		27.8	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)		3	-

[a] Multi-Layer PCB with 2 ground and 2 voltage planes.

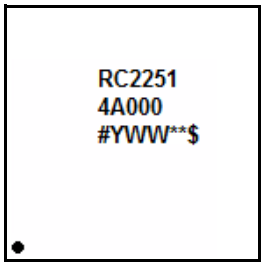
[b] Assumes ePad is connected to a ground plane using a grid of 9 × 9 thermal vias.

[c] Chip junction to ePad.

10. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

11. Marking Diagram



- Line 1 and 2 indicate the part number.
- Line 3 denotes the following:
  - “YWW” is the last digit of the year and week that the part was assembled.
  - “$” denotes mark code
  - “#” denotes stepping

12. Ordering Information

Part Number[a]	Package	MSL Rating	Carrier Type	Temperature Range
RC22514AdddGNL#BB0	4 × 4 × 1.5 mm, 28-VFQFPN	3	Tray	-40° to +85°C
RC22514AdddGNL#KB0	4 × 4 × 1.5 mm, 28-VFQFPN	3	Tape and Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C

[a] Replace “ddd” with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “000” for unprogrammed parts.

Table 37. Pin 1 Orientation in Tape and Reel Packaging

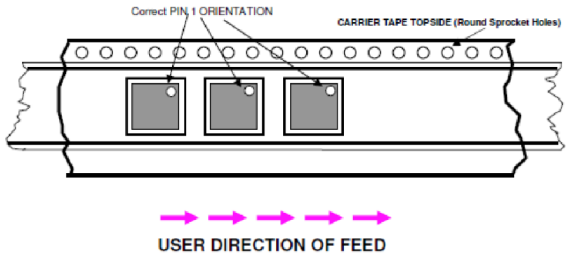
Part Number Suffix	Pin 1 Orientation	Illustration
NK#K	Quadrant 2 (EIA-481-D)	

Table 38. Product Identification

Part Number	Product ID
RC22514A	0x214A

13. Glossary

Term	Definition
3-level	Describes an input structure that support a high, middle and low logic level allowing one of three states to be selected.
ADC	Analog to Digital Converter – These devices require reference clock inputs with strict jitter budgets
AC-coupling	A method of connecting a transmitter to a receiver using series capacitors. This only transmits signal transitions, not DC voltage levels, so can be useful for constantly toggling signals like clocks, especially when trying to isolate the DC voltage levels.
APLL	Analog Phase Lock Loop – PLL technology that uses purely analog circuitry. Useful for low-noise applications without needs for low loop bandwidths or sophisticated switchover techniques.
ASIC	Application Specific Integrated Circuit – Custom chip design usually developed by a system vendor to meet the needs of a specific product family. Not available for general sale. Many ASICs include serial interfaces that need high-performance reference clock inputs
CDR	Clock/Data Recovery – Circuit that recovers a clock from a data stream and uses it to create a sampling clock for data recovery from the stream
C_L	Load Capacitance – A crystal parameter that affects the frequency accuracy of the crystal + oscillator circuit
CLKIN	Clock input signal (may be differential using pins CLKIN/nCLKIN or single-ended using CLKIN or nCLKIN)
CML	Current Mode Logic – A protocol for differential signaling between two chips. Referenced to V_{DD}.
CMOS	Complementary Metal-Oxide Semiconductor – Protocol for single-wire signaling between two chips. Referenced to Ground and VDD
CPLD	Complex Programmable Logic Device – Programmable IC with complexity less than an FPGA. Often used for power-up sequencing on printed circuit board designs
CPU	Central Processing Unit – A type of integrated circuit that executes software. Requires reference clocks with only time-domain jitter specifications.
CRC	Cyclic Redundancy Check – A method of determining if a block of data was stored or transmitted correctly. Involves the addition of one or more bytes of extra information to determine data integrity. One of several algorithms may be used. CCITT-16 is a commonly used algorithm.
DAC	Digital to Analog Converter – These devices require reference clock inputs with strict jitter budgets
DCO	Digitally Controlled Oscillator – An adjustable oscillator for generating frequencies that can be adjusted by writing a digital word to it
EEPROM	Electrically-Erasable Programmable Read-Only Memory – Commonly used non-volatile memory device.
ESR	Equivalent Series Resistance – A parameter for a quartz crystal indicating its ability to dissipate current from an oscillator circuit
FOD	Fractional Output Divider – Circuit that can divide down a clock frequency using non-integer ratios. Adds flexibility at a cost of increased size, complexity and power consumption and extra spurs
FPGA	Field-Programmable Gate Array – Highly complex custom programmed device that may include CPUs, serial interfaces and other logic. Able to be re-programmed at will. Depending on what it contains, an FPGA may need reference clocks with low or high performance
GPI	General-Purpose Input – An input signal that can be programmed for many different purposes
GPIO	General-Purpose Input/Output – A signal that can be programmed for many different purposes as either an input or an output
GPO	General-Purpose Output – An output signal that may be programmed to be used for many different purposes
GUI	Graphical User Interface – A Timing Commander Personality that includes graphical elements to make device programming simpler
HCSL	High-speed Current Steering Logic – Differential signaling protocol usually associated with PCIe components
HSTL	High-speed Transceiver Logic – Low voltage-swing single-ended signaling protocol. Not often used.
I^2C	Inter-Integrated Circuit signaling protocol – A serial data transmission scheme originally created by Philips Semiconductor and released into the public domain.
IBIS	Input/output Buffer Information Specification – Standard for providing information for signal integrity simulation of an integrated circuit's inputs and outputs
IDT	Integrated Device Technology – A wholly owned subsidiary of Renesas
IOD	Integer Output Divider – Circuit for dividing down a clock signal using whole numbers only.

Term	Definition
LAN	Local Area Network – Wired or wireless communication protocol between PC within a short distance
LGA	Land Grid Array – Type of integrated circuit package that has contact locations around the periphery of the package, but only on the bottom surface
LOL	Loss-of-Lock – A signal or register bit indicating that a PLL is not in the locked state
LOS	Loss-of-Signal – A signal or register bit indicating that a clock input is not receiving a valid input clock
LP-HCSL	Low-Power HCSL – Variant of an HCSL output buffer that includes the transmitter series termination internal to the part
LVDS	Low-Voltage Differential Signaling – Differential signaling protocol using a lower voltage swing. Referenced to VDD.
LVPECL	Low-Voltage Pseudo Emitter-Coupled Logic – Differential signaling protocol using a voltage swing similar to ECL logic, but uses a 2.5V or 3.3V positive reference voltage.
MMD	Multi-Modulus Divider - Clock divider circuit that applies one of several integer divide ratios under control of an SDM.
NTP	Network Time Protocol – Software based protocol that aligns real-time clocks across a wide-area network. Can align to less than 1 second of accuracy.
OCXO	Oven-Controlled Crystal Oscillator – A device that generates a highly stable clock frequency by using an internal oven to maintain the quartz crystal at an even internal temperature
OTN	Optical Transport Network – Asynchronous optical communication protocol defined in ITU-T G.709. Used for high-speed data communications. Able to carry many different protocols at the same time over large distances.
OTP	One-Time Programmable memory – Non-volatile storage medium that allows any individual memory bit to be programmed only once.
OTU3	OTN line rate of approximately 40Gbps
OTU4	OTN line rate of approximately 100Gbps
PCIe	Peripheral Component Interconnect Express – Interchip communication protocol primarily used in PC and datacenter equipment
PHY	Physical Layer Interconnection component. Integrated circuit that formats a signal for transmission over an inter-system interconnect medium. Requires reference clock inputs that may be strict if the interconnect medium is high speed
PLL	Phase Lock Loop – Integrated circuit that generates, cleans up, or translates clock signals
PSRR	Power Supply Rejection Ratio (sometimes referred to as Power Supply Noise Rejection) – Indicates the amount of noise energy received on the power pins of the PLL that appear on the output. May be expressed as a dB ratio of input to output power at the noise frequency or as an absolute value of the output power at the noise frequency
PVT	Process, Voltage, and Temperature – Three axes of stress that affect the performance of an integrated circuit
QFN	Quad Flat No-leads package – Type of integrated circuit package that has interconnection pads on all 4 sides of the package including on the bottom. Often has a heat-dissipation metal slug called an ePAD.
RAM	Random Access Memory – Type of integrated circuit that requires clock signals.
REA	Renesas Electronics America
RMS	Root-Mean-Square – Method of specifying the power content of an oscillating signal.
SD Card	Secure Digital memory card – Popular non-volatile storage medium that involves removable cards. Can provide firmware or software updates to a system.
SDM	Sigma-Delta Modulator - Control logic function that uses a sigma-delta algorithm to control an MMD to generate a fractional divide ratio that is dynamically adjustable to minimize noise contributions.
SPI	Serial Peripheral Interface – Serial communication protocol for inter-chip communication. Originally developed by Motorola Semiconductor. It is widely used in the industry but has never been standardized.
SSC	Spread Spectrum Clock – A clock signal that is modulated at a low rate to reduce electro-magnetic emissions from a system. Primarily used in data center equipment.
SSTL	Stub Series Terminated Logic – Signaling protocol commonly used with Dynamic RAMs
TCXO	Temperature Compensated Crystal Oscillator – Electronic component that uses a quartz crystal to generate a reference clock frequency and temperature-compensation logic to stabilize the frequency over temperature. Stability falls between XOs and OCXOs.
USB	Universal Serial Bus – device-device interconnection protocol used for short-range wired communication. Is used in some systems to provide management access for software or firmware update.
VCO	Voltage Controlled Oscillator - an adjustable oscillator for generating frequencies that can be adjusted by changing the voltage on a control pin

Term	Definition
V_{DD}	Generic term used for any power input reference or pin.
V_{DDO}	Power input pins that provide power and set a reference voltage for the output buffers. There are several such pins each associated with specific output buffers.
V_{DDREF}	Power input pin(s) that power and set a reference voltage for the input reference clocks
XO	Crystal Oscillator circuit – electronic component that generates a frequency reference by combining a quartz crystal and an oscillator circuit in a single package. Since the crystal is uncompensated, the frequency stability over temperature may be bad.
Xtal	Crystal – passive quartz crystal that provides a frequency reference when stimulated by an oscillator circuit

14. Device Errata

#	Parameter/Function	Description	Work Around
A1	odc, Output Duty Cycle in Table 10.	Violation to max 55% for /11 and /13.	None. Please use a VCO frequency that allows for an even divide to achieve the desired output frequency.

15. Revision History

Revision	Date	Description of Change
1.06	Nov 11, 2022	• Updated Figure 7; Standard HCSL Termination • Updated the I²C slave addressing examples in the following: ○ I2C 1-byte (1B) Addressing Example ○ I2C 2-byte (2B) Addressing Example ○ SPI 2-byte (2B) Addressing Example
1.05	Aug 5, 2022	• Updated the I2C slave addressing examples in I2C 1-byte (1B) Addressing Example and I2C 2-byte (2B) Addressing Example • Removed OTP information • Completed other minor changes
1.04	Mar 18, 2022	Updated the Ordering Information
1.03	Nov 8, 2021	Updated the test condition for the Frequency Stability (Free-run) parameter in Table 10
1.02	Oct 29, 2021	Updated the Frequency Stability (Free-run) parameter in Table 10
1.01	Jun 4, 2021	Updated the description of the HCSL internal resistor to 50Ω in Direct-Coupled HCSL Termination and Clock Output Driver.
1.00	May 12, 2021	Initial release.

28-VFQFPN, Package Outline Drawing

4.0 x 4.0 x 1.5 mm Body,0.40mm Pitch,Epad 2.7 x 2.7 mm

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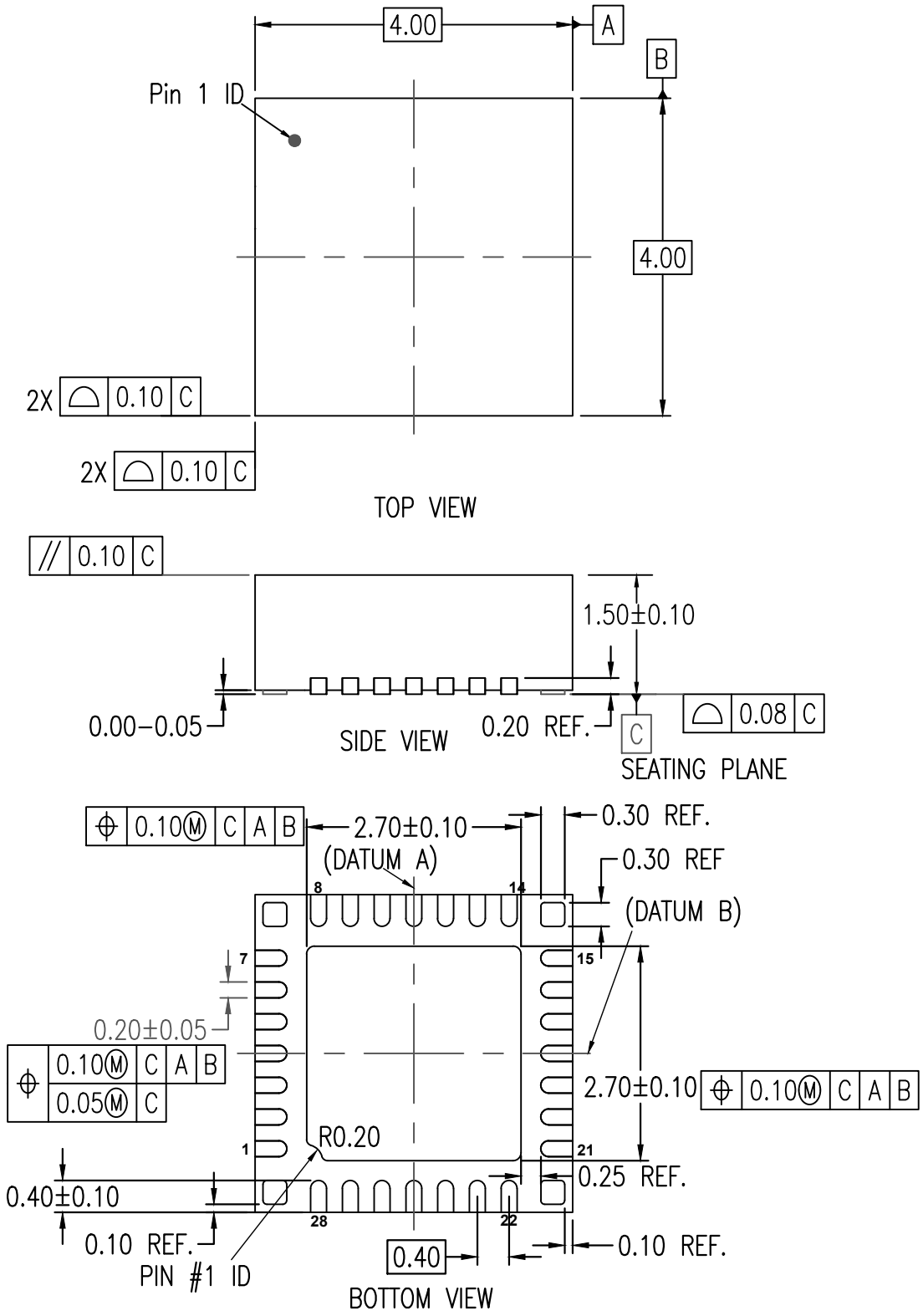
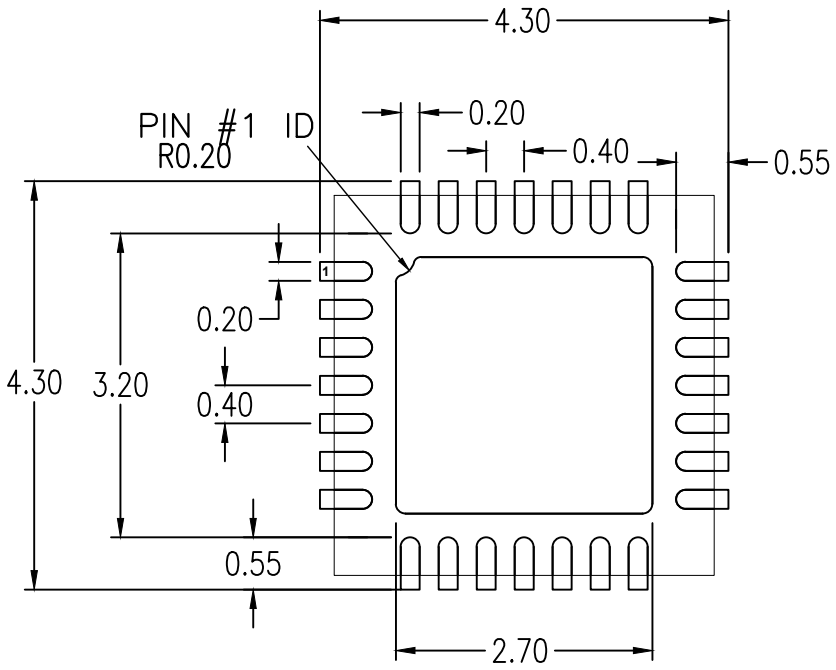


NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Oct 22, 2019	Rev 00	Initial Release