RC32504A

FemtoClock®2 Sub-100fs Universal Frequency Translator

The RC32504A is a small, low-power timing component designed to be placed immediately adjacent to a PHY, switch, ASIC or FPGA that requires several reference clocks with jitter performance less than 100fs. The RC32504A can act as a frequency synthesizer to locally generate the reference clock, a jitter attenuator to perform local clean-up and/or frequency translation of a centrally-supplied reference, a Synchronous Ethernet equipment clock to perform passband filtering and clean-up of network-supplied references or as a DCO for frequency margining or OTN clock applications.

The device is a member of the Renesas high-performance FemtoClock2 family.

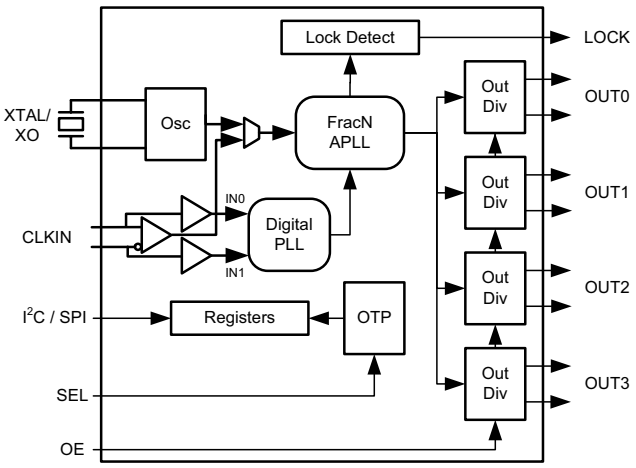
Features

- Jitter below 100fs RMS (10kHz to 20MHz)
- Compliant with ITU-T G.8262 for synchronous Ethernet/OTN (EEC/OEC) and ITU-T G.8262.1 for enhanced synchronous Ethernet/OTN (eEEC/eOEC)
- PLL core consists of fractional-feedback Analog PLL (APLL) which can optionally be steered by a Digital PLL (DPLL)
  - Operates from a 25MHz to 80MHz crystal or XO
  - APLL frequency independent of input/crystal frequency
  - Operates as a frequency synthesizer, jitter attenuator, synchronous equipment slave clock or Digitally Controlled Oscillator (DCO)
  - DPLL loop filter programmable from 0.1Hz to 12kHz
  - DCO has tuning granularity of < 1ppt
- Programmable input buffer supports HCSL, LVDS, or two LVCMOS with no external terminations needed
  - Input frequencies: 1MHz to 800MHz (250MHz for LVCMOS)
  - Reference monitor qualifies/disqualifies input clock
- Programmable status output
- 4 differential/8 LVCMOS outputs
  - Any frequency from 10MHz to 1GHz (180MHz for LVCMOS)
  - Programmable output buffer supports HCSL (DC-coupled), LVDS/LVPECL/CML (AC-coupled) or two LVCMOS
  - Differential output swing is selectable: 400mV to 800mV
  - Output Enable input with programmable effect
- Supports up to 1MHz I^2C or up to 20MHz SPI serial processor port
- Can configure itself automatically after reset through internal customer-definable One-Time Programmable (OTP) memory with up to four different configurations
- 4 × 4 mm 24-QFN package

Applications

- Synchronous Ethernet/OTN equipment
- Reference clock generator for 100Gbps/400Gbps PHYs or switches
- Adjustable OTN clock reference for OTU3/OTU4 mappers
- Reference clock for programmable FiberOptic Modules

Block Diagram



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1. About this Document

1.1 Document Conventions

This document uses the following conventions.

1.1.1 Signal Notation

Signals are either active low or active high. An active-low signal has an active state of logic 0 (or the lower voltage level) and is denoted by a lowercase n prefix. An active-high signal has an active state of logic 1 (or the higher voltage level) and is not denoted by a special character. The following table illustrates the signal naming convention.

Table 1. Signal Naming Convention

State	Signal Naming
Active low	nNAME
Active high	NAME

1.1.2 Object Size Notation

- A byte is an 8-bit object.
- A half-word (hword) is a 16-bit object.
- A word is a 32-bit object.
- A double-word (dword) is a 64-bit object.

1.1.3 Numeric Notation

- Hexadecimal numbers are denoted by the prefix 0x (for example, 0x04).
- Binary numbers are denoted by the prefix 0b (for example, 0b010).
- Register blocks that have multiple iterations are denoted by [x:y] in their names; where x is first instance, and y is the last instance. For example, BLOCK[0:1] with a base address of 0x10 += 0x08 indicates there are two iterations of the registers defined for BLOCK, with instance 0 at a base address of 0x10 and instance 1 at a base address of 0x18.

1.1.4 Endianness

RC32504A uses little-endian notation.

The Least Significant Bit (LSB) in a data object is numbered with 0, and the Most Significant Bit (MSB) is numbered with the width of the object minus 1. For example, the LSB index of a word is 0 and the MSB is 31.

The least significant byte of a multi-byte register field is located at the base address of the register and subsequent bytes up to the most significant byte are located at increasing byte addresses. For example, given a half-word located at address 0x42, the least significant byte (bits 7:0) can be accessed at address 0x42, and the most significant byte (bits 15:8) can be accessed at address 0x43.

Some multi-byte register fields are updated atomically, where the values written to the lower order bytes are buffered but not applied to the internal logic until the most significant bits are written, which then triggers the entire new register field value to be applied to the internal logic at once. Atomic registers fields are noted in the description.

When a multi-byte register field is non-atomic (the default if not noted otherwise), the value written to any byte of the field is immediately applied to the internal logic.

2. Pin Information

2.1 Pin Assignments

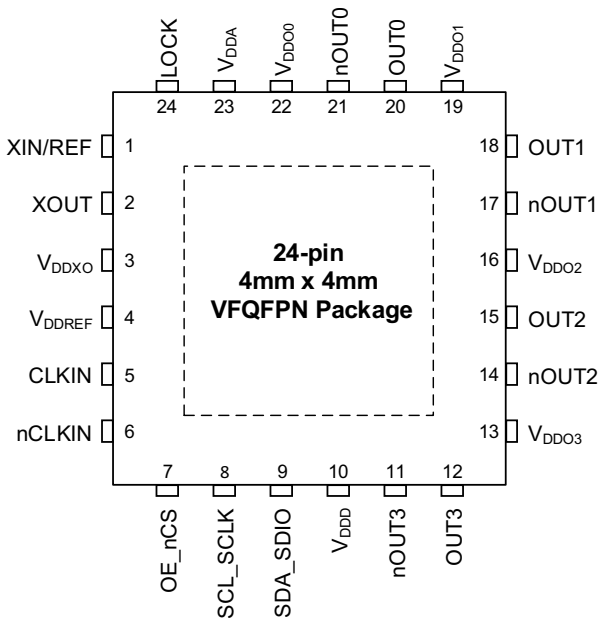


Figure 1. Pin Assignments – Top View

2.2 Pin Descriptions

Table 2. Pin Descriptions

Number	Name	Type		Description
1	XIN/REF	I		Crystal Input. Refer to Crystal Recommendation for details. The interface can be over-driven with an oscillator input. Refer to Overdriving the XTAL Interface for details.
2	XOUT	O		Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to XIN/REF, then this pin must be left unconnected.
3	V_{DDXO}	Power		Oscillator supply. 1.8V supported. XIN/REF and XOUT are referenced to this voltage supply.
4	V_{DDREF}	Power		Reference input supply. 1.8V supported. CLKIN and nCLKIN are referenced to this voltage supply.
5	CLKIN	I		Non-inverting differential reference clock input/CMOS single-ended reference clock input. If the clock signal is AC-coupled, then en_dc_bias must be set to 1 for a differential input, or en_selfbias_cmos must be set to 1 for single-ended inputs. When in single-ended operation, the input supports the termination of a single leg of an LVDS clock (no additional external termination). Input buffer should be disabled if unused by setting en_inbuff to 0. For information on input buffer configuration and termination strategies, see Clock Input Interface.
6	nCLKIN	I		Inverting differential reference clock input/CMOS single-ended reference clock input.
7	OE_nCS	I	Optional Pull-up/ Pull-down	I^2C Mode: Output Enable signal for all clock outputs when oe_sel is set to 0. Polarity, pull-up enable, and pull-down enable are controlled by the oe_pol, oe_pu, and oe_pd register fields, respectively. SPI Mode: Chip Select, active low.

Table 2. Pin Descriptions (Cont.)

Number	Name	Type		Description
8	SCL_SCLK	I	Optional Pull-up	I^2C Mode: I^2C interface bi-directional clock. SPI Mode: Serial Clock The pull-up enable is controlled by the scl_pu register field.
9	SDA_SDIO	I/O	Optional Pull-up	I^2C Mode: I^2C interface bi-directional data in open-drain mode. SPI Mode: Serial Data In and Out (3-wire) The pull-up enable is controlled by the sda_pu register field.
10	V_{DDD}	Power		Core digital function supply. 1.8V or 3.3V supported. Note that the digital power consumption is increased when operating above 1.8V (for information, see Power Considerations). OE_nCS, SCL_SCLK, and SDA_SDIO are referenced to this voltage.
11	nOUT3	O		Output Clock 3 negative.
12	OUT3	O		Output Clock 3 positive.
13	V_{DDO3}	Power		Supply voltage for output pair OUT3 and nOUT3. 1.8V supported. This pin can be left unconnected if clock output 3 is unused and the corresponding out_pd bit is set to 1.
14	nOUT2	O		Output Clock 2 negative.
15	OUT2	O		Output Clock 2 positive.
16	V_{DDO2}	Power		Supply voltage for output pair OUT2 and nOUT2. 1.8V supported. This pin can be left unconnected if clock output 2 is unused and the corresponding out_pd bit is set to 1.
17	nOUT1	O		Output Clock 1 negative.
18	OUT1	O		Output Clock 1 positive.
19	V_{DDO1}	Power		Supply voltage for output pair OUT1 and nOUT1. 1.8V supported. This pin can be left unconnected if clock output 1 is unused and the corresponding out_pd bit is set to 1.
20	OUT0	O		Output Clock 0 positive.
21	nOUT0	O		Output Clock 0 negative.
22	V_{DDO0}	Power		Supply voltage for output pair OUT0 and nOUT0. 1.8V supported. This pin can be left unconnected if clock output 0 is unused and the corresponding out_pd bit is set to 1.
23	V_{DDA}	Power		Analog function supply for core analog functions. 1.8V supported. LOCK is referenced to this voltage.
24	LOCK	O	See description	PLL lock status or other status as selected by lock_sel. Polarity, pull-up enable and pull-down enable are controlled by the lock_pol, lock_pu, and lock_pd register fields, respectively.
EPAD	V_{SS}	Power		Negative supply voltage. Epad must be connected before any positive supply voltage is applied.

Table 3. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLKIN		-	5	-	pF
		nCLKIN		-	5	-	pF
		XIN/REF		-	1.9	-	pF
		XOUT		-	170	-	pF
		OE_nCS		-	1.6	-	pF
		SCL_SCLK		-	8	-	pF
		SDA_SDIO		-	160	-	pF
R_{PULLUP}	Input Pull-Up Resistor	OE_nCS		51	54	57	kΩ
		SCL_SCLK		51	54	57	kΩ
		SDA_SDIO		51	54	57	kΩ
	Output Pull-Up Resistor	LOCK		51	54	57	kΩ
$R_{PULLDOWN}$	Input Pull-Down Resistor	CLKIN	en_HCSL = 1	44	50	57	kΩ
		nCLKIN		44	50	57	kΩ
		OE_nCS		51	54	57	kΩ
	Output Pull-Down Resistor	LOCK		51	54	57	kΩ
R_{OUT}[1]	Output Impedance	LOCK	V_{DDA} = 1.89V	30	43	70	Ω
		SDA_SDIO	V_{DDD} = 1.89V	48	49	50	Ω

[1] Output impedance for the clock outputs are provided in Table 21.

3. Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC32504A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
V_{DD33}	3.3V power supplies	V_{DDD}	-0.5	3.63	V
V_{DD18}	1.8V power supplies	V_{DDREF}, V_{DDXO}, V_{DDA}, V_{DDO3}, V_{DDO2}, V_{DDO1}, V_{DDO0}	-0.5	1.98	V
V_{IN}	Voltage on any input	CLKIN, nCLKIN	0	1.98	V
		XIN/REF[1]	0	2.75	V
		All other inputs	-0.5	3.63	V
I_{IN}	Differential Input Current	CLKIN, nCLKIN	-	±50	mA
I_O	Output Current - Continuous	OUT0/1/2/3	-	30	mA
		LOCK, SDA_SDIO	-	25	mA
	Output Current - Surge	OUT0/1/2/3	-	60	mA
		LOCK, SDA_SDIO	-	50	mA
T_{JMAX}	Maximum Junction Temperature		-	150	°C
T_S	Storage temperature		-65	150	°C
-	ESD - Human Body Model		-	2000	V
-	ESD - Charged Device Model		-	500	V

[1] This limit only applies to the XIN/REF input when being overdriven by an external signal. No limit is implied when this is connected directly to a crystal.

3.2 Recommended Operating Conditions

Table 5. Recommended Operating Conditions[1][2]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction temperature	-	-	125	°C
T_A	Ambient air temperature	-40	-	85	°C
V_{DDREF}	Supply Voltage for Input Clock Buffers and Dividers	1.71	1.8	1.89	V
V_{DDXO}	Supply Voltage for Crystal Oscillator	1.71	1.8	1.89	V
V_{DDA}	Supply Voltage for Analog Core	1.71	1.8	1.89	V
V_{DDD}	Supply Voltage for Digital Core[3]	1.71	1.8/3.3	3.465	V
V_{DDOx}[4]	Supply Voltage for Output Clock Driver and Divider[5]	1.71	1.8	1.89	V
t_{PU}	Power Up Time for V_{DDx} - for all supply voltages to reach minimum specified voltage (power ramps must be monotonic)[6]	0.05	-	5	ms

[1] It is your responsibility to ensure that device junction temperature remains below the maximum allowed.

[2] All conditions in this table must be met to ensure device functionality.

[3] Supports 1.8V ±5% or 3.3V ±5% operation, not a continuous range.

[4] V_{DDOx} represents any of V_{DDO3}, V_{DDO2}, V_{DDO1}, or V_{DDO0}.

[5] Currents for the outputs are shown in Table 13 as appropriate for the mode the individual output is operating in.

[6] This implies all supply rails must reach their minimum voltage within maximum T_{PU}.

3.3 Reference Clock Phase Jitter and Phase Noise

Table 6. Output Phase Jitter Characteristics[1][2]

Symbol	Parameter		Test Condition		Typical	Maximum	Unit
tjit(Φ)	Phase Jitter, RMS (Random)[3]		10kHz to 20MHz 78.125MHz Crystal[4]; Synthesizer Mode	106.25MHz	78	100	fs
				125MHz	73	100	fs
				156.25MHz	72	100	fs
				212.5MHz	71	100	fs
				312.5MHz	67	100	fs
tjit(Φ)	Phase Jitter, RMS (Random)[5]		10kHz to 20MHz 60MHz Crystal[6]; JA Mode Locked to 25MHz CLKIN	156.25MHz	105	130	fs
				245.76MHz	104	130	fs
				312.5MHz	101	130	fs
				322.265625MHz	104	130	fs
				491.52MHz	102	130	fs
				983.04MHz	101	130	fs
tjit(Φ)	Phase Jitter, RMS (Random)[7]		10kHz to 20MHz 156.25MHz Input[8]; Clock Generator Mode	125MHz	74	100	fs
				156.25MHz	73	100	fs
				312.5MHz	64	100	fs
Φ_{SSB}(100k)	Single Sideband Phase Noise	100kHz	156.25MHz input, Clock Generator Mode; All outputs enabled at 156.25MHz		-148	-	dBc/Hz
Φ_{SSB}(1M)		1MHz			-153	-	dBc/Hz
Φ_{SSB}(10M)		10MHz			-165	-	dBc/Hz
Φ_{SSB}(30M)		≥30MHz			-167	-	dBc/Hz
Φ_{SSB}(100)	Single Sideband Phase Noise	100Hz	60MHz Crystal, JA Mode with 25Hz loop bandwidth, 25MHz input from SMA-100; All outputs enabled at 156.25MHz		-103	-	dBc/Hz
Φ_{SSB}(1k)		1kHz			-113	-	dBc/Hz
Φ_{SSB}(10k)		10kHz			-132	-	dBc/Hz
Φ_{SSB}(100k)		100kHz			-140	-	dBc/Hz
Φ_{SSB}(1M)		1MHz			-154	-	dBc/Hz
Φ_{SSB}(10M)		10MHz			-164	-	dBc/Hz
Φ_{SSB}(30M)		≥30MHz			-166	-	dBc/Hz

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.

[4] APLL at 10.625GHz to allow for outputting common ETH/FC frequencies.

[5] Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.

[6] APLL at 9.8304GHz for 245.76MHz, 491.52MHz and 983.04MHz. APLL at 10.3125GHz for 156.25MHz, 312.5MHz, and 322.265625MHz.

[7] Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.

[8] Driven by output from ClockMatrix. APLL at 10GHz to allow for outputting common ETH frequencies.

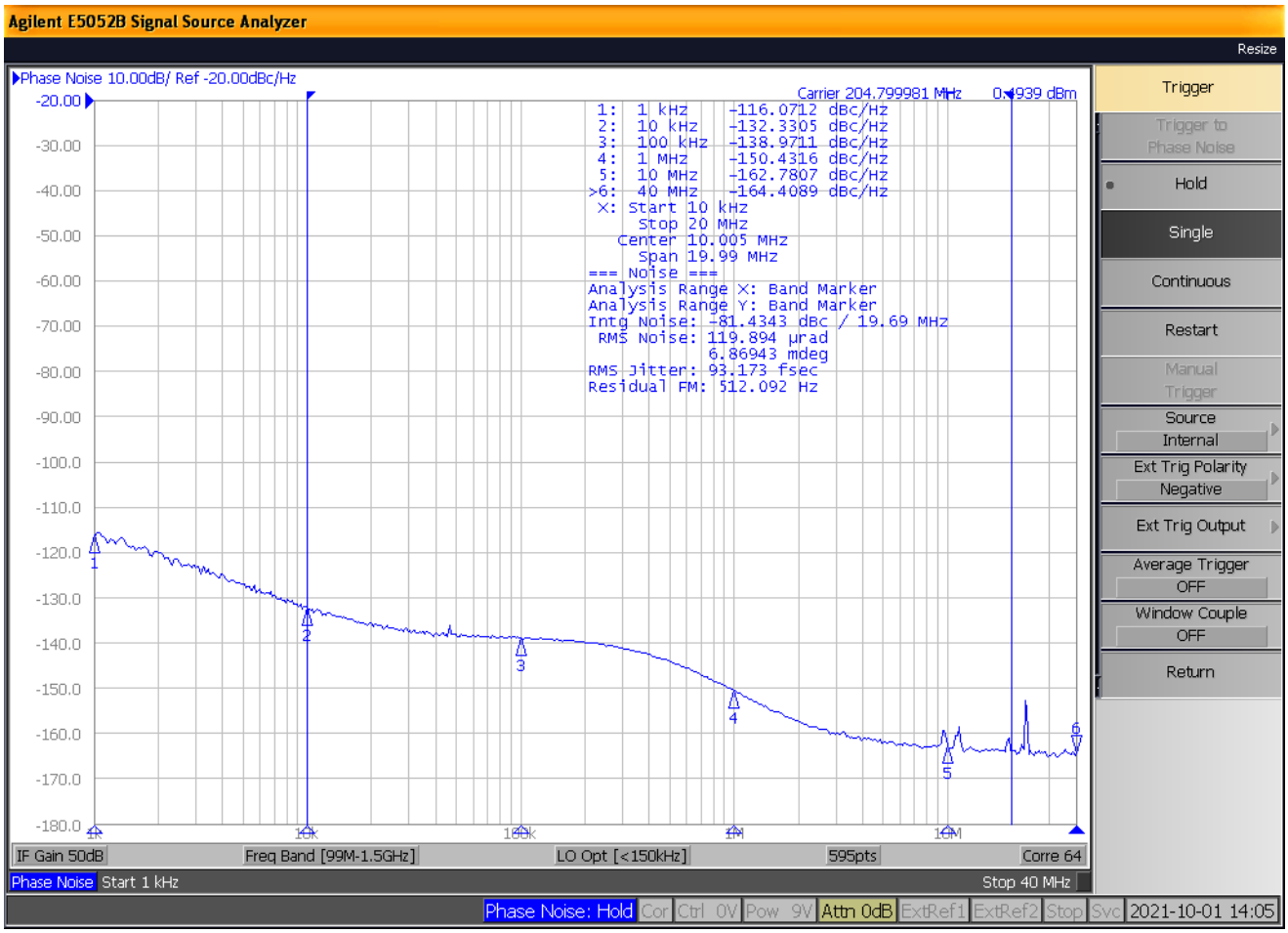


Figure 2. 204.8MHz Output with 93fs Jitter

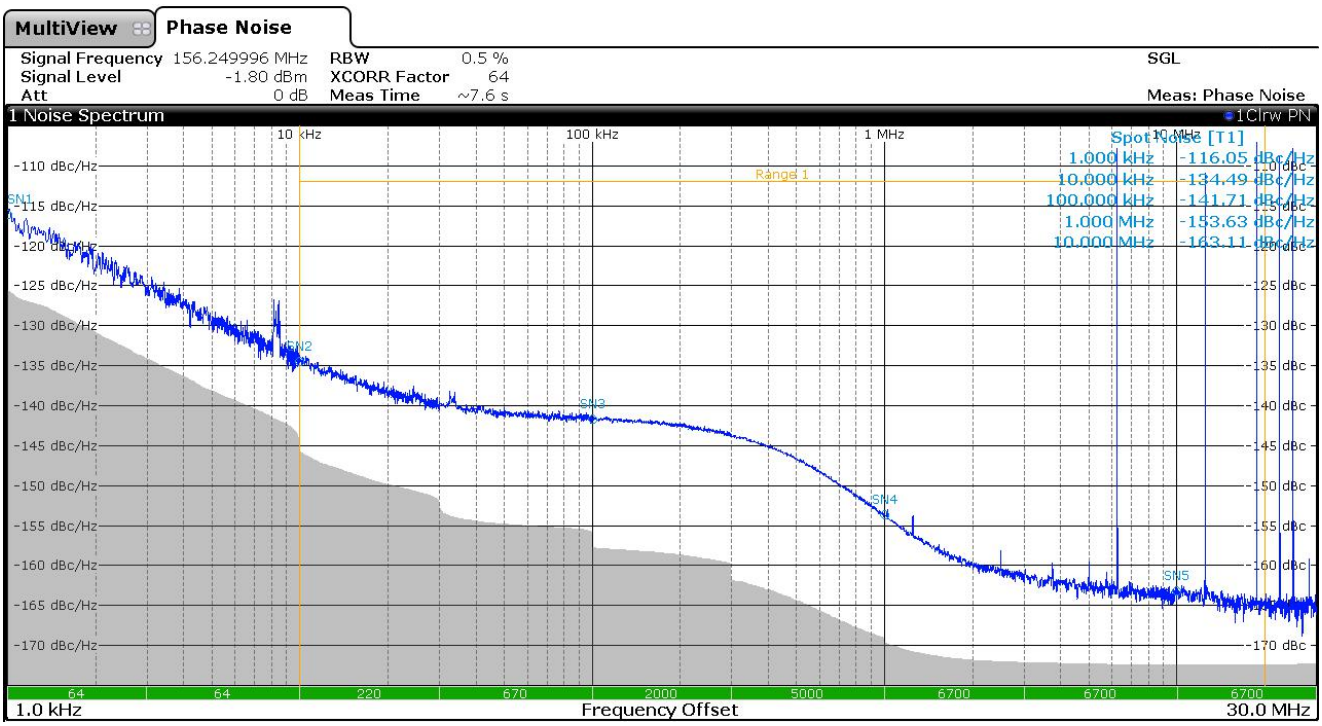


Figure 3. 156.25MHz Output Phase Noise – Fractional Jitter Attenuator Mode

Table 7. PCI Express Jitter Specifications[1][2]

Symbol	Parameter	Test Conditions	Typical	PCIe Industry Specification	Unit
$t_{jphPCIeG1-CC}$	PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen 1 (2.5 GT/s)[3][4]	0.836	86	ps (p-p)
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Lo Band (5.0 GT/s)[3][4]	0.014	3	ps (RMS)
		PCIe Gen 2 Hi Band (5.0 GT/s)[3][4]	0.055	3.1	ps (RMS)
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (8.0 GT/s)[3][4]	0.022	1	ps (RMS)
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (16.0 GT/s)[3][4][5]	0.029	0.5	ps (RMS)
$t_{jphPCIeG5-CC}$		PCIe Gen 5 (32.0 GT/s)[3][4][6]	0.008	0.15	ps (RMS)

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 5.0, Revision 1.0*. For the exact measurement setup, see the Test Loads section of the datasheet. The worst case results for each data rate are summarized in this table.

[4] Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a Real-Time Oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to a peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[5] In channel simulations to account for additional noise in a real system, 0.7ps RMS must be used.

[6] In channel simulations to account for additional noise in a real system, 0.25ps RMS must be used.

3.4 AC Electrical Characteristics

Table 8. Input Frequency Characteristics[1]

Symbol	Parameter		Test Condition	Minimum	Maximum	Unit
f_{XTAL}	Input Frequency for XIN/REF		Using a Crystal[2] (see Table 9)	25	80	MHz
			Over-driving Crystal Input[3] Doubler Logic Enabled	25	80	MHz
			Over-driving Crystal Input Doubler Logic Disabled	50	160	MHz
f_{CLKIN}	Input Frequency for CLKIN[4]		Clock Synthesizer Mode (Doubler Logic Disabled)	50	312.5	MHz
			Jitter Attenuator Mode - Differential Mode	1	800	MHz
			Jitter Attenuator Mode - Single-ended Mode	1	250	MHz
f_{SCLK}	Serial Port Clock SCL_SCLK	I^2C Operation	Slave Mode	100	1200	kHz
		SPI Operation	Slave Mode	0.1	20	MHz

[1] V_{DDXO} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C

[2] For crystal characteristics, see Table 9.

[3] Refer to Overdriving the XTAL Interface.

[4] For proper device operation, the input frequency must be divided down to f_{TDC} or less, see Table 10 for details.

Table 9. Crystal Characteristics[1]

Parameter	Test Condition	Minimum	Maximum	Unit
Mode of Oscillation		Fundamental		
Frequency		25	80	MHz
Equivalent Series Resistance (ESR)[2]	Crystal frequency ≤ 80MHz	-	80	Ω
Load Capacitance (C_L)	(see Crystal Recommendation)	8	12	pF
Drive Level	8pF Crystal	-	150	uW
	12pF Crystal	-	250	uW

[1] V_{DDXO} = 1.8V±5%, V_{SS} = 0V, T_A = -40°C to 85°C

[2] Measured ESR is always more than 2 × 80Ω.

Table 10. PLL Characteristics[1][2]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
f_{VCO}	Analog PLL VCO Operating Frequency			9.7	-	10.7	GHz
Δf_{OUT}	Output frequency tuning resolution		DCO Mode	$[2^{-40} \times 1e12] = 0.91$			ppt
f_{PFD}	Analog Phase/Frequency Detector (PFD) Operating Frequency		Integer VCO feedback	50	-	312.5	MHz
f_{TDC}	Digital Phase Detector (TDC) Operating Frequency			1	-	33	MHz
f_{MON}	Reference Monitor Operating Frequency	CLKMON0/1		-	-	33	MHz
		CLKMON2		-	-	312.5	MHz
$t_{startup}$	Start-up Time[3]	Internal OTP Start-up	Synthesizer mode	-	7	10	ms
			DPLL mode, with a loop bandwidth setting of 300Hz[4]	-	-	1	s

[1] $V_{DDXO} = V_{DDD} = V_{DDA} = V_{DDOx} = 1.8V \pm 5\%$, $V_{SS} = 0V$, $T_A = -40°C$ to $85°C$.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Measured from when all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.

[4] Start-up time depends on the actual configuration used. For more information on estimating start-up time, contact REA technical support.

Table 11. Output Frequency Characteristics[1][2]

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	Differential Output			10	-	1000	MHz
		LVCMOS Output			10	-	180	MHz
t_{SK}	Output to Output Skew[3][4]	Differential[5]	Any two outputs		-	40	45	ps
		LVCMOS[6]	Any OUTx to any other OUTx or any nOUTx to any other nOUTx		-	80	90	ps
			OUTx to nOUTx of the same output pair, configured in-phase		-	80	90	ps
Δt_{SK}	Temperature Variation[7] Output-Output				-	-	1	ps/°C
t_{PD}	Input to Output Skew[8] Differential[5] WRT CLKIN[9]		Delay for JA mode, integer DPLL feedback		760	860	960	ps
			Delay for JA mode, fractional DPLL feedback		810	910	1010	ps
			Delay for SYNTH mode		750	850	950	ps
Δt_{PD}	Input to Output Delay Variation Differential[5]		Any mode		-	-	±200	ps
t_R / t_F	Output Rise and Fall Times 20% to 80%	Differential Output[10]	HCSL Mode	SWING[11] = Any	-	-	120	ps
			LVDS Mode	SWING[12] = Any	-	-	180	ps
		LVCMOS Output[13]	V_{DDOx} = 1.8V ±5%		-	-	800	ps
odc	Output Duty Cycle	Differential Output	$f_{OUT} \le f_{VCO}$ / N; N = 10, 12, …		48	50	52	%
			$f_{OUT} \le f_{VCO}$ / N; N = 39, 41, …		48	50	52	%
			$f_{OUT} \le f_{VCO}$ / N; N = 11, 13, …37		45	50	55	%
		LVCMOS	Any frequency		45	50	55	%

[1] V_{DDXO} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.

[4] This parameter is defined in accordance with JEDEC Standard 65.

[5] Measured at the differential cross points.

[6] Measured at V_{DDOx} / 2.

[7] This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.

[8] Defined as the time between the output rising edge and the input rising edge that caused it.

[9] ClkIn was from Rhode and Schwarz SMA 100B Signal Generator.

[10] Measured with outputs terminated with 50Ω to GND.

[11] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[12] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

[13] Measured with outputs terminated with 50Ω to V_{DDOx} / 2.

Table 12. Power Supply Noise Rejection[1][2]

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection[3][4]	f_{NOISE} ≤1MHz	V_{DDOx} = 1.8V[5]	-105	-94	-	dBc
			V_{DDXO} = 1.8V	-95	-87	-	dBc
		f_{NOISE} ≤100kHz	V_{DDREF} = 1.8V	-95	-86	-	dBc
			V_{DDD} = 1.8V	-140	-114	-	dBc
		100kHz <f_{NOISE} ≤600kHz	V_{DDREF} = 1.8V	-140	-109	-	dBc
			V_{DDD} = 1.8V	-100	-96	-	dBc
		600kHz <f_{NOISE} ≤1MHz	V_{DDREF} = 1.8V	-155	-143	-	dBc
			V_{DDD} = 1.8V	-105	-99	-	dBc

[1] V_{DDXO} = V_{DDREF} = V_{DDA} = V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.

[3] 50mV peak-to-peak sine-wave noise signal injected on indicated power supply pin(s).

[4] Noise spur amplitude measured relative to 156.25MHz carrier.

[5] Excluding V_{DDOx} of the output being measured.

3.5 DC Electrical Characteristics

Table 13. Power Supply DC Characteristics - Supply Current[1][2][3]

Symbol	Parameter	Test Condition		Current Consumption		Unit
				Typ	Max	
I_{DDREF}	Supply Current for V_{DDREF}[4]	1.8V LVCMOS input		8	13	mA
		HCSL input (P_N_Diff_Sel = 0, en_HCSL = 1)		10		mA
		LVDS input (P_N_Diff_Sel = 1, en_LVDS = 1)		11		mA
		AC-coupled differential input		5.5		mA
I_{DDXO}	Supply Current for V_{DDXO}	V_{DDXO} = 1.89V		5.5	10	mA
I_{DDA}	Supply Current for V_{DDA}	V_{DDA} = 1.89V		129	150	mA
I_{DDD}	Supply Current for V_{DDD}	V_{DDD} = 1.89V		25	30	mA
		V_{DDD} = 3.465V		26		mA
I_{DDOx}[5]	Supply Current for V_{DDOx}[6][7]	HCSL Mode	SWING[8] = 200mV	31	50	mA
			SWING = 250mV	32		mA
			SWING = 300mV	33		mA
			SWING = 350mV	34		mA
			SWING = 400mV	35		mA
			SWING = 450mV	36		mA
			SWING = 500mV	37		mA
			SWING = 550mV	39		mA
			SWING = 600mV	40		mA
			SWING = 650mV	41		mA
			SWING = 700mV	42		mA
			SWING = 750mV	43		mA
			SWING = 800mV	44		mA
			SWING = 850mV	45		mA
			SWING = 875mV	45		mA
			SWING = 900mV	46		mA
		LVDS Mode	AMP[9] = 350mV	30	40	mA
			AMP = 400mV	31		mA
		Output Disabled		28	50	mA
		Output Hi-Z		26	30	mA
		LVCMOS Mode	In phase	34	45	mA
			Opposite phase	34		mA
			nOUTx Disabled	31	40	mA
			OUTx Disabled	31		mA

[1] Output current consumption is not affected by any of the core device power supply voltage levels.

[2] Internal dynamic switching current at maximum f_{OUT} is included.

[3] V_{SS} = 0V, T_A = -40°C to 85°C.

[4] Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.

[5] I_{DDOx} denotes the current consumed by each V_{DDOx} supply.

[6] V_{DDOx} = 1.89V.

[7] Measured with outputs unloaded.

[8] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[9] Refers to the output voltage (amplitude) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

Table 14. LVCMOS Status and Control Signal DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DDD} = 3.3V ±5%	2	-	V_{DDD} + 0.3	V
		V_{DDD} = 1.8V ±5%	0.65 × V_{DDD}	-	V_{DDD} + 0.3	
V_{IL}	Input Low Voltage	V_{DDD} = 3.3V ±5%	-0.3	-	0.8	V
		V_{DDD} = 1.8V ±5%	-0.3	-	0.35 × V_{DDD}	
I_{IH}	Input High Current	V_{IN} = V_{DDD} = V_{DDD} (max)	-	-	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V, V_{DDD} = V_{DDD} (max)	-75	-	-	µA
V_{OH}	Output High Voltage	V_{DDD} = 3.3V ±5% or 1.8V ±5% I_{OH} = -100µA	V_{DDD} - 0.2	-	-	V
		(LOCK Signal Only) V_{DDA} = 1.8V ±5% I_{OH} = -100µA	V_{DDA} - 0.2	-	-	V
V_{OL}	Output Low Voltage	V_{DDD} = 3.3V ±5% or 1.8V ±5% V_{DDA} = 1.8V ±5% I_{OL} = 100µA	-	-	0.2	V

[1] 3.3V characteristics in accordance with JESD8C-01, 1.8V characteristics in accordance with JESD8-7A.

[2] V_{SS} = 0V, T_A = -40°C to 85°C.

[3] Input specifications see signals SCL_SCLK, SDA_SDIO, OE_nCS. Output specifications see signals LOCK, SDA_SDIO (3-wire SPI).

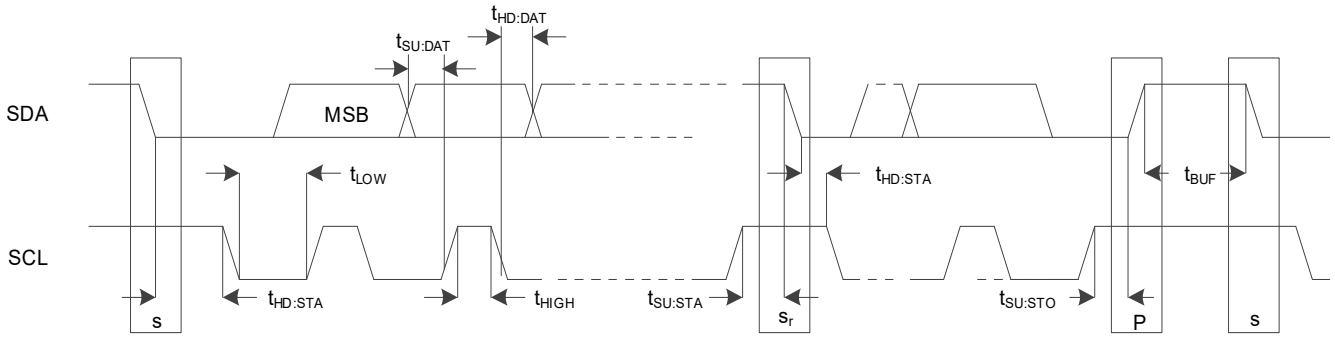


Figure 4. I²C Slave Timing Diagram

Table 15. I²C Slave Timing[1]

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD:STA}$	Hold time (repeated) START condition	4000	-	600	-	260	-	ns
t_{LOW}	LOW period of the SCL clock	4700	-	1300	-	500	-	ns
t_{HIGH}	HIGH period of the SCL clock	4000	-	600	-	260	-	ns
$t_{SU:STA}$	Set-up time for a repeated START condition	4700	-	600	-	260	-	ns
$t_{HD:DAT}$	Data hold time[2]	0[3]	-[4]	0[3]	-[4]	0	-	ns
$t_{SU:DAT}$	Data set-up time	250	-	100[5]	-	50	-	ns
$t_{SU:STO}$	Set-up time for STOP condition	4000	-	600	-	260	-	ns
t_{BUF}	Bus free time between a STOP and START condition	4700	-	1300	-	500	-	ns

[1] All values referred to V_{IH} (minimum) and V_{IL} (maximum) levels (see Table 14).

[2] $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, and applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] The maximum $t_{HD:DAT}$ could be 3.45µs and 0.9µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[5] A Fast mode I²C-bus device can be used in a Standard mode I²C-bus system, but the requirement $t_{SU:DAT}$ 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Table 16. I²C-Bus Characteristics

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	-	120	ns
t_f	Fall time of both SDA and SCL signals[1][2][3][4]	-	300	20 × (V_{DDD} / 5.5 V)	300	20 × (V_{DDD} / 5.5 V)[5]	120[4]	ns
C_D	Capacitive load for device on bus	-	5	-	5	-	5	pF

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[2] If mixed with Hs-mode devices, faster fall times are allowed.

[3] The maximum t_f for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_f is specified at 250ns, allowing series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[4] In Fast Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[5] Necessary to be backwards compatible to Fast mode.

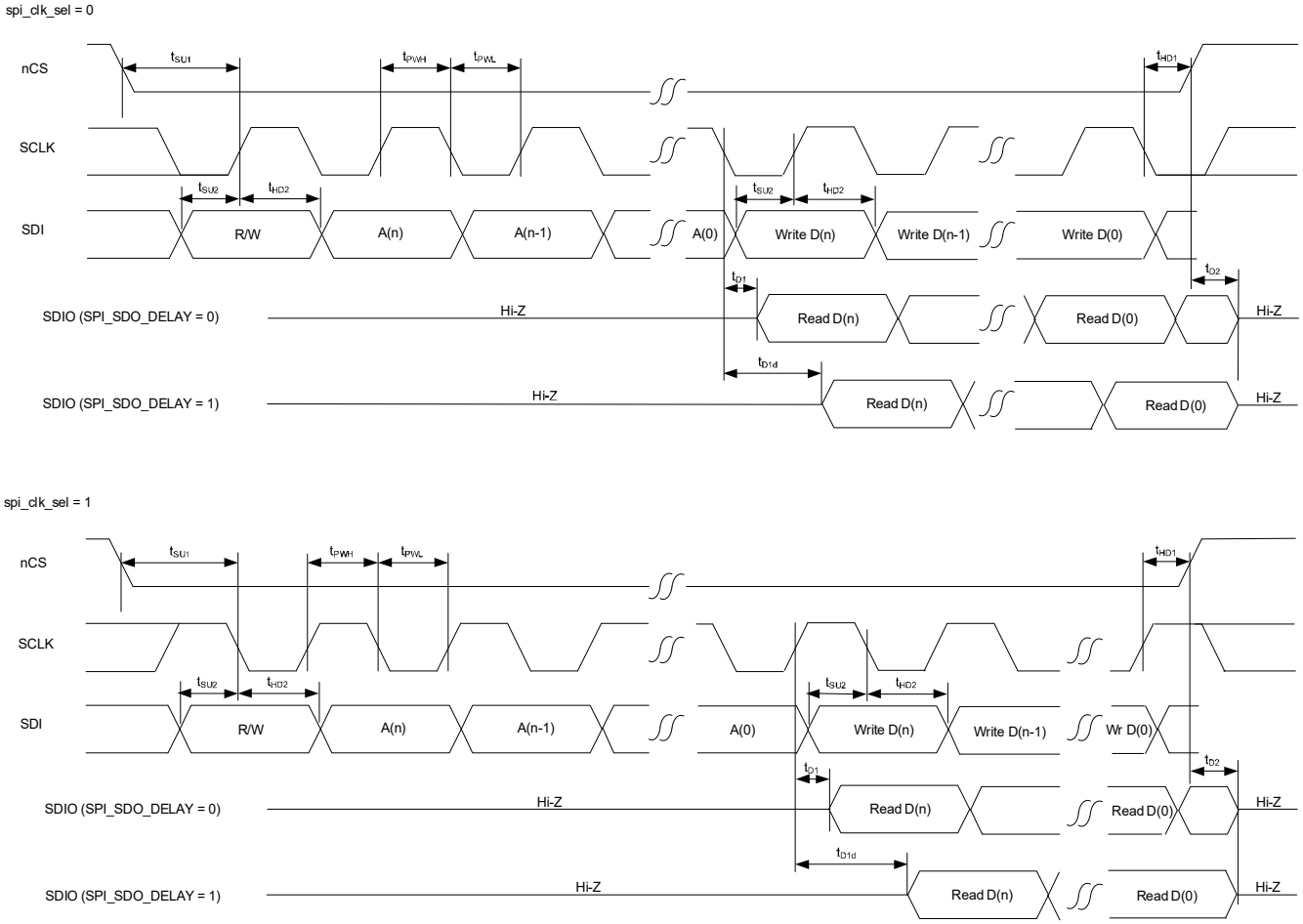


Figure 5. SPI Timing Diagram

Table 17. SPI Slave Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	-	-	20	MHz
t_{PWH}	SCLK Pulse Width High	25	-	-	ns
t_{PWL}	SCLK Pulse Width Low	25	-	-	ns
t_{SU1}	nCS Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{SU2}	SDIO Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD2}	SDIO Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{D1}	Read Data Valid Time from SCLK rising or falling edge with no data delay added	4	5.6	-	ns
t_{D1d}	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing[1]	t_{D1} + half SCLK period	-	-	ns
t_{D2}	SDIO Read Data Hi-Z Time from CS High[2]	-	10	-	ns

[1] Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.

[2] This is the time until the RC32504A releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

Table 18. Differential Clock Input DC Characteristics[1]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	CLKIN	V_{IN} = V_{DDREF} = V_{DDREF} (max)	-	-	100	µA
		nCLKIN		-	-	100	µA
I_{IL}	Input Low Current	CLKIN	V_{IN} = 0V	-50	-	-	µA
		nCLKIN		-50	-	-	µA
$V_{I(PP)}$	Peak-to-Peak Voltage[2][3][4]			0.15	-	1.2	V
V_{CMR}	Common Mode Input Voltage[2][4][5][6]		PMOS input buffer (HCSL, P_N_Diff_Sel = 0)	VI(PP) / 2	0.35	V_{DDREF} - 1.2	V
			NMOS input buffer (LVDS, P_N_Diff_Sel = 1)	0.7	1.2	V_{DDREF} - (VI(PP) / 2)	V

[1] V_{DDREF} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] V^{IL} should not be less than -0.3V.

[3] V_{PP} is the single-ended amplitude of the input signal. The differential specification is 2*V_{PP}.

[4] V_{DDREF} = 1.8V ±5%. Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.

[5] Common-mode voltage is defined as the cross-point.

[6] Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection. For example, when supplying an LVDS input signal that is referenced to a 2.5V supply at its source, the V_{DDREF} supply must also be 2.5V nominal voltage.

Table 19. LVCMOS Clock Input DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DDREF} = 1.8V ±5%	0.65 × V_{DDREF}	-	V_{DDREF} + 0.3	V
V_{IL}	Input Low Voltage	V_{DDREF} = 1.8V ±5%	-0.3	-	0.35 × V_{DDREF}	V
I_{IH}	Input High Current	VIN = V_{DDREF} = V_{DDREF} (max)	-	-	150	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-150	-	-	µA

[1] 1.8V characteristics in accordance with JESD8-7A.

[2] V_{SS} = 0V, T_A = -40°C to 85°C.

[3] Input specifications see both CLKIN and nCLKIN.

Table 20. Differential Clock Output DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{OUT}	Absolute Voltage on HCSL output	[4]	-125[5]	-	1150[6]	mV
V_{CROSS}	Absolute Voltage Output Crossing	HCSL Mode[7]	350	-	500	mV
ΔV_{CROSS}	Total Variation on HCSL output crossing over all edges[8]	[9]	-	30	100	mV

Table 20. Differential Clock Output DC Characteristics[1][2][3] (Cont.)

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
V_{OVS}[10]	Output Voltage Swing	HCSL Mode	SWING = 200mV[11]	195	-	250	mV
			SWING = 250mV	245	-	315	mV
			SWING = 300mV	295	-	380	mV
			SWING = 350mV	345	-	450	mV
			SWING = 400mV	395	-	520	mV
			SWING = 450mV	445	-	585	mV
			SWING = 500mV	495	-	645	mV
			SWING = 550mV	545	-	725	mV
			SWING = 600mV	595	-	780	mV
			SWING = 650mV	645	-	820	mV
			SWING = 700mV	685	-	855	mV
			SWING = 750mV	725	-	880	mV
			SWING = 800mV	755	-	915	mV
			SWING = 850mV	785	-	960	mV
			SWING = 875mV	810	-	1005	mV
			SWING = 900mV	825	-	1045	mV
		LVDS Mode	AMP = 350mV[12]	350	-	460	mV
			AMP = 400mV	365	-	500	mV
V_{CMR}	Output Common Mode Voltage	LVDS Mode[13]	CENTER = 700mV[14]	650	-	750	mV
			CENTER = 800mV	750	-	850	mV
			CENTER = 900mV	800	-	950	mV
			CENTER = 1000mV	900	-	1050	mV

[1] V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Terminated with 100Ω across OUTx and nOUTx.

[3] OUTx refers to any of the output pairs OUT3/nOUT3, OUT2/nOUT2, OUT1/nOUT1 or OUT0/nOUT0.

[4] Measurement taken from single-ended waveform.

[5] Defined as the minimum instantaneous voltage including undershoot.

[6] Defined as the maximum instantaneous voltage including overshoot.

[7] Terminated with 50Ω to GND on each of OUTx and nOUTx.

[8] Defined as the total variation of all crossing voltages of rising OUTx and falling nOUTx, This is the maximum allowed variance for any particular system.

[9] Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[10] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.

[11] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_hcsl_swing field for each output.

[12] Refers to the output voltage (swing) setting programed into device registers for each output using the ODRV_AMP_CNFG Register.out_cnf_lvds_amp field for each output.

[13] Terminated with 100Ω across OUTx and nOUTx.

[14] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output using the ODRV_MODE_CNFG Register.out_lvds_cm_voltage field for each output.

Table 21. LVCMOS Clock Output DC Characteristics[1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{DDOx} = ±100µA	V_{DDOx} - 0.2	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
Z_{OUT}	Output Impedance		41	51	67	Ω

[1] V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[2] Applies to any of OUT3, nOUT3, OUT2, nOUT2, OUT1, nOUT1, nOUT0, or OUT0.

[3] Output voltages compliant with JESD8-7A, Normal Range.

4. Applications Information

4.1 Power Considerations

For power and current consumption calculations, see the Renesas Timing Commander tool.

4.2 Recommendations for Unused Input and Output Pins

4.2.1 CLKIN/nCLKIN Input

For applications that do not require the use of the reference clock input, both CLKIN and nCLKIN should be left floating. If the CLKIN/CLKIN input is connected but not used by the device, Renesas recommends that both CLKIN and nCLKIN are not driven with active signals.

4.2.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

4.2.3 LVCMOS Outputs

Any LVCMOS output must be left floating if unused. There should be no trace attached. Set the mode of the output buffer to a high-impedance state to avoid any noise being generated.

4.2.4 Differential Outputs

All unused differential outputs must be left floating. Renesas recommends that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

4.3 Clock Input Interface

The RC32504A provides a programmable input buffer for reference clock inputs, as shown in Figure 6. This programmable buffer allows most standard signaling protocols to be supported with no need for external termination components at the receiver end of the transmission line.

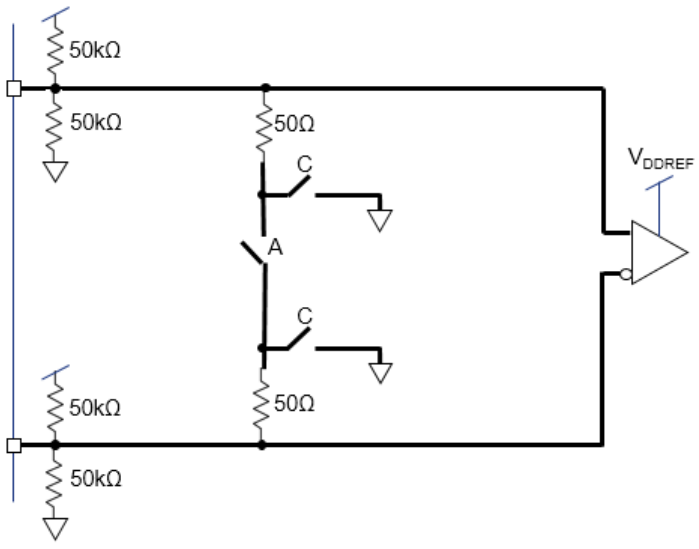


Figure 6. Programmable Input Buffer Logical Diagram

By making appropriate register selections, the switches labeled A and C in Figure 6 can be closed as shown in Table 22 to support the indicated protocols. With the switches closed as indicated, the input buffer behaves as shown in Figure 7 for the various input reference signal protocols.

Note: HCSL is sometimes used in an 85Ω transmission line environment and this input buffer supports that with no external terminations needed. However, this is not expected to be used often in RC32504A applications.

Table 22. Input Buffer Programming Options for Specific Signaling Protocols

Input Signaling Protocol	Register Setting	Switches Closed	V_{DDREF} Voltage Required
LVDS	REF_CLK_IN_CNFG Register.en_LVDS	A	1.8V
HCSL	REF_CLK_IN_CNFG Register.en_HCSL	C	1.8V[1]
1.8V LVCMOS	REF_CLK_IN_CNFG Register.CMOS_Sel	-	1.8V
Externally AC-coupled LVCMOS[2]	REF_CLK_IN_CNFG Register.en_selfbias_cmos	-	1.8V
Externally AC-coupled[2]	REF_CLK_IN_CNFG Register.en_dc_bias	-	1.8V

[1] Only a 1.8V V_{DDREF} is supported. If a higher VDD is used by the transmitter, then External AC-coupling must be used.

[2] In this mode of operation, AC-coupling capacitors must isolate the voltage level of the transmitter from the receiver. The signal must be properly termination on the transmitter side of the AC-coupling capacitors. No terminations are needed between the AC-coupling capacitors and the RC32504A.

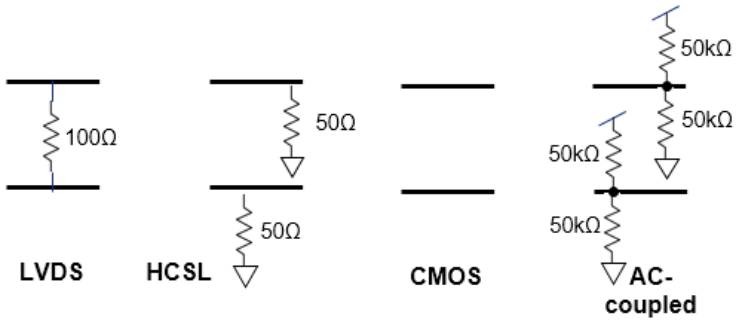


Figure 7. Input Buffer Behavior by Protocol

4.4 Crystal Recommendation

For the latest vendor and frequency recommendations, contact Renesas.

The RC32504A provides internal capacitors with programmable values to support tuning with the external crystal without the need for external tuning capacitors for most crystals (See Crystal Oscillator). With all the on-chip capacitance disabled (Tuning Capacitor registers are zero), the minimum load capacitance is 4.1pF. For recommended values for external tuning capacitors, see Table 23.

Table 23. Recommended Tuning Capacitors for Crystal Input

Crystal Nominal C_L Value (pF)	Recommended Tuning Capacitor Value (pF)[1]	
	XIN Capacitor (pF)	XOUT Capacitor (pF)
8	7.8	7.8
10	11.8	11.8
12	15.8	15.8
18[2]	21.8	21.8

[1] Recommendations are based on 4pF stray capacitance on each leg of the crystal. Adjust according to the PCB capacitance.

[2] This tunes the crystal to a C_L of 5pF, which is fine when channels are running in jitter attenuator mode or referenced to an XO. It presents a positive ppm offset for channels running exclusively in Synthesizer mode and referenced only to the crystal.

4.5 Overdriving the XTAL Interface

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 1.8V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 8. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing to prevent signal interference with the power rail and to reduce internal noise. For limits on the frequency that can be used, see Table 8.

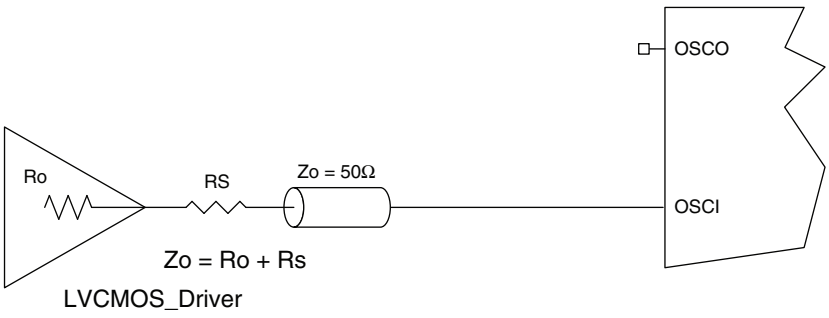


Figure 8. 1.8V LVCMOS Driver to XTAL Input Interface

Figure 9 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input attenuates the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

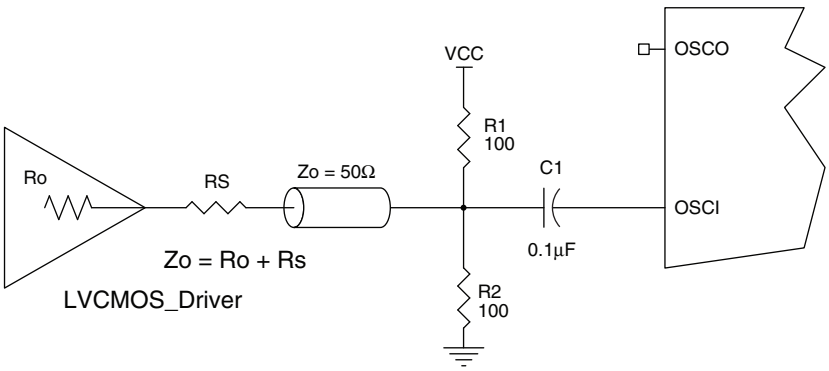


Figure 9. LVCMOS Driver to XTAL Input Interface

Figure 10 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. Renesas recommends placing all the components of the schematics in the layout. Though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and assured by using a quartz crystal as the input.

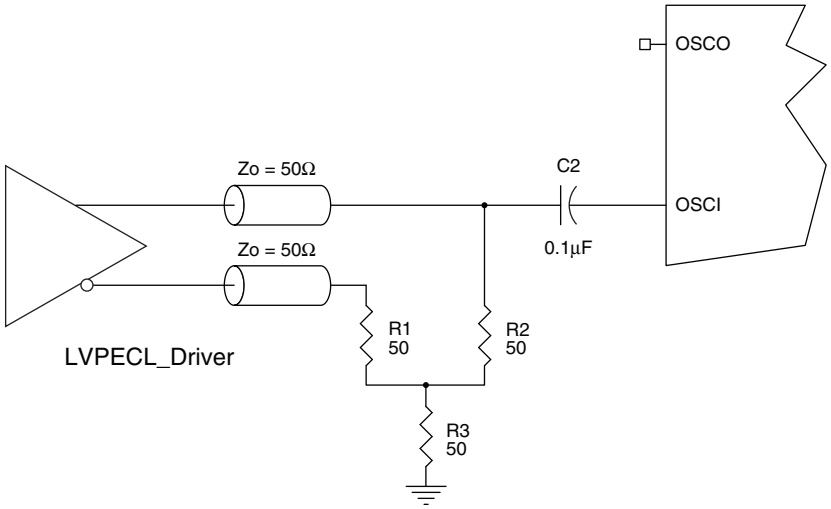


Figure 10. LVPECL Driver to XTAL Input Interface

4.6 Differential Output Termination

The RC32504A provides a programmable output buffer for clock outputs. This buffer allows most standard signaling protocols to be supported with no need for external termination components at the transmitter side of the transmission line.

Note: Many receivers of the type expected to be used with a high-performance device like RC32504A are equipped with internal terminations that can include trace termination, voltage biasing, and even AC-coupling in some cases. Consult with the receiver specifications to determine if any or all of the following indicated external components are needed.

4.6.1 Direct-Coupled HCSL Termination

For HCSL differential protocol, the following termination scheme is recommended (see Figure 11). A typical HCSL design uses a 50Ω resistor to ground at the receiver. The RC32504A supports source termination (see Figure 11), with an internal 50Ω resistor to ground at the transmitter. This is enabled by setting ODRV_MODE_CNFG Register.out_hcsl_term_en.

For alternate termination schemes, see HCSL Terminations in *Quick Guide - Output Terminations (AN-953)* located on the RC32504A product page, or contact Renesas for support.

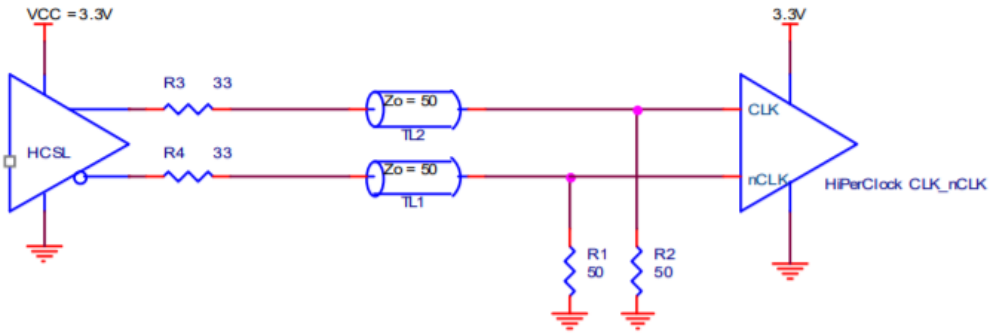


Figure 11. Standard HCSL Termination

4.6.2 Direct-Coupled LVDS Termination

For LVDS differential protocol, the following termination scheme is recommended (see Figure 12). The recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. To avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

For alternate termination schemes, see LVDS Terminations in *Quick Guide - Output Terminations (AN-953)* located on the RC32504A product page, or contact Renesas for support.

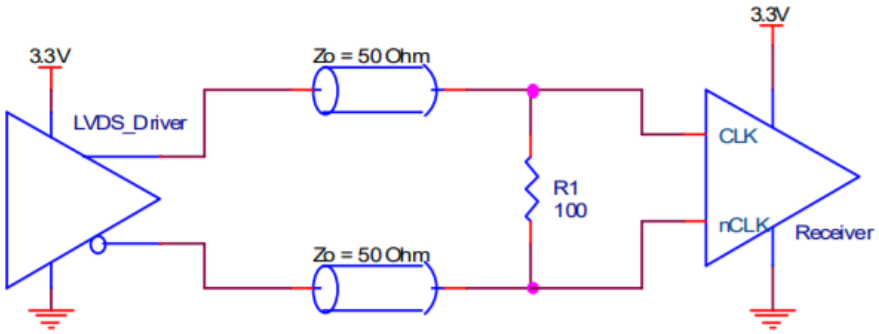


Figure 12. Standard LVDS Termination

4.6.3 AC-Coupled Differential Termination

For any other type of differential protocol, AC-coupling should be used as shown in Figure 13, which assumes a 100Ω differential transmission-line environment. The RC32504A should be programmed in HCSL mode when using AC-coupling, with an appropriate voltage swing selection for the receiver being driven. The device supports a wide range of programmable voltage swing options.

No terminations are needed between the RC32504A and the AC-coupling capacitors. Select the resistors on the receiver side of the AC-coupling capacitors to provide an appropriate voltage bias for the particular receiver. Consult receiver specifications for details. Finally, a 100Ω resistor across the differential pair, located near the receiver attenuates or prevents reflections that may corrupt the clock signal integrity.

It may also be useful to consult *Quick Guide - Output Terminations (AN-953)* located on the RC32504A product page, or contact Renesas for support.

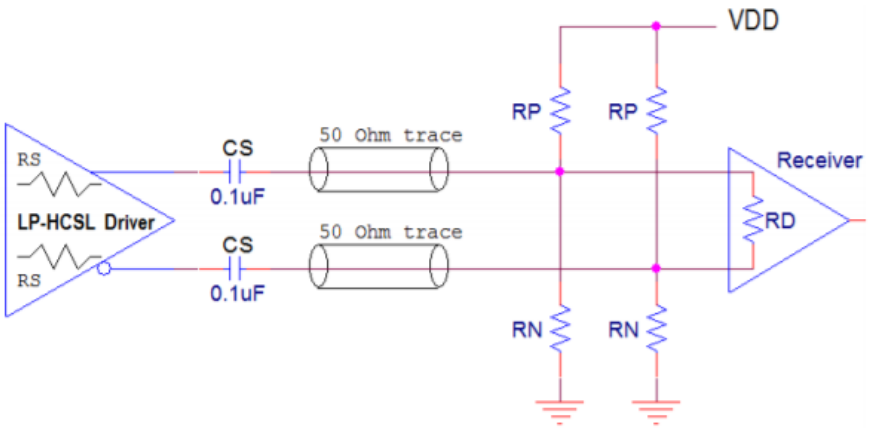


Figure 13. AC-Coupling Termination

5. Architecture

The detailed block diagram is shown in Figure 14. Blocks are described in the following chapter. The crystal shown is outside the RC32504A and connected using the XIN/REF and XOUT pins.

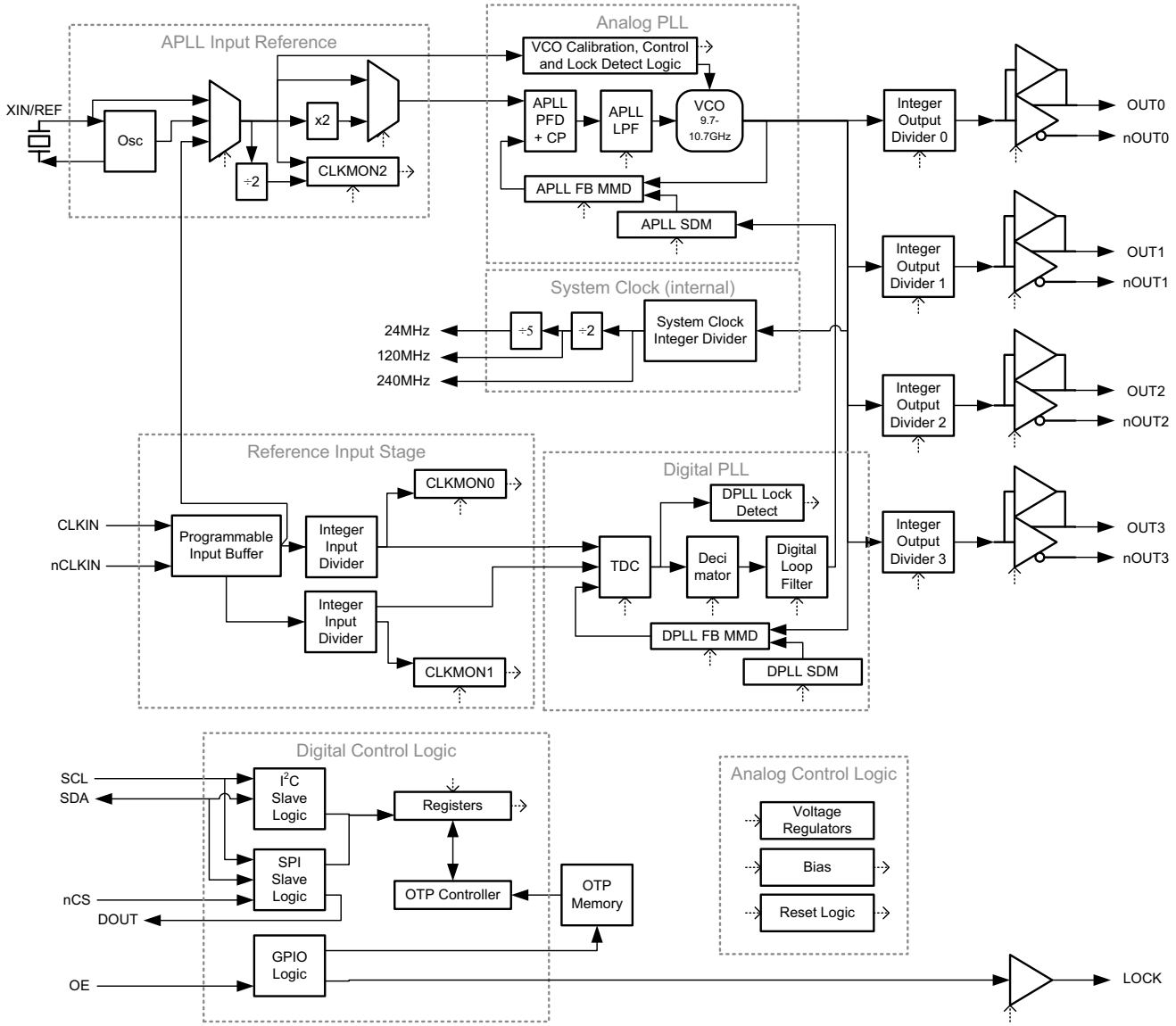


Figure 14. Detailed Block Diagram

5.1 Modes of Operation

5.1.1 Frequency Synthesizer/Digitally Controlled Oscillator (DCO)

When operating as a frequency synthesizer or DCO, the device receives its clock input from a crystal external to the device (XIN/REF) or from CLKIN and nCLKIN. The clock is multiplied-up internally to a high frequency using a fractional-feedback Analog PLL (APLL) that can generate a wide range of frequencies that are unrelated to the crystal frequency. The APLL frequency in turn is used by integer output dividers to generate several output frequencies that are related to each other, but unrelated to the crystal frequency.

In DCO mode, a frequency control word is passed directly from an external processor or FPGA to the fractional APLL. The frequency control word (specifying ppm offset) is written to the write_freq register. This value is scaled according to the APLL feedback divide ratio and then applied to the feedback divider.

A fixed frequency offset can be programmed to compensate for the initial frequency offset of the crystal, if known.

In these modes, the reference clock inputs are unused and the Digital PLL (DPLL) is bypassed. The DPLL logic can also be disabled to save power.

5.1.2 Jitter Attenuator/SyncE

When operating as a Jitter Attenuator (JA) or frequency translator, the single input reference clock drives a DPLL that monitors the fractional APLL output frequency and generates a phase error. That phase error is filtered by a programmable low bandwidth filter and applied to the fractional APLL.

In this mode, the frequency control word is not available.

The register settings default to select Synthesizer/DCO mode. To enable JA mode, the following mode bits must be set appropriately:

- en_inbuff
- out_startup
- lock_sel
- dpll_en

6. Blocks

6.1 Device Reset Logic

The Reset Logic holds all internal logic in reset from the initial ramping of the power supply pins until the on-chip voltage regulators have stabilized. After that it controls the sequence of bringing the individual logic blocks out of reset. For information, see Power-up Sequence.

6.1.1 Bias Calibration

The bias circuits provide precision reference voltages needed by other internal circuits. During the Power-up Sequence these undergo a calibration process. Completion of the calibration process sets bias_cal_done. If in the unlikely event there is an issue, it sets bias_cal_fail, and the startup sequence continues. You can read these bits using the serial port to confirm that the bias calibration succeeded. If bias calibration fails, contact Renesas for assistance.

6.2 Crystal Oscillator

The crystal oscillator (XO) supports a fundamental-mode parallel-resonant crystal from 25MHz to 80MHz connected on the pins XIN/REF and XOUT. The RC32504A provides internal capacitors with programmable values to support tuning with the crystal without the need for external tuning capacitors for most crystals. The internal capacitance applied at the crystal pins is configured by the en_cap_xin and en_cap_xout register fields.

6.3 Reference Clock Input

The reference clock input supports a differential clock supplied on the CLKIN/nCLKIN pins or a CMOS single-ended clock supplied on the CLKIN or nCLKIN pin. Differential vs single-ended operation is controlled by the CMOS_Sel register bit. When an externally AC-coupled clock is provided, the en_dc_bias register bit must be set to 1 for differential input or en_selfbias_cmos must be set to 1 for single-ended inputs. The input pad is disabled by default; when operating in Jitter Attenuator Clock Generator mode, it must be enabled by setting the en_inbuff register bit to 1.

In differential operation, the supported reference clock frequency range is 1MHz to 800MHz with a worst case duty cycle of 45/55%. In single-ended operation, the supported reference clock frequency range 1MHz to 250MHz.

6.4 Analog Phase Lock Loop

The Analog Phase Lock Loop (APLL) consists of a frequency doubler, a Phase-Frequency Detector (PFD), a Loop Filter (LPF), a Voltage-Controlled Oscillator (VCO), and a feedback divider. Renesas recommends using Renesas' Timing Commander software to provide optimized register setting recommendations for the APLL.

6.4.1 Frequency Doubler

The reference clock frequency is doubled using the frequency doubler before entering into the PFD, enabled by the en_doubler register bit.Reference clock selection to the frequency doubler, between the XO or CLKIN, can be set by the apll_ref_sel register bit.

6.4.2 APLL Loop Filter (LPF)

The LPF is a lead-lag filter with the topology shown in Figure 15. This circuit accepts the current from the PFD/CP circuit and provides the filtered control voltage to adjust the frequency of the VCO.

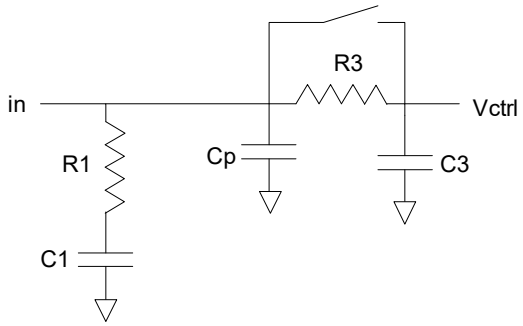


Figure 15. APLL LPF Topology

C1 has a fixed nominal capacitance of 1100 pF. The values of R1, Cp, R3, and C3 can be adjusted using the cnf_LPF_res, cnf_LPF_cp, cnf_LPF_R3, and cnf_LPF_C3 register fields, respectively. The switch bypassing the third pole is controlled by byp_p3, and can be enabled only when the APLL feedback divider is set to an integer value. All loop filter components are internal to the device.

The default effective bandwidth (BW) of the APLL is 365kHz.

6.4.3 Voltage-Controlled Oscillator (VCO)

The VCO is a quad-core LC VCO with a tunable frequency range of 9.7GHz to 10.7GHz across PVT. There is temperature compensation to allow the VCO frequency to remain stable across the operating temperature range regardless of the temperature at which calibration was performed.

6.4.4 APLL Feedback Divider

The APLL Feedback divider consists of two parts. The Multi-Modulus Divider (MMD) performs the actual division of the VCO frequency down to the nominal frequency needed to match the PFD input reference frequency (from frequency doubler). The MMD contains a number of integer divide ratios that are switched between under control of the Sigma-Delta Modulator (SDM) block. This allows a fractional divide ratio to be achieved while also providing noise shaping to minimize the spurs that switching would otherwise cause. The divide ratio is configured using the apll_fb_div_frac and apll_fb_div_int register fields.The fractional portion of the divide ratio is a 27-bit integer representing the numerator of an M/N fraction. The denominator is fixed at 2^{27}. It is recommended that fractions close to 0, 1, or 1/2 be avoided for best phase noise performance.

6.4.5 APLL Lock Detector

The analog lock detector indicates whether the APLL is locked to a input reference. The current lock status can be read in the apll_lock_sts register bit or reflected on one of the general purpose output pins (see GPIOs). The falling edge of the lock status sets the apll_lol event bit. This bit remains set until cleared by the user.

The lck_detect_ref_sel register field must be programmed according to the input reference frequency range.

6.4.6 Direct DCO Control

When the APLL is in Synthesizer mode, a frequency offset can be programmed using the write_freq register field. The frequency adjustment's LSB resolution is 2^{-40}, which translates to approximately 0.91ppt. An offset to compensate for the external crystal's initial frequency offset may be programmed by you in xtal_trim.

6.5 Reference Clock Outputs

6.5.1 Integer Output Divider (IOD)

There are four independent integer output dividers (IOD0/1/2/3), corresponding to the four differential output clocks, which divide the VCO frequency to the desired output frequency. The integer divide ratio is programmed in the outdiv_ratio register field.

When operating in differential mode, the output clocks support a continuous frequency range from 1MHz to 1000MHz. When operating in LVCMOS mode, the output clocks support a continuous frequency range from 1MHz to 180MHz.

The output clock disable (from the OE_nCS pin or out_dis; for details, see Clock Output Driver) acts synchronously to avoid glitches or runt pulses when disabling or enabling the output.

The maximum skew between any outputs configured for the same output type is shown in Table 11. This is achieved by:

- The output dividers and DPLL feedback divider are automatically synchronized after the PLL is configured on startup, and can be manually synchronized by writing the divider_sync register bit following reconfiguration. The output clocks are interrupted for 50µs to 300µs during synchronization, depending on the APLL re-lock time. On power-up, this interruption is hidden because the output drivers are not enabled until after it is complete. However on a manual synchronization command, this interruption is visible if the outputs are enabled.
- The delay in the clock fanout from the VCO to each divider is balanced to minimize output-output skew.

6.5.2 Clock Output Driver

There are four independent differential clock output drivers supporting receiver-only termination schemes using termination values of 100Ω across OUTx and nOUTx. The output type (HCSL, LVDS, or LVCMOS) is selected by the out_mode register field. The output swing level is selected by the out_cnf_hcsl_swing or out_cnf_lvds_amp register field depending on the output type. In HCSL mode, internal termination of 50Ω resistor to ground on both of OUTx and nOUTx can be enabled as configured by out_hcsl_term_en. In CMOS mode, one or both of OUTx and nOUTx can be active as configured by out_cmos_mode.

When output x is disabled, OUTx and nOUTx are held low by default. The disabled state can be set to low/high or tristate by setting the out_dis_state register field. When output x is enabled, OUTx and nOUTx operate normally.

If a clock output is unused, the corresponding out_pd register bit can be set to 1 to power down the output driver logic and tristate the outputs. While powered down, the output cannot be enabled and its output enable is ignored. If a clock output is never used, it can be powered down and the corresponding V_{DDOx} pin can be left unconnected.

6.5.3 Output Enable Control

During the Power-up Sequence, the clock output drivers are powered down (OUTx and nOUTx are tri-stated) until the power supplies have stabilized. Then the output drivers are powered up in the default disabled state (OUTx and nOUTx are both held low).

After the OTP configuration load completes, the clock output drivers can be held disabled until the APLL and/or DPLL locks according to the out_startup setting:

- Clock output drivers are disabled until APLL lock asserts
- Clock output drivers are disabled until DPLL lock asserts
- Clock output drivers are enabled immediately

The APLL/DPLL lock status no longer affects the clock output drivers, regardless of the out_startup setting.

After startup, the clock output drivers are then user-controllable using output enable control. When the oe_sel register bit is set to 1, each clock's output can be independently disabled by setting the corresponding out_dis register bit to 1, and enabled by setting out_dis to 0. When the oe_sel register bit is set to 0, de-assertion of the

OE_nCS input pin disables all powered-up clock output drivers. Assertion of OE_nCS enables the powered-up clock output drivers that are not disabled by their corresponding out_dis register bits. For more information on polarity and pull-up/pull-down control, see Output Enable.

6.6 DPLL

In jitter attenuator mode, the DPLL and APLL are nested and form a fractional-N PLL architecture. The APLL locks to an input clock from the crystal and generates an output clock of approx. 10GHz. The APLL uses a fractional feedback divider to generate its feedback clock. The fractional feedback divide ratio is dynamically controlled by the DPLL. The DPLL also uses the APLL's VCO clock to generate the fractional divided DPLL feedback clock. The DPLL fractional feedback clock divide ratio is static during normal operation. The DPLL must be enabled by setting the dpll_en register bit to 1.

In synthesizer/DCO modes, the unused DPLL logic may be disabled by setting the dpll_en register bit to 0. This saves power and avoids the creation of unnecessary noise within the device.

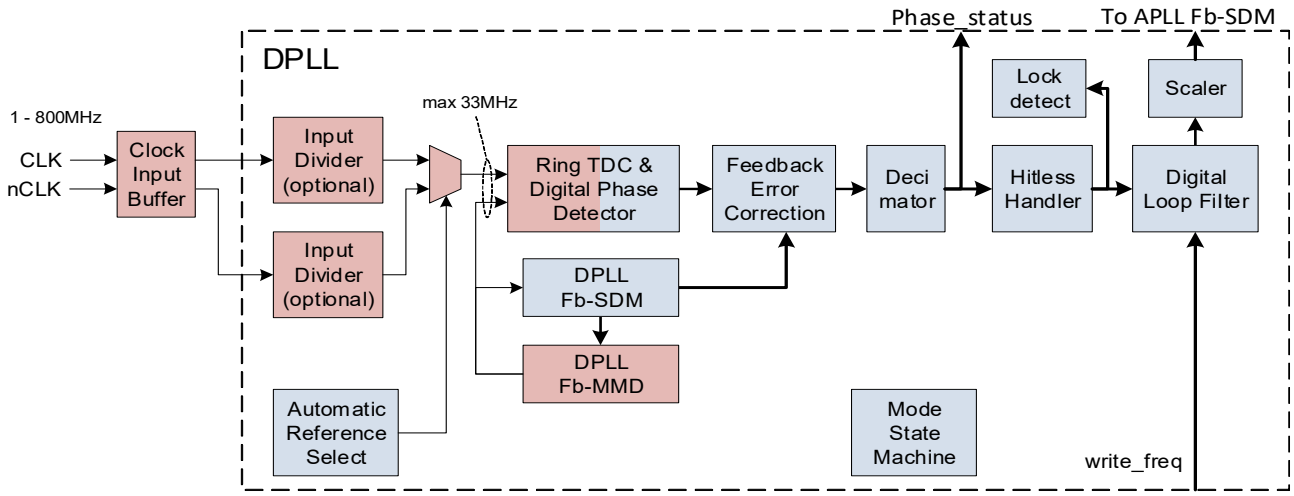


Figure 16. DPLL Block Diagram

6.6.1 Reference Clock Input Buffer

The CLKIN input buffer is designed to minimize or eliminate the need for external terminations and still support most common input clock signaling protocols. When operating in differential mode, it supports clocks up to 800MHz. When operating in single-ended LVCMOS mode, it supports clock rates up to 250MHz and the nCLKIN input can be used as a second reference clock.

6.6.2 Input Dividers

The TDC supports a maximum clock frequency of 33 MHz. If the reference clock frequency is higher than this limit, it must be divided down below the limit by the Input Divider. The integer divide ratio is controlled by the id_ratio register field, and the output is guaranteed to be 50/50 duty cycle.

6.6.3 DPLL Reference Selection

The DPLL can lock to the differential CLKIN input, or to either CLKIN or nCLKIN in single-ended mode.The reference selection can be either automatic or manual which is set by dpll_ref_sel_mode.

6.6.3.1 Manual Reference Selection

In manual mode, the reference is selected through the dpll_ref_sel field.

6.6.3.2 Automatic Reference Selection

In automatic mode, the selection is based on clock quality statuses and priorities. The quality statuses are from clock monitors. The priorities can be re-programmed in register ref_priority. If the two clock inputs are programmed to the same priority, the p CLK (CLK0) takes precedence,.

The automatic reference selection can either be revertive or non-revertive which is set in register dpll_revertive_en. In revertive mode, the reference clock that is qualified and of the highest priority is always selected. In non-revertive mode, if there is a higher priority reference clock coming back from disqualified to qualified, the current selected reference clock remains selected unless it gets disqualified.

6.6.3.3 Hitless Reference Switching

If hitless switching is enabled by setting register dpll_hitless_en to '1', the output clock initial phase hit is minimized (<200ps) during reference switching or the DPLL exiting from holdover, while the input clock and output clock may no longer be aligned.

If hitless is disabled, the output clock phase change slope is determined by DPLL loop characteristics and phase slope limit settings in register phase_slope_limit.

Hitless (<200ps) only can be met when the reference clocks are of same fractional frequency offset. If they are of different fractional frequency offset (up to ±244ppm), the output clock phase tracks to the new reference clock. Although the initial phase hit could be minimized by setting dpll_hitless_en to '1', the total amount of output phase change and the change slope depends on the fractional frequency offset difference, the loop characteristics, and phase slope limit settings.

When dpll_hitless_en is set to one and enabled, the phase_offset register is ignored by the DPLL and only the internally stored hitless offset affects the input-output phase offset. When dpll_hitless_en is set to zero and disabled, the hitless phase offset stored in the hitless handler is reset to zero and the phase_offset register is used again. Hitless switching minimizes the output phase movement at the expense of a defined input-output phase offset while the use of the phase offset register enables a defined input-output phase offset at the expense of output phase movement during reference switching. Defined input-output phase offset and minimizing output phase movement are mutually exclusive.

6.6.4 Digital Loop Filter

The digital loop filter is a Proportional - Integrator (PI) type filter as shown in Figure 17. It is programmable to a bandwidth of approximately 0.1Hz to 12kHz.

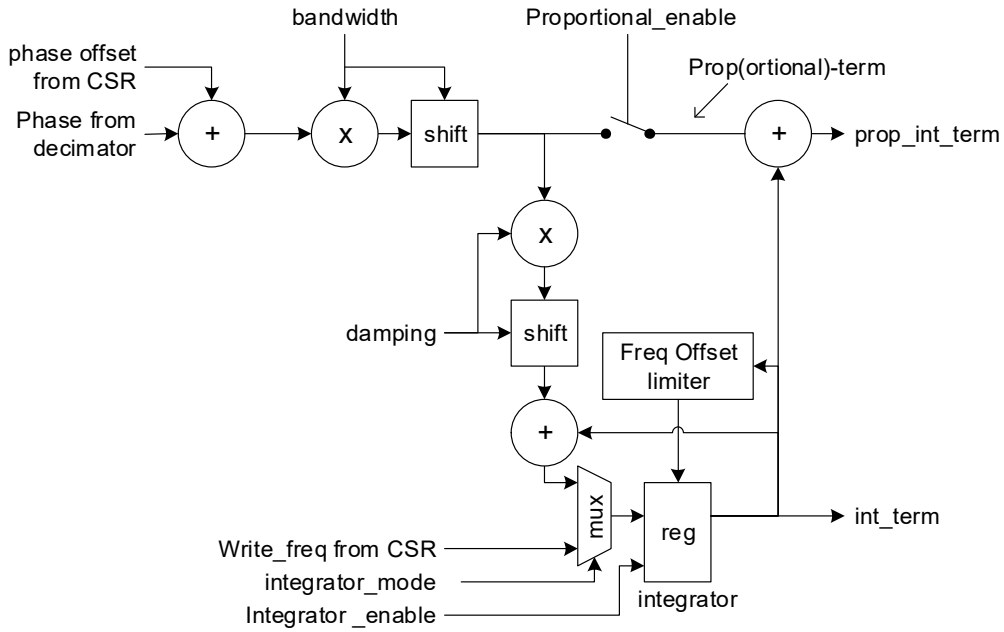


Figure 17. Loop Filter Block Diagram

The phase corrections are mainly done through the proportional path while the frequency offset is done in the integrator. The phase input can come from the phase detector/decimator and an offset from CSR. The phase value gets multiplied by a bandwidth factor. These are programmed in the normal_bw_mult and normal_bw_shift

register fields. Renesas's Timing Commander software can simplify the settings of these registers based on a target loop bandwidth.

The damping is set by another shifter and multiplier that attenuates the input to the integrator. The damping is programmable such that the frequency domain peaking ranges between 0.02 to 2.0 dB. These are programmed in the normal_damping_mult and normal_damping_shift register fields. Renesas's RICBox software can simplify the settings of these registers based on a target maximum gain peaking.

The integrator selects its input from either the damping shifter (in Jitter Attenuator mode) or the programmable Write Frequency (write_freq) register field (in Synthesizer or DCO modes).

When the DPLL is in Synthesizer/DCO mode, the Write Frequency register input is selected, the Proportional path is disabled, and the output frequency offset is purely the user-programmed value.

In Jitter Attenuator mode, if the Reference Monitors detects the selected reference to be invalid, the DPLL enters holdover mode (either temporarily while waiting to switch to the other reference, or indefinitely while waiting for a reference to become re-qualified). The DPLL may be forced into holdover mode or freerun mode by writing the dpll_mode register field to the Holdover or Freerun setting.

When the DPLL enters holdover mode, the integrator is no longer updated and the proportional path is disabled. That way the output frequency is purely based on the integrator value which represents the averaged fractional frequency offset of the input clock while still valid. The integrator range is limited to ±244 ppm.

When the DPLL enters freerun mode, the integrator is reset to zero and the proportional path is disabled. That way the output frequency is purely based on the APLL the apll_fb_div_int and apll_fb_div_frac registers.

Because of the lowest bandwidth of 0.1Hz, the required data width is 28 bits. The LSB resolution of the frequency adjustment is 2^{-40}, which translates to approximately 0.91ppt.

6.6.5 Lock Detector

The lock detector declares lock when the phase from the phase detector remains within a programmable range (dpll_lock_thresh) for a programmable time interval (dpll_lock_timer). This indicates that the DPLL is locked to the reference clock input. The current lock status may be read in the dpll_lock_sts register bit or reflected on one of the general purpose output pins (see GPIOs). The falling edge of the lock status sets the dpll_lol event bit. This bit remains set until cleared by you.

Two instances of the same scaler are used: one for the APLL feedback SDM and one for the system clock SDM.

6.6.6 DPLL Feedback Divider

The Feedback Divider is a multi-modulus divider which divides the APLL's output frequency of 9.7 to 10.7 GHz down to a frequency between 1MHz and 33MHz, to match the (pre-divided) reference clock. The divide ratio is dynamically controlled by the DPLL FB-SDM. The divided feedback clock has a phase error of up to 1 cycle of the APLL clock.

6.6.7 DPLL State Machine

The DPLL can work in 6 different states; Freerun, Acquire, Normal, Holdover, Hitless_switch and Write_frequency. The state selection and transitions can either be manual or automatic which is set in register dpll_mode. In manual mode, the states Freerun, Holdover and Write_frequency can be forced in the register dpll_mode.If the automatic/normal mode is selected, the state machine follows the state transitions in DPLL State Machine Diagram. The thick arrows in the state diagram indicate global state transitions that take priority over the thin state transition arrows.

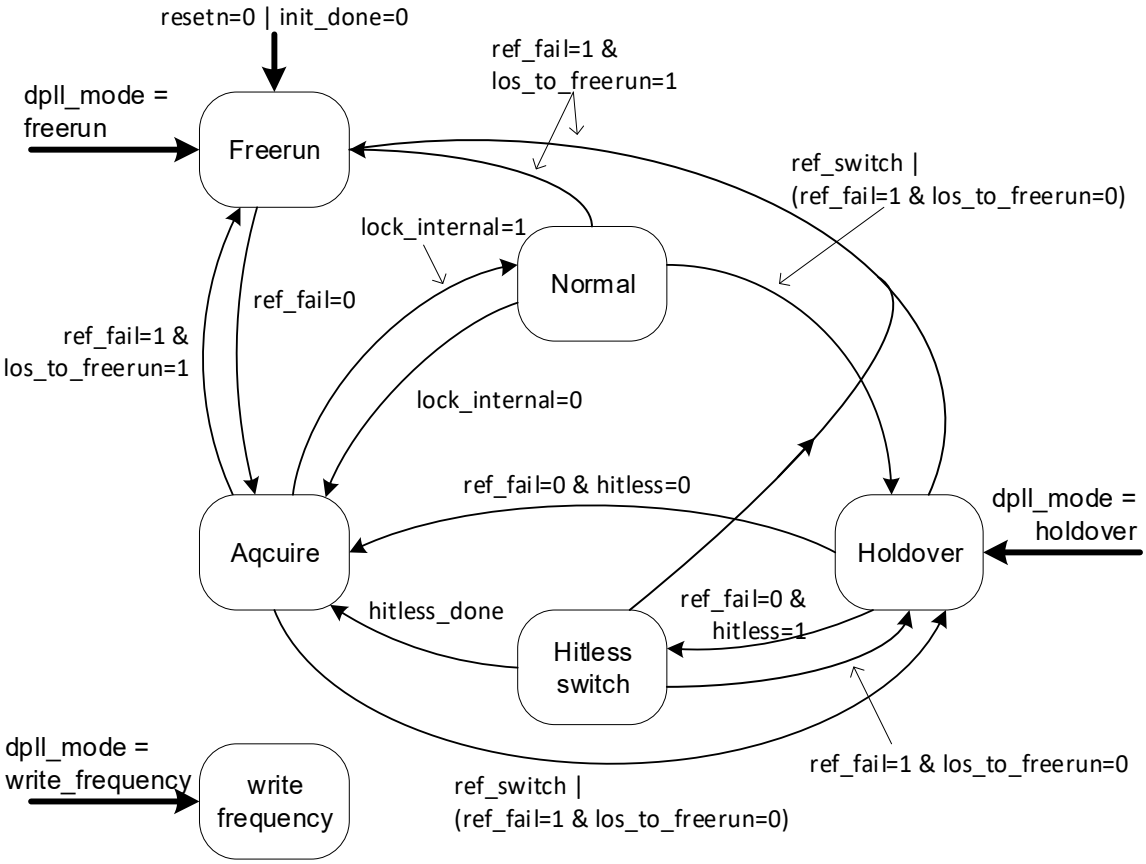


Figure 18. DPLL State Machine Diagram

6.6.7.1 Freerun

During power-up reset, VCO calibration or synthesizer mode, the DPLL is in the Freerun state. In this state, no reference clock is used and the output clocks are tracking the APLL reference clock (crystal). If init_done is low, the state machine goes in the Freerun state regardless of the value of dpll_mode.

6.6.7.2 Acquire

When there is at least one qualified reference, the DPLL is tracking the selected qualified reference clock with the acquisition bandwidth and damping settings.

If the reference clock is disqualified and no other qualified reference clock is available, the state machine goes either to the Freerun state or to the Holdover state dependent on the value of the CSR bit los_to_holdover.

When the lock-detector detects a lock, it reports the ‘locked’ status in the CSR and the state machine goes to the Normal state.

6.6.7.3 Normal

In this state, the DPLL is tracking the selected reference clock with the normal locking bandwidth and damping settings.

If the selected reference clock is disqualified or a reference switch occurs, state machine goes to the Holdover state.

6.6.7.4 Holdover

In this state, the DPLL frequency can be held at the instantaneous value or a value that is low pass filtered and/or restored from the holdover history registers. This can be selected through the CSR register DPLL_HOLDOVER_CNFG Register. The initial holdover accuracy is less than 1ppb.

6.6.7.5 Hitless Switch

At a hitless reference switch or a hitless transition from the Holdover state, the TDC of the DPLL measures the phase offset between the (newly) selected reference clock and the feedback clock. This offset is stored in the phase offset register. As a result, the output clocks experience a minimal phase transient because of the reference switch or coming out of Holdover. After the hitless switch procedure has finished, the state machine transitions to the Acquire state unless the reference clock fails.

6.6.7.6 Write Frequency

In this mode the DPLL is not tracking any reference clock. The DPLL output frequency offset is directly controlled by the value in the CSR write_freq register.

6.6.7.7 Manual Modes

The state machine can be forced to the Freerun, Holdover, and Write_frequency states by the CSR register dpll_mode. These state transitions are indicated by the thick arrows in the state diagram.

6.7 Reference Monitors

There is one reference monitor core for each reference. The monitor core consists of a short-term (Loss Of Signal) monitor and a medium-term (Activity) monitor.

- The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least 8 times that of the measuring clock period. The measuring clock period for the LOS monitor is the system clock.
- The activity monitor measures the reference over a nominal 10ms time window to achieve ~1ppm granularity with a ~216MHz measurement clock.

There are short-term clock monitors on the post-Input Divider reference clock inputs (LOSMON0 and LOSMON1) and the crystal clock input (LOSMON2). There are activity monitors only on the post-Input Divider reference clock inputs (ACTMON0 and ACTMON1).The implementation structure of the monitors are the same but with different configuration settings.

The LOS and Activity monitors nominal value should be programmed as follows:

- LOS monitor – sys_clk_2x / ref clock, where ref clock should be at least 8x less than sys_clk_2x for best results.
- Activity monitor – N / T, where N is the closest to 10ms that can be achieved with an integer number of monitored clock edges, and. T is the period of the measuring clock. The resulting accuracy of the measurement is T / N (for a nominal window of 10ms and a system clock of 108MHz, this means the accuracy is 0.926ppm).

6.7.1 Comparator

All monitors have both reject and accept threshold values that are all programmable in CSRs (los_nom_num, los_acc_margin, los_rej_margin, act_nom_num, act_acc_margin and act_rej_margin). The nominal value is compared with the nominal value +/- accept_margin or reject_margin.

When the counter value exceeds the reject threshold, the internal “failure counter” increments, and the internal “good counter” value resets it to 0. When the counter value is within the accept threshold, the “failure counter” resets to 0 and the “good counter” increments.

When the “good counter” reaches los_good_times for the LOS monitor, or the value of 1 for the Activity monitor, the monitor’s status (los_sts or act_sts) get cleared, indicating a valid reference.

When the “failure counter” reaches los_fail_times for the LOS monitor, or the value of 1 for the Activity monitor, the monitor’s status (los_sts or act_sts) get set, indicating an out-of-spec reference.

6.7.2 Alarm and Interrupt

The combinational OR of the LOS monitor’s los_sts and Activity monitor’s act_sts outputs are used to qualify/disqualify the reference, unless masked by los_fail_mask and act_fail_mask bits. It is also possible to force a reference to be disqualified by setting the ref_disable control bit.

When the status (los_sts or act_sts) changes from valid to invalid, the corresponding los_evt or act_evt bit gets set and can be cleared only by a CSR write, unless the underlying failing condition is still there, in which case the write does not take effect.

6.8 OTP

The RC32504A supports four user-definable, non-volatile start-up configurations stored in an internal OTP (one-time programmable) memory. Each configuration is capable of storing values for all write-able configuration registers. The configuration is selected by the values of the Configuration Select Pins latched at power-up. The serial interfaces are inactive until all register values specified in the selected configuration are written.

6.9 Serial Interfaces

I^{2}C or SPI operation is selected by the ssi_enable register field which defaults to I^{2}C mode. The serial interfaces are inactive until the OTP load completes during the power-up sequence.

6.9.1 Paging

You can choose to operate the serial port providing the full offset address within each burst, or to operate in a paged mode where part of the address offset is provided in each transaction and another part comes from an internal page register in each serial port. Figure 19 shows how page register and offset bytes from each serial transaction interact to address a register within the RC32504A.

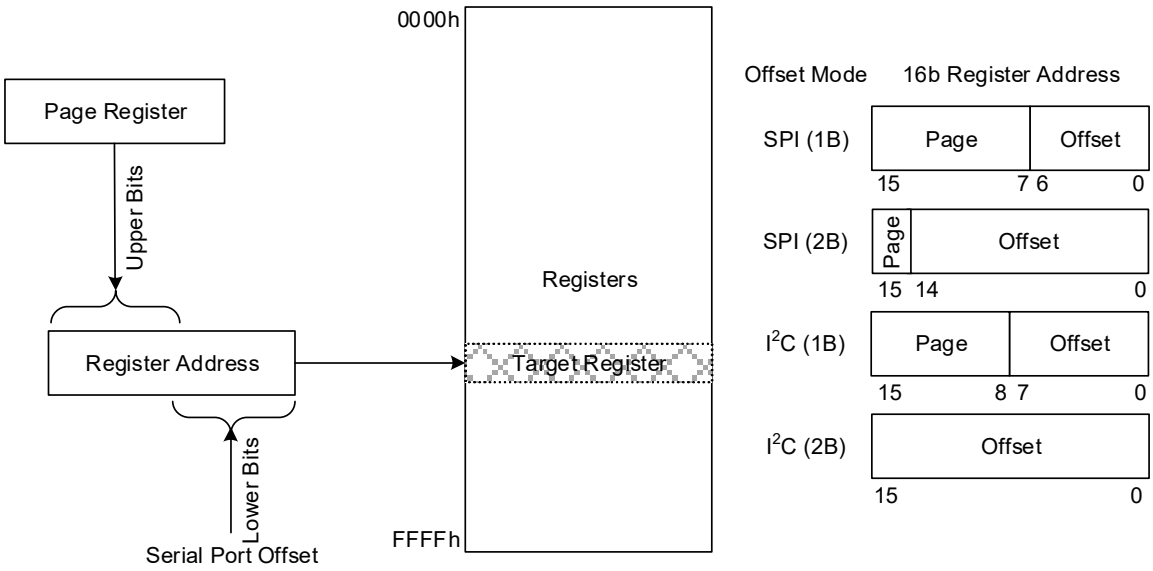


Figure 19. Register Addressing Modes Using Serial Port

6.9.2 I^{2}C Slave

The I^{2}C slave protocol of the RC32504A complies with the I^{2}C specification, version UM10204 Rev.6 – 4 April 2014. In the following description, SCL refers to the SCL_SCLK pin and SDA refers to the SDA_SDIO pin.

Figure 20 shows the sequence of states on the I^{2}C SDA signal for the supported modes of operation.

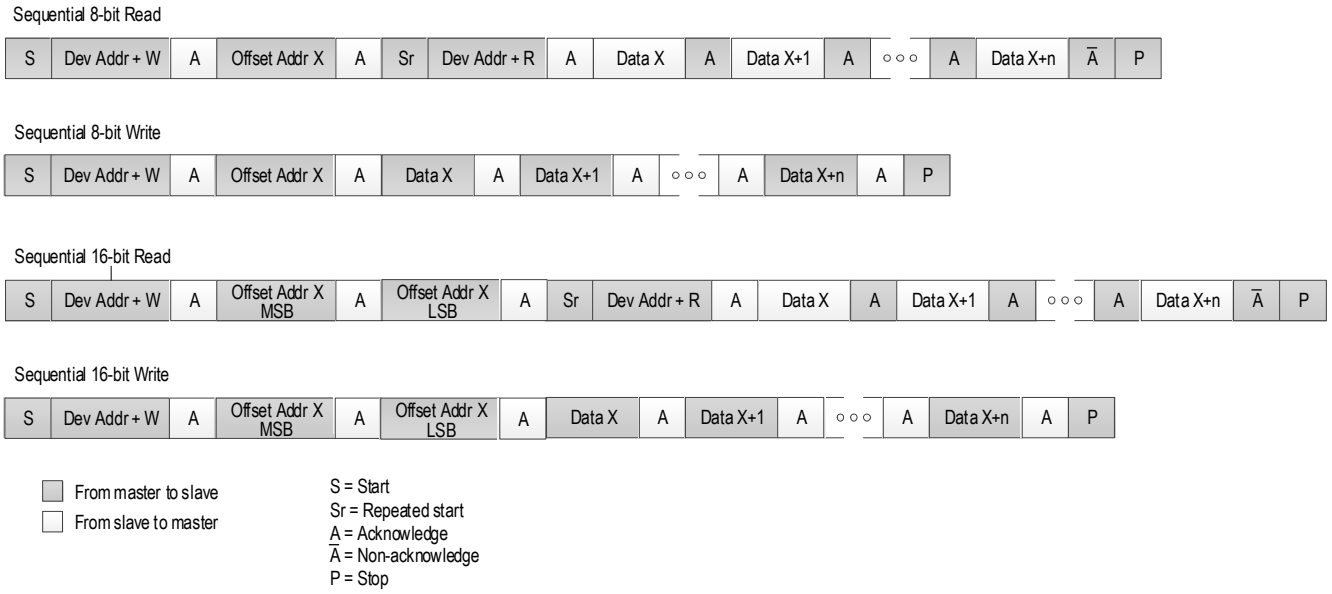


Figure 20. I²C Slave Sequencing

The Dev Addr shown in the figure represents the I²C bus address that the device responds to. This 7-bit value in the i2c_addr register field defaults to 0x09 if not programmed using the OTP load, or controlled through pins, as per Table 24.

The selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be configured using the ssi_addr_size register field. These offsets are used in conjunction with the page register to access registers internal to the device (see Figure 19). Because the I²C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8 bits of the register offset address come from the Offset Addr byte and the upper 8 bits come from the page register. The page register can be accessed at any time using an offset byte value of 0xFC. This 4-byte register must be written in a single-burst write transaction.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes.

Note: I²C burst mode operation is recommended to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I²C burst access. Bursts can be of greater length if required but must not extend beyond the end of the register page (Offset Addr 0xFF in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

Figure 4 and Table 15 show the detailed timing on the interface. 100kHz (Standard mode), 400kHz (Fast mode), and 1MHz (Fast mode Plus) operation are supported. The output slew rate is set according to the speed selected by the i2c_speed register field.

The I²C interface operating at 1MHz supports a DCO update rate of approximately 16k updates per second.

6.9.2.1 I²C 1-byte (1B) Addressing Example

RC32504A I²C 7-bit I²C address is 0x5B with LSB = R/W

Example write 0x50 to register 0xCBE4:

```
B6* FC 00 CB 00 00        #Set Page Register, *I2C Address is left-shifted one bit.
B6 E4 50                  #Write data 50 to CB E4
```

Example read from register 0xC024:

```
B6* FC 00 C0 00 00        #Set Page Register, *I2C Address is left-shifted one bit.
B6 24*                    #Set I2C pointer to 0xC024, *I2C instruction should use "No Stop"
B7 <read back data>       #Send address with Read bit set.
```

6.9.2.2 I²C 2-byte (2B) Addressing Example

RC32504A I²C 7-bit I²C address is 0x5B with LSB = R/W

Example write “50” to register 0xCBE4:

```
B6* FF FD 00 00 00        #Set Page Register, *I2C Address is left-shifted one bit.
B6 CB E4 50               #Write data to CB E4
```

Example read from register 0xC024:

```
B6* FF FD 00 00 00        #Set Page Register (*I2C Address is left-shifted one bit.)
B6 C0 24*                 #Set I2C pointer to 0xC024, *I2C instruction should use “No Stop”
B7 <read back data>       #Send address with Read bit set.
```

6.9.3 SPI Slave

In the following description, nCS refers to the OE_nCS pin, SCLK refers to the SCL_SCLK pin, and SDIO refer to the SDA_SDIO pin.

The RC32504A supports 3-wire SPI operation as a selectable protocol on the serial port. In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal.

When reading, a configurable number of dummy bytes can be read before the requested data byte(s) as controlled by the spi_dummy_en and spi_dummy_size register fields. When the SPI clock is faster than the system clock frequency divided by 4, at least 1 dummy byte must be enabled. Writes do not use dummy bytes.

Figure 21. SPI Sequencing

Figure 21 shows the sequencing of address and data on the serial port. The R/W bit is high for read cycles and low for write cycles. The read sequence is shown without dummy bytes (spi_dummy_en set to 0). If 1 dummy byte were enabled, then the data bits labeled Data byte from Address provided would be zero, the data bits labeled Data byte from Address + 1 would become Data byte from Address provided, and they would be followed by another 8 bits containing Data byte from Address + 1.

SPI operation can be configured for the following settings through register fields:

- 1-byte (1B) or 2-byte (2B) offset addressing (ssi_addr_size) (see Figure 19)
- In 1B operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed using an Offset Address of 0x7C with a 4-byte burst access.
- In 2B operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and the upper 1-bit is fixed to b'0.
- Data sampling on falling or rising edge of SCLK (spi_clk_sel)
- Output (read) data positioning relative to active SCLK edge (spi_del_out)

Note: SPI burst mode operation is recommended to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts can be of greater length if desired but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

SPI timing is shown in Figure 5 and Table 17.

The SPI interface operating at 20MHz supports a DCO update rate of approximately 400k updates per second.

6.9.3.1 SPI 1-byte (1B) Addressing Example

Example write to "50" to register 0xE4:

```
7C 80 00 00 00          #Set Page register
64* 50                  #*MSB is 0 for write transactions
```

Example read from 0x24:

```
7C 00 00 00 00          #Set Page register
A4* 00                  #*MSB is set, so this is a read command
```

6.9.3.2 SPI 2-byte (2B) Addressing Example

Example write to "50" to register 0xCBE4

```
4B E4* 50               #*MSB is 0 for write transactions
```

Example read from 0xC024:

```
C0* 24 00               #*MSB is set, so this is a read command
```

6.10 GPIOs

6.10.1 Lock Status

The LOCK output pin reflects one of these conditions as selected by the lock_sel register field:

- APLL lock
- DPLL lock
- Reference #0 loss-of-signal
- Reference #1 loss-of-signal
- Crystal loss-of-signal
- Reference #0 activity monitor status
- Reference #1 activity monitor status
- Reference #0 ref_invalid status
- Reference #1 ref_invalid status

- Device Interrupt (Refer to the device_int_sts register bit)
- Device ready (OTP load is complete and the serial port is active)
- Logic low
- Logic high

The polarity of LOCK is controlled by the lock_pol register bit. Internal pull-up resistors can be enabled by setting the lock_pu and the and pull-down resistors by enabling the lock_pd register bits. The output can be tri-stated by setting the lock_hiz register bit. LOCK can be configured as an open-drain output by setting the lock_od register bit.

The LOCK output driver is disabled until the OTP configuration load completes, allowing it to function as one of the Configuration Select Pins.

6.10.2 Output Enable

After the clock output drivers become user controllable during the startup sequence, the OE_nCS input pin controls the output enable of the output drivers if appropriately configured (for details, see Output Enable Control).

The polarity of the OE_nCS input is controlled by the oe_pol register bit. Internal pull-up resistors can be enabled by setting the oe_pu register bits and the pull-down resistors can be enabled by setting the oe_pd register bits.

The OE_nCS input also can function as one of the Configuration Select Pins.

6.11 Power-up Sequence

There are no power-up/down sequencing requirements on the power supply pins, or between the power supply pins and input signals. There are no external reset sequencing requirements.

After VCO calibration, the output dividers, APLL feedback divider and DPLL feedback divider are synchronized. The VCO output clock is gated, the divider resets are de-asserted, and the VCO output clock is ungated. Each divider outputs a rising edge on the first cycle of the VCO clock.

After the APLL locks (generally within 200us), the reference clock monitors are enabled.

In synthesizer/DCO mode, the enabled output drivers are set to normal operation and the output clocks begin to toggle. The power-up sequence is complete.

In JA mode, the DPLL is allowed to move to the Acquire state (by dpll_init_done) once the reference clock is qualified. After the DPLL locks, the enabled output drivers are set to normal operation and the output clocks begin to toggle. The power-up sequence is complete.

Setting the divider_sync register bit triggers the divider synchronization sequence and waits for the APLL to relock. The output drivers are disabled during this time.

Setting the apll_reinit bit restarts the power-up sequence from the VCO calibration step. The output drivers are disabled and are re-enabled after the APLL or DPLL locks as in the regular power-up sequence.

6.11.1 Configuration Select Pins

When the power-on-reset de-assets, the logic level of the following pins are latched into the gpio_at_startup register field:

- LOCK
- OE_nCS
- SDA_SDIO

A 2-bit index of the OTP user configuration is selected according to the config_sel register field (this field is intended to be written in the OTP Common Configuration), which determines the OTP user configuration to use.

The config_sel register also determines how the lower two bits of the I2C address (according to the i2c_addr register field) are selected, if applicable.

Table 24. OTP and I2C Address User Configuration Selection

config_sel[3:0]	Configuration Index [1]	Configuration Index [0]	I2C Address [1]	I2C Address [0]
0x0	0	0	i2c_addr[1]	i2c_addr[0]
0x1	0	1	i2c_addr[1]	i2c_addr[0]
0x2	1	0	i2c_addr[1]	i2c_addr[0]
0x3	1	1	i2c_addr[1]	i2c_addr[0]
0x4 (default)	OE_nCS	LOCK	i2c_addr[1]	i2c_addr[0]
0x5	SDA_SDIO	LOCK	i2c_addr[1]	OE_nCS
0x6	SDA_SDIO	OE_nCS	i2c_addr[1]	LOCK
0x7	SDA_SDIO	SCL_SCLK	i2c_addr[1]	i2c_addr[0]
0x8	0	LOCK	SDA_SDIO	OE_nCS
0x9	0	OE_nCS	SDA_SDIO	LOCK
0xA~F	Reserved			

The LOCK, SDA_SDIO and OE_nCS levels at power-up can be selected by connecting pull-up or pull-down resistors on the board. When I2C mode is selected, SCL_SCLK and SDA_SDIOmust have a pull-up resistor and should not be used for OTP configuration or I2C address selection.

If only two pin selectable user configurations are required, any one of the three inputs can be used as the select by programming two pairs of user configurations to use the same blocks, such that the value of the uncontrolled input pin is irrelevant. For example, to use only the LOCK pin, config_sel can be set to 0x8.

6.11.2 Divider Synchronization

The output dividers must be synchronized with each other to align the output clocks to the common multiple of their divide ratios.The DPLL feedback divider must be synchronized to provide a deterministic phase relationship between the input reference clock and the output clocks in JA mode; the input-to-output skew for a particular device configuration must be deterministic across PVT. Similarly, when the APLL reference is the input reference clock (selected by apll_ref_sel) in synthesizer mode, the APLL feedback divider must be synchronized to provide the deterministic input-to-output phase relationship. If the APLL reference is the crystal, synchronizing the APLL feedback divider is not necessary but causes the APLL to lose lock and re-lock; in JA mode, the DPLL also loses lock and relock.

6.11.2.1 Divider Synchronization Procedure

The Divider Sync Procedure is illustrated in Figure 22.

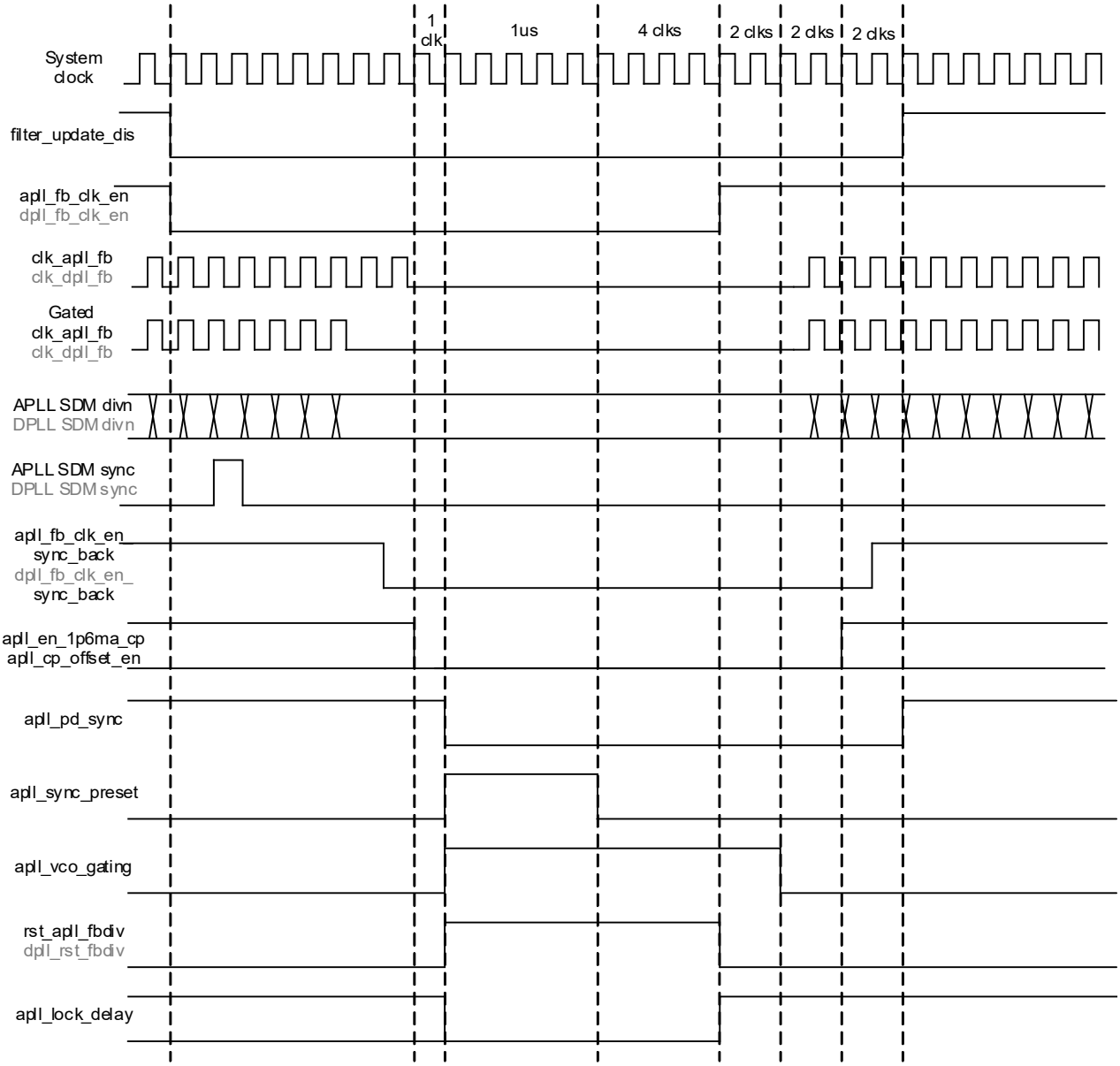


Figure 22. Divider Synchronization Procedure

6.11.3 Maximum PLL Lock Times

When operating in clock synthesizer mode, the maximum start-up and APLL lock time is 10ms. This is measured from the last voltage rail achieving nominal limits to the output clock being stable (no locking transients, no clock interruptions).

When in jitter attenuator mode, the maximum start-up and DPLL lock time is 1 second. This may be achieved by increasing the loop filter bandwidth while acquiring lock by setting bw_damp_sw to 1, and setting acquire_bw_shift, acquire_bw_mult, acquire_damping_shift and acquire_damping_mult to different values than normal_bw_shift, normal_bw_mult, normal_damping_shift and normal_damping_mult. Faster lock times can also be achieved by disabling the activity monitor for the input reference qualification.

7. Register Organization

7.1 Register Block Offsets

Table 25. Register Block Offset

Block Offsets	Block Name	Register Block Address Table Links	Register Block Description
0x00	GLOBAL	Global Block Register Offsets	GLOBAL Registers
0x20	INT	Interrupt Block Register Offsets	INT Registers
0x30	LOSMON[0]	LOS Monitor Block Register Offsets	LOSMON Registers
0x40	LOSMON[1]	LOS Monitor Block Register Offsets	LOSMON Registers[1]
0x50	LOSMON[2]	LOS Monitor Block Register Offsets	LOSMON Registers[1]
0x60	ACTMON[0]	ACT Monitor Block Register Offsets	ACTMON Registers
0x80	ACTMON[1]	ACT Monitor Block Register Offsets	ACTMON Registers[1]
0xA0	DPLL	DPLL Block Register Offsets	DPLL Registers
0xE0	TDC	TDC Block Register Offsets	TDC Registers
0xF0	SYSDIV	System Clock Divider Block Register Offsets	SYSDIV Registers
0xF4	BIAS	Bias Block Register Offsets	BIAS Registers
0xF8	XO	Crystal Block Register Offsets	XO Registers
0x100	OUT[0]	Clock Output Block Register Offsets	OUT Registers
0x108	OUT[1]	Clock Output Block Register Offsets	OUT Registers[1]
0x110	OUT[2]	Clock Output Block Register Offsets	OUT Registers[1]
0x118	OUT[3]	Clock Output Block Register Offsets	OUT Registers[1]
0x120	REF[0]	Clock Reference Addresses	REF Registers
0x124	REF[1]	Clock Reference Addresses	REF Registers[1]
0x130	GPIO	GPIO Block Register Offsets	GPIO Registers
0x140	SSI	SSI Block Register Offsets	SSI Registers
0x150	APLL	APLL Block Register Offsets	APLL Registers
0x190	INP	Clock Input Block Register Offsets	INP Registers
0x1D0	Rsvd	Reserved	-

[1] Register block functionality is the same, so the description is not duplicated.

7.2 Register Block Address Maps

7.2.1 Global Register Block Address Map

The Global Register block has a base address of 0x00. The addresses shown in Table 26 are offsets starting from this base address.

Table 26. Global Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	VENDOR_ID Register	Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.
0x02	hword	DEVICE_ID Register	Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.
0x04	hword	DEVICE_REV Register	Device revision identification information. Address map for this block of registers: Global Block Register Offsets.
0x06	hword	DEVICE_PGM Register	Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.
0x08	byte	DEVICE_CNFG Register	Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.
0x0A	byte	DEV_RESET Register	Device reset commands. Address map for this block of registers: Global Block Register Offsets.
0x0C	hword	SW_RESET Register	Software reset command. Address map for this block of registers: Global Block Register Offsets.
0x0E	hword	CLOCK_GATE Register	Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas if further details are needed.
0x10	byte	DEVICE_STS Register	Device status. Address map for this block of registers: Global Block Register Offsets.

7.2.2 Interrupt Register Block Address Map

The Interrupt block has a base address of 0x20. The addresses shown below are offsets starting from this base address.

Table 27. Interrupt Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	INT_EN Register	Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.
0x02	hword	INT_STS Register	Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

7.2.3 Loss of Signal Monitor Register Block Address Map

The LOS Monitor 0 block has a base address of 0x30. The LOS Monitor 1 block has a base address of 0x40. The LOS Monitor 2 block has a base address of 0x50. The addresses shown below are offsets starting from this base address. Note that before reprogramming a Loss of Signal Monitor block, the corresponding losmon0_sw_rst, losmon1_sw_rst, or losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

Table 28. LOS Monitor Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	LOSMON_STS Register	LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x01	byte	LOSMON_EVENT Register	LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x02	byte	LOSMON_QUAL Register	LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x04	hword	LOSMON_WINDOW Register	LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x08	word	LOSMON_THRESH Register	LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x0C	word	LOSMON_NOMINAL Register	LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

7.2.4 Activity Monitor Register Block Address Map

The ACT Monitor 0 block has a base address of 0x60. The LOS Monitor 1 block has a base address of 0x80. The addresses shown below are offsets starting from this base address. Note that before reprogramming an Activity Monitor, the corresponding actmon0_sw_rst or actmon1_sw_rst bit should be set. Once programming is done, it should then be cleared.

Table 29. ACT Monitor Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	ACTMON_STS Register	Activity Monitor Status. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x01	byte	ACTMON_EVENT Register	Activity Monitor Event Status. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x04	word	ACTMON_WINDOW Register	Activity Monitor Window Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x08	dword	ACTMON_THRESH Register	Activity Monitor Threshold Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x10	word	ACTMON_NOMINAL Register	Activity Monitor Nominal Number Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

7.2.5 DPLL Register Block Address Map

The Digital PLL block has a base address of 0xA0. The addresses shown below are offsets starting from this base address.

Table 30. DPLL Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	DPLL_REF_FB_CNFG Register	DPLL Ref and Fb Clock Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x01	byte	DPLL_MODE Register	Digital PLL mode control. Address map for this block of registers: DPLL Block Register Offsets.
0x02	byte	DPLL_DECIMATOR Register	Decimator configuration control. Address map for this block of registers: DPLL Block Register Offsets.
0x03	byte	DPLL_TRIM_OFFSET Register	DPLL Crystal trim offset. Address map for this block of registers: DPLL Block Register Offsets.
0x04	hword	DPLL_HOLDOVER_CNFG Register	Holdover Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x06	hword	DPLL_BANDWIDTH Register	DPLL Bandwidth configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x08	hword	DPLL_DAMPING Register	DPLL Damping control. Address map for this block of registers: DPLL Block Register Offsets
0x0C	word	DPLL_PHASE_SLOPE_LIMIT Register	DPLL Phase Slope Limit control. Address map for this block of registers: DPLL Block Register Offsets
0x10	dword	DPLL_FB_DIV_NUM Register	DPLL Feedback Fraction Numerator value. Address map for this block of registers: DPLL Block Register Offsets.
0x18	dword	DPLL_FB_DIV_DEN Register	DPLL Feedback Fraction Denominator value. Address map for this block of registers: DPLL Block Register Offsets.
0x20	hword	DPLL_FB_DIV_INT Register	DPLL Feedback Integer value. Address map for this block of registers: DPLL Block Register Offsets.
0x22	hword	DPLL_FB_CORR Register	DPLL Feedback Correction Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x24	word	DPLL_PHASE_OFFSET Register	DPLL Phase Offset configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x28	word	DPLL_WRITE_FREQ Register	DPLL Write Frequency command. Address map for this block of registers: DPLL Block Register Offsets.
0x2C	word	DPLL_LOCK Register	DPLL Lock Detection control. Address map for this block of registers: DPLL Block Register Offsets.
0x30	byte	DPLL_TDC_DELAY Register	DPLL TDC Delay Control. Address map for this block of registers: DPLL Block Register Offsets.
0x31	byte	DPLL_STS Register	DPLL Status. Address map for this block of registers: DPLL Block Register Offsets.
0x32	byte	DPLL_EVENT Register	DPLL Event status. Address map for this block of registers: DPLL Block Register Offsets.
0x33	byte	DPLL_LOL_CNT Register	DPLL Loss-of-Lock Event Counter. Address map for this block of registers: DPLL Block Register Offsets.
0x34	word	Reserved	Reserved
0x38	word	Reserved	Reserved
0x3C	byte	Reserved	Reserved

7.2.6 TDC Register Block Address Map

The TDC block has a base address of 0xE0. The addresses shown below are offsets starting from this base address.

Table 31. TDC Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	Reserved	Reserved
0x02	byte	TDC_REF_DIV_CNFG Register	TDC reference divider control. Address map for this block of registers: TDC Block Register Offsets.
0x03	byte	TDC_FB_SDM_CNFG Register	TDC internal APLL Feedback Divider SDM control. Address map for this block of registers: TDC Block Register Offsets.
0x04	byte	TDC_FB_DIV_INT Register	TDC internal APLL Feedback Divider Integer value. Address map for this block of registers: TDC Block Register Offsets.
0x06	hword	TDC_FB_DIV_FRAC Register	TDC internal APLL Feedback Divider Fraction value. Address map for this block of registers: TDC Block Register Offsets.
0x0A	byte	TDC_DAC_CNFG Register	TDC internal APLL Digital to Analog Converter (DAC) control. Address map for this block of registers: TDC Block Register Offsets.

7.2.7 System Clock Divider Register Block Address Map

The System Clock Divider block has a base address of 0xF0. The addresses shown below are offsets starting from this base address.

Table 32. System Clock Divider Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SYS_DIV_INT Register	System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

7.2.8 Bias Register Block Address Map

The Bias block has a base address of 0xF4. The addresses shown below are offsets starting from this base address.

Table 33. Bias Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	Reserved	Reserved
0x02	hword	BIAS_STS Register	Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

7.2.9 Crystal Register Block Address Map

The Crystal block has a base address of 0xF8. The addresses shown below are offsets starting from this base address.

Table 34. Crystal Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	XO_CNFG Register	Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets. For information on how to set up this interface, see Differential Output Termination.

7.2.10 Clock Output Register Block Address Map

The Clock Output 0 block has a base address of 0x100.
The Clock Output 1 block has a base address of 0x108.
The Clock Output 2 block has a base address of 0x110.
The Clock Output 3 block has a base address of 0x118.
The addresses shown below are offsets starting from this base address.

Table 35. Clock Output Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	OD_CNFG Register	Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.
0x02	byte	ODRV_EN Register	Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.
0x03	byte	ODRV_MODE_CNFG Register	Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.
0x04	byte	ODRV_AMP_CNFG Register	Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

7.2.11 Clock Reference Register Block Address Map

The Clock Reference Register block has a base address of 0x120. The addresses shown below are offsets starting from this base address

Table 36. Clock Reference Addresses

Offset	Size	Register Name	Register Description
0x00	word	PREDIV_CNFG Register	Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

7.2.12 GPIO Register Block Address Map

The GPIO Register block has a base address of 0x130. The addresses shown below are offsets starting from this base address.

Table 37. GPIO Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	OE_CNFG Register	Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.
0x01	byte	IO_CNFG Register	Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.
0x02	hword	LOCK_CNFG Register	Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.
0x04	hword	Reserved	-
0x06	byte	Reserved	Reserved
0x07	byte	STARTUP_STS Register	Start-up status. Address map for this block of registers: GPIO Block Register Offsets.
0x08	byte	GPIO_STS Register	GPIO status. Address map for this block of registers: GPIO Block Register Offsets.
0x0C	word	SCRATCH0 Register	Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

7.2.13 SSI Register Block Address Map

The SSI Register block has a base address of 0x140. The addresses shown below are offsets starting from this base address.

Table 38. SSI Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SPI_CNFG Register	SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x01	byte	I2C_FLTR_CNFG Register	I2C mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x02	byte	I2C_TIMING_CNFG Register	I2C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.
0x03	byte	I2C_ADDR_CNFG Register	I2C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.
0x04	byte	SSI_GLOBAL_CNFG Register	Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

7.2.14 APLL Register Block Address Map

The Analog PLL block has a base address of 0x150. The addresses shown below are offsets starting from this base address.

Table 39. APLL Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	APLL_FB_DIV_FRAC Register	APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.
0x04	hword	APLL_FB_DIV_INT Register	APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.
0x06	byte	APLL_FB_SDM_CNFG Register	APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.
0x07	byte	APLL_CNFG Register	APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.
0x08	hword	Reserved	Reserved
0x0A	byte	LPF_CNFG Register	APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.
0x0B	byte	LPF_3RD_CNFG Register	APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.
0x0C	byte	Reserved	Reserved
0x0D	byte	Reserved	Reserved
0x0E	byte	Reserved	Reserved
0x0F	byte	Reserved	Reserved
0x10	byte	Reserved	Reserved
0x12	hword	Reserved	Reserved
0x14	hword	APLL_LOCK_CNFG Register	APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.
0x16	byte	APLL_LOCK_THRSH Register	APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.
0x17	byte	VCO_CAL_STS Register	APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.

Table 39. APLL Block Register Offsets (Cont.)

Offset	Size	Register Name	Register Description
0x18	byte	APLL_STS Register	APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.
0x19	byte	APLL_EVENT Register	APLL Event status. Address map for this block of registers: APLL Block Register Offsets.
0x1A	byte	APLL_LOL_CNT Register	APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

7.2.15 Clock Input Register Block Address Map

The Clock Input block has a base address of 0x190. The addresses shown below are offsets starting from this base address.

Table 40. Clock Input Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	REF_CLK_IN_CNFG Register	Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

8. Register Descriptions

8.1 GLOBAL Registers

8.1.1 VENDOR_ID Register

Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default	Description
15:12	dev_id_type	RO	0x1	Device ID Block Type. A value of 0x1 indicates that this register is followed by a 16-bit Device ID register, a 16-bit Device Revision register, and a 16-bit Device Programming register.
11	reserved	RO	0x0	reserved.
10:0	vendor_id	RO	0x33	Vendor ID. Renesas JTAG ID.

8.1.2 DEVICE_ID Register

Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	device_id	RW	0x304A	Device ID. For default value refer to the Product Id in Table 43.

8.1.3 DEVICE_REV Register

Device revision identification information. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	Reserved
12:8	font_id	RO	0x2	Font ID. Font ID to distinguish die variants. Decode as follows: • 0x0 = Font 0 (Font 0) • 0x1 = Font 1 (Font 1) • 0x2 = Font 2 (Font 2)
7:4	ana_rev	RO	0x3	Hardware analog revision. Decode as follows: • 0x1 = First revision (TV) • 0x2 = Second revision (RevA) • 0x3 = Third revision (RevB)
3:0	dig_rev	RO	0x2	Hardware digital revision. Decode as follows: • 0x1 = First revision (TV) • 0x2 = Second revision (RevA/B)

8.1.4 DEVICE_PGM Register

Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	dash_code	RW	0x0	Dash code. Decimal value assigned by Renesas to identify the user configuration loaded in OTP at the factory. This field is writeable and is configured from the OTP common configuration programmed at the factory. • 0x0 = No user configurations are programmed at the factory

8.1.5 DEVICE_CNFG Register

Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	digldo_cnf	RW	0x0	Digital LDO voltage select. Selects the digital LDO voltage level. This setting is intended for test purposes only. • 0x0 = 1.25V • 0x1 = 1.32V
6:4	xo_delay	RW	0x0	Crystal Startup Delay. Selects the wait time for the internal crystal oscillator circuit during the startup sequence. The default setting of 1ms should be sufficient for all crystals. This setting is intended for debug purposes only. • 0x0 = 1 ms • 0x1 = 2.5 ms • 0x2 = 5 ms • 0x3 = 7.5 ms • 0x4 = 10 ms • 0x5 = 0.5 ms • 0x6 = 15 ms • 0x7 = reserved
3:0	config_sel	RW	0x4	User Configuration Select. Controls the selection of the user configuration stored in OTP to read on start-up (for details, see OTP and I2C Address User Configuration Selection).

8.1.6 DEV_RESET Register

Device reset commands. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	input_div_global_setb	RW	0x1	Input Dividers Common Set. When cleared, both input dividers get held in set mode (bit is active low). This allows to set and release both dividers at roughly the same time.
4	out_global_oe	RW	0x1	Output Global OE. This bit allows manual CSR control of the output OE.
3:2	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
1	divider_sync	RW	0x0	Divider synchronization. Writing this bit to 1 synchronizes the Output Dividers and the DPLL feedback divider (if the DPLL is enabled). The output clocks are squelched for approximately 10µs. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.
0	apll_reinit	RW	0x0	APLL Reinitialization. Writing this bit to 1 restarts the startup sequence from the VCO calibration step, including divider synchronization. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.

8.1.7 SW_RESET Register

Software reset command. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	reserved	RW	0x0	reserved
10:9	reserved	RO	0x0	reserved.
8	bias_cal_sw_rst	RW	0x0	Bias Cal Software reset. The bias calibration logic is held in reset while this bit is set to 1.
7	tdc_apll_dig_sw_rst	RW	0x0	TDC Software reset. The TDC logic is held in reset while this bit is set to 1.
6	dpll_sw_rst	RW	0x0	DPLL Software reset. The DPLL is held in reset while this bit is set to 1.
5	actmon1_sw_rst	RW	0x0	ACTMON1 Software reset. The Activity Monitor 1, which monitors the nCLKIN input, is held in reset while this bit is set to 1.
4	actmon0_sw_rst	RW	0x0	ACTMON0 Software reset. The Activity Monitor 0, which monitors the CLKIN input, is held in reset while this bit is set to 1.
3	losmon2_sw_rst	RW	0x0	LOSMON2 Software reset. The Loss-of-signal Monitor 2, which monitors the crystal input (XIN/REF), is held in reset while this bit is set to 1.
2	losmon1_sw_rst	RW	0x0	LOSMON1 Software reset. The Loss-of-signal Monitor 1, which monitors the nCLKIN input, is held in reset while this bit is set to 1.
1	losmon0_sw_rst	RW	0x0	LOSMON0 Software reset. The Loss-of-signal Monitor 0, which monitors the CLKIN input, is held in reset while this bit is set to 1.
0	otp_sw_rst	RW	0x0	OTP Software reset. The OTP logic is held in reset while this bit is set to 1.

8.1.8 CLOCK_GATE Register

Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas if further details are needed.

Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	dig_cg	RW	0x0	Digital Logic Clock Gate. All digital clocks that do not have separate clock gating control bits in this register are gated while this bit is set to 1. Because this gates the register bus clock, no further register access is possible through the serial port. The device must be power cycled to recover. This bit is intended for test purposes only (shut down all digital logic during analog characterization or debug).
10:9	reserved	RO	0x0	reserved.
8	reserved	RW	0x0	reserved
7	reserved	RO	0x0	reserved.
6	reserved	RW	0x0	reserved
5	actmon1_cg	RW	0x0	ACTMON1 Clock Gate. The Activity Monitor 1 is clock gated while this bit is set to 1.
4	actmon0_cg	RW	0x0	ACTMON0 Clock Gate. The Activity Monitor 0 is clock gated while this bit is set to 1.
3	losmon2_cg	RW	0x0	LOSMON2 Clock Gate. The Loss-of-signal Monitor 2 is clock gated while this bit is set to 1.
2	losmon1_cg	RW	0x0	LOSMON1 Clock Gate. The Loss-of-signal Monitor 1 is clock gated while this bit is set to 1.
1	losmon0_cg	RW	0x0	LOSMON0 Clock Gate. The Loss-of-signal Monitor 0 is clock gated while this bit is set to 1.
0	reserved	RW	0x0	reserved.

8.1.9 DEVICE_STS Register

Device status. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	startup_seq_sts	RO	0x0	Startup Sequence Status. Status related to the startup sequence. This field is intended for debug purposes only. bit [0] = Bias calibration timeout (2ms) bit [1] = OTP load timeout (10ms) bit [2] = APLL lock timeout (2ms)
4	osc_fallback	RO	0x0	Power-on-Reset Ring Oscillator Fallback. Set to 1 if the system clock divider output does not begin toggling during the startup sequence and the reset controller muxes the ring oscillator clock onto the system clock instead.
3	device_ready	RO	0x0	Device Ready. Set to 1 when the OTP load completes during the startup sequence.
2	reserved	RO	0x0	reserved.
1:0	config_loaded	RO	0x0	User Configuration Loaded. Indicates the user configuration loaded from OTP on start-up. Note that the common configuration is always loaded in addition to any user configurations are loaded.

8.2 INT Registers

8.2.1 INT_EN Register

Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_en	RW	0x0	Device interrupt enable. Overall device interrupt enable. When this field is set to 1, the device interrupt is asserted while device_int_sts is 1.
14:12	reserved	RO	0x0	reserved.
11:9	reserved	RW	0x0	reserved.
8	act1_int_en	RW	0x0	nCLKIN Activity Monitor interrupt enable. When this field is set to 1, the act1_int_sts bit contributes to the device interrupt
7	act0_int_en	RW	0x0	CLKIN Activity Monitor interrupt enable. When this field is set to 1, the act0_int_sts bit contributes to the device interrupt.
6	los2_int_en	RW	0x0	XTAL Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los2_int_sts bit contributes to the device interrupt.
5	los1_int_en	RW	0x0	nCLKIN Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los1_int_sts bit contributes to the device interrupt
4	los0_int_en	RW	0x0	CLKIN Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los0_int_sts bit contributes to the device interrupt.
3	dpll_state_ch_int_en	RW	0x0	DPLL State Change interrupt enable. When this field is set to 1, the dpll_state_ch_int_sts bit contributes to the device interrupt.
2	dpll_holdover_int_en	RW	0x0	DPLL Holdover interrupt enable. When this field is set to 1, the dpll_holdover_int_sts bit contributes to the device interrupt.
1	dpll_lol_int_en	RW	0x0	DPLL Loss-of-Lock interrupt enable. When this field is set to 1, the dpll_lol_int_sts bit contributes to the device interrupt.
0	apll_lol_int_en	RW	0x0	APLL Loss-of-Lock interrupt enable. When this field is set to 1, the apll_lol_int_sts bit contributes to the device interrupt.

8.2.2 INT_STS Register

Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_sts	RO	0x0	Device interrupt status. Overall device interrupt status. This bit is the OR of all the other interrupt status bits in this register after masking by their respective interrupt enable bits in INT_EN Register. This bit is masked by device_int_en. The resulting signal is output on the LOCK pin when lock_sel selects the device interrupt.
14:9	reserved	RO	0x0	reserved.
8	act1_int_sts	RO	0x0	nCLKIN Activity Monitor interrupt status Mirrors the nCLKIN act_evt event bit
7	act0_int_sts	RO	0x0	CLKIN Activity Monitor interrupt status Mirrors the CLKIN act_evt event bit
6	los2_int_sts	RO	0x0	XTAL Monitor Loss-of-Signal interrupt status Mirrors the XIN/REF los_evt event bit

Bit Field	Field Name	Type	Default Value	Description
5	los1_int_sts	RO	0x0	nCLKIN Monitor Loss-of-Signal interrupt status Mirrors the nCLKIN los_evt event bit
4	los0_int_sts	RO	0x0	CLKIN Monitor Loss-of-Signal interrupt status Mirrors the CLKIN los_evt event bit
3	dpll_state_ch_int_sts	RO	0x0	DPLL State Change interrupt status Mirrors the dpll_state_ch event bit
2	dpll_holdover_int_sts	RO	0x0	DPLL Holdover interrupt status. Mirrors the dpll_holdover event bit.
1	dpll_lol_int_sts	RO	0x0	DPLL Loss-of-Lock interrupt status. Mirrors the dpll_lol event bit.
0	apll_lol_int_sts	RO	0x0	APLL Loss-of-Lock interrupt status. Mirrors the apll_lol event bit.

8.3 LOSMON Registers

Before reprogramming a Loss of Signal Monitor block, the corresponding losmon0_sw_rst, losmon1_sw_rst, or losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

8.3.1 LOSMON_STS Register

LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	ref_invalid	RO	0x1	Reference Clock Invalid status. Indicates whether this reference clock is currently considered to be invalid. This occurs if the clock is disqualified by one or more of the Loss-of-Signal and Activity monitors or ref_disable is set to 1. • 0x0 = Clock is valid • 0x1 = Clock is invalid
0	los_sts	RO	0x1	Loss-of-Signal status. Current value of the LOS status from the clock monitor: • 0x0 = Clock meets the monitoring criteria • 0x1 = Loss-of-signal detected

8.3.2 LOSMON_EVENT Register

LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	los_evt	RW1C	0x1	Loss-of-Signal Event status. Set while the clock monitor asserts LOS. This bit cannot be cleared by software while the LOS condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. • 0x0 = Loss-of-signal not detected since the last time the bit was cleared • 0x1 = Loss-of-signal detected since the last time the bit was cleared

8.3.3 LOSMON_QUAL Register

LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	los_good_times	RW	0x0	LOS Monitor Qualification Count If this number of consecutive accepted clock LOS monitoring windows occur without a rejected window, then the clock is qualified and los_sts is set to 0. A value of 0 is the same as using the value 1.
3:0	los_fail_times	RW	0x0	LOS Monitor Disqualification Count If this number of rejected clock LOS monitoring windows occur without qualifying the clock, then the clock is disqualified and los_sts is set to 1. A value of 0 is the same as using the value 1.

8.3.4 LOSMON_WINDOW Register

LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:8	reserved	RO	0x0	reserved.
7:3	los_div_ratio	RW	0x0	LOS Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by los_div_ratio is less than 1/8 of the system clock frequency to achieve 25% accuracy. One period of the divided clock is the monitoring window duration. A value of 0 or 1 means divide by 1. The value 0x1F is not supported.
2	reserved	RO	0x0	reserved.
1	ref_disable	RW	0x0	Reference Clock Selection Disable Controls whether this reference clock may be selected as the DPLL reference clock. Not applicable for LOSMON2 (XTAL monitor). • 0 = Reference clock may be selected, subject to qualification by the Loss-of-Signal, Activity and Frequency monitors, and prioritization according to ref_priority • 1 = Reference clock cannot be selected, ref_invalid is 1.
0	los_fail_mask	RW	0x0	LOS Monitor Failure Mask Masks the LOS monitor status los_sts contribution to ref_invalid. • 0 = los_sts contributes to ref_invalid • 1 = los_sts does not contribute to ref_invalid

8.3.5 LOSMON_THRESH Register

LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:16	los_acc_margin	RW	0x0	LOS Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within los_nom_num ± los_acc_margin.
15:13	reserved	RO	0x0	reserved.
12:0	los_rej_margin	RW	0x0	LOS Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of los_nom_num ± los_rej_margin.

8.3.6 LOSMON_NOMINAL Register

LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:13	reserved	RO	0x0	reserved.
12:0	los_nom_num	RW	0x0	LOS Monitor Nominal Cycle Count Sets the expected number of system clock periods within one monitor window. Set to 0x0 to disable the LOS monitor. Disabling the monitor causes the los_sts to get asserted, therefore the los_fail_mask should also be set when this field is written to 0x0.

8.4 ACTMON Registers

Note that before reprogramming an Activity Monitor, the corresponding actmon0_sw_rst or actmon1_sw_rst bit should be set. When programming is done, it should then be cleared.

8.4.1 ACTMON_STS Register

Activity Monitor Status. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	act_sts	RO	0x1	Activity Monitor status. Current value of the qualification status from the activity monitor: • 0x0 = Clock meets the monitoring criteria, clock qualified • 0x1 = failure detected, clock disqualified

8.4.2 ACTMON_EVENT Register

Activity Monitor Event Status. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	act_evt	RW1C	0x1	Activity Monitor event status. Set while the activity monitor disqualifies the clock. This bit cannot be cleared by software while the disqualified condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. • 0x0 = Activity monitor has not disqualified the clock since the last time the bit was cleared • 0x1 = Activity monitor has disqualified the clock since the last time the bit was cleared

8.4.3 ACTMON_WINDOW Register

Activity Monitor Window Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:21	reserved	RO	0x0	reserved.
20	act_fail_mask	RW	0x0	Activity Monitor Failure Mask Masks the activity monitor status act_sts. • 0 = Status is not masked • 1 = Forces clock to be considered as qualified
19	reserved	RO	0x0	reserved.
18:0	act_div_ratio	RW	0x0	Activity Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by act_div_ratio is as close as possible to 100Hz, creating a 10ms monitoring window. A value of 0 means divide by 1. A value of 0x7FFFF is reserved.

8.4.4 ACTMON_THRESH Register

Activity Monitor Threshold Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
63:54	reserved	RO	0x0	reserved.
53:32	act_acc_margin	RW	0x0	Activity Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within act_nom_num ± act_acc_margin. One accepted window qualifies the clock and act_sts is set to 0.
31:22	reserved	RO	0x0	reserved.
21:0	act_rej_margin	RW	0x0	Activity Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of act_nom_num ± act_rej_margin. One rejected window disqualifies the clock and act_sts is set to 1.

8.4.5 ACTMON_NOMINAL Register

Activity Monitor Nominal Number Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:22	reserved	RO	0x0	reserved.
21:0	act_nom_num	RW	0x0	Activity Monitor Nominal Cycle Count Sets the expected number of clock periods of the ring oscillator frequency divided by 4 (nominally 216MHz) within one monitor window. Set to 0x0 to disable the activity monitor. Disabling the monitor causes the act_sts to get asserted, therefore the act_fail_mask should also be set when this field gets written to 0x0.

8.5 DPLL Registers

8.5.1 DPLL_REF_FB_CNFG Register

DPLL Ref and Fb Clock Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	dpll_ref_sel_mode	RW	0x0	DPLL reference clock selection mode • 0x0 = manual mode, reference selection is based on the setting of dpll_ref_sel • 0x2 = auto mode
5	reserved	RO	0x0	reserved.
4	dpll_ref_sel	RW	0x0	DPLL manual reference clock selection • 0x0 = clkin0 • 0x1 = clkin1
3:2	reserved	RO	0x0	reserved.
1	dpll_revertive_en	RW	0x0	DPLL revertive reference switch • 0x0 = non-revertive • 0x1 = revertive
0	dpll_hitless_en	RW	0x0	DPLL hitless reference switch • 0x0 = hitless disabled • 0x1 = hitless enabled

8.5.2 DPLL_MODE Register

Digital PLL mode control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	bw_damp_sw	RW	0x1	Automatic bandwidth/damping switching. Enables the DPLL to switch to the Locking Loop Filter bandwidth and damping settings when the DPLL is in the Acquire state while locking. Refer to dpll_lock_timer. • 0x0 = always use Normal Operation settings. • 0x1 = use Locking settings when the DPLL is in the Acquire state.
6	los_to_freerun	RW	0x0	Reference Loss-of-Signal to Freerun. Controls whether the DPLL enters Freerun or Holdover mode when the current reference clock is invalid. • 0x0 = Holdover. • 0x1 = Freerun.
5:4	reserved	RW	0x0	reserved
3	filter_update_dis	RW	0x0	DPLL filter update disable. This bit must be set to 1 before reconfiguring any DPLL registers while the DPLL is enabled, and then must be cleared after the reconfiguration finishes. The exception is write_freq which may be controlled dynamically and automatically suppresses filter_update when written.
2	dpll_en	RW	0x0	DPLL Enable. Controls whether the DPLL is enabled. • 0x0 = Synthesizer/DCO mode. DPLL (except loop filter and scaler blocks) is disabled (clock gated to reduce power) • 0x1 = Jitter Attenuator mode. DPLL is enabled.

Bit Field	Field Name	Type	Default Value	Description
1:0	dpll_mode	RW	0x1	DPLL mode selection. Selects DPLL mode: • 0x0 = Forces DPLL into Freerun state • 0x1 = Places the DPLL in Normal (automatic) mode. This is the normal setting for Jitter Attenuator mode • 0x2 = Forces DPLL into Holdover state. • 0x3 = Places DPLL in Write Frequency mode. This is the normal setting in DCO mode.

8.5.3 DPLL_DECIMATOR Register

Decimator configuration control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:4	dec_hitless_bw_shift	RW	0x3	Hitless Switch Decimator Bandwidth Shift to set the decimator bandwidth during a hitless reference switch or holdover-normal switch for measuring the phase offset. If dpll_histless_en is set to zero, this field is ignored.
3:0	dec_bw_shift	RW	0x6	Main Decimator Bandwidth. Shift to set the main decimator bandwidth. 0 puts the decimator in feed-through (infinite bandwidth).

8.5.4 DPLL_TRIM_OFFSET Register

DPLL Crystal trim offset. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	xtal_trim	RW	0x0	Crystal Trim Offset. Crystal fractional frequency offset compensation. This is an 8-bit 2's complement value. Resolution = $2^{-20} \approx 1$ ppm, Range = $\pm 2^{-13} \approx \pm 122$ ppm.

8.5.5 DPLL_HOLDOVER_CNFG Register

Holdover Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:11	holdover_bw_shift	RW	0x7	Holdover Filter Bandwidth Shift. Coarse control of the holdover bandwidth. A value of zero disables the holdover filter (infinite bandwidth). The valid range is 0-20. Values larger than 20 are limited internally to 20.
10:8	holdover_bw_mult	RW	0x0	Holdover Filter Bandwidth Multiplier. Fine control of the holdover filter bandwidth. A value of zero disables the holdover filter (infinite bandwidth), which is also the default setting.
7:4	holdover_history	RW	0x0	Holdover history • 0x0 = instantaneous • 0x1 = 1 second • 0x2 = 2 seconds • 0x3 = 3 seconds • ... • 0x9 = 9 seconds • 0xA = 10 seconds
3:0	dpll_lol_cnt_thresh	RW	0x0	DPLL Loss-of-Lock Counter Threshold. While the DPLL Loss-of-Lock counter (*dpll_lol_cnt*) exceeds this threshold, the *dpll_lol_lmt* bit is set.

8.5.6 DPLL_BANDWIDTH Register

DPLL Bandwidth configuration. Address map for this block of registers: DPLL Block Register Offsets.

Refer to Digital Loop Filter for details on configuring these settings. Or use Renesas's Timing Commander SW to provide appropriate settings.

This section supports separate settings for fast-lock acquisition (Acquire) and regular locked operation (Normal Operation).

Bit Field	Field Name	Type	Default Value	Description
15:11	acquire_bw_shift	RW	0xE	Acquire Loop Filter Bandwidth Shift. Coarse control of the DPLL loop filter bandwidth in the Acquire state while locking to the input clock. Default bandwidth = 1023 Hz.
10:8	acquire_bw_mult	RW	0x0	Acquire Loop Filter Bandwidth Multiplier. Fine control of the DPLL loop filter bandwidth in the Acquire state while locking to the input clock. Default bandwidth = 1023 Hz.
7:3	normal_bw_shift	RW	0xB	Normal Operation Loop Filter Bandwidth Shift. Coarse control of the DPLL loop filter bandwidth in the Normal state when locked to the input clock. Default bandwidth = 127 Hz.
2:0	normal_bw_mult	RW	0x0	Normal Operation Loop Filter Bandwidth Multiplier. Fine control of the DPLL loop filter bandwidth in the Normal state when locked to the input clock. Default bandwidth = 127 Hz.

8.5.7 DPLL_DAMPING Register

DPLL Damping control. Address map for this block of registers: DPLL Block Register Offsets

Refer to Digital Loop Filter for details on configuring these settings. Or use Renesas's Timing Commander SW to provide appropriate settings. This section supports separate settings for fast-lock acquisition (Acquire) and regular locked operation (Normal Operation).

Bit Field	Field Name	Type	Default Value	Description
15:14	reserved	RO	0x0	reserved.
13:11	acquire_damping_shift	RW	0x5	Acquire Loop Filter Damping Shift. Coarse control of the DPLL loop filter damping in the Acquire state while locking to the input clock. Default damping causes 1.1 dB peaking in the frequency domain jitter transfer function.
10:8	acquire_damping_mult	RW	0x1	Acquire Loop Filter Damping Multiplier. Fine control of the DPLL loop filter damping in the Acquire state while locking to the input clock. Default damping causes 1.1 dB peaking in the frequency domain jitter transfer function.
7:6	reserved	RO	0x0	reserved.
5:3	normal_damping_shift	RW	0x0	Normal Operation Loop Filter Damping Shift. Coarse control of the DPLL loop filter damping in the Normal state when locked to the input clock. Default damping causes 0.1 dB peaking in the frequency domain jitter transfer function.
2:0	normal_damping_mult	RW	0x1	Normal Operation Loop Filter Damping Multiplier. Fine control of the DPLL loop filter damping in the Normal state when locked to the input clock. Default damping causes 0.1 dB peaking in the frequency domain jitter transfer function.

8.5.8 DPLL_PHASE_SLOPE_LIMIT Register

DPLL Phase Slope Limit control. Address map for this block of registers: DPLL Block Register Offsets

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:0	phase_slope_limit	RW	0x1FFFFFF	Phase Slope Limit. Control of the phase slope limit of the output clocks. This represents the maximum instant relative frequency change of the output clock. This is an unsigned unitless number although it is often expressed as µs/ or ns/s. Renesas recommends programming a value that is approx. 10% smaller than the required limit to leave some room for the integrator to adjust to frequency offsets. The resolution of 1 LSB is 2-35 = 2.91e-11 = 29. ps/s.

8.5.9 DPLL_FB_DIV_NUM Register

DPLL Feedback Fraction Numerator value. Address map for this block of registers: DPLL Block Register Offsets.

Refer to DPLL Feedback Divider for details on configuring these settings. Or use Renesas's Timing Commander SW to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
63:48	reserved	RO	0x0	reserved.
47:0	fb_div_num	RW	0x0	Feedback Divider Numerator. DPLL feedback divide numerator value. Refer to fb_div_int for details. This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When the most significant byte (bits [47:40]) of fb_div_num or fb_div_den, is written, the value of both these fields, in addition to the one in fb_div_int is applied to the DPLL.

8.5.10 DPLL_FB_DIV_DEN Register

DPLL Feedback Fraction Denominator value. Address map for this block of registers: DPLL Block Register Offsets.

Refer to DPLL Feedback Divider for details on configuring these settings. Or use Renesas's Timing Commander SW to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
63:48	reserved	RO	0x0	reserved.
47:0	fb_div_den	RW	0x800000	Feedback Divider Denominator. DPLL feedback divide denominator value. Refer to fb_div_int for details. When the fb_div_num field is non-zero, the fraction has to be set such that the MSB of the fb_div_den is set (both fields should be shifted up by the same amount). This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When the most significant byte (bits [47:40]) of fb_div_num or fb_div_den, is written, the value of both these fields, in addition to the one in fb_div_int is applied to the DPLL.

8.5.11 DPLL_FB_DIV_INT Register

DPLL Feedback Integer value. Address map for this block of registers: DPLL Block Register Offsets.

Refer to DPLL Feedback Divider for details on configuring these settings. Or use Renesas's Timing Commander SW to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
15:14	reserved	RO	0x0	reserved.
13:0	fb_div_int	RW	0x190	DPLL Feedback Clock Divider Integer. DPLL feedback divide integer value. The DPLL feedback clock frequency must be no more than 33 MHz, and must be equal to the frequency of the reference clock divided by id_ratio, or equal to the reference clock when the input divider is bypassed by id_byp_en. This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When this field is changed from its previous value, the value of this field, in addition to the values from fb_div_num, fb_div_den get applied to the DPLL.

8.5.12 DPLL_FB_CORR Register

DPLL Feedback Correction Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	fine_rev	RW	0x0	TDC Fine Timestamp Bit Reversal. Selects the bit ordering of the fine timestamp signals from the TDC analog to digital. This setting is intended for debug purposes only. • 0x0 = Analog 30:0 maps to digital 30:0 • 0x1 = Analog 0:30 maps to digital 30:0
8:7	pec_delay	RW	0x0	PEC Delay. Phase error correction delay. Intended for debug purposes only. • 0x0 = sdm error no delay • 0x1 = sdm error delay one cycle • 0x2 = same as 0x0 • 0x3 = same as 0x0
6:0	pec_corr_mult	RW	0x0	Feedback Correction Multiplier. Multiplier to get the FB SDM remainder bits on the same resolution as the TDC phase bits (resolution ≈18.7 ps if TDC APLL runs at 864MHz). Should be set as follows: pec_cor_mult = (Tvco/TDC_step) * (128/fb_div_den[47:41])

8.5.13 DPLL_PHASE_OFFSET Register

DPLL Phase Offset configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:30	reserved	RO	0x0	reserved.
29:0	phase_offset	RW	0x0	Phase Offset. Manually sets the phase offset between the reference and feedback clocks. This is a 30-bit 2's complement value. The resolution is the TDC resolution / 8 (≈ 2.3 ps) and the range is ≈ ±1.26 ms. This allows all outputs to be adjusted in terms of their phase relationship to the input. All outputs move together using this precision setting. This field is not used when hitless switching is enabled. This register is atomic. When the most significant byte (bits [31:24]) is written, the new value is applied to the APLL.

8.5.14 DPLL_WRITE_FREQ Register

DPLL Write Frequency command. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:0	write_freq	RW	0x0	Write Frequency. Frequency control word for synthesizer/DCO mode. This is a 29-bit 2's complement value. The units are 2^{-40} * 1e6 [ppm]. This provides a maximum setting of ±244ppm. An update to this multi-byte register only takes effect when the most significant byte (bits [28:24]) are written, the new value is applied to the DPLL.

8.5.15 DPLL_LOCK Register

DPLL Lock Detection control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:16	dpll_lock_timer	RW	0x00FF	DPLL lock timer. Specifies the time interval during which the absolute value of the phase detector error must remain below the DPLL lock threshold (dpll_lock_thresh) to declare lock. The DPLL switches from the Acquire state to the Normal state when the threshold has been met for half of this time interval. If enabled by bw_damp_sw, the loop filter bandwidth and damping settings revert at this time from the Acquire settings to the Normal settings. When the threshold has been met again for half of this time interval, the DPLL declares lock. The units are ms.
15:0	dpll_lock_thresh	RW	0x0155	DPLL lock threshold. Specifies the threshold that the absolute value of the phase detector error must remain below during the DPLL lock timer (dpll_lock_timer) to declare lock. The units are the 8 * TDC resolution (≈ 149 ps if TDC APLL runs at 864MHz).

8.5.16 DPLL_TDC_DELAY Register

DPLL TDC Delay Control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	tdc_delay	RW	0x1F	TDC delay. Sets the TDC delay which goes to the DPLL, for debug purposes only.

8.5.17 DPLL_STS Register

DPLL Status. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:4	dpll_state_sts	RO	0x0	DPLL state machine's current state. Decode as follows: • 0x0 = freerun • 0x1 = normal/locked • 0x2 = holdover • 0x3 = write_frequency • 0x4 = acquire • 0x5 = hitless switch
3:2	reserved	RO	0x0	reserved.
1	dpll_ref_sel_sts	RO	0x0	DPLL reference clock selection status Indicates the reference clock selected by the DPLL. • 0x0 = clkin0 • 0x1 = clkin1
0	dpll_lock_sts	RO	0x0	DPLL lock status. Indicates the DPLL lock status: • 0x0 = unlocked • 0x1 = locked

8.5.18 DPLL_EVENT Register

DPLL Event status. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3	dpll_state_ch	RW1C	0x0	DPLL State Change event. Set to 1 when the DPLL state machine changes state.
2	dpll_holdover	RW1C	0x0	DPLL Holdover event. Set to 1 when the DPLL state machine enters the holdover state. When asserted, this bit remains asserted until cleared by a write of '1' to this bit position.
1	dpll_lol_lmt	RW1C	0x0	DPLL Loss-of-Lock Counter Threshold Exceeded status. Set while the DPLL Loss-of-Lock counter (*dpll_lol_cnt*) exceeds the threshold set in *dpll_lol_cnt_thresh*. This bit cannot be cleared by software while the condition persists. • 0x0 = Loss-of-lock counter has not exceeded the threshold since the last time the bit was cleared • 0x1 = Loss-of-lock counter exceeded the threshold since the last time the bit was cleared

Bit Field	Field Name	Type	Default Value	Description
0	dpll_lol	RW1C	0x0	DPLL Loss-of-lock event. Set to 1 when the DPLL lock status transitions from locked to unlocked. When asserted, this bit remains asserted until cleared by a write of '1' to this bit position.

8.5.19 DPLL_LOL_CNT Register

DPLL Loss-of-Lock Event Counter. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:0	dpll_lol_cnt	RW	0x0	DPLL Loss-of-Lock Counter. This counter increments each time the DPLL lock status de-asserts, and saturates at 0xF. It is cleared by writing it to 0x0, and may be preset by writing the desired value. Preset may be used either as a debug tool or to cause a threshold alarm to happen sooner because the alarm threshold is not configurable. This register can only be written if the block is not clock gated or held in reset (dpll_sw_rst).

8.6 TDC Registers

8.6.1 TDC_REF_DIV_CNFG Register

TDC reference divider control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2:0	tdc_ref_div_cnfg	RW	0x1	TDC Reference Divider Control. Controls the divide ratio of the TDC reference (either input or CLKIN input, selected by apll_ref_sel). This field should be programmed such that the reference to the TDC APLL is between 10MHz and 30MHz • 0x0 = bypass divider. • 0x1 = divide by2 • 0x2 = divide by 4 • 0x3 = divide by 8 • 0x4 = divide by 16

8.6.2 TDC_FB_SDM_CNFG Register

TDC internal APLL Feedback Divider SDM control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	tdc_fb_sdm_en	RW	0x1	TDC APLL Feedback SDM Enable. Enables the SDM controlling the TDC APLL feedback divider. • 0x0 = SDM disabled, constant integer division by tdc_fb_div_int • 0x1 = SDM enabled, MMD mode
6:2	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
1:0	tdc_fb_sdm_order	RW	0x1	TDC APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the TDC APLL. • 0x0 = Integer • 0x1 = 1st order • 0x2 = 2nd order • 0x3 = reserved

8.6.3 TDC_FB_DIV_INT Register

TDC internal APLL Feedback Divider Integer value. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	tdc_fb_div_int	RW	0x23	TDC APLL Feedback Divider Integer. Integer portion of the TDC APLL feedback divider.

8.6.4 TDC_FB_DIV_FRAC Register

TDC internal APLL Feedback Divider Fraction value. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	tdc_fb_div_frac	RW	0x2800	TDC APLL Feedback Fraction. Fraction of the TDC APLL feedback divider. The fraction is calculated as follows: tdc_fb_div_frac/2^{16}.

8.6.5 TDC_DAC_CNFG Register

TDC internal APLL Digital to Analog Converter (DAC) control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
4:0	tdc_dig_set	RW	0x4	TDC APLL Set value. Increases the baseline APLL DCO voltage. The step size is 1/32nd of the full range (nominally 37.5 mV). The dynamic control signal generated by the DAC SDM (0-16) is added to this value to create the DAC input. Values 0x11 to 0x1F are reserved. • 0x0 = no increase • 0x1 = 1/32 increase • 0x2 = 2/32 increase • 0x3 = 3/32 increase • 0x4 = 4/32 increase • 0x5 = 5/32 increase • 0x6 = 6/32 increase • 0x7 = 7/32 increase • 0x8 = 8/32 increase • 0x9 = 9/32 increase • 0xA = 10/32 increase • 0xB = 11/32 increase • 0xC = 12/32 increase • 0xD = 13/32 increase • 0xE = 14/32 increase • 0xF = 15/32 increase • 0x10 = 16/32 increase

8.7 SYSDIV Registers

8.7.1 SYS_DIV_INT Register

System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	reserved.
4:0	sys_div_int	RW	0xC	System Clock Divide Integer. The system clock divide integer value must be set to produce a system frequency between 180MHz and 333MHz, divided down from the APLL VCO frequency divided by 4. The frequency picked has side effects on various calculations done in other blocks (LOSMON Registers). Normally expected to be between 210MHz and 240MHz. The minimum valid value for this field is10 and the maximum is 15.

8.8 BIAS Registers

8.8.1 BIAS_STS Register

Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:9	reserved	RO	0x0	reserved.
8	bias_cal_in	RO	0x0	Bias Calibration comparator value. Raw bias_cal_in value.

Bit Field	Field Name	Type	Default Value	Description
7:5	cnf_bias_cal_eff	RO	0x0	Bias Calibration effective configuration value. Indicates the configuration value selected as sent to the bias control circuit. Valid when bias_cal_done is set to 1.
4:2	cnf_bias_cal	RO	0x0	Bias Calibration configuration value. Indicates the configuration value selected by the bias calibration logic. Valid when bias_cal_done is set to 1.
1	bias_cal_fail	RO	0x0	Bias Calibration failed. Indicates whether bias calibration completed successfully. Valid when bias_cal_done is set to 1. • 0x0 = Bias calibration succeeded • 0x1 = Bias calibration failed
0	bias_cal_done	RO	0x0	Bias Calibration done. Indicates whether bias calibration is running: • 0x0 = Bias calibration is in progress • 0x1 = Bias calibration is completed

8.9 XO Registers

8.9.1 XO_CNFG Register

Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets. For information on how to set up this interface, see Differential Output Termination.

Bit Field	Field Name	Type	Default Value	Description
31:19	Reserved	RO	0x0	reserved.
18:17	xo_cfg_res	RW	0x0	reserved. Not used.
16	en_ldo_xo	RW	0x1	XO LDO Enable. When set, enables the XO LDO.
15:14	en_gain	RW	0x1	XO gain boosting control. Selects the number of gain boosting amplifiers enabled during startup. • 0x0 = Gain boosting amplifiers are disabled • 0x1 = One parallel amplifier is enabled • 0x2 = Two parallel amplifiers are enabled • 0x3 = All three parallel amplifiers are enabled
13:8	en_cap_xout	RW	0x1F	XO additional tuning capacitance at XOUT terminal. Controls the internal tuning capacitance applied at the XOUT terminal. The capacitance rises monotonically n steps of 0.5pF from 0pF to 23.5pF as the control setting increases from 0x00 to the maximum of 0x2F. Values 0x30 to 0x3F are reserved.
7:6	Reserved	RW	0x0	reserved.
5:0	en_cap_xin	RW	0x1F	XO additional tuning capacitance at XIN/REF terminal. Controls the internal tuning capacitance applied at the **XIN/REF** terminal. The capacitance rises monotonically in steps of 0.5pF from 0pF to 23.5pF as the control setting increases from 0x00 to the maximum of 0x2F. Values 0x30 to 0x3F are reserved.

8.10 OUT Registers

8.10.1 OD_CNFG Register

Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	en_ldo_od	RW	0x1	Output Divider LDO Enable. When set, enables the corresponding output divider LDO.
14	reserved	RO	0x0	reserved.
13:0	outdiv_ratio	RW	0x69	Output Divider ratio. Output divider ratio. The minimum divide value is 10 (decimal).

8.10.2 ODRV_EN Register

Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:2	out_dis_state	RW	0x0	Output Driver disabled state. Controls the state of OUTx/nOUTx when the output driver is disabled. • 0x0 = Held Low/Low (except LVDS mode is held Low/High) • 0x1 = Held Low/High • 0x2 = Held Hi-Z/Hi-Z • 0x3 = Normal operation (not held static). This is intended for debug purposes only.
1	out_dis	RW	0x0	Output Driver disable. Forces the Output Driver to be disabled (for details, see Output Enable Control). • 0 = Output Driver is enabled if not disabled by other means • 1 = Output Driver is disabled
0	out_pd	RW	0x0	Output Driver power down. Powers down the Output Driver. When powered down, OUTx/nOUTx are tri-stated and the output enable control is ignored. • 0 = Output Driver is powered up and can be enabled/disabled • 1 = Output Driver is powered down

8.10.3 ODRV_MODE_CNFG Register

Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_cmos_mode	RW	0x1	Output Driver CMOS mode. Controls how OUTx and nOUTx are driven when CMOS mode is selected. • 0x0 = OUTx, nOUTx are driven with the same phase • 0x1 = OUTx, nOUTx are driven with the opposite phase • 0x2 = Only OUTx is driven. nOUTx is held low. • 0x3 = Only nOUTx is driven. OUTx is held low.

Bit Field	Field Name	Type	Default Value	Description
5:4	out_lvds_cm_voltage	RW	0x2	Output Driver LVDS common mode voltage control. Controls the common mode voltage of the output driver when LVDS mode is selected. • 0x0 = 700mV • 0x1 = 800mV • 0x2 = 900mV • 0x3 = 1000mV
3	out_hcsl_term_en	RW	0x1	Output Driver HCSL termination enable. Controls the internal HCSL termination. • 0x0 = Internal HCSL termination is disabled. An external termination resistor to ground is required. • 0x1 = Internal HCSL termination is enabled, providing an internal 50ohm resistor to ground.
2	en_out_bias	RW	0x1	Output Driver Bias Enable. When set, enables the output driver bias circuit.
1:0	out_mode	RW	0x0	Output Driver type. Selects the output driver type. • 0x0 = HCSL • 0x1 = reserved • 0x2 = LVDS • 0x3 = CMOS

8.10.4 ODRV_AMP_CNFG Register

Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	out_cnf_hcsl_swing	RW	0xB	Output Driver HCSL amplitude control. Controls the amplitude of the output driver when CML mode is selected. Each value provides a 50mV increment. • 0x0 = 200mV • 0x1 = 250mV • 0x2 = 300mV • 0x3 = 350mV • 0x4 = 400mV • 0x5 = 450mV • 0x6 = 500mV • 0x7 = 550mV • 0x8 = 600mV • 0x9 = 650mV • 0xA = 700mV • 0xB = 750mV • 0xC = 800mV • 0xD = 850mV • 0xE = 875mV • 0xF = 900mV
3	out_cnf_lvds_amp	RW	0x0	Output Driver LVDS amplitude control. Controls the amplitude of the output driver when LVDS mode is selected. • 0 = 350mV • 1 = 400mV
2:0	reserved	RW	0x4	reserved.

8.11 REF Registers

8.11.1 PREDIV_CNFG Register

Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

Refer to Input Dividers for details on how to set up this interface. Or use the Renesas Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
31:25	reserved	RO	0x0	reserved.
24	ref_priority	RW	0x0	Reference Clock Priority Sets the clock's priority for DPLL reference switching. If multiple clocks are set to the same priority level, they are prioritized from the lowest numbered (clkin0) to the highest numbered (clkin3). • 0x0 = first priority • 0x1 = second priority
23	reserved	RO	0x0	reserved.
22	input_div_setb	RW	0x1	Input Divider Set When cleared, the corresponding input divider gets held in set mode (bit is active low).
21	enb_input_div	RW	0x0	Input Divider Enable When cleared, enables the corresponding input divider (active low).
20	id_byp_en	RW	0x1	Input Divider Bypass. Allows the input divider to be bypassed and the reference clock input is passed directly to the DPLL and clock monitor. Bypass must be disabled if the reference clock frequency is greater than 33 MHz. • 0 = divided reference clock is selected, divide ratio is id_ratio • 1 = reference clock is selected, effective divide ratio is 1
19:0	id_ratio	RW	0x0	Input Divider ratio. Input divider ratio. The reference clock frequency divided by this value must be no more than 33 MHz, and must be equal to the DPLL feedback clock frequency. The minimum divide value is 2. To divide by 1 (when the input reference clock frequency is no more than 33 MHz), bypass the divider by setting id_byp_en to 1.

8.12 GPIO Registers

8.12.1 OE_CNFG Register

Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	oe_pd	RW	0x0	OE_nCS Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the OE_nCS pin.
4	oe_pu	RW	0x1	OE_nCS Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the OE_nCS pin.
3	oe_pol	RW	0x0	OE Input Polarity. Controls the active polarity of the OE_nCS input pin when oe_sel is set to 0. • 0x0 = Active high (1 = enable outputs, 0 = disable outputs) • 0x1 = Active low (0 = enable outputs, 1 = disable outputs)
2:1	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
0	oe_sel	RW	0x0	OE Select. Selects whether the OE_nCS input pin can control the output enable of the clock output drivers: • 0x0 = The OE_nCS input disables the clock output drivers when deasserted. This setting is ignored in SPI mode. • 0x1 = The OE_nCS input does not affect the clock output drivers.

8.12.2 IO_CNFG Register

Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_startup	RW	0x0	Output Disable on startup until PLL locks. Controls whether the clock output drivers are disabled until the APLL or DPLL locks during the startup sequence. • 0x0 = Clock output drivers are disabled until APLL lock asserts • 0x1 = Clock output drivers are disabled until DPLL lock asserts • 0x2 = Clock output drivers are not disabled by APLL or DPLL lock status • 0x3 = Reserved
5:4	pp_drv	RW	0x2	Push-Pull Drive Strength • Applies to pads LOCK and SDA_SDIO (for 3-wire SPI only) when configured for push-pull mode. Drive strength increases as this setting increases.
3:2	od_drv	RW	0x3	Open-Drain Drive Strength • Applies to pads LOCK when configured for open-drain mode. Drive strength increases as this setting increases.
1	sda_pu	RW	0x1	SDA Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SDA_SDIO pin.
0	scl_pu	RW	0x1	SCL Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SCL_SCLK pin.

8.12.3 LOCK_CNFG Register

Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	reserved.
12	lock_od	RW	0x0	LOCK Open-drain enable. Set to 1 to configure the LOCK pin as an open-drain output. When lock_pol is set to 0, LOCK is driven low when the value to output is 0 and LOCK is open-drain when the value to output is 1. When lock_pol is set to 1, LOCK is driven low when the value to output is 1 and LOCK is open-drain when the value to output is 0.
11	lock_hiz	RW	0x0	LOCK Tristate Enable. Set to 1 to place the LOCK pin in a high-impedance state.
10	lock_pd	RW	0x0	LOCK Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the LOCK pin. This should not be used when lock_od is set to 1.
9	lock_pu	RW	0x1	LOCK Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the LOCK pin. Note that this internal pull-up is weak, so an external pull-up, tied to the V_{DDA} voltage rail is recommended when lock_od is set to 1.

Bit Field	Field Name	Type	Default Value	Description
8	lock_pol	RW	0x0	LOCK Output Polarity. Selects the polarity of the signal driven on the LOCK pin. When set to active high, the true value of the signal is driven. When set to active low, the inverse of the signal is driven. For example, when lock_sel selects APLL lock, and lock_pol is set to active high, LOCK drives high when the APLL is locked, and drives low when the APLL is unlocked. When lock_pol is set to active low, LOCK drives low when the APLL is locked, and drives high when the APLL is unlocked. This setting is ignored when lock_sel is set to 0x1F. • 0x0 = Active high • 0x1 = Active low
7:5	reserved	RO	0x0	reserved.
4:0	lock_sel	RW	0x0	LOCK Output Mode Select. Selects the status/clock to output on the LOCK pin: • 0x0 = APLL lock (apll_lock_sts) • 0x1 = DPLL lock (dpll_lock_sts) • 0x2 = Reference #0 loss-of-signal (LOSMON0 los_sts) • 0x3 = Reference #1 loss-of-signal (LOSMON1 los_sts) • 0x4 = Crystal loss-of-signal (LOSMON2 los_sts) • 0x5 = Reference #0 activity monitor status (ACTMON0 act_sts) • 0x6 = Reference #1 activity monitor status (ACTMON1 act_sts) • 0x7 = Reference #0 ref_invalid status • 0x8 = Reference #1 ref_invalid status • 0x9 = Device Interrupt (device_int_sts & device_int_en) • 0xA = Device ready (startup sequence completed) • 0x1D: Logic low • 0x1E: Logic high • Others: reserved

8.12.4 STARTUP_STS Register

Start-up status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	bond_id	RO	0x0	Bond ID value. Value of bond id die pad.
6	reserved	RO	0x0	Reserved
5:0	gpio_at_startup	RO	0x0	GPIO startup value. Value of pins latched at startup. bit [0] = LOCK bit [1] = SDA_SDIO bit [2] = SCL_SCLK bit [3] = OE_nCS bit [4] = Reserved bit [5] = Reserved

8.12.5 GPIO_STS Register

GPIO status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	lock_o	RO	0x0	LOCK Output value. Reflects the value driven on the LOCK pin when lock_sel is set to 0x0 through 0x4. This bit reads as 0 when lock_sel is set to any other value.
0	oe_i	RO	0x0	OE Input value. Reflects the value input on the OE_nCS pin when oe_sel is set to 0. This bit reads as 0 when oe_sel is set to 1.

8.12.6 SCRATCH0 Register

Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:0	scratch0	RW	0x0	Scratch register. This value can be stored in OTP on a per-configuration basis. It is not used by the device hardware for any purpose. Users can set this to any value.

8.13 SSI Registers

The acronym SSI refers to items that are generic to the Slave Serial Interface in any mode of operation. SPI or I^2C is used for features and functions that are specific to those operating modes.

8.13.1 SPI_CNFG Register

SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:5	spi_dummy_size	RW	0x1	SPI dummy read byte count. Number of dummy bytes shifted out before the read data when spi_dummy_en is 1. • 0x0 = reserved • 0x1 = 1 byte • 0x2 = 2 bytes • 0x3 = 3 bytes
4	spi_dummy_en	RW	0x0	SPI dummy read byte enable. Enables insertion of dummy read bytes. • 0x0 = Read data is immediately available (no dummy bytes) • 0x1 = spi_dummy_size number of bytes are shifted out before the read data
3	spi_del_out	RW	0x0	SDO driving edge selection. Selects the clock edge that drives SDO. • 0x0 = SDO is driven on opposite SCLK edge than the sampling edge • 0x1 = SDO is delayed one half cycle of SCLK
2	reserved	RO	0x0	reserved.
1	spi_clk_sel	RW	0x0	SDI sampling edge selection. Selects the clock edge that samples SDI. • 0x0 = SDI is sampled on rising SCLK edge • 0x1 = SDI is sampled on falling SCLK edge

Bit Field	Field Name	Type	Default Value	Description
0	spi_3wire	RW	0x1	Select SPI 3-wire mode. Selects 3-wire or 4-wire mode. • 0x0 = reserved • 0x1 = 3-wire SPI. Data is received and transmitted on SDA_SDIO

8.13.2 I2C_FLTR_CNFG Register

I²C mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5:4	i2c_speed	RW	0x0	I2C speed selection. Selects the operating speed of the I2C interface. Only the output driver slew rate is affected by this setting (higher setting means higher drive strength). The I2C master must provide the appropriate SCL frequency and other timing requirements according to the selected speed. • 0x0 = 1.8V Standard mode (100 kHz) or 3.3V Standard (100kHz) and Fast mode (400kHz) • 0x1 = 1.8V Fast mode (400 kHz) • 0x2 = reserved • 0x3 = 1.8V and 3.3V Fast mode plus (1 MHz)
3:0	i2c_spike_fltr	RW	0x1	I2C digital spike filter duration. Controls the duration of the digital spike filters on the SCL and SDA inputs, specified in number of system clock cycles. 0 disables filtering.

8.13.3 I2C_TIMING_CNFG Register

I²C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	i2c_sda_high_hold	RW	0x4	I2C/SMBus transmit one bit delay. Delays transmission of 1 value by 8x this number of system clock cycles.
3:0	i2c_sda_low_hold	RW	0x4	I2C/SMBus transmit zero bit delay. Delays transmission of 0 value by8x this number of system clock cycles.

8.13.4 I2C_ADDR_CNFG Register

I²C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:0	i2c_addr	RW	0x09	I2C device address. Sets I2C device address that the SSI acknowledges and accepts accesses on. Bits[1:0] are set by OTP only and can be overridden by pins as per Table 24.

8.13.5 SSI_GLOBAL_CNFG Register

Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	ssi_addr_size	RW	0x0	SSI address size. When 0 the SSI expects 1-byte CSR addresses; when 1 the SSI expects 2-byte CSR addresses. Upper address bits are taken from the SSI's page register to create a full 32-bit CSR address. • 0x0 = 1-byte address • 0x1 = 2-byte address
1:0	ssi_enable	RW	0x1	SSI mode. Selects the serial port mode: • 0x0 = SSI is disabled • 0x1 = SSI is in I2C mode • 0x2 = SSI is in SPI mode • 0x3 = Reserved

8.14 APLL Registers

8.14.1 APLL_FB_DIV_FRAC Register

APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:27	reserved	RO	0x0	reserved.
26:0	apll_fb_div_frac	RW	0x0	APLL Feedback Divider Fraction Numerator. APLL feedback divider numerator value. The denominator is a fixed value of 2^{27}. This register is atomic. When the most significant byte (bits [31:24]) is written, the new value is applied to the APLL.

8.14.2 APLL_FB_DIV_INT Register

APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9:0	apll_fb_div_int	RW	0x6C	APLL Feedback Divider Integer. APLL feedback divider integer value. This register is atomic. When the most significant byte (bits [15:8]) is written, the new value is applied to the APLL.

8.14.3 APLL_FB_SDM_CNFG Register

APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
5	apll_fb_dither_en	RW	0x0	APLL Feedback SDM Dither Enable. Dither enable for the SDM controlling the APLL feedback divider. • 0x0 = dither disabled • 0x1 = dither enabled
4	apll_fb_dither_ns	RW	0x0	APLL Feedback SDM Dither Noise shaping. Dither noise shaping enable for the SDM controlling the APLL feedback divider. • 0x0 = dither not shaped • 0x1 = dither shaped
3:2	apll_fb_dither_gain	RW	0x0	APLL Feedback SDM Dither Gain. Gain control for the SDM controlling the APLL feedback divider. • 0x0 = LSB • 0x1 = 2*LSB • 0x2 = 4*LSB • 0x3 = 8*LSB
1:0	apll_fb_sdm_order	RW	0x3	APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the APLL. • 0x0 = Integer • 0x1 = 1st order • 0x2 = 2nd order • 0x3 = 3rd order

8.14.4 APLL_CNFG Register

APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	apll_ref_sel	RW	0x0	APLL Reference Selection Configuration. • 0x0 = Selects XIN/REF • 0x1 = Selects CLKIN
0	en_doubler	RW	0x1	Frequency doubler enable. Enables the frequency doubler. • 0 = Disable • 1 = Enable

8.14.5 LPF_CNFG Register

APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.

See to APLL Loop Filter (LPF) for details. Use the Renesas Timing Commander Software to provide optimal setting recommendations for a specific device configuration.

Bit Field	Field Name	Type	Default Value	Description
7	apll_vco_filter_byp	RW	0x0	VCO current source filter bypass. • 0 = Filter active • 1 = Filter bypassed

Bit Field	Field Name	Type	Default Value	Description
6:4	cnf_LPF_cp	RW	0x7	Loop filter pole capacitor setting. • 0x0 = 33.3pF • 0x1 = 36pF • 0x2 = 38.7pF • 0x3 = 41.4pF • 0x4 = 44.1pF • 0x5 = 46.8pF • 0x6 = 49.5pF • 0x7 = 52.2pF
3:0	cnf_LPF_res	RW	0x6	Loop filter resistor setting. • 0x0 = 0Ohm • 0x1 = 400Ohm • 0x2 = 800Ohm • 0x3 = 1.2kOhm • 0x4 = 1.6kOhm • 0x5 = 2kOhm • 0x6 = 2.4kOhm • 0x7 = 2.8kOhm • 0x8 = 3.2kOhm • 0x9 = 3.6kOhm • 0xA = 4kOhm • 0xB = 4.4kOhm • 0xC = 4.8kOhm • 0xD = 5.2kOhm • 0xE = 5.6kOhm • 0xF = 6kOhm

8.14.6 LPF_3RD_CNFG Register

APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	byp_p3	RW	0x0	Bypass 3rd pole. This bit can only be set to 1 when operating with an integer feedback divider. • 0 = 3rd pole active • 1 = 3rd pole bypassed
6:4	cnf_LPF_R3	RW	0x3	Loop filter 3rd pole resistor setting. • 0x0 = 0Ohm • 0x1 = 800Ohm • 0x2 = 1.6kOhm • 0x3 = 2.4kOhm • 0x4 = 3.2kOhm • 0x5 = 4kOhm • 0x6 = 4.8kOhm • 0x7 = 5.6kOhm
3	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
2:0	cnf_LPF_C3	RW	0x7	Loop filter 3rd pole capacitor setting. • 0x0 = 2pF • 0x1 = 3pF • 0x2 = 4pF • 0x3 = 5pF • 0x4 = 6pF • 0x5 = 7pF • 0x6 = 8pF • 0x7 = 9pF

8.14.7 APLL_LOCK_CNFG Register

APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	use_raw_lock	RW	0x0	APLL Lock Status Select to Pin. When set, the raw selected lock (precision or original) is sent to the GPIO status pin (LOCK)
8	apll_precision_lock_en	RW	0x1	APLL Precision Lock Detector Enable. When set, enables the lock detector using the ranges controlled by apll_th_refl and apll_th_refh.
7:6	apll_lock_timer	RW	0x2	APLL Lock Timer. Controls the digital debounce interval for the lock indication for the APLL. This duration is a function of the system clock cycles. • 0x0 = 0us • 0x1 = 570 cycles of the system clock • 0x2 = 5700 cycles of the system clock • 0x3 = 57000 cycles of the system clock.
5	sel_1time_lock	RW	0x0	One time lock select. Controls whether lock detection occurs once or continuously. • 0x0 = Real-time lock. • 0x1 = One-time lock. When the lock signal asserts, it remains asserted even if the APLL loses lock.
4	lck_detect_cal_byp	RW	0x0	Lock detect during calibration enable. Selects when the lock detector is enabled. • 0x0 = Lock detector is enabled after VCO calibration completes • 0x1 = Lock detector is enabled during and after VCO calibration
3	lck_byp	RW	0x0	Lock detector disable. • 0x0 = Lock detector is enabled according to lck_detect_cal_byp and sel_1time_lock • 0x1 = Lock detector is disabled and the lock signal is asserted
2:0	lck_detect_ref_sel	RW	0x0	Analog Lock Detect RC filter resistor Selects the filter resistor. C=5pF. • 0x0 = 7.5kΩ • 0x1 = 15kΩ • 0x2 = 23kΩ • 0x3 = 30kΩ • 0x4 = 37.5kΩ • 0x5 = 45kΩ • 0x6 = 53kΩ • 0x7 = 60kΩ

8.14.8 APLL_LOCK_THRSH Register

APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	apll_th_refh	RW	0x8	APLL Precision Lock High Threshold. Controls the high threshold voltage of the precision lock detector. The threshold is approximately 750mV + 20mV * apll_th_refh. The default is around 900mV.
3:0	apll_th_refl	RW	0x8	APLL Precision Lock Low Threshold. Controls the low threshold voltage of the precision lock detector. The threshold is approximately 50mV + 18mV * apll_th_refl. The default is around 200mV.

8.14.9 VCO_CAL_STS Register

APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	vco_cal_fail	RO	0x0	VCO Calibration failed. Indicates whether VCO calibration completed successfully. Valid when vco_cal_done is set to 1. • 0x0 = VCO calibration succeeded • 0x1 = VCO calibration failed
6	vco_cal_done	RO	0x0	VCO Calibration done. Indicates whether VCO calibration is running: • 0x0 = VCO calibration is in progress • 0x1 = VCO calibration is completed
5:0	vco_cap	RO	0x0	VCO Calibration frequency band. Indicates the frequency band selected by the VCO calibration logic. Valid when vco_cal_done is set to 1.

8.14.10 APLL_STS Register

APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_sts	RO	0x0	APLL rail high real-time status. When high, indicates that the APLL is railed high.
1	apll_rail_low_sts	RO	0x0	APLL rail low real-time status. When high, indicates that the APLL is railed low.
0	apll_lock_sts	RO	0x0	APLL lock real-time status. Indicates if the APLL is locked to its reference. • 0x0 = unlocked • 0x1 = locked

8.14.11 APLL_EVENT Register

APLL Event status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_evt	RW1C	0x0	APLL Rail High event. Set to 1 when the APLL lock detects a rail high status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
1	apll_rail_low_evt	RW1C	0x0	APLL Rail Low event. Set to 1 when the APLL lock detects a rail low status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
0	apll_lol	RW1C	0x0	APLL Loss-of-lock event. Set to 1 when the APLL lock status transitions from locked to unlocked. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.

8.14.12 APLL_LOL_CNT Register

APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:0	apll_lol_cnt	RW	0x0	APLL Loss-of-Lock Counter. This counter increments each time the APLL lock status de-asserts, and saturates at 0xF. It is cleared by writing it to 0x0, and can be preset by writing the desired value. Preset can be used either as a debug tool or to cause a threshold alarm to happen sooner because the alarm threshold is not configurable.

8.15 INP Registers

8.15.1 REF_CLK_IN_CNFG Register

Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

Refer to Reference Clock Input Buffer section for details on how to set up this interface. Or use the Renesas Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	en_LVDS	RW	0x0	Reference Clock LVDS Enable. Enables compatible termination when the reference clock input signal is LVDS. • 0 = LVDS input termination is disabled • 1 = LVDS input termination is enabled
8	en_HCSL	RW	0x0	Reference Clock HCSL Enable. Enables compatible termination when the reference clock input signal is HCSL. • 0 = HCSL input termination is disabled • 1 = HCSL input termination is enabled
7	en_ldo_ib	RW	0x1	Reference Clock Input Pad LDO enable. When set, enables the input buffer LDO.

Bit Field	Field Name	Type	Default Value	Description
6	en_selfbias_cmos	RW	0x0	Reference Clock Input Pad internal self-bias enable. When the single-ended reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. • 0x0 = Internal self-bias is disabled (input signal is DC-coupled) • 0x1 = Internal self-bias is enabled (input signal is AC-coupled)
5:4	en_term	RW	0x0	Unused. No defined function. Reserved for future use.
3	en_dc_bias	RW	0x0	Reference Clock Input Pad internal DC bias enable. When the differential reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. • 0 = Internal DC bias is disabled (input signal is DC-coupled) • 1 = Internal DC bias is enabled (input signal is AC-coupled)
2	en_inbuff	RW	0x0	Reference Clock Input Pad enable. The reference clock input pad must be enabled in Jitter Attenuator mode and should be left disabled in synthesizer/DCO mode. • 0 = Input pad is disabled • 1 = Input pad is enabled
1	CMOS_Sel	RW	0x0	Reference Clock Input Pad CMOS/differential select. Configures the reference clock input pad for a single-ended CMOS or differential input signal. • 0 = Differential input is selected • 1 = CMOS input is selected
0	P_N_Diff_Sel	RW	0x0	Reference Clock Input Pad PMOS/NMOS select. Configures the reference clock input pad according to the common mode voltage of the provided input signal. • 0 = PMOS input pair is enabled (low common mode voltage) • 1 = NMOS input pair is enabled (higher common mode voltage)

9. Package Thermal Information

9.1 Epad Thermal Release Path

To maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 23. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as heat pipes. The number of vias (such as heat pipes) are application specific and dependent upon the package power dissipation in addition to electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. Renesas recommends using as many vias connected to ground as possible. Renesas also recommends that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad/slug and the thermal land. Take precautions to eliminate any solder voids between the exposed heat slug and the land pattern. **Note:** These recommendations are to be used as a guideline only. For further information, see the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

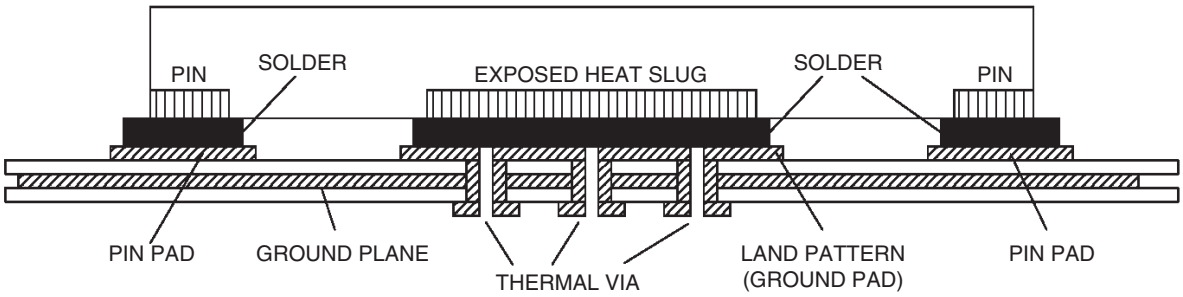


Figure 23. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)

9.2 Thermal Characteristics

Table 41. Thermal Characteristics

Symbol	Parameter		Value	Units
θ_{JA}	Theta J_A. Junction to Ambient Air Thermal Coefficient[1][2]	0 m/s air flow	35.6	°C/W
		1 m/s air flow	32	°C/W
		2 m/s air flow	30.3	°C/W
		3 m/s air flow	29.3	°C/W
θ_{JB}	Theta J_B. Junction to Board Thermal Coefficient[1]		2.6	°C/W
θ_{JC}	Theta J_C. Junction to Device Case Thermal Coefficient[1]		45.1	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)		3	

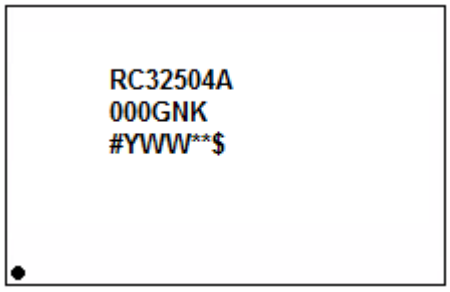
[1] Multi-Layer PCB with 2 ground and 2 voltage planes.

[2] Assumes ePAD is connected to a ground plane using a grid of 9x9 thermal vias.

10. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the Renesas website. The package information is the most current data available, and is subject to change without revision of this document.

11. Marking Diagram



- Lines 1 and 2 indicate the part number.
- Line 3 indicates the following:
  - “#” denotes stepping.
  - “YY” is the last two digits of the year; “WW” is the work week number when the part was assembled.
  - “$” denotes the mark code.

12. Ordering Information

Part Number[1]	Package Description	MSL Rating	Carrier Type	Temperature Range
RC32504AdddGNK#BB0	4 × 4 × 0.75 mm, 24-VFQFN	1	Tray	-40° to +85°C
RC32504AdddGNK#KB0		1	Tape and Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C

[1] Replace ddd with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use 000 for unprogrammed parts.

Table 42. Pin 1 Orientation in Tape and Reel Packaging

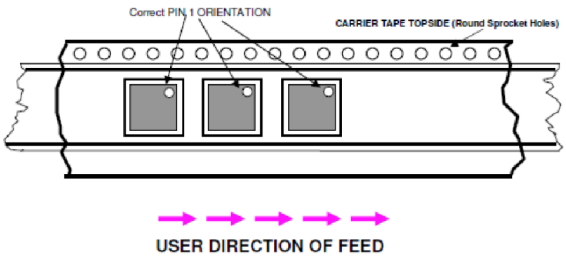
Part Number Suffix	Pin 1 Orientation	Illustration
NK#K	Quadrant 2 (EIA-481-D)	

Table 43. Product Identification

Part Number	Product ID
RC32504A	0x304A

13. Glossary

Term	Definition
3-level	Describes an input structure that support a high, middle and low logic level allowing one of three states to be selected.
ADC	Analog to Digital Converter – These devices require reference clock inputs with strict jitter budgets
AC-coupling	A method of connecting a transmitter to a receiver using series capacitors. This only transmits signal transitions, not DC voltage levels, so can be useful for constantly toggling signals like clocks, especially when trying to isolate the DC voltage levels.
APLL	Analog Phase Lock Loop – PLL technology that uses purely analog circuitry. Useful for low-noise applications without needs for low loop bandwidths or sophisticated switchover techniques.
ASIC	Application Specific Integrated Circuit – Custom chip design usually developed by a system vendor to meet the needs of a specific product family. Not available for general sale. Many ASICs include serial interfaces that need high-performance reference clock inputs
CDR	Clock/Data Recovery – Circuit that recovers a clock from a data stream and uses it to create a sampling clock for data recovery from the stream
C_L	Load Capacitance – A crystal parameter that affects the frequency accuracy of the crystal + oscillator circuit
CLKIN	Clock input signal (may be differential using pins CLKIN/nCLKIN or single-ended using CLKIN or nCLKIN)
CML	Current Mode Logic – A protocol for differential signaling between two chips. Referenced to V_{DD}.
CMOS	Complementary Metal-Oxide Semiconductor – Protocol for single-wire signaling between two chips. Referenced to Ground and VDD
CPLD	Complex Programmable Logic Device – Programmable IC with complexity less than an FPGA. Often used for power-up sequencing on printed circuit board designs
CPU	Central Processing Unit – A type of integrated circuit that executes software. Requires reference clocks with only time-domain jitter specifications.
CRC	Cyclic Redundancy Check – A method of determining if a block of data was stored or transmitted correctly. Involves the addition of one or more bytes of extra information to determine data integrity. One of several algorithms may be used. CCITT-16 is a commonly used algorithm.
DAC	Digital to Analog Converter – These devices require reference clock inputs with strict jitter budgets
DCO	Digitally Controlled Oscillator – An adjustable oscillator for generating frequencies that can be adjusted by writing a digital word to it
DPLL	Digital Phase Lock Loop – Type of PLL that uses at least a digital filter, if not a digital phase detector. Useful for implementing low loop bandwidths and/or complex switchover/holdover techniques
EEPROM	Electrically-Erasable Programmable Read-Only Memory – Commonly used non-volatile memory device.
ESR	Equivalent Series Resistance – A parameter for a quartz crystal indicating its ability to dissipate current from an oscillator circuit
FOD	Fractional Output Divider – Circuit that can divide down a clock frequency using non-integer ratios. Adds flexibility at a cost of increased size, complexity and power consumption and extra spurs
FPGA	Field-Programmable Gate Array – Highly complex custom programmed device that may include CPUs, serial interfaces and other logic. Able to be re-programmed at will. Depending on what it contains, an FPGA may need reference clocks with low or high performance
GPI	General-Purpose Input – An input signal that can be programmed for many different purposes
GPIO	General-Purpose Input/Output – A signal that can be programmed for many different purposes as either an input or an output
GPO	General-Purpose Output – An output signal that may be programmed to be used for many different purposes
GUI	Graphical User Interface – A Timing Commander Personality that includes graphical elements to make device programming simpler
HCSL	High-speed Current Steering Logic – Differential signaling protocol usually associated with PCIe components
HSTL	High-speed Transceiver Logic – Low voltage-swing single-ended signaling protocol. Not often used.
I^2C	Inter-Integrated Circuit signaling protocol – A serial data transmission scheme originally created by Philips Semiconductor and released into the public domain.
IBIS	Input/output Buffer Information Specification – Standard for providing information for signal integrity simulation of an integrated circuit's inputs and outputs

Term	Definition
IDT	Integrated Device Technology – A wholly owned subsidiary of Renesas
IOD	Integer Output Divider – Circuit for dividing down a clock signal using whole numbers only.
LAN	Local Area Network – Wired or wireless communication protocol between PC within a short distance
LGA	Land Grid Array – Type of integrated circuit package that has contact locations around the periphery of the package, but only on the bottom surface
LOL	Loss-of-Lock – A signal or register bit indicating that a PLL is not in the locked state
LOS	Loss-of-Signal – A signal or register bit indicating that a clock input is not receiving a valid input clock
LP-HCSL	Low-Power HCSL – Variant of an HCSL output buffer that includes the transmitter series termination internal to the part
LVDS	Low-Voltage Differential Signaling – Differential signaling protocol using a lower voltage swing. Referenced to VDD.
LVPECL	Low-Voltage Pseudo Emitter-Coupled Logic – Differential signaling protocol using a voltage swing similar to ECL logic, but uses a 2.5V or 3.3V positive reference voltage.
MMD	Multi-Modulus Divider - Clock divider circuit that applies one of several integer divide ratios under control of an SDM.
NTP	Network Time Protocol – Software based protocol that aligns real-time clocks across a wide-area network. Can align to less than 1 second of accuracy.
OCXO	Oven-Controlled Crystal Oscillator – A device that generates a highly stable clock frequency by using an internal oven to maintain the quartz crystal at an even internal temperature
OTN	Optical Transport Network – Asynchronous optical communication protocol defined in ITU-T G.709. Used for high-speed data communications. Able to carry many different protocols at the same time over large distances.
OTP	One-Time Programmable memory – Non-volatile storage medium that allows any individual memory bit to be programmed only once.
OTU3	OTN line rate of approximately 40Gbps
OTU4	OTN line rate of approximately 100Gbps
PCIe	Peripheral Component Interconnect Express – Interchip communication protocol primarily used in PC and datacenter equipment
PHY	Physical Layer Interconnection component. Integrated circuit that formats a signal for transmission over an inter-system interconnect medium. Requires reference clock inputs that may be strict if the interconnect medium is high speed
PLL	Phase Lock Loop – Integrated circuit that generates, cleans up, or translates clock signals
PSRR	Power Supply Rejection Ratio (sometimes referred to as Power Supply Noise Rejection) – Indicates the amount of noise energy received on the power pins of the PLL that appear on the output. May be expressed as a dB ratio of input to output power at the noise frequency or as an absolute value of the output power at the noise frequency
PVT	Process, Voltage, and Temperature – Three axes of stress that affect the performance of an integrated circuit
QFN	Quad Flat No-leads package – Type of integrated circuit package that has interconnection pads on all 4 sides of the package including on the bottom. Often has a heat-dissipation metal slug called an ePAD.
RAM	Random Access Memory – Type of integrated circuit that requires clock signals.
REA	Renesas Electronics America
RMS	Root-Mean-Square – Method of specifying the power content of an oscillating signal.
SD Card	Secure Digital memory card – Popular non-volatile storage medium that involves removable cards. Can provide firmware or software updates to a system.
SDM	Sigma-Delta Modulator - Control logic function that uses a sigma-delta algorithm to control an MMD to generate a fractional divide ratio that is dynamically adjustable to minimize noise contributions.
SPI	Serial Peripheral Interface – Serial communication protocol for inter-chip communication. Originally developed by Motorola Semiconductor. It is widely used in the industry but has never been standardized.
SSC	Spread Spectrum Clock – A clock signal that is modulated at a low rate to reduce electro-magnetic emissions from a system. Primarily used in data center equipment.
SSTL	Stub Series Terminated Logic – Signaling protocol commonly used with Dynamic RAMs
SyncE	Synchronous Ethernet – Extensions to the Ethernet protocol to make it synchronous and so able to transmit frequency information in addition to data. Defined by ITU-T G.8261 and G.8262
TCXO	Temperature Compensated Crystal Oscillator – Electronic component that uses a quartz crystal to generate a reference clock frequency and temperature-compensation logic to stabilize the frequency over temperature. Stability falls between XOs and OCXOs.

Term	Definition
TDC	Time-to-Digital Converter - High precision sampling logic that detects the rising edges on its two input signals and converts the time difference between those two edges into a digital word.
USB	Universal Serial Bus – device-device interconnection protocol used for short-range wired communication. Is used in some systems to provide management access for software or firmware update.
VCO	Voltage Controlled Oscillator - an adjustable oscillator for generating frequencies that can be adjusted by changing the voltage on a control pin
V_{DD}	Generic term used for any power input reference or pin.
V_{DDO}	Power input pins that provide power and set a reference voltage for the output buffers. There are several such pins each associated with specific output buffers.
V_{DDREF}	Power input pin(s) that power and set a reference voltage for the input reference clocks
XO	Crystal Oscillator circuit – electronic component that generates a frequency reference by combining a quartz crystal and an oscillator circuit in a single package. Since the crystal is uncompensated, the frequency stability over temperature may be bad.
Xtal	Crystal – passive quartz crystal that provides a frequency reference when stimulated by an oscillator circuit

14. Device Errata

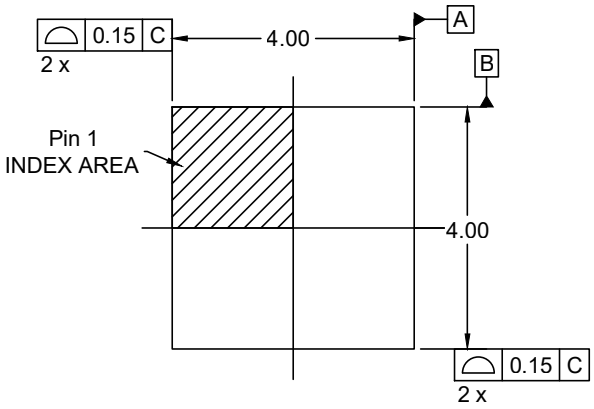
#	Parameter/Function	Description	Work Around
A1	odc, Output Duty Cycle in Table 11.	Violation to max 55% for /11 and /13.	None. Please use a VCO frequency that allows for an even divide to achieve the desired output frequency.

15. Revision History

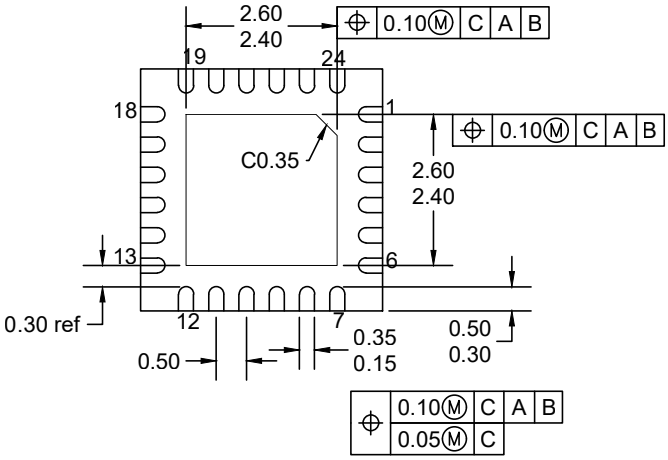
Revision	Date	Description of Change
1.06	Jul 29, 2022	• Updated the input capacitance for nCLKIN in Table 3 • Updated the I²C slave addressing examples in I²C 1-byte (1B) Addressing Example and I²C 2-byte (2B) Addressing Example • Added the Load Level parameter to Table 9
1.05	May 11, 2022	• Removed OTP information • Completed other minor changes
1.04	Mar 18, 2022	Updated the Ordering Information
1.03	Nov 3, 2021	Completed minor changes
1.02	Oct 28, 2021	Added plot diagram Figure 2 “204.8 MHz Output with 93fs Jitter”.
1.01	Jun 3, 2021	• Updated Table 14 • Updated the description of the HCSL internal resistor to 50Ω in Direct-Coupled HCSL Termination and Clock Output Driver
1.00	Mar 30, 2021	Initial release.

Package Outline Drawing

Package Code: NBG24P4
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.5mm Pitch
PSC-4313-04, Revision: 01, Date Created: Mar 16, 2022



TOP VIEW



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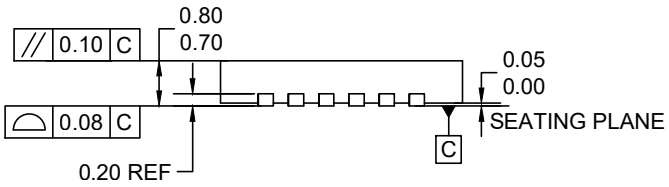
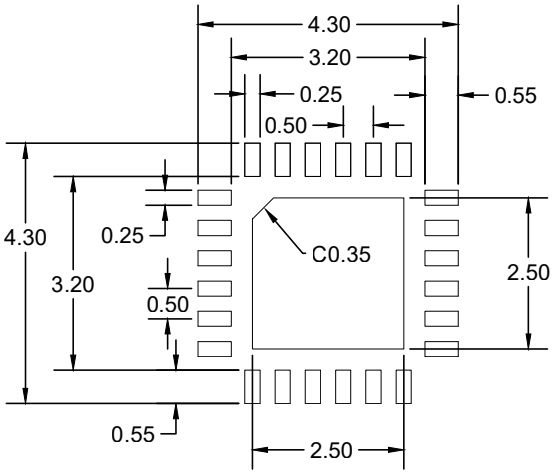


SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatibles.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.