

**PROTECTION PRODUCTS - RailClamp®**
**Description**

RailClamps are ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The RClamp™0544M has a typical capacitance of only 0.30pF. This means it can be used on circuits operating in excess of 2GHz without signal attenuation. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

These devices are in a MSOP 10L package and feature a lead-free, matte tin finish. They are compatible with both lead free and SnPb assembly techniques. They are designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for protecting high-speed HDMI and DVI video interfaces.

**Features**

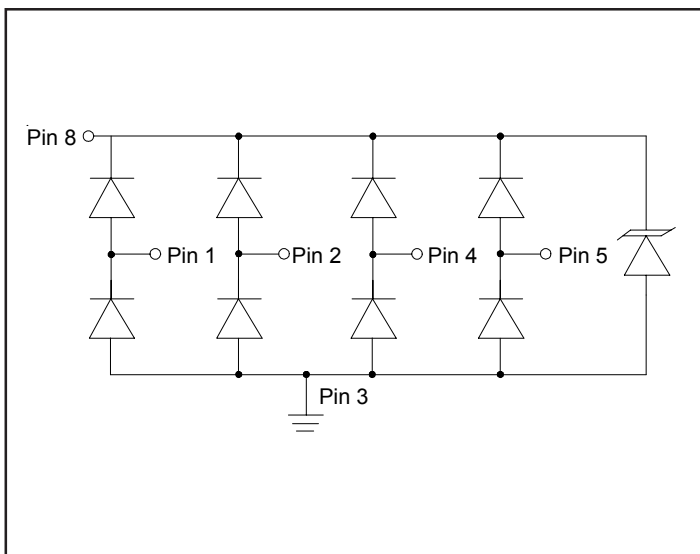
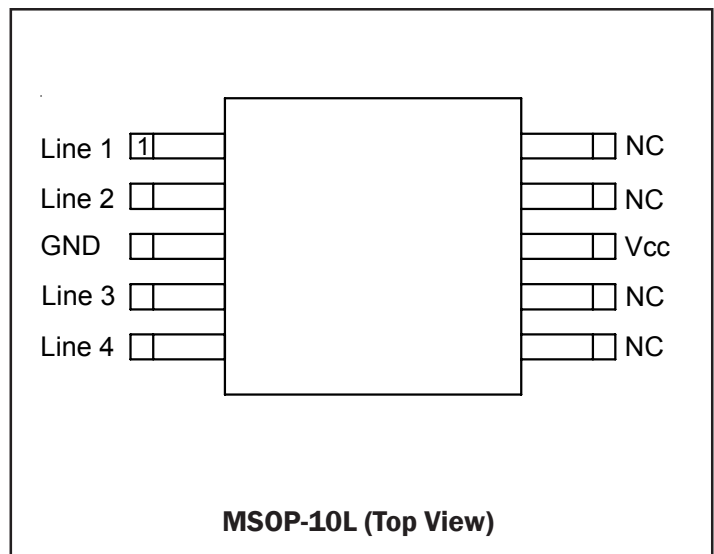
- ◆ ESD protection for high-speed data lines to **IEC 61000-4-2 (ESD)  $\pm 18\text{kV}$  (air),  $\pm 12\text{kV}$  (contact)**
- ◆ **IEC 61000-4-5 (Lightning) 5A (8/20 $\mu\text{s}$ )**
- ◆ **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Array of surge rated diodes with internal TVS Diode
- ◆ Small package saves board space
- ◆ Protects four I/O lines and one Vcc line
- ◆ Low capacitance: **0.3pF** typical (I/O to I/O)
- ◆ Low clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

**Mechanical Characteristics**

- ◆ JEDEC MSOP 10L package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking code and date code
- ◆ Packaging : Tape and Reel per EIA 481
- ◆ Lead Finish: Matte Tin
- ◆ RoHS/WEEE Compliant

**Applications**

- ◆ High Definition Multi-Media Interface (HDMI)
- ◆ Digital Visual Interface (DVI)
- ◆ 10/100/1000 Ethernet
- ◆ Monitors and Flat Panel Displays
- ◆ Notebook Computers
- ◆ Set Top Box
- ◆ Projection TV

**Circuit Diagram**

**Schematic & PIN Configuration**


**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>pk</sub>	125	Watts
Peak Pulse Current (tp = 8/20μs)	I <sub>pp</sub>	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	18 12	kV
Operating Temperature	T <sub>J</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

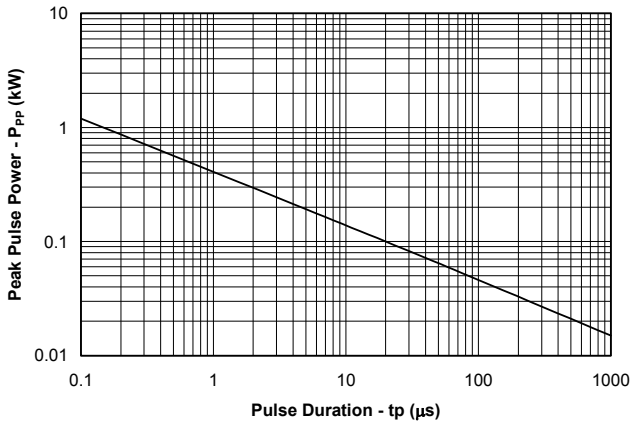
**Electrical Characteristics (T=25°C)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin 3 to 8			5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA Pin 3 to 8	6			V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, T=25 °C Pin 3 to 8			1	μA
Clamping Voltage	V <sub>C</sub>	I <sub>pp</sub> = 1A, tp = 8/20μs Any I/O pin to ground			15	V
Clamping Voltage	V <sub>C</sub>	I <sub>pp</sub> = 5A, tp = 8/20μs Any I/O pin to ground			20	V
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz Between I/O pins		0.30	0.7	pF
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz Any I/O pin to ground		0.70	0.9	pF

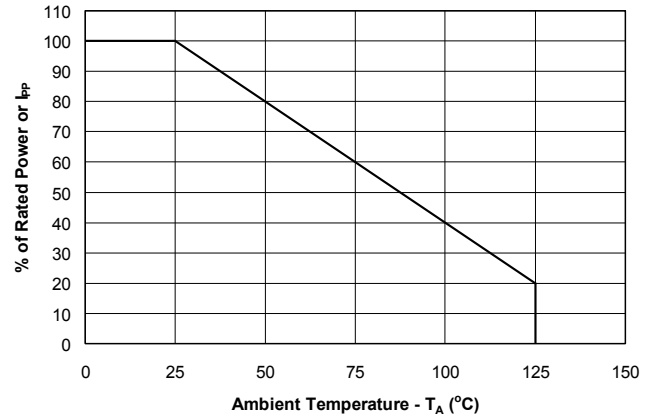
## PROTECTION PRODUCTS

### Typical Characteristics

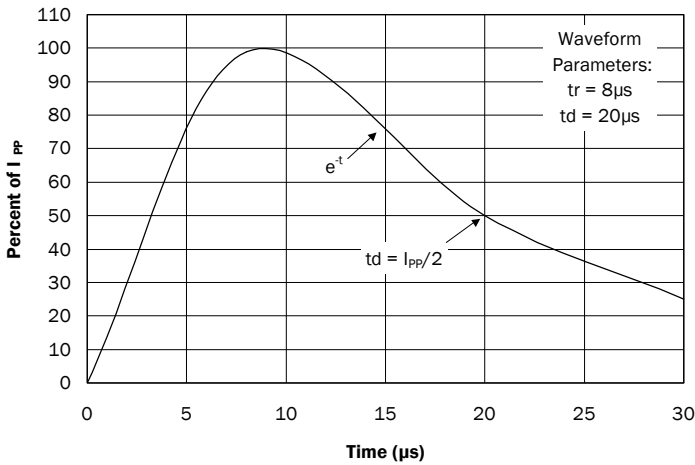
#### Non-Repetitive Peak Pulse Power vs. Pulse Time



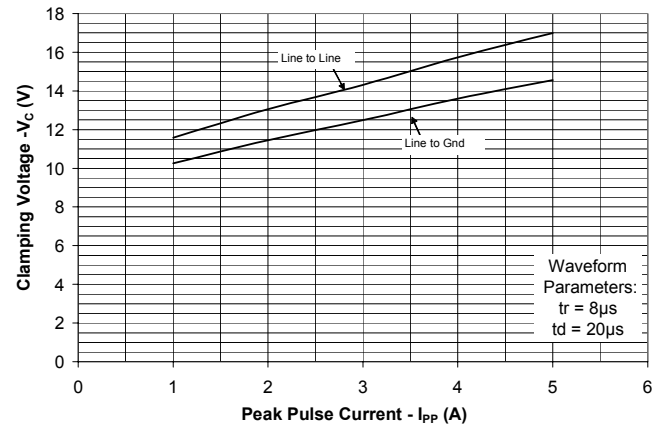
#### Power Derating Curve



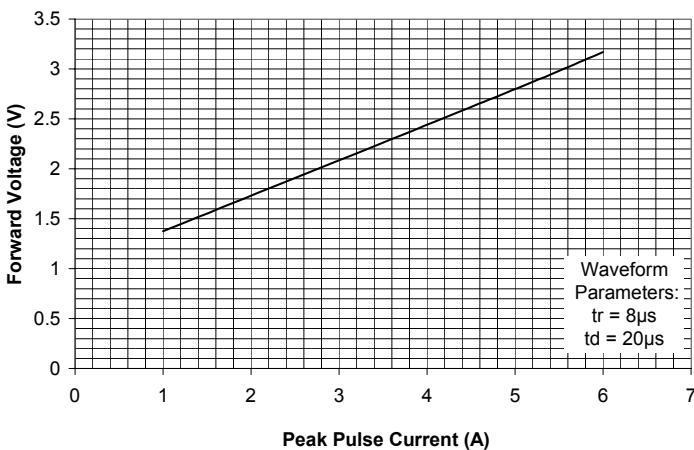
#### Pulse Waveform



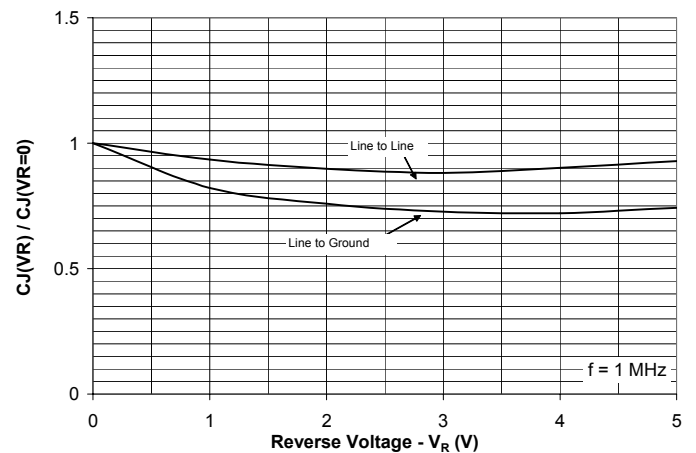
#### Clamping Voltage vs. Peak Pulse Current



#### Forward Voltage vs. Forward Current



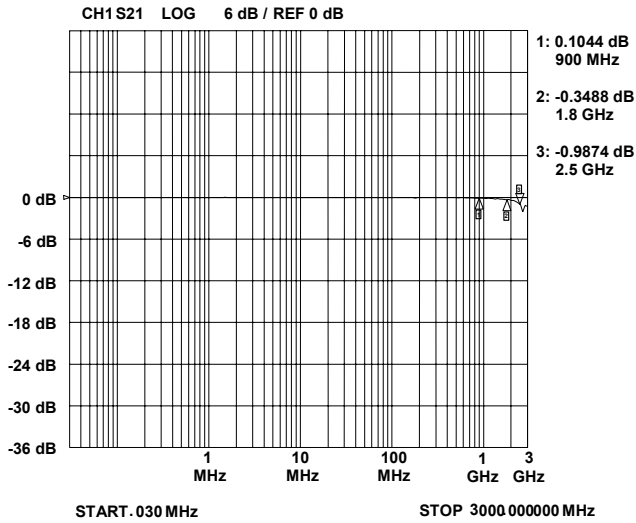
#### Normalized Capacitance vs. Reverse Voltage



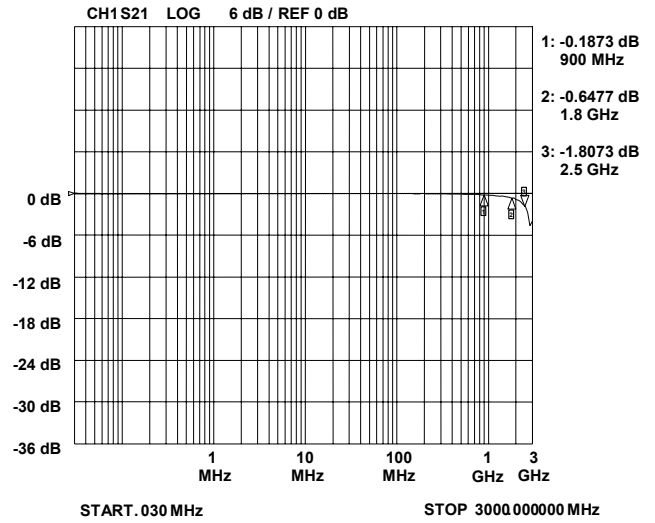
## PROTECTION PRODUCTS

### Typical Characteristics (Con't)

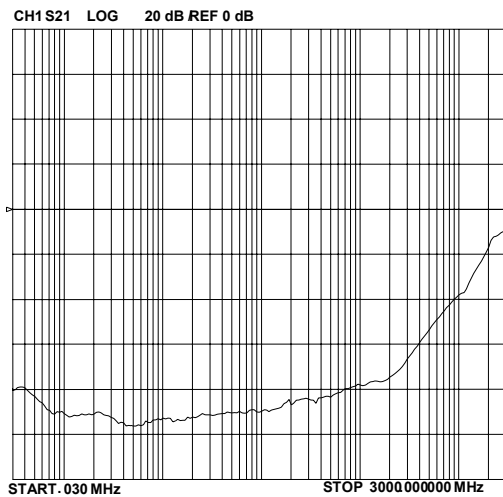
#### Insertion Loss S21 - I/O to I/O



#### Insertion Loss S21 - I/O to GND



#### Analog Cross Talk



## PROTECTION PRODUCTS

### Applications Information

#### Device Connection Options for Protection of Four High-Speed Data Lines

The RClamp0544M TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode  $V_F$ ) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

#### Flow Through Layout

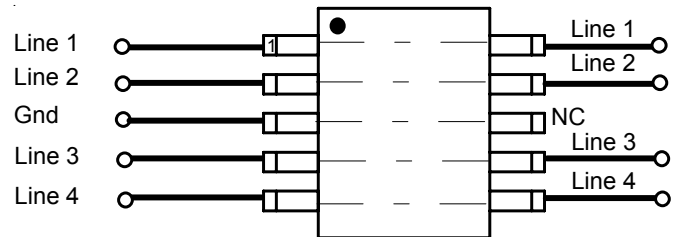
The RClamp0544M is designed for ease of PCB layout by allowing the traces to run straight through the device. Figure 1 shows the proper way to design the PCB board trace in order to use the flow through layout for two line pairs. The solid line represents the PCB trace. Note that the PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines 2, 3, and 4. Ground is connected at pin 3. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

#### Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the device near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Figure 1. Flow through Layout for two Line Pairs



#### Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

## PROTECTION PRODUCTS

### Applications Information (continued)

#### ESD Protection With RailClamps®

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 4 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the  $V_F$  drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the  $V_F$  of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$$V_C = V_{CC} + V_F \quad (\text{for positive duration pulses})$$

$$V_C = -V_F \quad (\text{for negative duration pulses})$$

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 5. Therefore, the actual clamping voltage seen by the protected circuit will be:

$$V_C = V_{CC} + V_F + L_p \frac{di_{ESD}}{dt} \quad (\text{for positive duration pulses})$$

$$V_C = -V_F - L_G \frac{di_{ESD}}{dt} \quad (\text{for negative duration pulses})$$

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

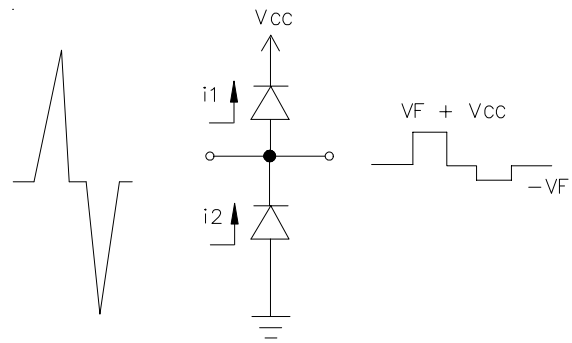
$$V = L_p \frac{di_{ESD}}{dt} = 1 \times 10^{-9} (30 / 1 \times 10^{-9}) = 30V$$

Example:

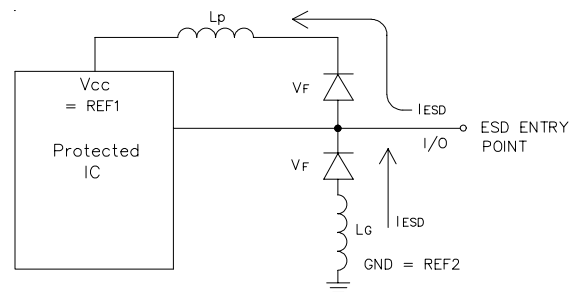
Consider a  $V_{CC} = 5V$ , a typical  $V_F$  of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$$

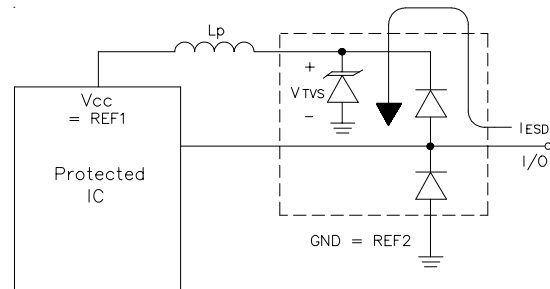
This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the  $V_F$  of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power



**Figure 4 - "Rail-To-Rail" Protection Topology (First Approximation)**



**Figure 5 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection**



**Figure 6 - Rail-To-Rail Protection Using RailClamp TVS Arrays**

dissipation capability of the discrete diode will be exceeded, thus destroying the device.

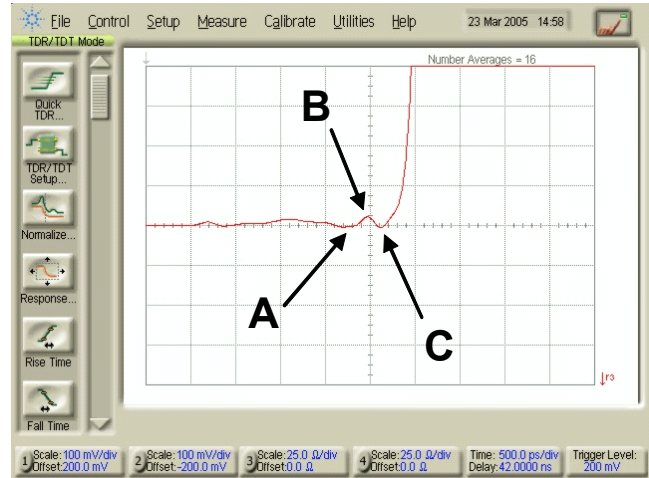
The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device.

## PROTECTION PRODUCTS

### Applications Information (continued)

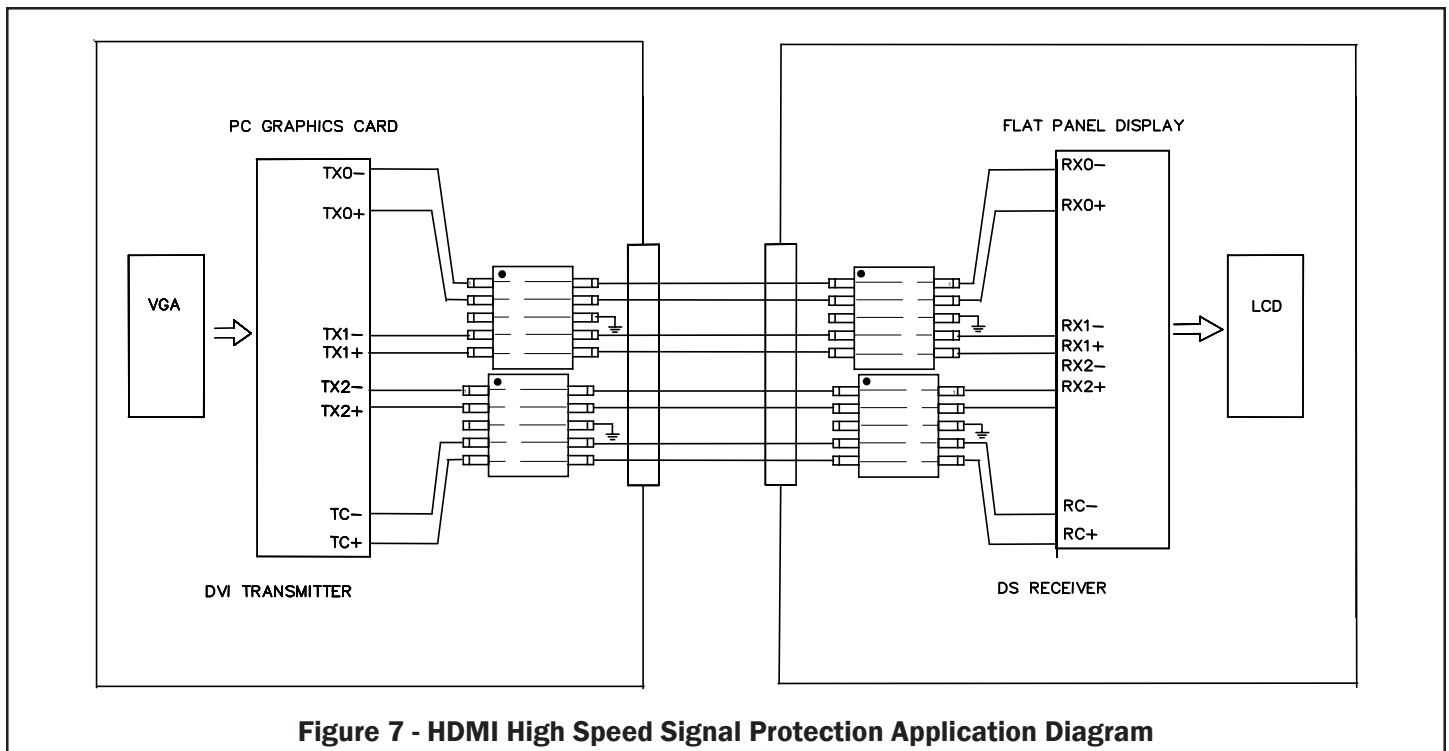
The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%. The measurement is taken using a Time Domain Reflectometry (TDR) method that utilizes a pulse with a risetime  $\leq 200$ ps.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on an HDMI port will cause the impedance of the differential pair to drop. As such, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The RClamp0544M presents  $<1$ pF capacitance between the pairs while being rated to handle  $>8$ kV ESD contact discharges ( $>15$ kV air discharge) as outlined in IEC 61000-4-2. As such, it is possible to make minor adjustments to the board layout parameters to compensate for the added capacitance of the RClamp0544M. Figure 7 shows how to implement the RClamp0544M in an HDMI application (transmitter and receiver). Figure 8 shows impedance test results using a Semtech evaluation board with layout compensation. As shown, the device meets the HDMI CTS impedance requirements.



	A	B	C	
<b>X-axis</b>	1.640	1.796	1.953	<b>(nsec)</b>
<b>Y-axis</b>	99.3	105.3	98.7	<b>(Ohm)</b>

**Figure 8 - TDR Measurement using Semtech Evaluation Board**



**Figure 7 - HDMI High Speed Signal Protection Application Diagram**

PROTECTION PRODUCTS

Applications Information

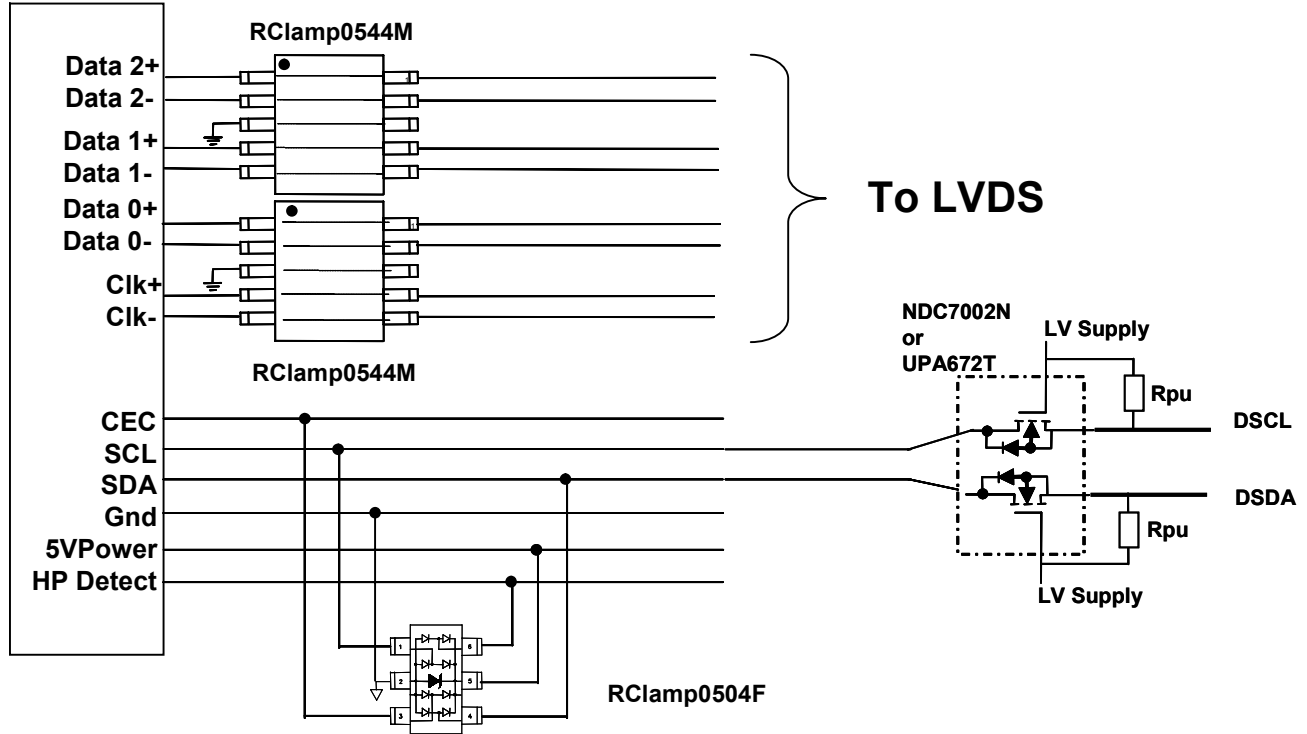


Figure 9 - HDMI Protection for High and Low speed signals



## PROTECTION PRODUCTS

### Applications Information *Spice Model*

#### RClamp0544M Spice Model & Parameters

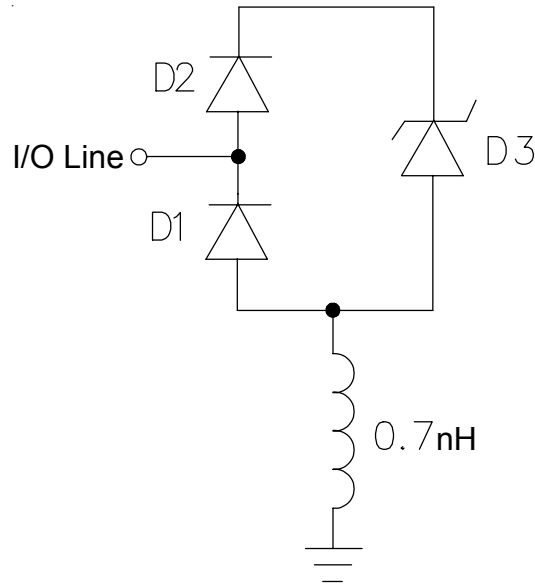
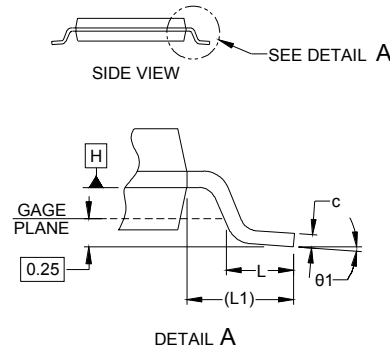
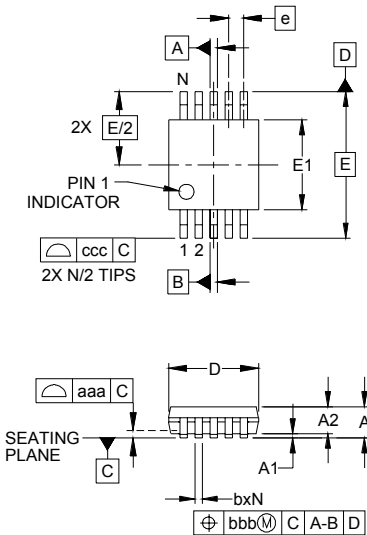


Figure 9 - RClamp0544M Spice Model

Table 1 - RClamp0544M Spice Parameters				
Parameter	Unit	D1 (LCRD)	D2 (LCRD)	D3 (TVS)
IS	Amp	4.01E-18	4.01E-18	3.39E-15
BV	Volt	180	20	7.66
VJ	Volt	0.68	0.67	0.61
RS	Ohm	0.38	0.548	0.637
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	0.7E-12	0.7E-12	190E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.23
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

## PROTECTION PRODUCTS

### Outline Drawing -MSOP 10L

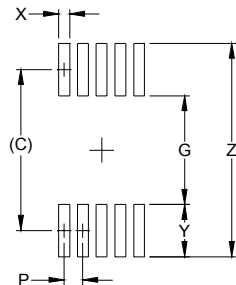


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(0.037)			(0.95)		
N	10			10		
theta 1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

### Land Pattern - MSOP 10L



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

**NOTES:**

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.