RClamp0564P

Femto Farad RailClamp®
4-Line, 170fF ESD Protection

PROTECTION PRODUCTS

Description

RClamp®0564P is an ultra low capacitance ESD protection device specifically designed to protect high-speed differential lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp0564P features extremely good ESD protection characteristics highlighted by low peak ESD clamping voltage, and high ESD withstand voltage (+/-10kV contact per IEC 61000-4-2). RClamp0564P is designed to minimize both the ESD peak clamping and the TLP clamping. Package inductance is reduced at each pin resulting in lower peak ESD clamping voltage. RClamp0564P has a typical capacitance of 0.17pF allowing it to be used in high bandwidth applications such as HDMI 2.0 4K/2K, Thunderbolt, and USB 3.1. Each device will protect four high-speed data lines operating up to 5 volts.

RClamp0564P is in a 5-pin SGP2010N5 package measuring 2.0 x 1.0mm with a nominal height of 0.50mm. The leads have a nominal pin-to-pin pitch of 0.40mm. Flow- through package design simplifies PCB layout and maintains signal integrity on high-speed lines.

Features

- High ESD Withstand Voltage
  - IEC 61000-4-2 (ESD) 10kV (contact)
- Ultra-Low Capacitance: 0.17pF Typical
- Very Small PCB Area
- Protects Four High-Speed Data Lines
- Working Voltage: 5V
- Low Dynamic Resistance: 0.65 Ohms
- Large Operating Bandwidth: 12GHz
- Solid-State Silicon-Avalanche Technology

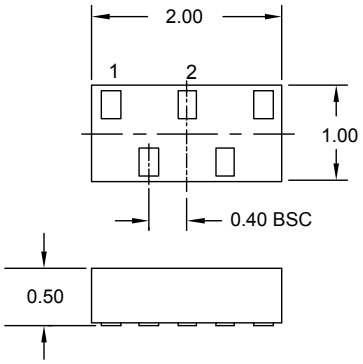
Mechanical Characteristics

- SGP2010N5 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.0 x 1.0 x 0.50 mm
- Lead Pitch: 0.40mm
- Lead Finish: NiPdAu
- Marking : Marking Code
- Packaging : Tape and Reel

Applications

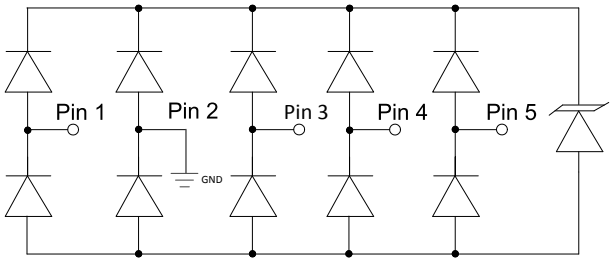
- HDMI 1.4, HDMI1.4b and HDMI 2.0
- DisplayPort
- USB 3.0 and USB 3.1
- USB Type-C
- Thunderbolt
- MIPI / MDDI

Nominal Dimensions



Nominal Dimensions in mm

Schematic



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20µs)	I_{PP}	3	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(2)	V_{ESD}	±10 ±15	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

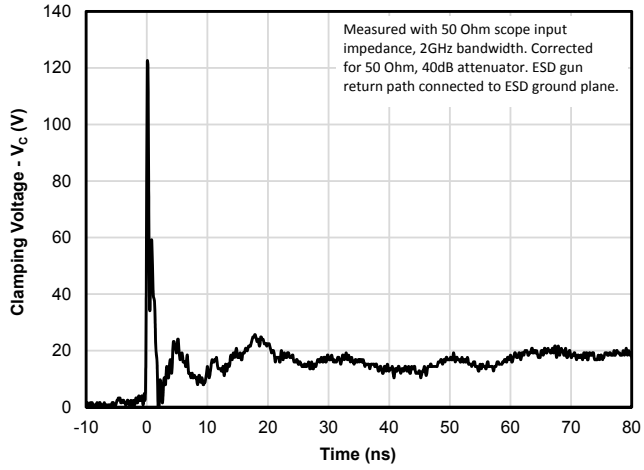
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 85°C				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA	-40°C to 85°C	6.5	9.5	10.5	V
Holding Current	I_H				100		mA
Reverse Leakage Current	I_R	V_{RWM} = 5V	T = 25°C		1	50	nA
			T = 85°C		10	150	nA
Clamping Voltage[3]	V_C	I_{PP} = 3A, tp = 8/20µs			4		V
ESD Clamping Voltage[4]	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP)			5.5		V
ESD Clamping Voltage[4]	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP)			13.5		V
Dynamic Resistance[4, 5]	R_{DYN}	tp = 0.2/100ns (TLP)			0.65		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz	T = 25°C		0.17	0.20	pF
Cutoff Frequency	F_C	-3dB			12		GHz

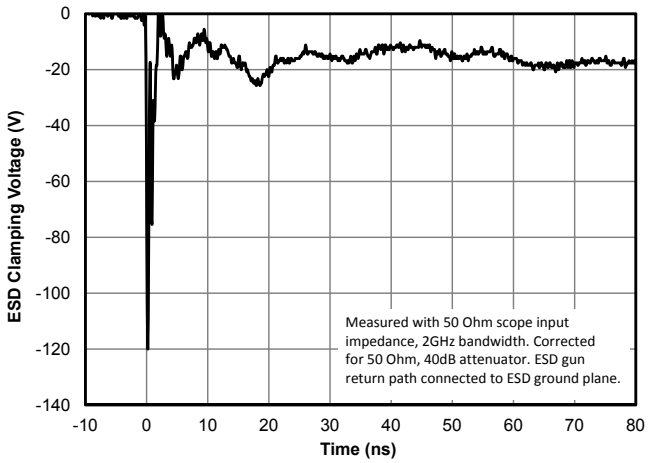
Notes:
(1) Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to Ground Reference Plane (GRP)
(2) In-System ESD withstand voltage
(3) Measured using a 1.2/50us voltage, 8/20us current combination waveform. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(4) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(5) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

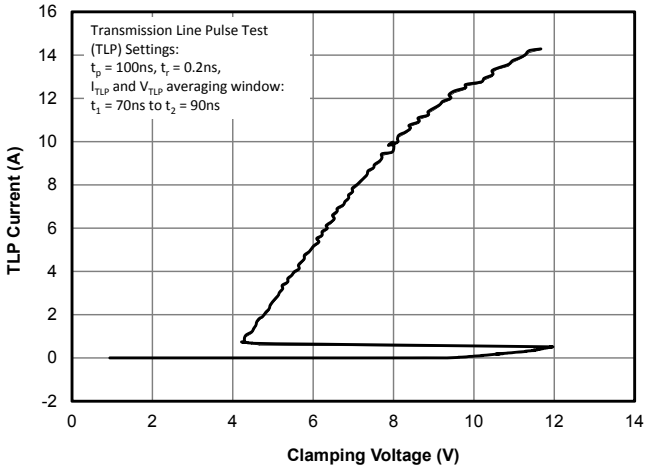
ESD Clamping (+8kV Contact per IEC 61000-4-2)



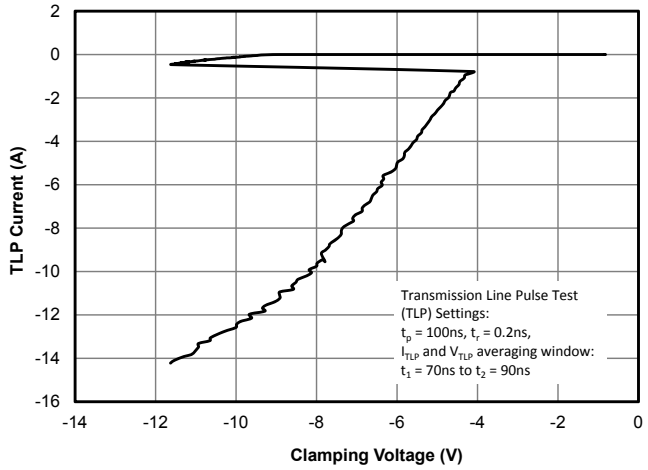
ESD Clamping (-8kV Contact per IEC 61000-4-2)



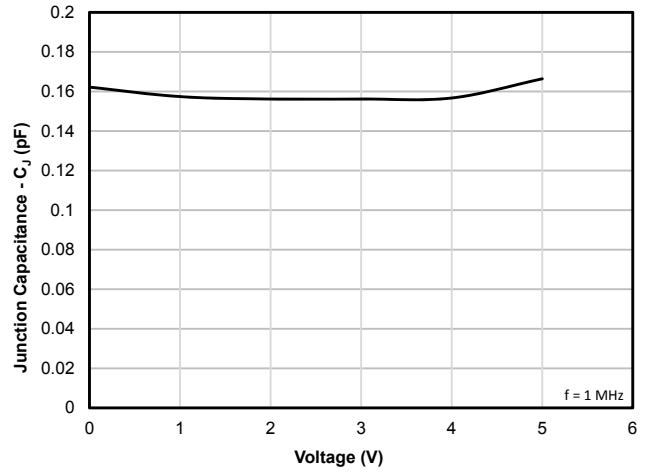
TLP IV Curve - Positive Pulse



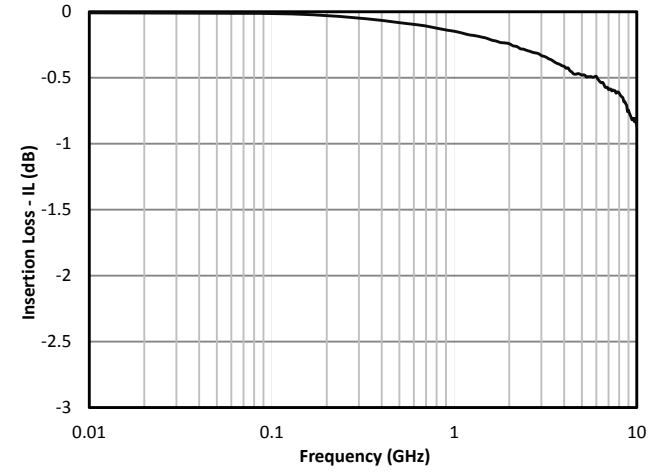
TLP IV Curve - Negative Pulse



Capacitance vs. Reverse Voltage



Insertion Loss (S21)



Application Information

HDMI 2.0 Interface Protection

HDMI 2.0 chips are constantly exposed to external ESD and cable discharge threats. Adding external ESD protection is critical but can be challenging. Both electrical and mechanical requirements must be considered. HDMI 2.0 provides the necessary bandwidth to support the higher resolution and frame rates of Ultra HD. This is accomplished by increasing the data rate on each data lane from 3.4 Gbps to 6 Gbps, which means the protection device must present an extremely low capacitance to preserve signal integrity. The external protection device should also have good ESD protection properties including low ESD peak clamping voltage and low dynamic resistance. Mechanically, the package design should allow the traces to easily flow through the package. This is important since differential pair trace lengths should be matched to avoid signal skew.

Protection Solutions

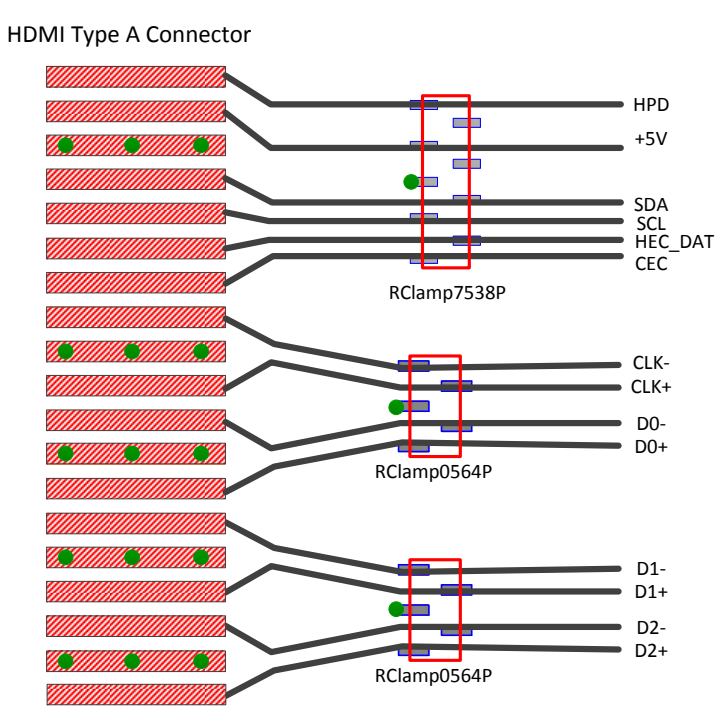
RClamp0564P has been specifically designed to protect high-speed interfaces. It has a typical capacitance of 0.17pF and a flow through package design.

A typical HDMI 2.0 protection solution is shown below. RClamp0564P is used to protect two high-speed differential data pairs. Line pairs are routed through pins 1, 5 and pins 3, 4. Ground connection is made at pin 2. RClamp0564P has little affect on a 5.94Gb/s signal with an HDMI 2.0 eye mask as shown in the eye diagrams below. Two RClamp0564P are required to protect all four clock and data differential pairs. The remaining six lines can also be protected using RClamp0564P. However, since they are not as sensitive to capacitive loading as the TMDS lines, a device such as RClamp7538P may be used as shown.

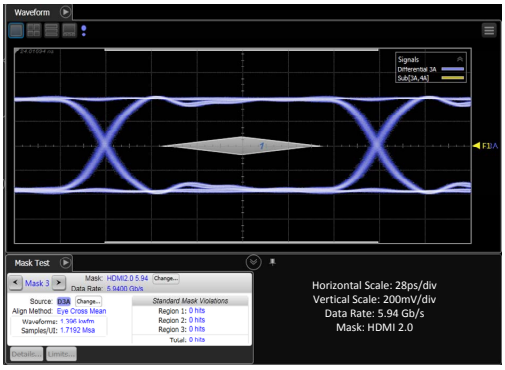
Device Placement

Placement of the protection component is a critical element for effective ESD suppression. TVS diodes should be placed as close to the connector as possible to reduce transient coupling to nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

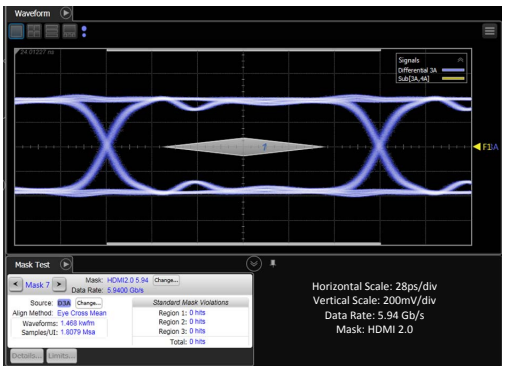
HDMI 2.0 Protection Example



5.94Gb/s Eye Diagram with RClamp0564P



5.94Gb/s Eye Diagram without RClamp0564P



Application Information

DisplayPort Interface Protection

DisplayPort chips are constantly exposed to external ESD and cable discharge threats. Adding external ESD protection is critical but can be challenging. Both electrical and mechanical requirements must be considered. DisplayPort version 1.4 can use the HBR3 transmission mode (32.4 Gbits/s) provides the necessary bandwidth to support the higher resolution and frame rates of Ultra HD. This is accomplished by increasing the data rate on each data lane from 5.4 Gbps to 8.1 Gbps, which means the protection device must present an extremely low capacitance to preserve signal integrity. The external protection device should also have good ESD protection properties including low ESD peak clamping voltage and low dynamic resistance. Mechanically, the package design should allow the traces to easily flow through the package. This is important since differential pair trace lengths should be matched to avoid signal skew.

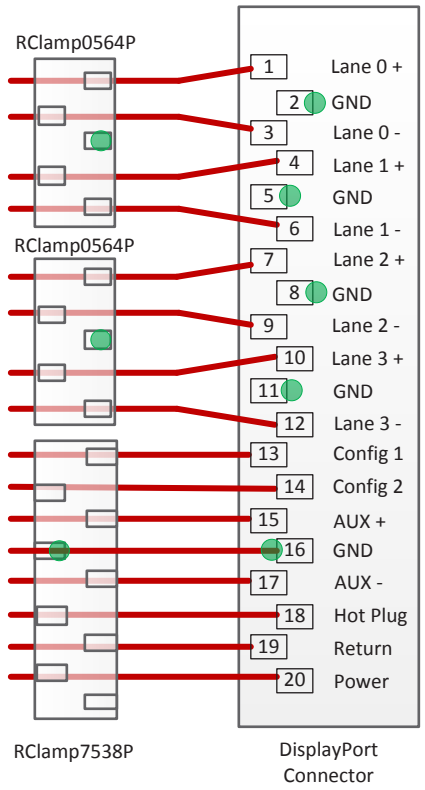
Protection Solutions

RClamp0564P has been specifically designed to protect high-speed interfaces. It has a typical capacitance of 0.17pF and a flow through package design. A typical DisplayPort protection solution is shown below. RClamp0564P is used to protect two high-speed differential data pairs. Line pairs are routed through pins 1, 5 and pins 3, 4. Ground connection is made at pin 2. Two RClamp0564P are required to protect all four clock and data differential pairs. The remaining six lines can also be protected using RClamp0564P. However, since they are not as sensitive to capacitive loading as the ML lines, a device such as RClamp7538P may be used as shown.

Device Placement

Placement of the protection component is a critical element for effective ESD suppression. TVS diodes should be placed as close to the connector as possible to reduce transient coupling to nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

DisplayPort Protection Example



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

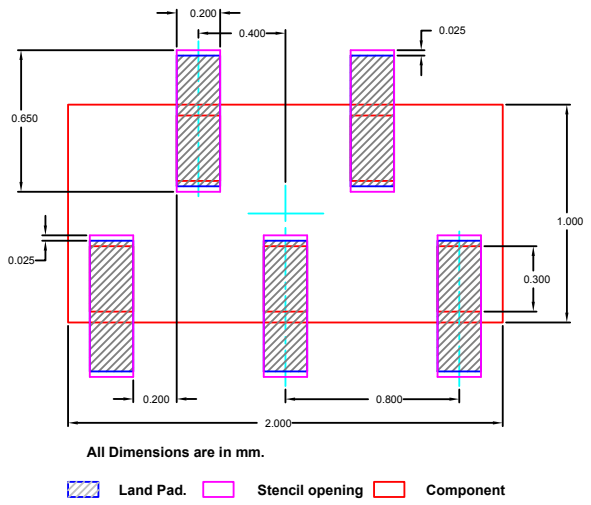
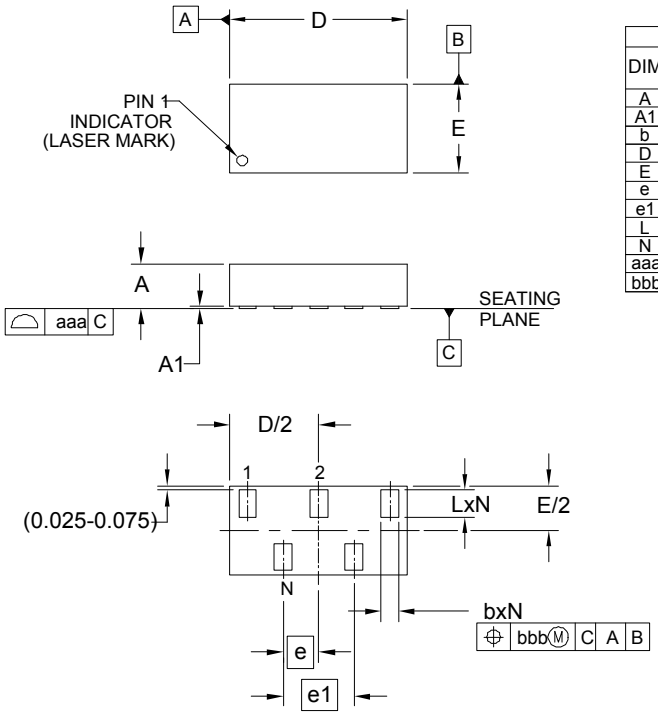


Table 1 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

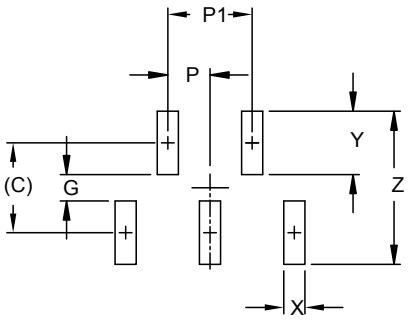
Outline Drawing - SGP2010N5



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.95	2.00	2.08
E	0.95	1.00	1.08
e	0.40 BSC		
e1	0.80 BSC		
L	0.25	0.30	0.35
N	5		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SGP2010N5

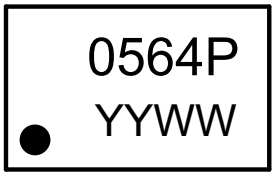


DIMENSIONS	
DIM	MILLIMETERS
C	(0.85)
G	0.25
P	0.40
P1	0.80
X	0.20
Y	0.60
Z	1.45

NOTES:

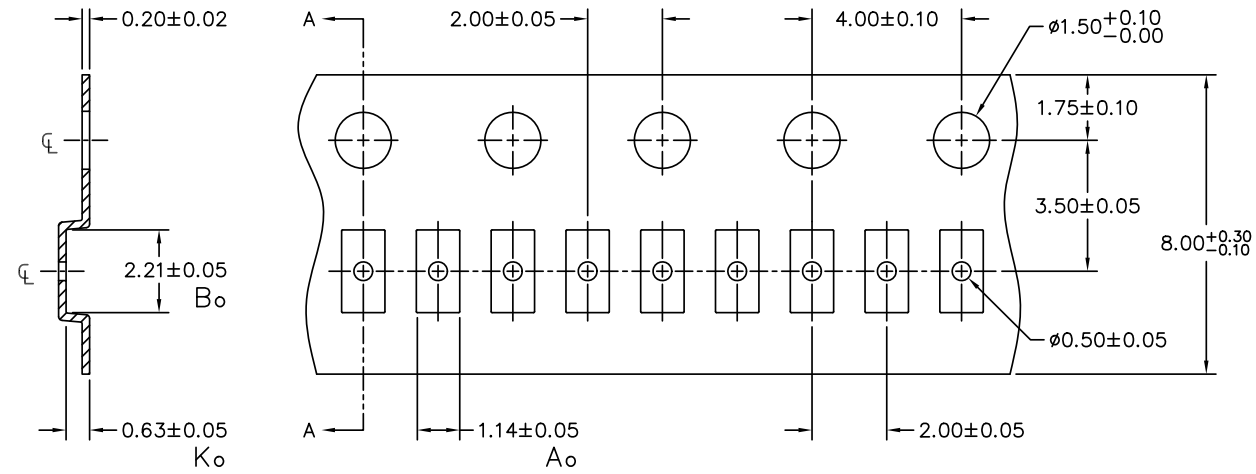
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

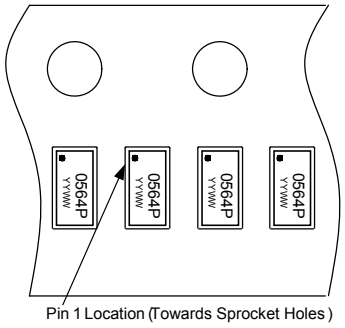


Notes: YYWW = Alphanumeric Date Code

Tape and Reel Specification



NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp0564P.TNT	10000	7 Inch

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