RClamp0584J
Ultra Low Capacitance TVS Array

PROTECTION PRODUCTS - RailClamp®

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The RClamp®0584J has a typical capacitance of only 0.25pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz without signal attenuation. It may be used to meet the ESD immunity requirements of IEC 61000-4-2. Each device is designed to protect four lines (two differential pairs).

The RClamp0584J is in a 10-pin SLP2710P8 package. It measures 2.7 x 1.0 with a nominal height of 0.5mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPdAu. It is designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection makes this device a flexible solution for applications such as HDMI, DisplayPort™, MDDI, and eSATA interfaces.

Features

- ESD protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±18kV (air), ±12kV (contact)
  IEC 61000-4-5 (Lightning) 5A (8/20µs)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Package design optimized for high speed lines
- Flow-Through design
- Protects four I/O lines
- Low capacitance: **0.25pF** typical (I/O to I/O)
- Low clamping voltage
- Low operating voltage: 5V
- Solid-state silicon-avalanche technology

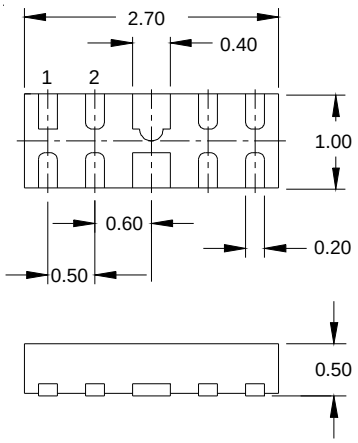
Mechanical Characteristics

- SLP2710P8 10-pin package (2.7 x 1.0 x 0.5mm)
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Pitch: 0.5mm
- Lead finish: NiPdAu
- Marking: Marking Code
- Packaging: Tape and Reel

Applications

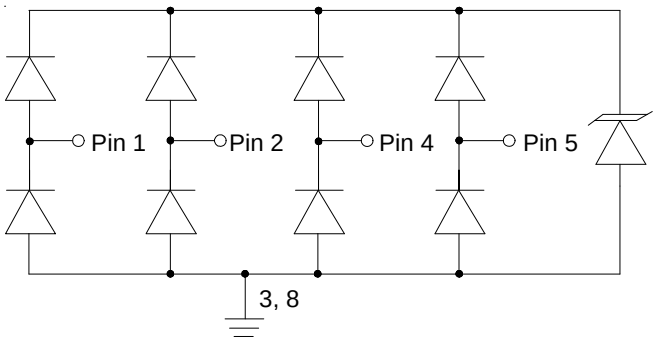
- HDMI 1.3 and HDMI 1.4
- USB 3.0
- Digital Visual Interface (DVI)
- DisplayPort™ Interface
- LVDS Interfaces
- PCI Express
- eSATA Interfaces

Dimensions



Nominal Dimensions in mm

Circuit Diagram



4-Line Protection

Absolute Maximum Rating

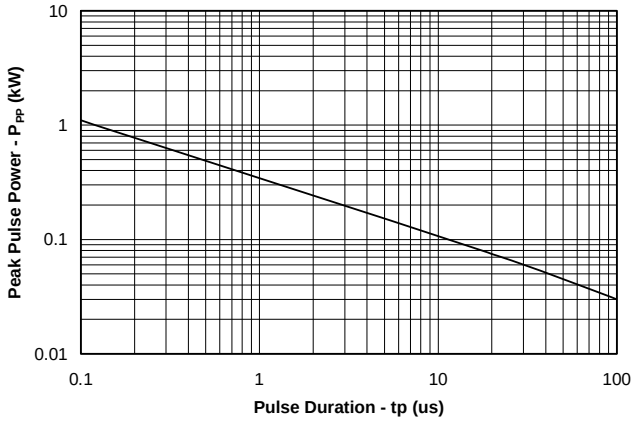
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	75	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 18 +/- 12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

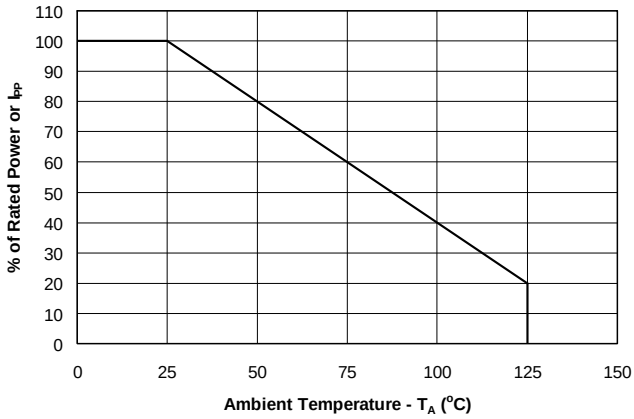
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O to GND			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Any I/O to GND	6.5	8	11	V
Reverse Leakage Current	I_R	V_{RWM} = 5.0V, Any I/O to GND		0.005	0.100	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs Any I/O to GND			12	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Any I/O to GND			15	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz, Any I/O to GND		0.45	0.60	pF
		V_R = 0V, f = 1MHz, Between I/O pins		0.25	0.4	pF

Typical Characteristics

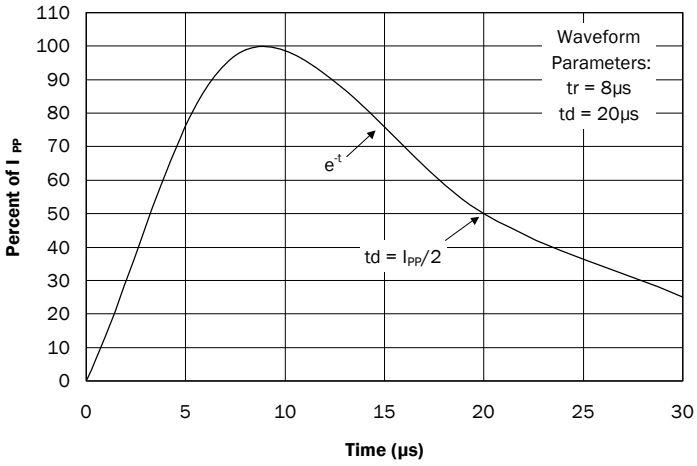
Non-Repetitive Peak Pulse Power vs. Pulse Time



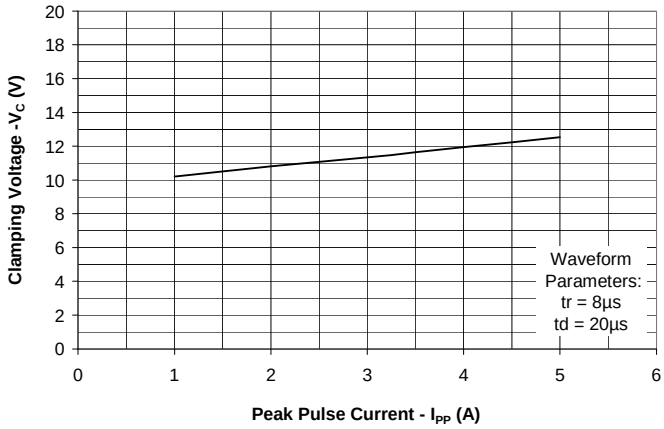
Power Derating Curve



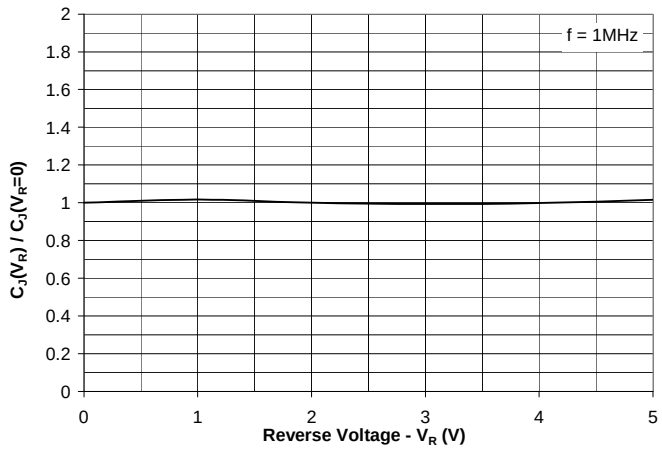
Pulse Waveform



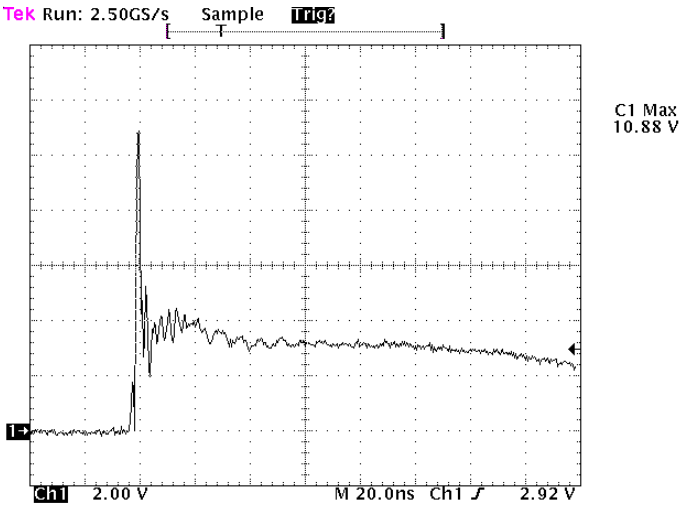
Clamping Voltage vs. Peak Pulse Current (Between any I/O and Ground)



Normalized Capacitance vs. Reverse Voltage



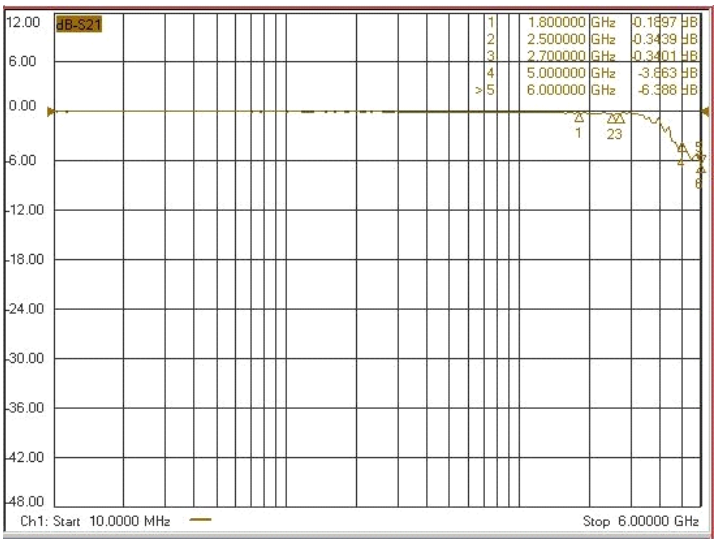
ESD Clamping (Pin 1, 2, 3, or 4 to GND) (+8kV Contact per IEC 61000-4-2)



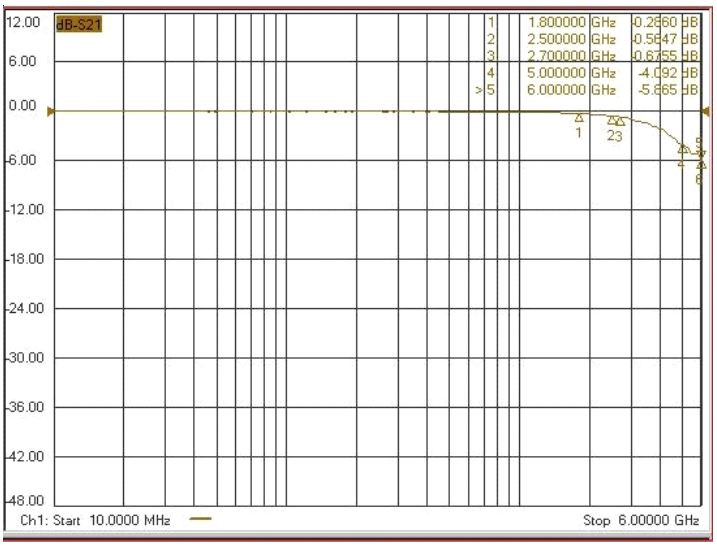
Note: Data is taken with a 10x attenuator

Typical Characteristics (Con't)

Insertion Loss S21 - I/O to I/O



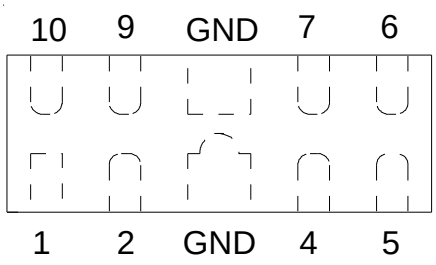
Insertion Loss S21 - I/O to GND



Applications Information

Design Recommendations for HDMI Protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The RClamp0584J is specifically designed for protection of high-speed interfaces such as HDMI. They present <0.3pF capacitance between the pairs while being rated to handle >±8kV ESD contact discharges (>±15kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.



Pin	Identification
1, 2, 4, 5	Input Lines
6, 7, 9, 10	Output Lines (No Internal Connection)
3, 8	Ground

Figure 1 - SLP2710P8 Pin Configuration (Top View)

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the RClamp0584J. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads.

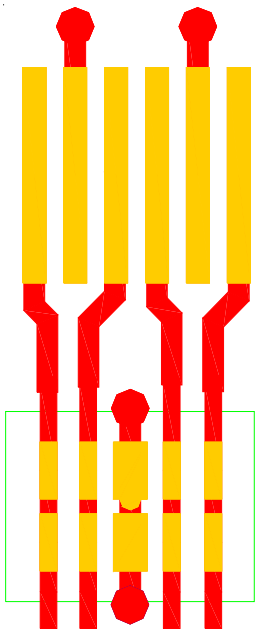


Figure 2 - Flow through Layout Using RClamp0584J

TDR Measurements for HDMI

The combination of low capacitance, small package, and flow-through design means it is possible to use these devices to meet the HDMI impedance requirements of 100 Ohms ±15% without any PCB board modification. Figure 3 shows a typical impedance test result for a TDR risetime of 200ps using a Semtech evaluation board with 100 Ohm traces throughout. Measurements were taken using a TDR method as outlined in the HDMI Compliance Test Specification (CTS). As shown, the device meets the HDMI CTS requirement of 100 Ohm ±15% with plenty of margin.

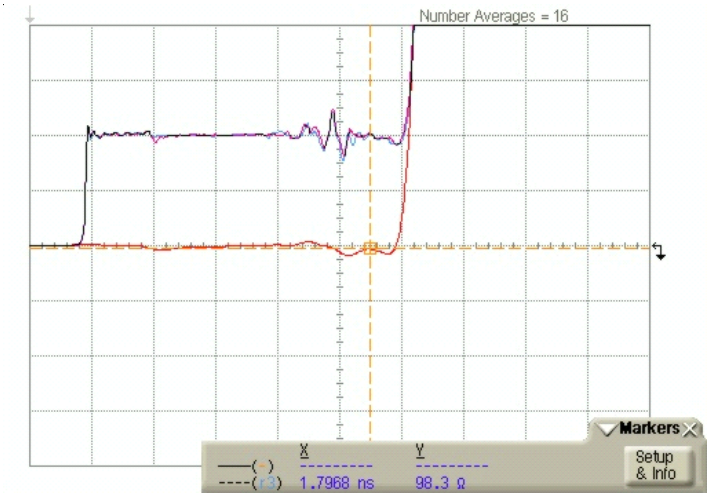
Applications Information

Figure 3 shows a typical HDMI 1.3 eye pattern at 1080p resolution. As shown there are no violations of the eye pattern with RClamp0584J in the circuit. The RClamp0506T can be used to protect the remaining lines (I2C, CEC, hot plug, etc.).

Layout Guidelines for Optimum ESD Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.



X-axis	1.79	**(nsec)**
Y-axis	98.3	**(Ohm)**

Figure 2 - TDR Measurement with 200ps risetime using Semtech Evaluation Board

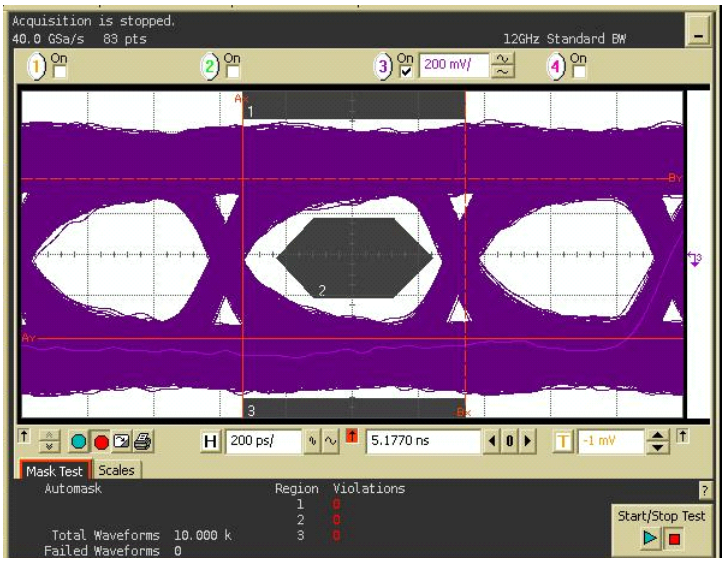
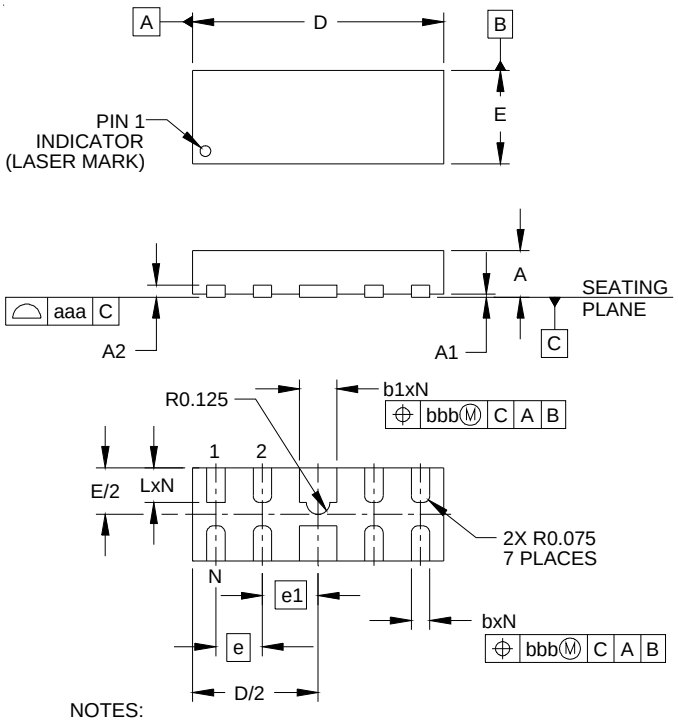


Figure 3 - Typical HDMI 1.3 Eye Pattern (1080p) with RClamp0584J

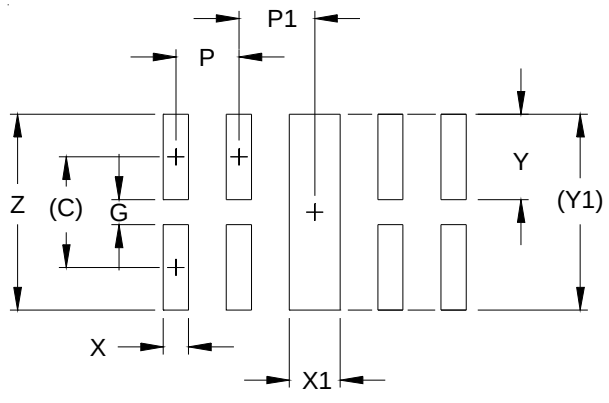
Outline Drawing - SLP2710P8



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.47	0.50	0.53
A1	0.00	0.03	0.05
A2		(0.13)	
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	2.60	2.70	2.80
E	0.90	1.00	1.10
e		0.50 BSC	
e1		0.60 BSC	
L	0.30	0.38	0.43
N		8	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP2710P8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.020	0.50
P1	.024	0.60
X	.008	0.20
X1	.016	0.40
Y	.027	0.675
Y1	(.061)	(1.55)
Z	.061	1.55

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.