

PROTECTION PRODUCTS - RailClamp®
Description

RailClamp® is a low capacitance TVS array designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The RClamp1624T is specifically designed to protect portable devices that utilize a uUSB port. The unique design of this device features low capacitance TVS diodes for protection of the USB data (DP, DM) and USB ID pins operating up to 5 volts. Loading capacitance on these lines is <1pF for maximum signal integrity. An integrated 12 volt TVS diode is used for protection of the USB voltage bus. This ensures the device will remain in a high-impedance state during normal USB operation or when the battery is being charged. Leakage current of the VBus protection is <50nA when operating at 12 volts.

The RClamp1624T is in a 6-pin SLP1710P4T package. It measures 1.7 x 1.0 x 0.40mm. The leads are spaced at a pitch of 0.4mm and are finished with lead-free NiPdAu. They may be used to meet the ESD immunity requirements of IEC 61000-4-2.

Features

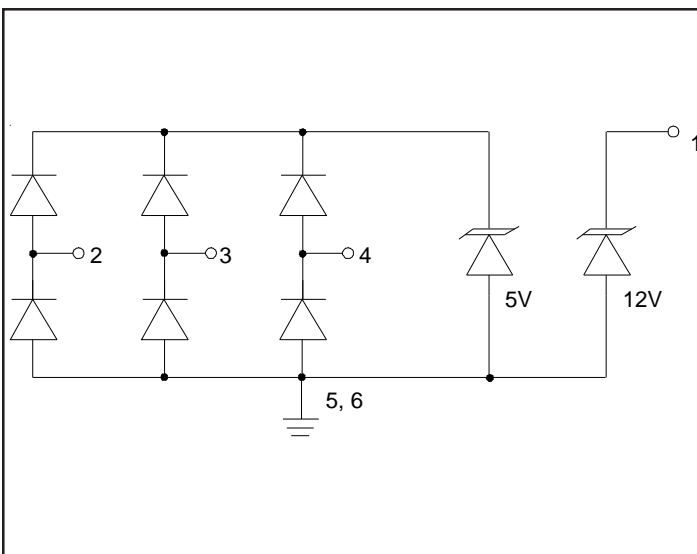
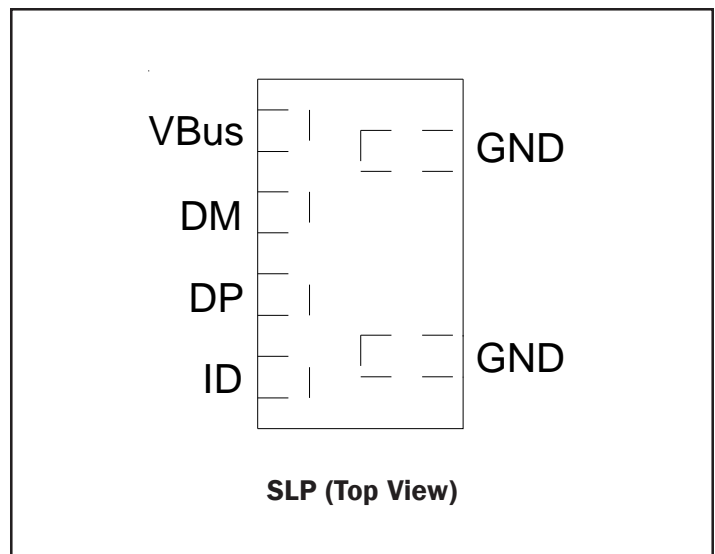
- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) ±18kV (air), ±12kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Array of surge rated diodes with internal TVS Diode
- ◆ Small package saves board space
- ◆ Protects USB DP, DM, and ID Pins to 5V
- ◆ Protects USB VBus operating up to 12V
- ◆ Low capacitance (**<1pF**) on DP, DM, and ID Pins
- ◆ No insertion loss to **2.0GHz**
- ◆ Low leakage current
- ◆ Low clamping voltage
- ◆ Innovative flow-through design allows easy pcb layout
- ◆ Solid-state silicon-avalanche technology

Mechanical Characteristics

- ◆ SLP1710P4T 6L package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Nominal Dimensions: 1.7 x 1.0 x 0.40 mm
- ◆ Lead Finish: NiPdAu
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking code + date code
- ◆ Packaging : Tape and Reel

Applications

- ◆ USB 2.0
- ◆ USB OTG
- ◆ Micro USB

Circuit Diagram

PIN Configuration


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Absolute Maximum Rating

Rating	Symbol	Value	Units
DP, DM, USB ID (Pins 2, 3, 4)			
Peak Pulse Power (tp = 8/20μs)	P_{pk}	75	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±18 ±12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C
VBus (Pin 1)			
Peak Pulse Power (tp = 8/20μs)	P_{pk}	125	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±18 ±12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

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Electrical Characteristics (T = 25°C)

DM, DP, USB ID (Pins 2, 3, 4)						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 2, 3, or 4 to GND			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1\text{mA}$, Pin 2, 3, or 4 to GND	6.5	8	11	V
Reverse Leakage Current	I_R	$V_{RWM} = 5.0\text{V}$, Pin 2, 3, or 4 to GND		0.005	0.100	μA
Forward Voltage	V_F	$I_f = 15\text{mA}$ Pin 2, 3, or 4 to GND	0.6		1.2	V
Clamping Voltage	V_C	$I_{pp} = 1\text{A}$, $t_p = 8/20\mu\text{s}$ Pin 2, 3, or 4 to GND			12	V
Clamping Voltage	V_C	$I_{pp} = 5\text{A}$, $t_p = 8/20\mu\text{s}$ Pin 2, 3, or 4 to GND			15	V
Junction Capacitance	C_j	$V_R = 0\text{V}$, $f = 1\text{MHz}$, Pin 2, 3, or 4 to GND		0.7	0.80	pF
		$V_R = 0\text{V}$, $f = 1\text{MHz}$, Between I/O pins			0.4	pF

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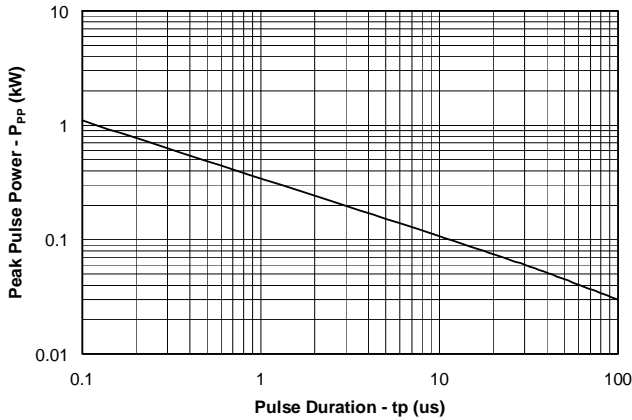
Electrical Characteristics (T = 25°C)

VBus TVS (Pin 1)						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 to GND			12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$, Pin 1 to GND	15	16.5	18	V
Reverse Leakage Current	I_R	$V_{RWM} = 12V$ Pin 1 to GND		0.005	0.05	μA
Forward Voltage	V_F	$I_f = 10mA$ GND to Pin 1	0.6		1.0	V
Clamping Voltage	V_C	$I_{PP} = 5A$, $t_p = 8/20\mu s$ Pin 1 to Ground			25	V
Forward Clamping Voltage	V_{FC}	$I_{PP} = 10A$, $t_p = 8/20\mu s$ Ground to Pin 1			3	V
Junction Capacitance	C_j	$V_R = 0V$, $f = 1MHz$ Pin 1 to GND		50	75	pF

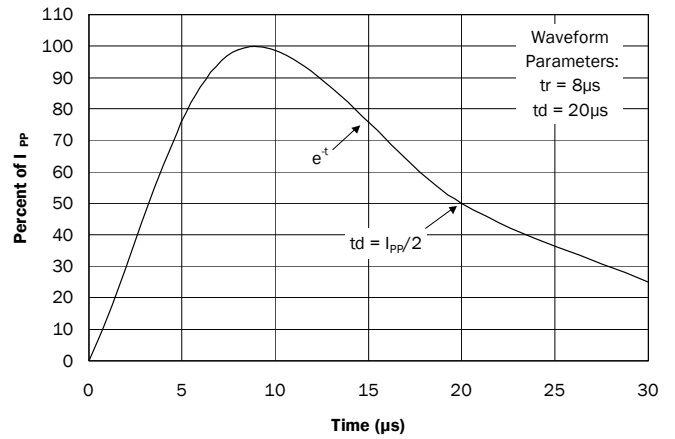
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Typical Characteristics

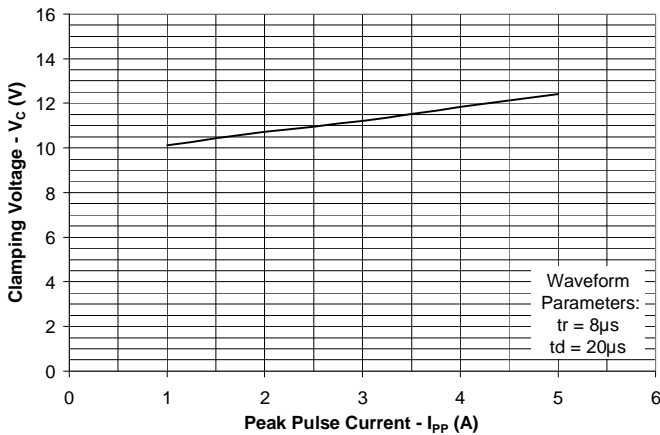
**Non-Repetitive Peak Pulse Power vs. Pulse Time
(Data Lines - Pins 2, 3, 4 to GND)**



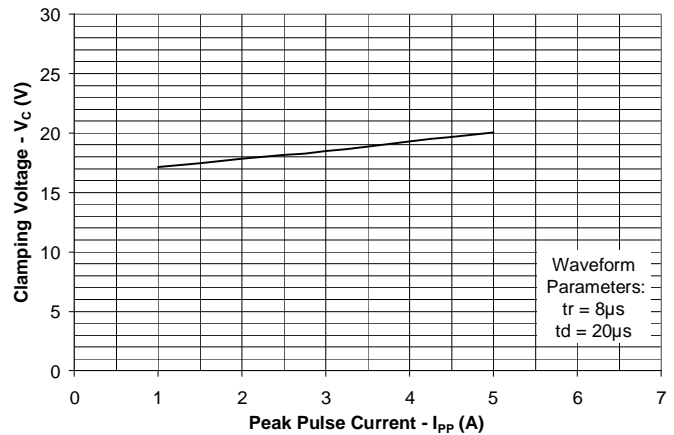
Pulse Waveform



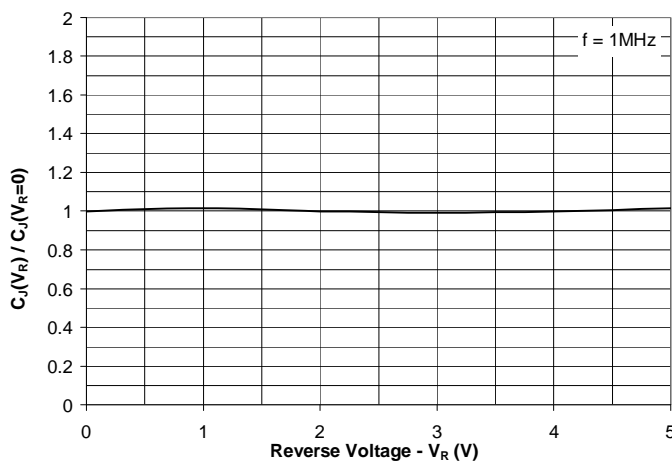
**Clamping Voltage vs. Peak Pulse Current
(Data Lines - Pins 2, 3, 4 to GND)**



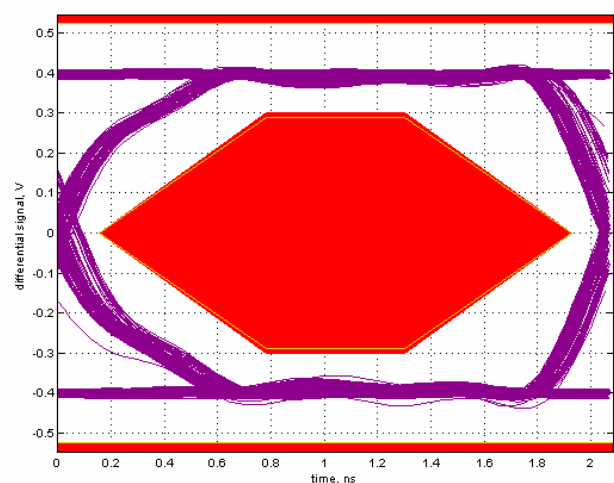
**Clamping Voltage vs. Peak Pulse Current
(VBus - Pin 1 to GND)**



**Normalized Capacitance vs. Reverse Voltage
(Data Lines - Pins 2, 3, 4 to GND)**



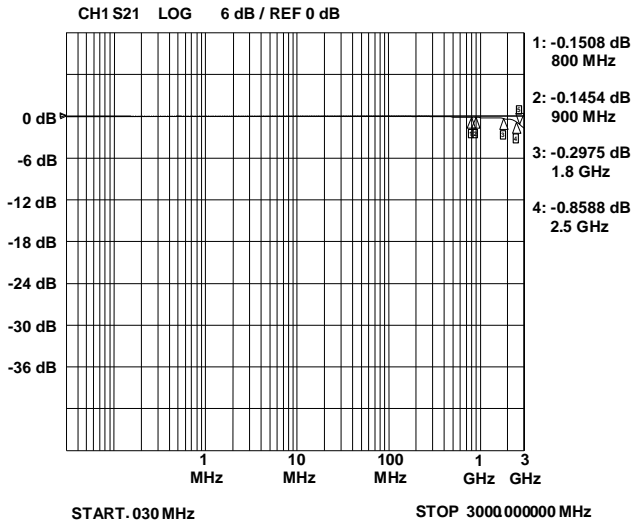
**USB 2.0 Eye Pattern with RClamp1624T
(Data Lines - Pin 2 and 3)**



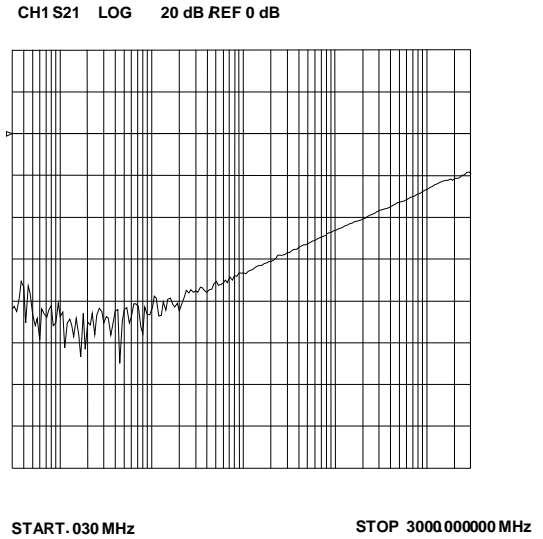
PROTECTION PRODUCTS

Typical Characteristics

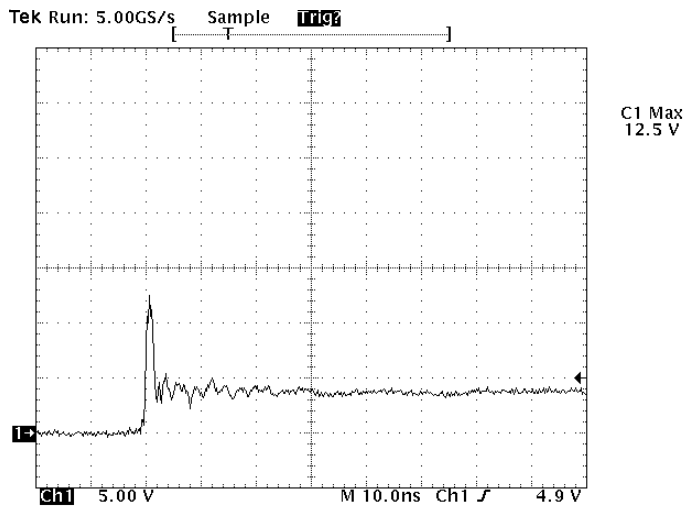
Insertion Loss S21
(Data Lines - Pins 2, 3, 4 to GND)



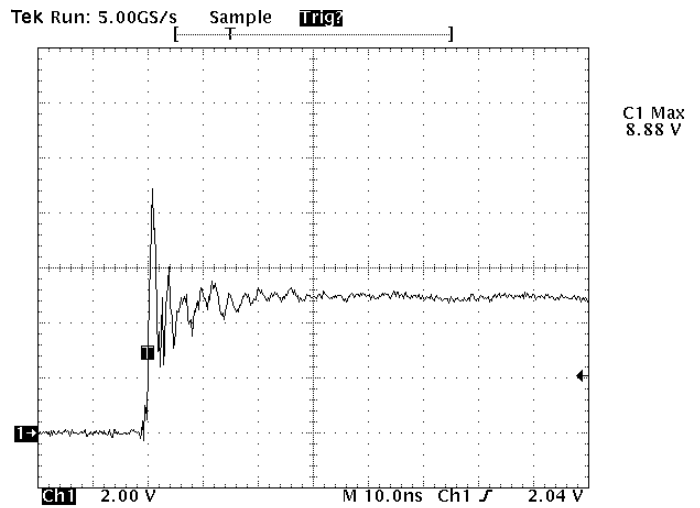
Analog Crosstalk



ESD Clamping (Pins 2, 3, 4 to GND)
(8kV Contact per IEC 61000-4-2)



ESD Clamping (Pin 1 to GND)
(8kV Contact per IEC 61000-4-2)



Note: Data is taken with a 10x attenuator

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Applications Information

Device Connection and Layout Options for Protecting One USB Port

The RClamp1624T is optimized for protection of USB ports. Low capacitance protection is provided for the USB data (DM, DP) and USB ID pins. The maximum capacitance on these lines is <math><1\text{pF}</math> for maximum signal integrity. USB Data and ID lines are connected at pins 2, 3, and 4. These inputs are referenced to an internal 5 volt TVS protection device. When the voltage on these lines exceed 5 volts, the TVS will conduct. Pin 1 is connected to the USB voltage bus (VBus). This device will conduct when the voltage on the bus exceeds 12 volts. Ground is provided at pins 5 and 6. Note that it is not necessary to connect both ground pins of the device as both are connected internally. Multiple micro vias connected to ground are recommended for best ESD performance. This will reduce parasitic inductance in the ground path and minimize the clamping voltage seen by the protected device. The package is designed for easy trace routing as shown in Figure 2. In this example, the VBus pin is connected to the voltage layer of the PCB with a micro via. Connection to ground is made at pin 6 using two micro vias. Connection to the ID pin is shown, however if the application does not utilize the ID function, pin 4 can be left not connected.

Figure 1- Pin Configuration

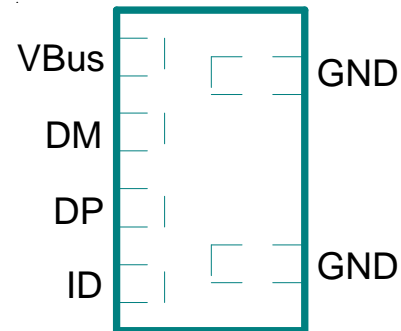
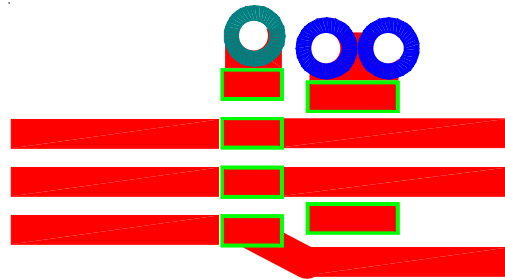
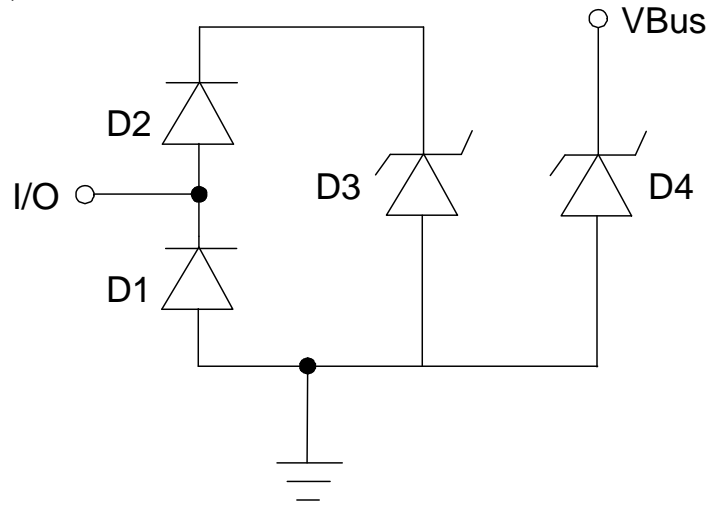


Figure 2 - Layout Example

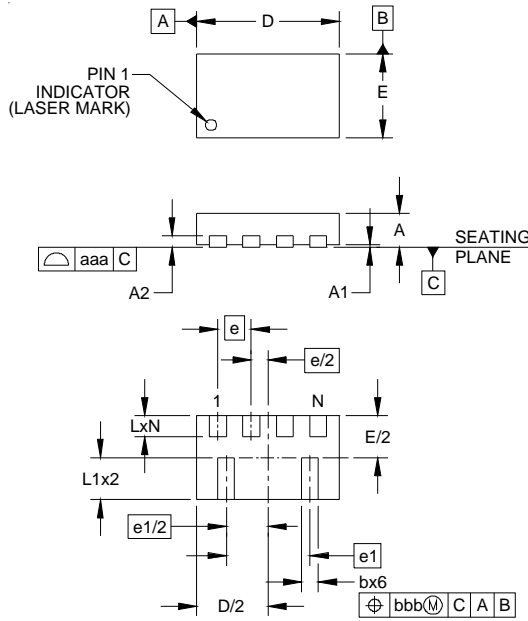


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Applications Information - Spice Model

Spice Model

RClamp1624T Spice Parameters					
Parameter	Unit	D1	D2	D3	D4
IS	Amp	1E-20	1E-20	2E-12	7.38E-15
BV	Volt	100	100	8.2	16.4
VJ	Volt	0.83	0.83	0.6	0.73
RS	Ohm	1.5	0.6	0.2	0.735
IBV	Amp	1E-3	1E-3	1E-3	1E-3
CJO	Farad	0.25E-12	0.25E-12	56E-12	51E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.23	0.30
N	--	1.1	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11	1.11

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Outline Drawing - SLP1710P4T

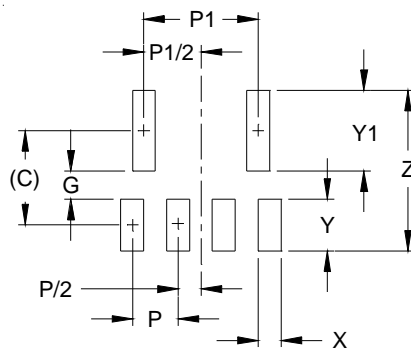


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.37	0.40	0.43
A1	0.00	0.02	0.05
A2	(0.13)		
b	0.15	0.20	0.25
D	1.65	1.70	1.78
E	0.95	1.00	1.08
e	0.40 BSC		
e1	1.00 BSC		
L	0.20	0.25	0.30
L1	0.45	0.50	0.55
N	4		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - SLP1710P4T



DIMENSIONS	
DIM	MILLIMETERS
C	(0.825)
G	0.25
P	0.40
P1	1.00
X	0.20
Y	0.45
Y1	0.70
Z	1.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.