

PROTECTION PRODUCTS - RailClamp®

Description

RailClamp® is a low capacitance TVS array designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The RClamp1644T is specifically designed to protect portable devices that utilize a uUSB port. The unique design of this device features low capacitance TVS diodes for protection of the USB data (DP, DM) and USB ID pins operating up to 5 volts. Loading capacitance on these lines is <0.6pF for maximum signal integrity. An integrated 12 volt TVS diode is used for protection of the USB voltage bus. This ensures the device will remain in a high-impedance state during normal USB operation or when the battery is being charged. Leakage current of the VBus protection is <50nA when operating at 12 volts.

The RClamp1644T is in a 6-pin SLP1508N5T package. It measures 1.5 x 0.8 x 0.40mm. The leads are spaced at a pitch of 0.35mm and are finished with lead-free NiPdAu. They may be used to meet the ESD immunity requirements of IEC 61000-4-2.

Features

- ◆ ESD protection for high-speed data lines to **IEC 61000-4-2 (ESD) ±25kV (air), ±20kV (contact) IEC 61000-4-5 (Lightning) 10A (8/20µs) IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Protects USB DP, DM, and ID Pin operating to 5V
- ◆ Protects USB VBus operating up to 12V
- ◆ Low capacitance (**<0.60pF**) on DP, DM, and ID Pins
- ◆ Low clamping voltage
- ◆ Extremely low dynamic resistance: 0.33 Ohms (Typ) on DP, DM, and ID Pins
- ◆ Innovative flow-through design allows easy pcb layout
- ◆ Solid-state silicon-avalanche technology

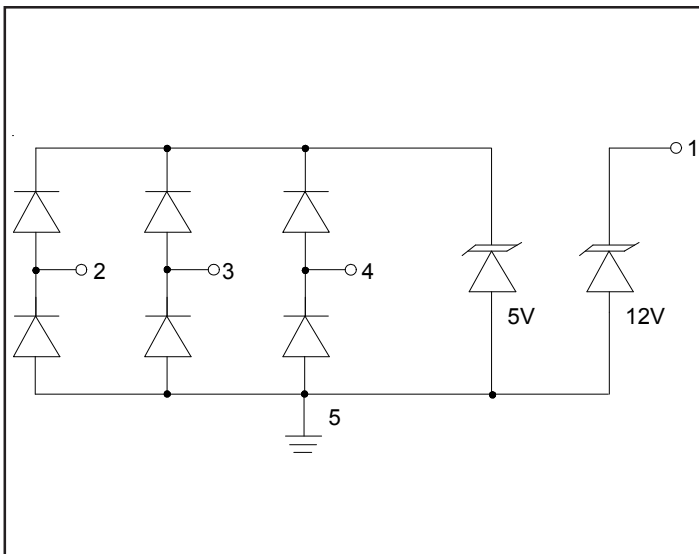
Mechanical Characteristics

- ◆ SLP1508N5T 5L package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Nominal Dimensions: 1.5 x 0.8 x 0.40 mm
- ◆ Lead Finish: NiPdAu
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking code + date code
- ◆ Packaging : Tape and Reel

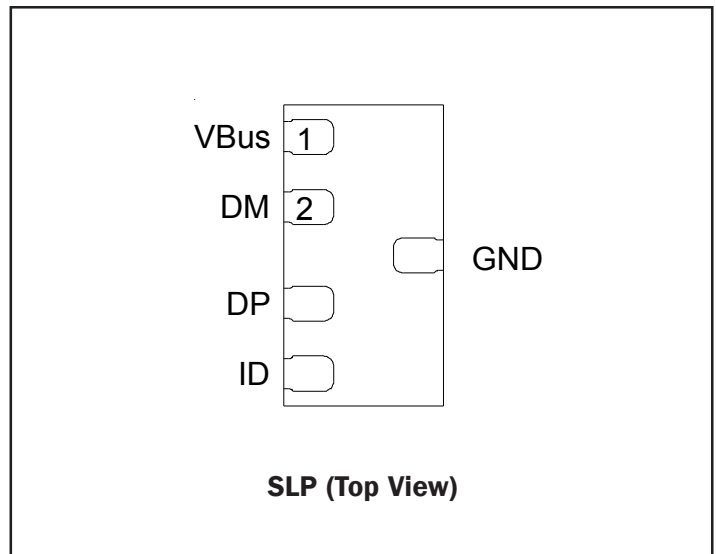
Applications

- ◆ USB 2.0
- ◆ USB OTG
- ◆ Micro USB

Circuit Diagram



Pin Configuration



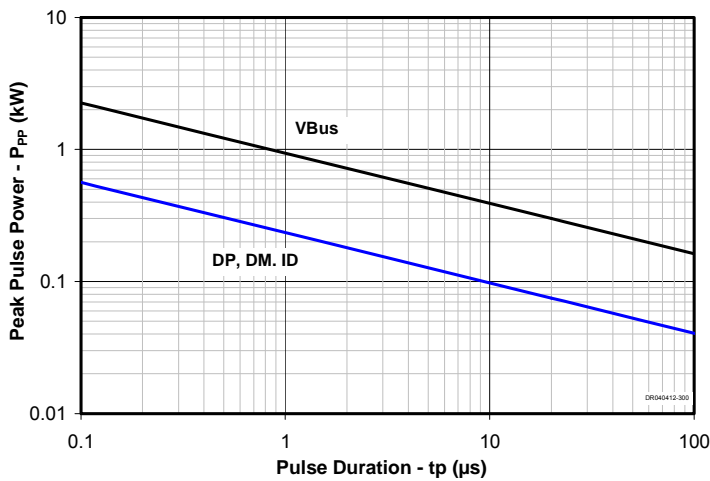
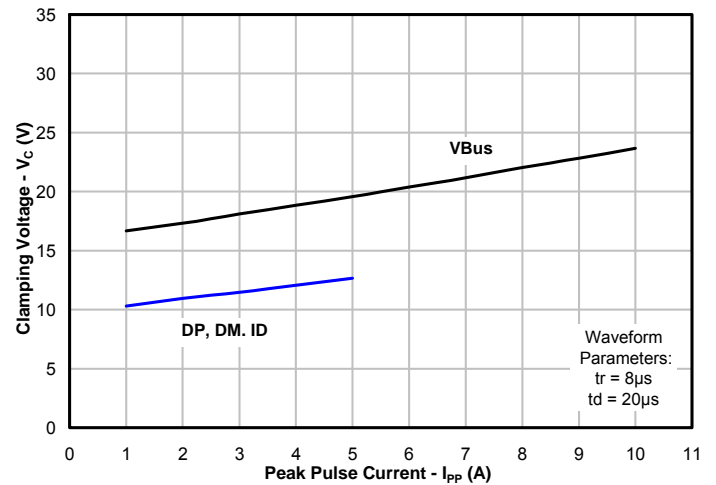
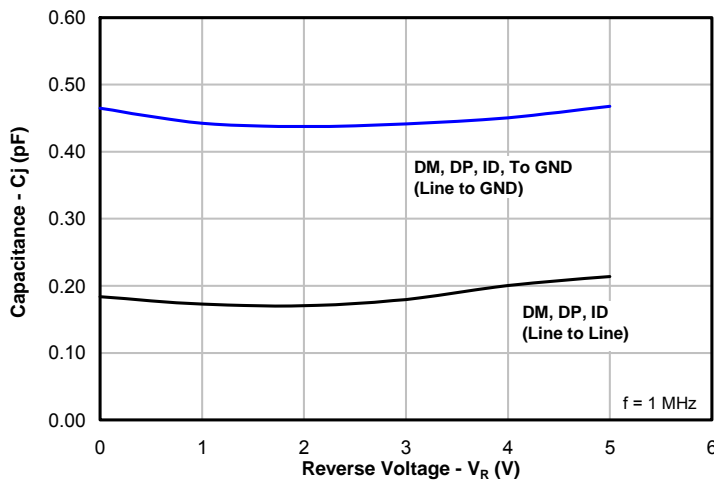
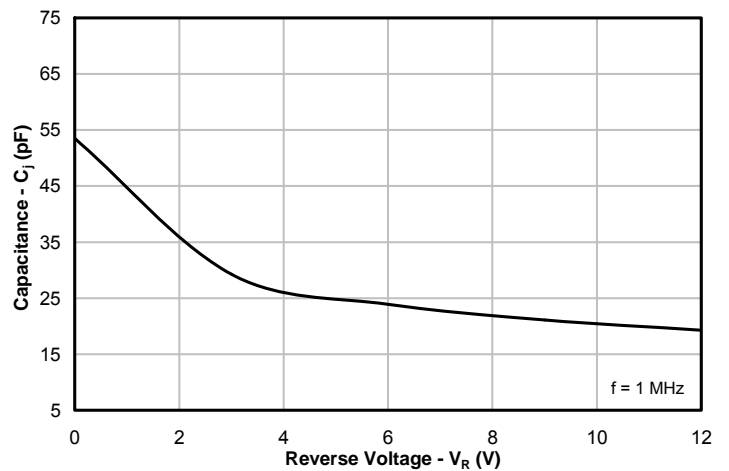
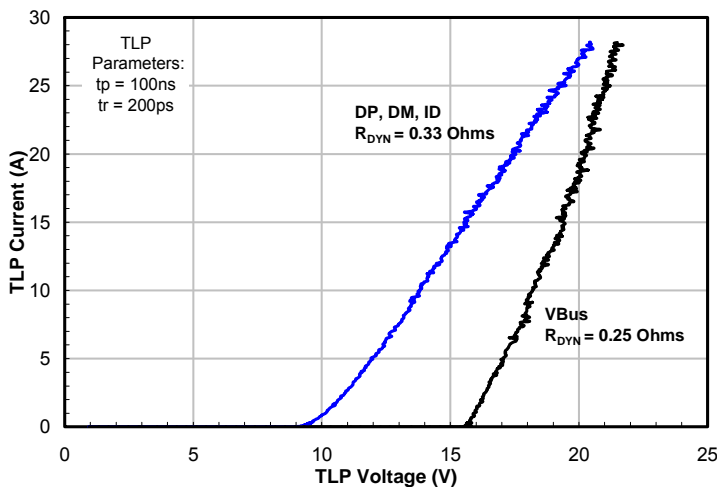
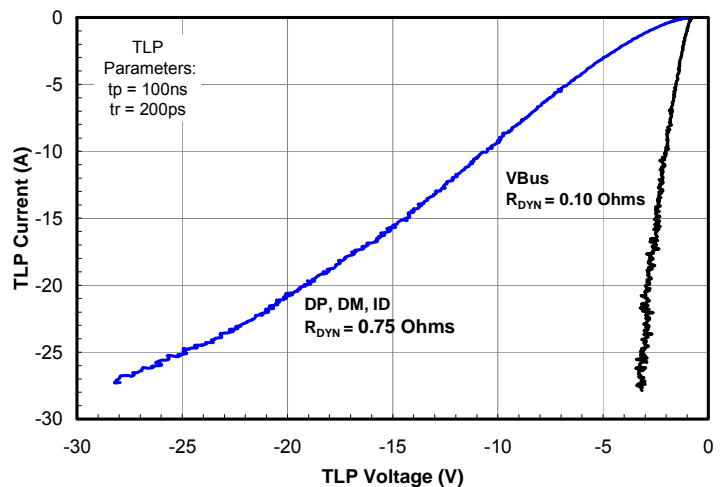
PROTECTION PRODUCTS
Absolute Maximum Rating

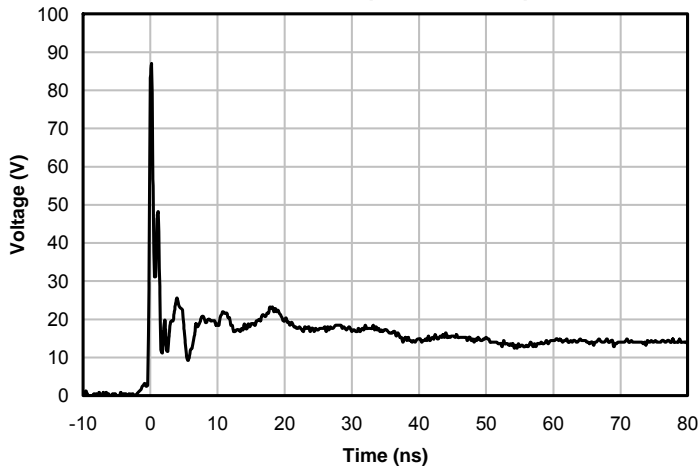
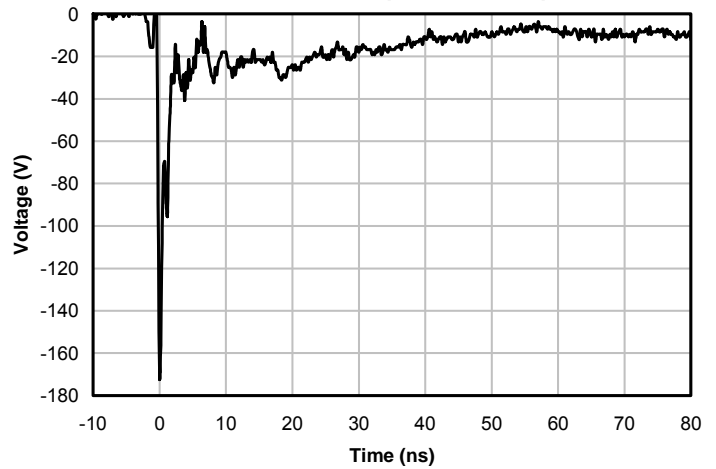
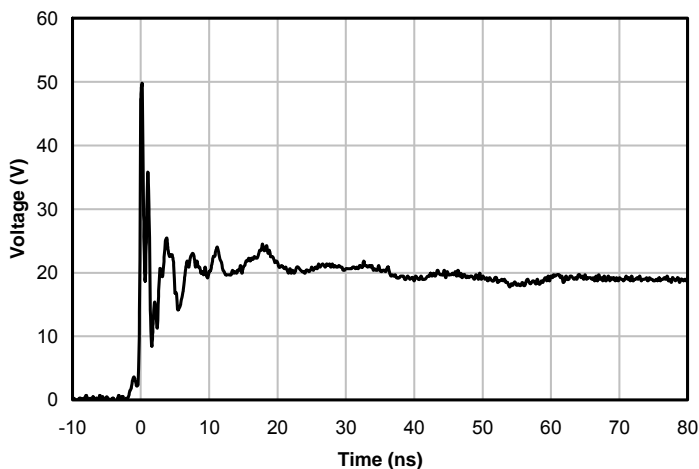
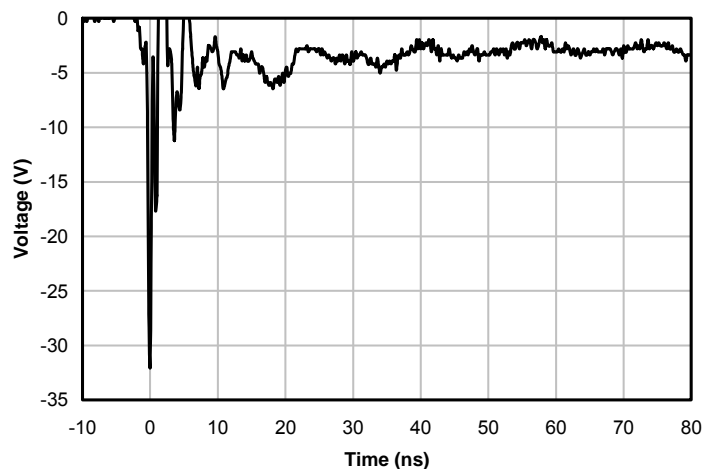
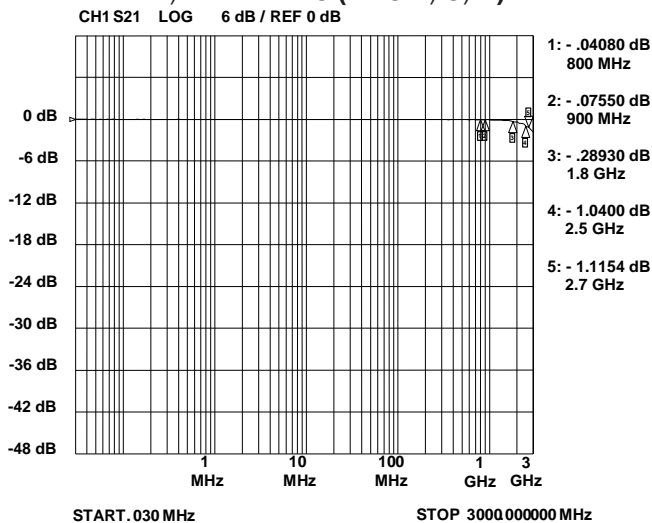
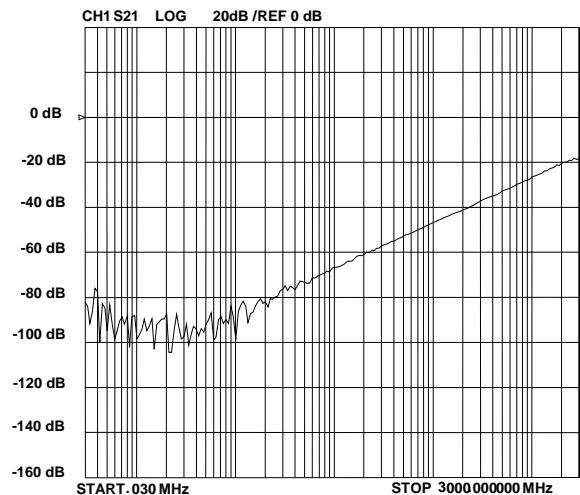
Rating	Symbol	Value	Units
DP, DM, USB ID			
Peak Pulse Power (tp = 8/20μs)	P_{pk}	75	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±25 ±20	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C
VBus TVS			
Peak Pulse Power (tp = 8/20μs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	10	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±30	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

VBus TVS						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 to GND			12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$, Pin 1 to GND	15	16.5	18	V
Reverse Leakage Current	I_R	$V_{RWM} = 12V$ Pin 1 to GND		0.005	0.100	μA
Forward Voltage	V_F	$I_f = 10mA$ GND to Pin 1	0.6		1.0	V
Clamping Voltage	V_C	$I_{PP} = 10A$, tp = 8/20μs Pin 1 to Ground			30	V
Forward Clamping Voltage	V_{FC}	$I_{PP} = 10A$, tp = 8/20μs Ground to Pin 1			3	V
Junction Capacitance	C_J	$V_R = 0V$, f = 1MHz Pin 1 to GND		55	75	pF

PROTECTION PRODUCTS
Electrical Characteristics (T=25°C)

DM, DP, USB ID						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 2, 3, or 4 to GND			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$, Pin 2, 3, or 4 to GND	6.5	9	11	V
Reverse Leakage Current	I_R	$V_{RWM} = 5.0V$, Pin 2, 3, or 4 to GND		0.005	0.100	μA
Forward Voltage	V_F	$I_f = 15mA$ Pin 2, 3, or 4 to GND	0.6		1.2	V
Clamping Voltage	V_C	$I_{PP} = 1A$, $t_p = 8/20\mu s$ Pin 2, 3, or 4 to GND			12	V
Clamping Voltage	V_C	$I_{PP} = 5A$, $t_p = 8/20\mu s$ Pin 2, 3, or 4 to GND			15	V
ESD Clamping Voltage	V_C	$I_{PP} = 4A$, $t_{lp} = 0.2/100ns$		12		V
ESD Clamping Voltage	V_C	$I_{PP} = 16A$, $t_{lp} = 0.2/100ns$		16		V
Dynamic Resistance	R_D	$t_p = 100ns$		0.33		Ohms
Junction Capacitance	C_j	$V_R = 0V$, $f = 1MHz$, Pin 2, 3, or 4 to GND		0.45	0.60	pF
		$V_R = 0V$, $f = 1MHz$, Between I/O pins		0.20	0.4	pF

PROTECTION PRODUCTS
Typical Characteristics
Non-Repetitive Peak Pulse Power vs. Pulse Time

Clamping Voltage vs. Peak Pulse Current

**Capacitance vs. Reverse Voltage
DM, DP, ID Pins (Pins 2, 3, 4)**

**Capacitance vs. Reverse Voltage
VBus Pin (Pin 1)**

TLP Characteristic (Positive Pulse)

TLP Characteristic (Negative Pulse)


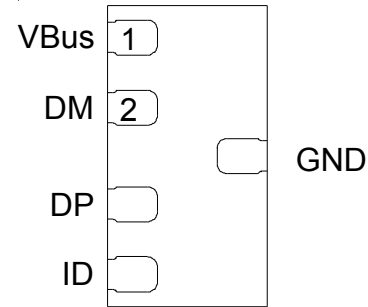
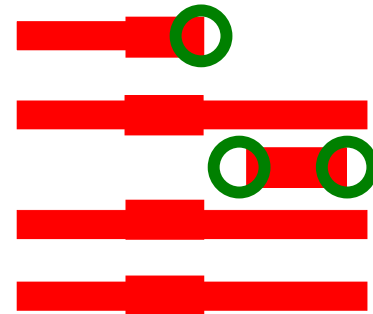
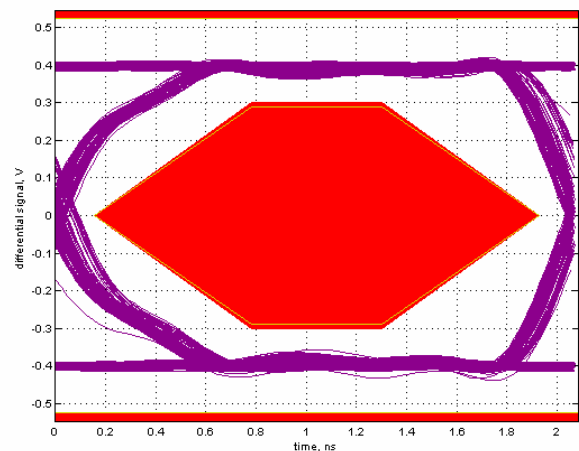
PROTECTION PRODUCTS
Typical Characteristics
**ESD Clamping (+8kV Contact per IEC 61000-4-2)
DM, DP, ID Pins (Pins 2, 3, 4)**

**ESD Clamping (-8kV Contact per IEC 61000-4-2)
DM, DP, ID Pins (Pins 2, 3, 4)**

**ESD Clamping (+8kV Contact per IEC 61000-4-2)
VBus Pin (Pin 1)**

**ESD Clamping (-8kV Contact per IEC 61000-4-2)
VBus Pin (Pin 1)**

**Typical Insertion Loss S21
DM, DP, ID Pins (Pins 2, 3, 4)**

**Analog Crosstalk
DM, DP, ID Pins (Pins 2, 3, 4)**


Device Connection and Layout Options for Protecting One USB Port

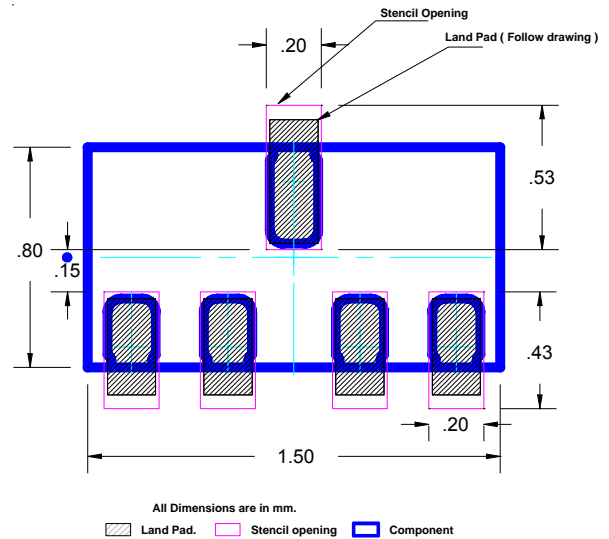
The RClamp1644T is optimized for protection of USB ports. Low capacitance protection is provided for the USB data (DM, DP) and USB ID pins. The maximum capacitance on these lines is <math><0.60\text{pF}</math>. USB Data and ID lines are connected at pins 2, 3, and 4. These inputs are referenced to an internal 5 volt TVS protection device. When the voltage on these lines exceed 5 volts, the TVS will conduct. Pin 1 is connected to the USB voltage bus (VBus). This device will conduct when the voltage on the bus exceeds 12 volts. Ground is provided at pin 5. Multiple micro vias connected to ground are recommended for best ESD performance. This will reduce parasitic inductance in the ground path and minimize the clamping voltage seen by the protected device. The package is designed for easy trace routing. The VBus pin is connected to the voltage layer of the PCB with a micro via as shown. Connection to ground is made at pin 5 using two micro vias. Connection to the ID pin is shown, however if the application does not utilize the ID function, pin 4 can be left not connected. The flow through layout combined with extremely low capacitance means the RClamp1644T will have minimal effect on high speed signal integrity. A typical USB 2.0 eye diagram test result with RClamp1644T is shown in Figure 3.

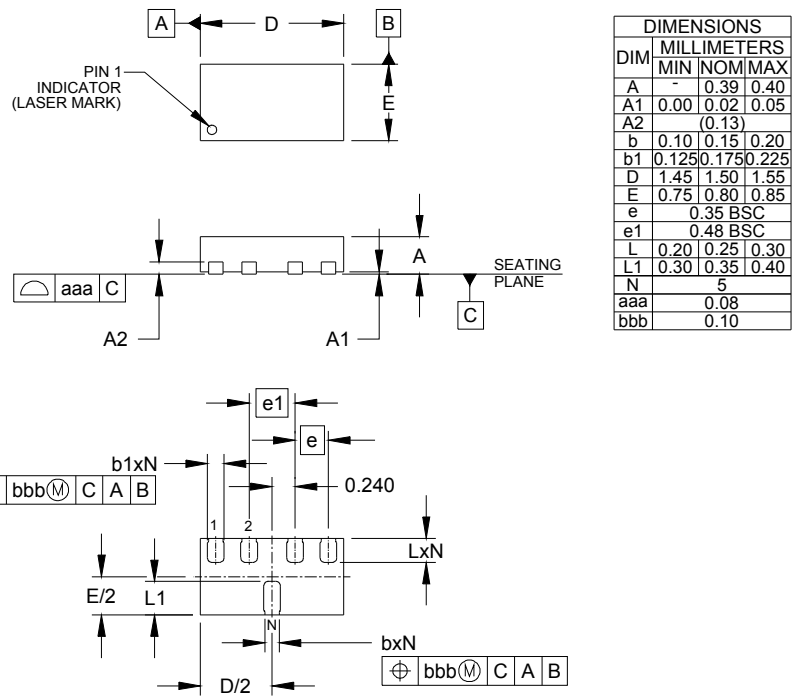
Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The table below provides Semtech's recommended assembly guidelines for mounting this device. The figure at the right details Semtech's recommended aperture based on the below recommendations. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. The exact manufacturing parameters will require some experimentation to get the desired solder application.

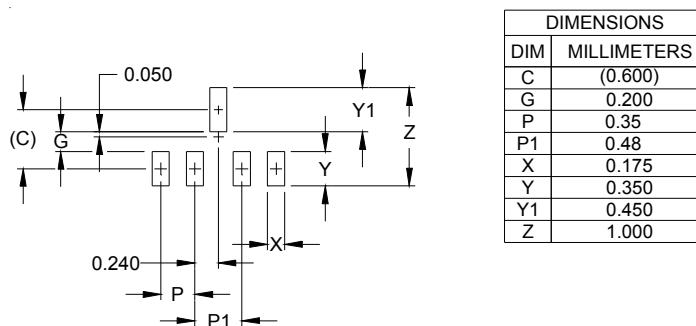

Figure 1 - Pin Configuration (Top View)

Figure 2 - PCB Layout Example

Figure 3 - USB Eye Pattern with RClamp1644T

Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu


Figure 4 - Recommended Mounting Pattern

PROTECTION PRODUCTS
Outline Drawing - SLP1508N5T


NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP1508N5T


NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.