

PROTECTION PRODUCTS

Description

RailClamp® TVS diodes are designed to provide ESD and EOS protection on high-speed ports. RClamp3521ZA is a 1-line, bidirectional device with a typical capacitance is only 0.45pF and working voltage of 3.5V. It is manufactured using Semtech's proprietary snap-back technology which minimizes both ESD peak clamping and TLP clamping voltage. The dynamic resistance is extremely low (0.12 Ohms typical) providing optimum protection of sensitive circuits.

RClamp3521ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 x 0.25mm. Leads are finished with lead-free NiAu.

Features

- High ESD withstand Voltage: +/-20kV (Contact) per IEC 61000-4-2
- Ultra-small package
- Protects one line
- Low ESD clamping voltage
- Working voltage: 3.5V
- Low capacitance: 0.45 pF Typical
- Low leakage current
- Low dynamic resistance
- Solid-state silicon-avalanche technology

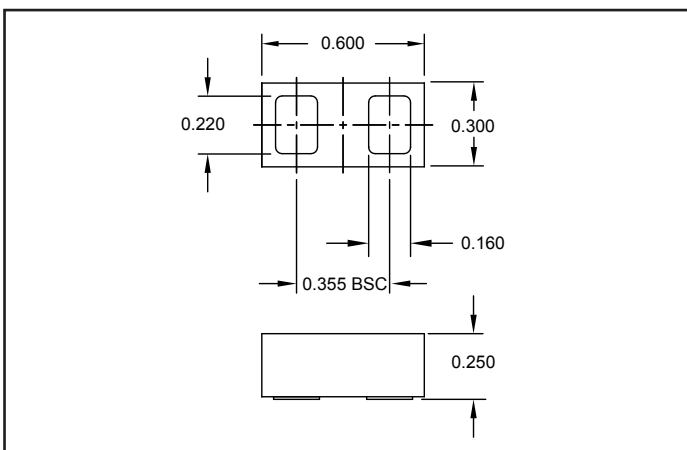
Mechanical Characteristics

- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

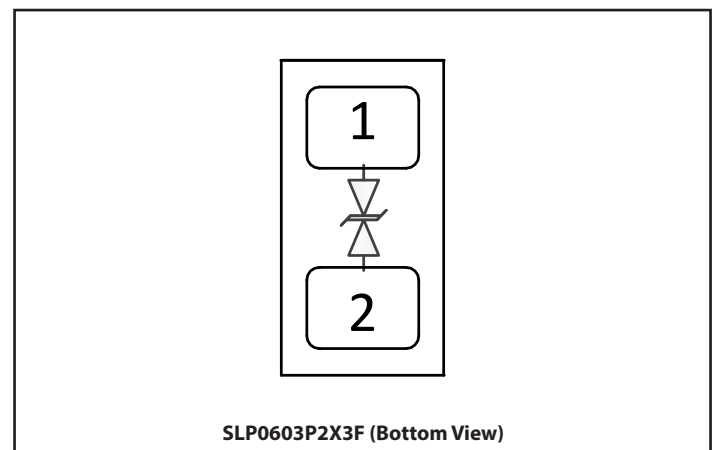
Applications

- USB3.0 / USB 3.1
- USB Type-C
- V-By-One
- MHL / MDDI
- LVDS Interfaces

Package Dimension



Schematic & Pin Configuration



Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 1.2/50µs)	P_{PK}	30	W
Peak Pulse Current (tp = 1.2/50µs)	I_{PP}	6	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	±25 ±20	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

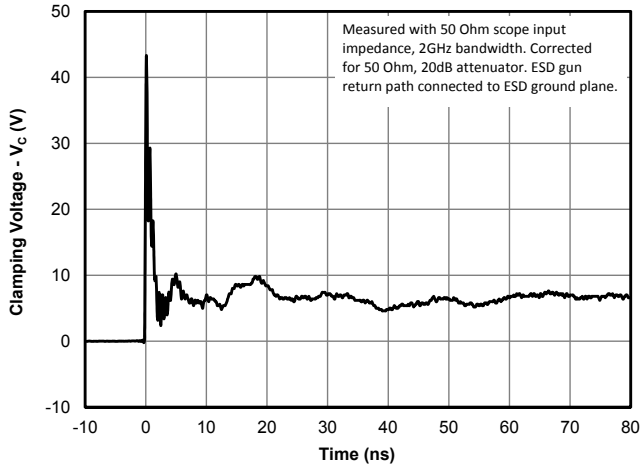
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}				3.5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1\text{mA}$	5.5	7.5	8.5	V
Reverse Leakage Current	I_R	$V_{RWM} = 3.5\text{V}$		<1	50	nA
Holding Current	I_H		50	120		mA
Clamping Voltage ²	V_C	$I_{PP} = 6\text{A}$, tp = 1.2/50µs, 8/20µs Combination Waveform		5		V
ESD Clamping Voltage ³	V_C	$I = 4\text{A}$, tlp = 0.2/100ns		4.5		V
		$I = 16\text{A}$, tlp = 0.2/100ns		6		
Dynamic Resistance ^{3,4}	R_{DYN}	tlp = 0.2/100ns		0.12		Ω
Junction Capacitance	C_J	$V_R = 0\text{V}$, f = 1MHz		0.45	0.55	pF

Notes

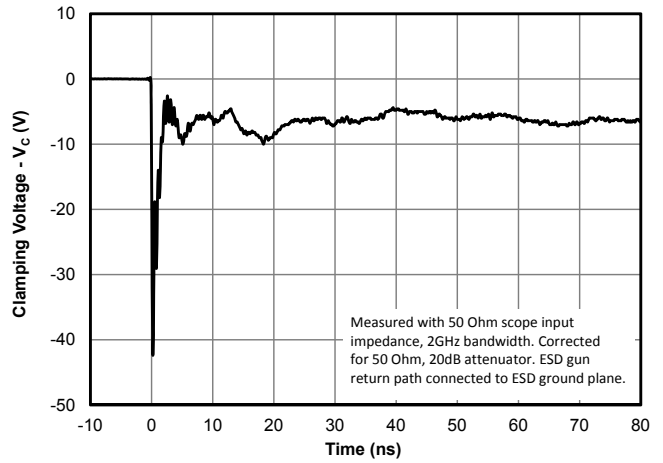
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Measured using a 1.2/50us voltage, 8/20us current combination waveform, RS = 8 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
- 3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.
- 4) Dynamic resistance calculated from $I_{TLP} = 4\text{A}$ to $I_{TLP} = 16\text{A}$

Typical Characteristics

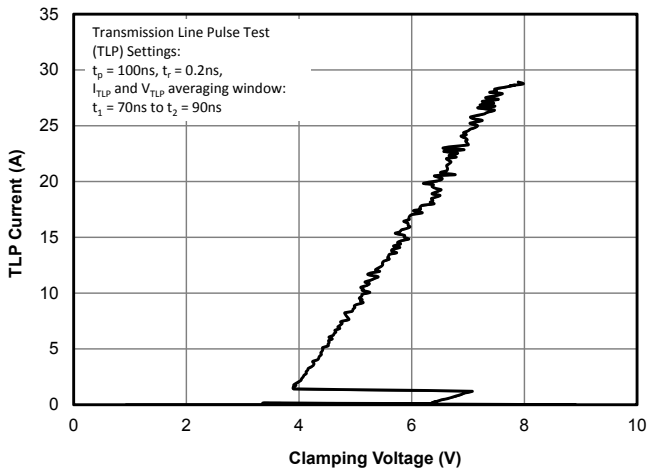
ESD Clamping (8kV Contact per IEC 61000-4-2)



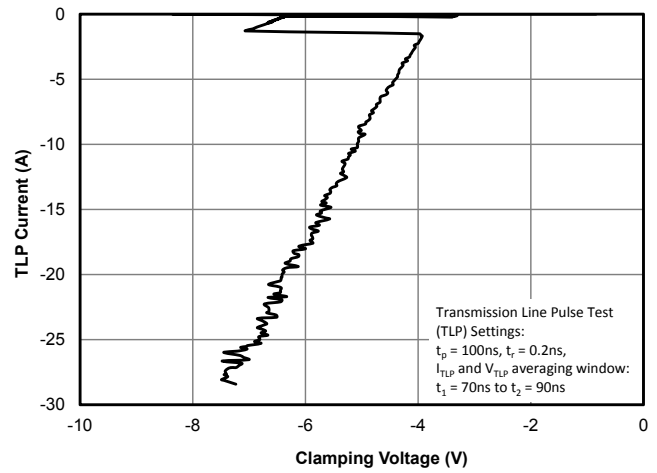
ESD Clamping (-8kV Contact per IEC 61000-4-2)



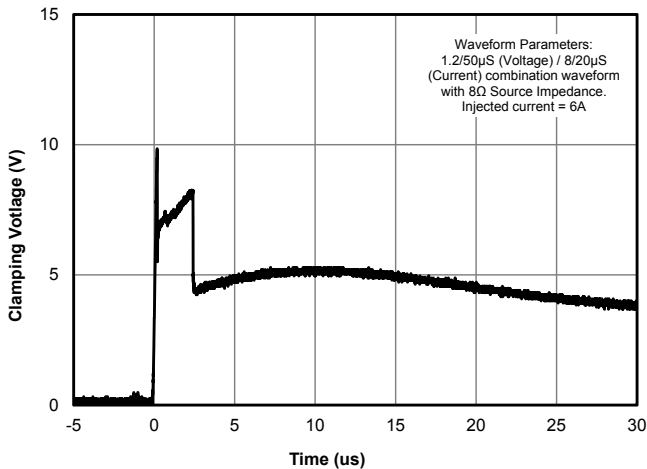
TLP Characteristic (Positive Pulse)



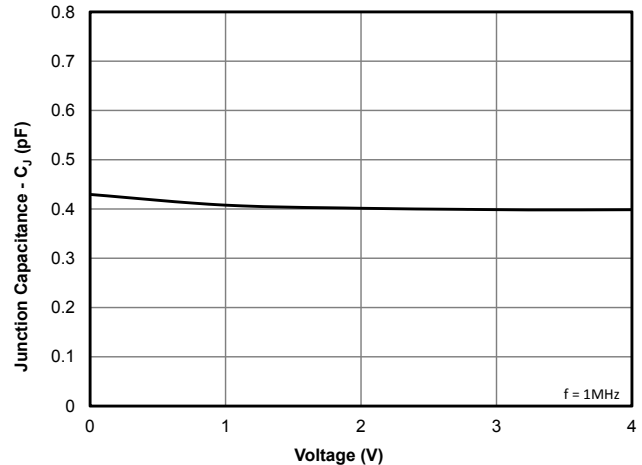
TLP Characteristic (Negative Pulse)



Clamping Characteristic (6A, Combination Waveform)

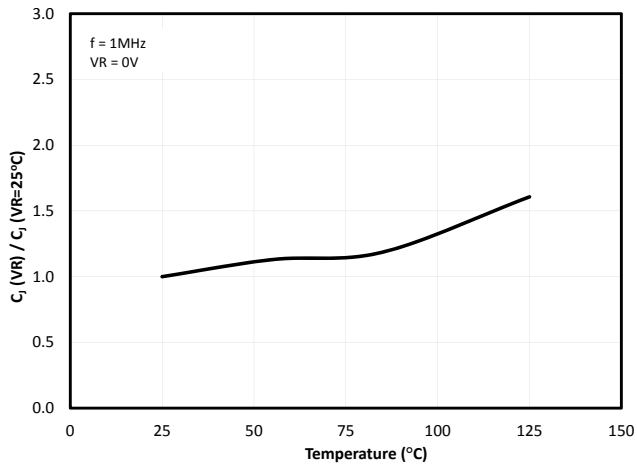


Capacitance vs. Reverse Voltage

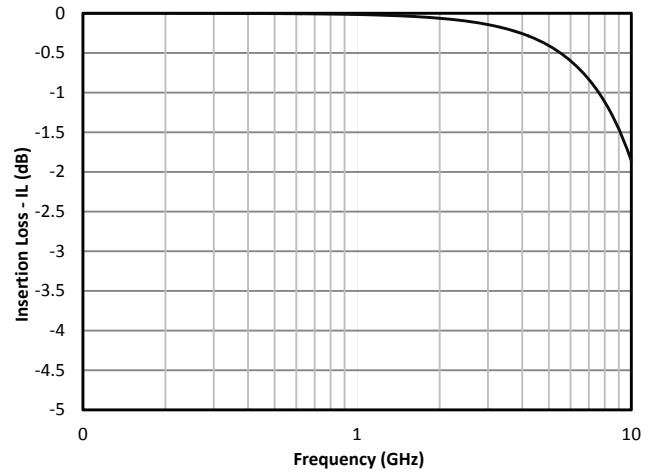


Typical Characteristics (Continued)

Capacitance vs. Temperature



Insertion Loss - S21



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

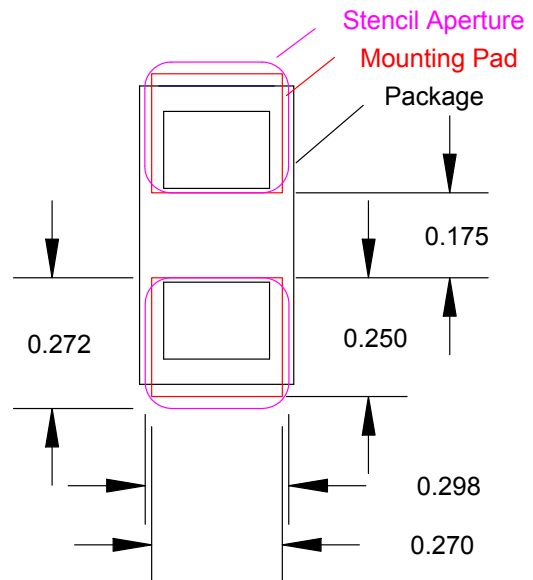
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

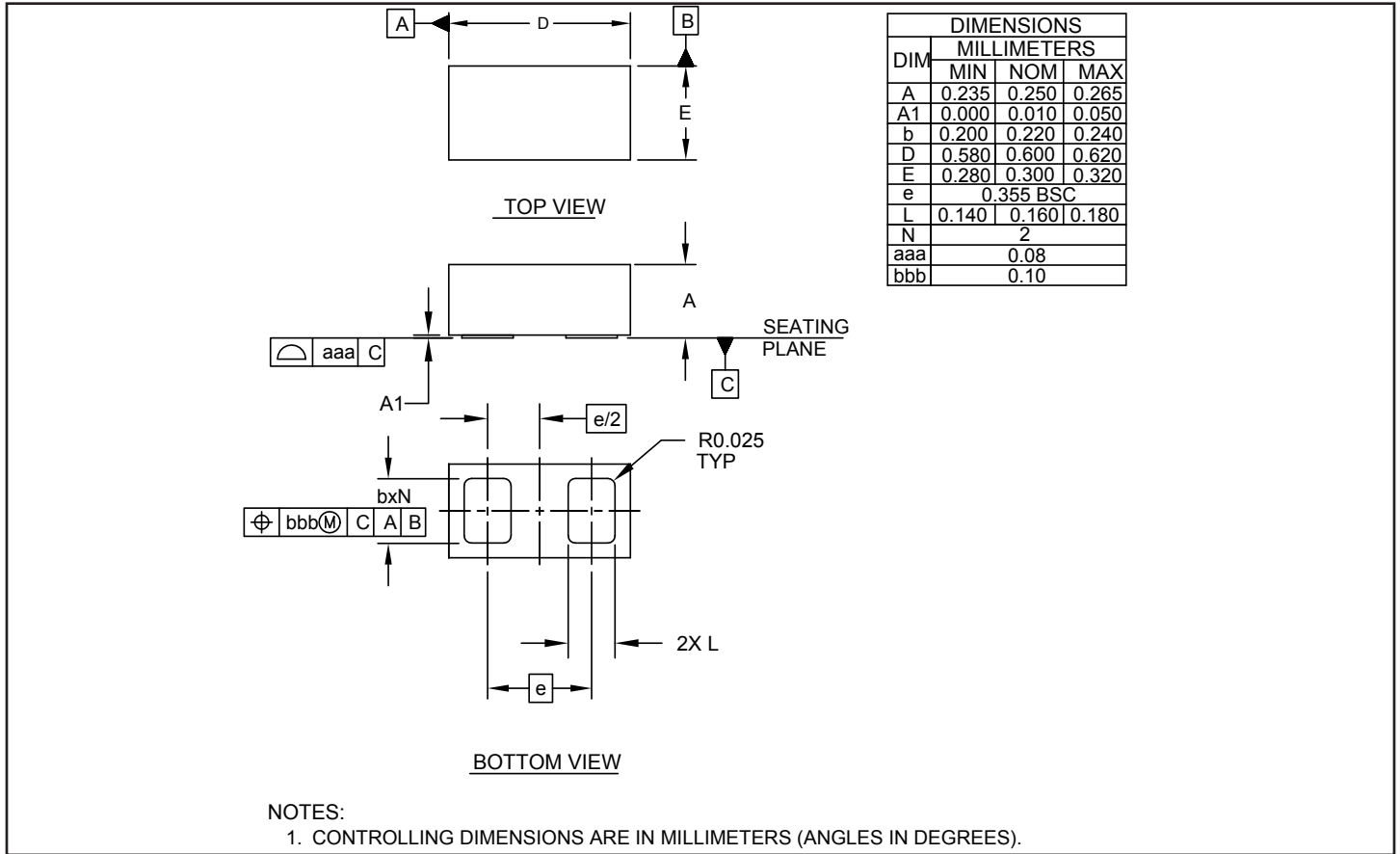
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

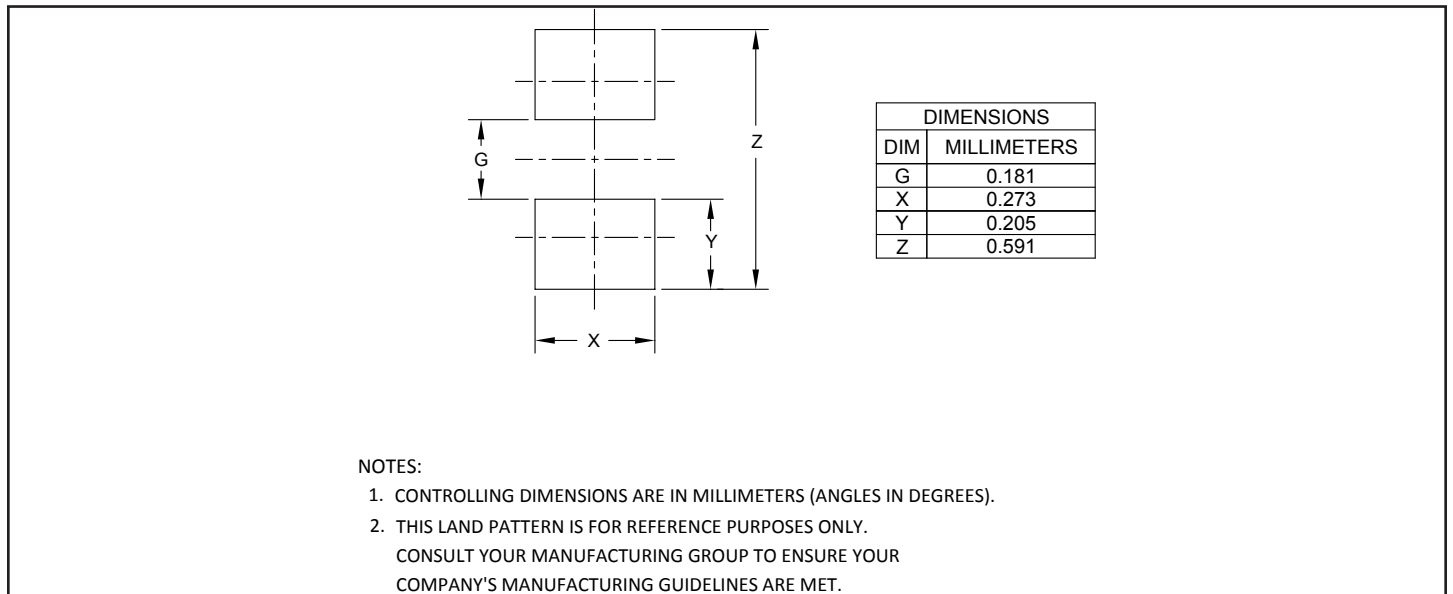


Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

Outline Drawing - SLP0603P2X3F



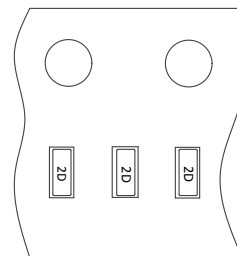
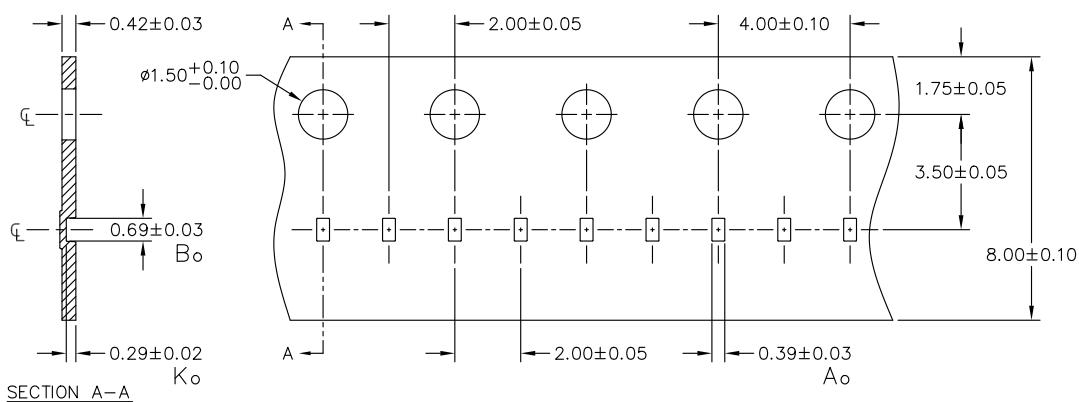
Land Pattern - SLP0603P2X3F



Marking Code

2D

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3521ZATFT	15,000	7"
RClamp3521ZATNT	10,000	7"