UM11470

RD-UAMP-SENSOR user manual

Rev. 2 — 26 January 2021 User manual

Document information

Information	Content
Keywords	RD-UAMP-SENSOR, current measurement shield, shunt resistors, acquisition, bank switching
Abstract	RD-UAMP-SENSOR User manual

Revision history

Rev	Date	Description
2	20210126	• Global changes: Performed minor grammatical, content and typographical changes througout. • Section 2, revised the range in the second bullet from "~60 nA – 1.3 mA" to "~60 nA – 5 mA." • Section 3, revised the image in Figure 1. • Section 4.1, added new paragraph after Figure 2 starting with "The SHLD current...." • Section 4.3, revised the first paragraph. • Section 5.1, Figure 4, updated the center board image for the RD-UAMP-SENSOR board. • Section 5.2, Table 1, revised as follows: – Revised "Shunt resistor selection" to "Range selection" for "SHLD current measurement." – Revised "100 nF / 1 µF / 10 µF capacitor enable" to "Low/Med/High filtering enable" for "SHLD current measurement." – Revised "Shunt resistor selection" to "Range selection" for "MCU current measurement." – Revised "100 nF / 1 µF / 10 µF capacitor enable" to "Low/Med/High filtering enable" for "MCU current measurement." • Section 6.1, revised the image in Figure 5. • Section 6.2.22, revised Table 36 and Table 37. • Section 7, revised as follows: – Moved Figure 7 from Section 7 to Section 7.3. – Inserted new sections,Section 7.1 and Section 7.2. • Inserted new section, Section 8.
1	20201009	Initial release

1 Introduction

The UAMP-SENSOR reference design is a Cortex-M4-based current measurement board, for use with the Freedom Development Ecosystem or any other Arduino-like development boards.

The board embeds two controllable current measurement units that allow for signal filtering, automatic, and manual range switching. The board also includes an LCD module and capacitive buttons for quick visualization and configuration.

2 Features

- Non-intrusive interfacing with any MCU board and 3.3 V shield
- Measurement of a large range of low currents: ~60 nA – 5 mA
- Multiple communication methods: LCD module, I^2C sensor emulation, Bluetooth module, serial port / custom protocol through USB
- Integration with Freedom Sensor Toolbox (CE)
- Open-source firmware powered by FreeRTOS

3 Block diagram

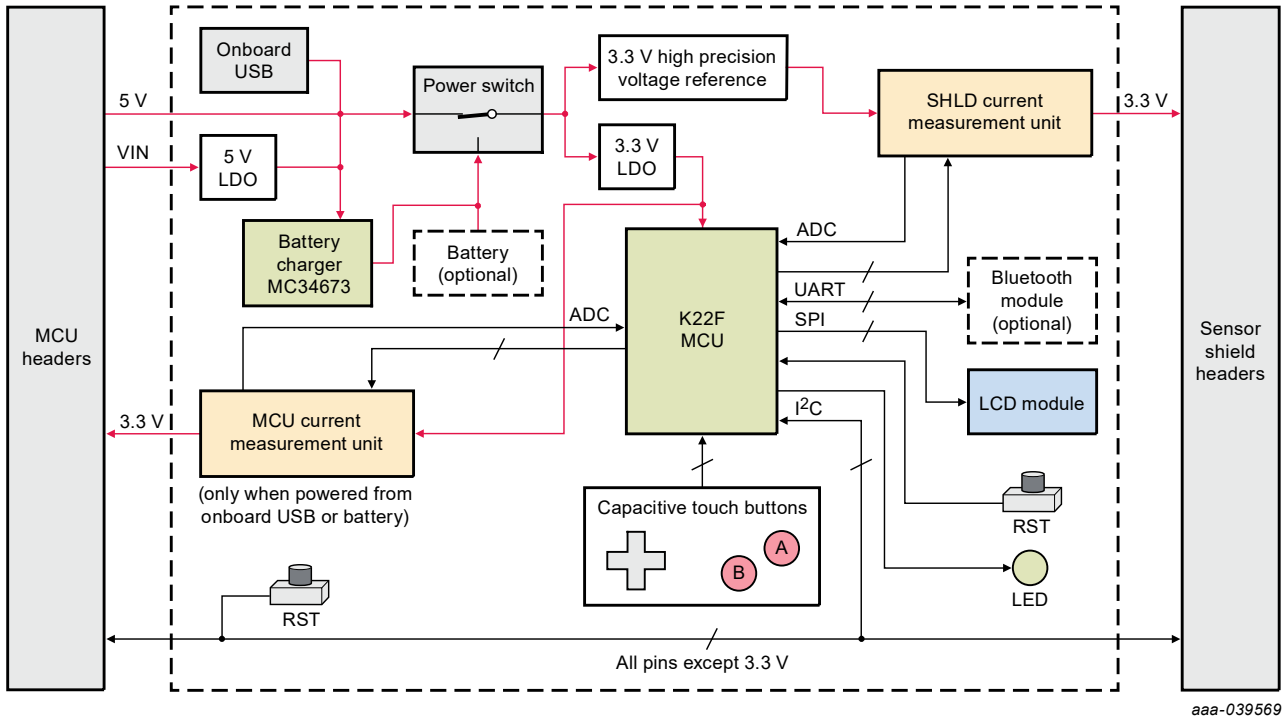


Figure 1. Internal block diagram

4 Current measurement method

4.1 Current measurement unit schematic

Each unit provides four shunt resistors and an amplifier with a gain of 25 to allow for a wide and precise measurement range.

Optional filtering capacitors can be connected, depending on the current profile that has to be observed.

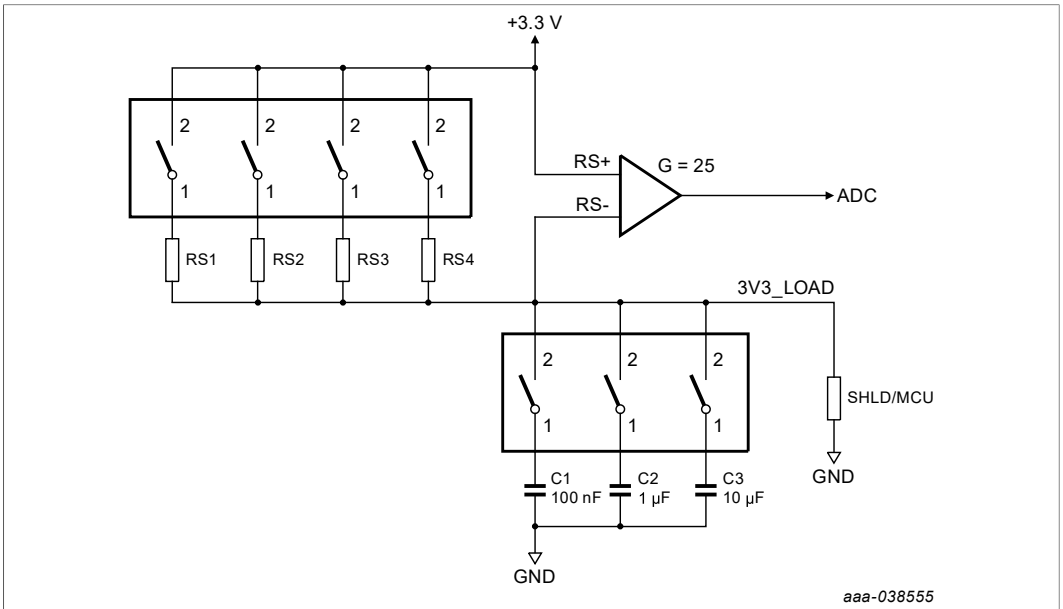


Figure 2. Current measurement unit schematic

The SHLD current measurement unit uses a dedicated, very high precision, 3.3 V voltage reference to ensure the highest measurement accuracy possible at low currents.

4.2 Measurement processing pipeline

The measurement processing pipeline provides average, minimum, and maximum current values over a specified period of time (see acquisition time in Table 1).

These values are calculated by repeatedly processing buffers of 100 samples provided by the eDMA module (*subacquisition*), and combining them until the acquisition time is fully covered.

Note: *The final acquisition time is approximated by multiple subacquisitions that are entirely dependent on the ADC output sampling time, and is therefore always slightly lower than the configured one.*

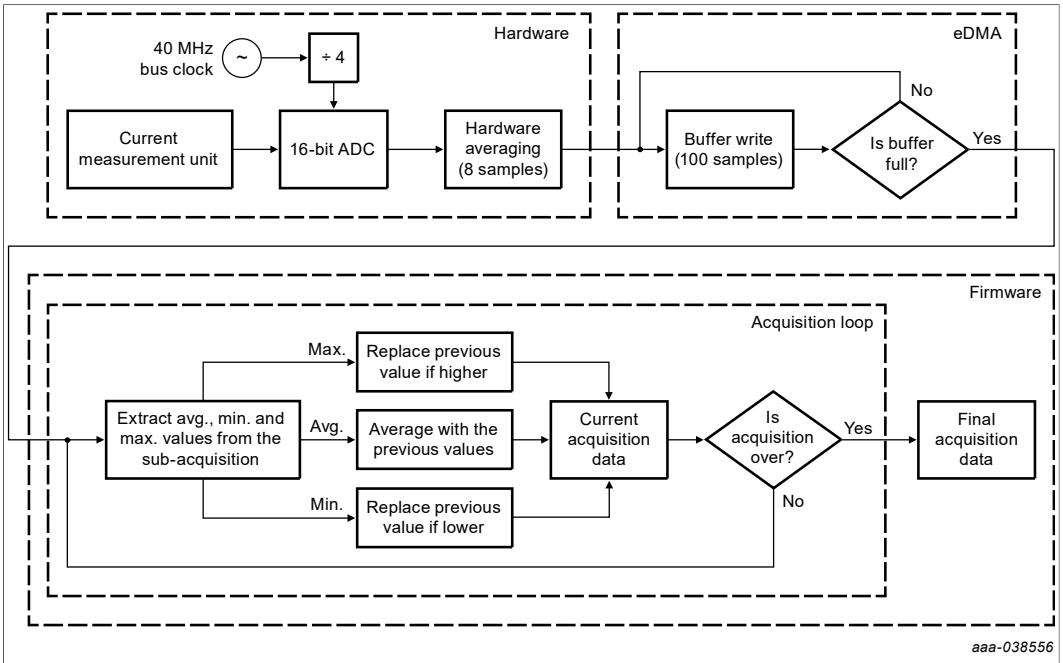


Figure 3. Measurement processing pipeline

4.3 Calibration

To ensure the maximum measurement accuracy, an offset calibration procedure is implemented for each shunt resistor. The offset calibration procedure eliminates any constant residual bias error, and can be performed at any time without needing to unplug the shield or MCU.

Unlike the ADC internal calibration, which is executed on each boot-up, and circumvents the effects of the external environment, the offset calibration runs automatically during the first ever boot-up, or manually by the user.

Note: *Factory resets do not clear offset calibration values.*

5 Usage

5.1 Physical connection

The UAMP-SENSOR reference design is designed to interface with any existing 3.3 V MCU and shield combo, such as the NXP Freedom sensor development kits.

The UAMP-SENSOR board simply plugs in between the MCU and shield, mirroring all pins except for the 3.3 V supplies that now go through the current measurement units.

Note: *The MCU current measurement is possible only when powered from the UAMP-SENSOR's onboard USB or battery.*

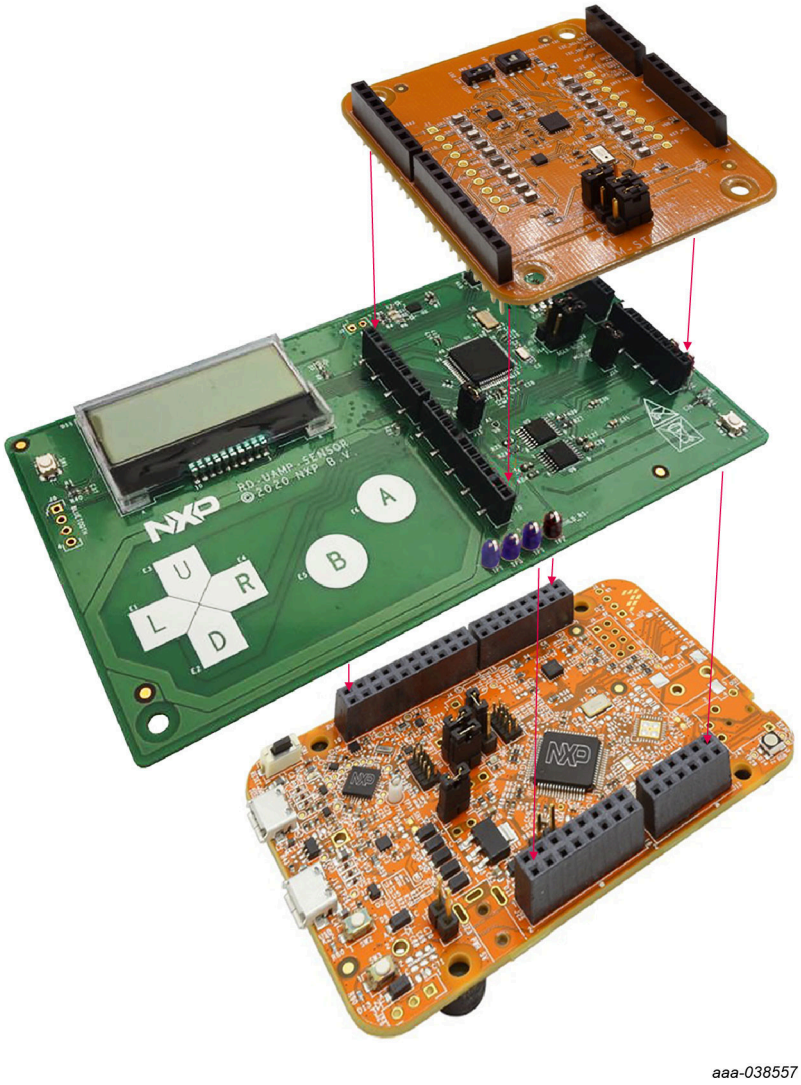


Figure 4. Physical connection

5.2 Configurable parameters

The reference design provides several parameters for its operation, accessible through the different communication interfaces.

The parameters are organized in Table 1.

Table 1. Configurable parameters

Category		Parameter	Access	Reset reset value
RC banks configuration	Range selection	Auto-range enable	Boolean	true
		Range selection	unsigned int	0
		Low / Med / High filtering enable	Boolean array	{ true, true, true }
		Calibration resistor enable	Boolean	false
	MCU current measurement[1]	Auto-range enable	Boolean	true
		Range selection	Unsigned int	0
		Low / Med / High filtering enable	Boolean array	{ true, true, true }
Acquisition settings		*Standby / Active* mode selection	Boolean	true
		Acquisition time in milliseconds	Unsigned int	500
		GPIO pin *Disabled / Pulse / DRDY interrupt* mode selection	Unsigned int	1
Calibration settings	SHLD current measurements	Offset currents for the 4 shunt resistors	Float array	Last calibration values
	MCU current measurements	Offset currents for the 4 shunt resistors	Float array	Last calibration values
Screen settings		Screen brightness percentage	Unsigned int	50

[1] This feature is present in the hardware but has not yet been implemented in firmware.

6 Communication interfaces

6.1 LCD module

The LCD module provides quick and easy access to all configurable parameters, as well as live visualization of the acquisition values through a menu.

Capacitive buttons are used to control it, and all inputs are described in Table 2.

The menu is composed of pages, which contain a title and elements. Elements can be interactable or not, and are used for displaying data or running special actions:

- Navigate to other pages.
- Cancel all changes and load the parent page.
- Run a calibration routine.
- Perform a factory reset.

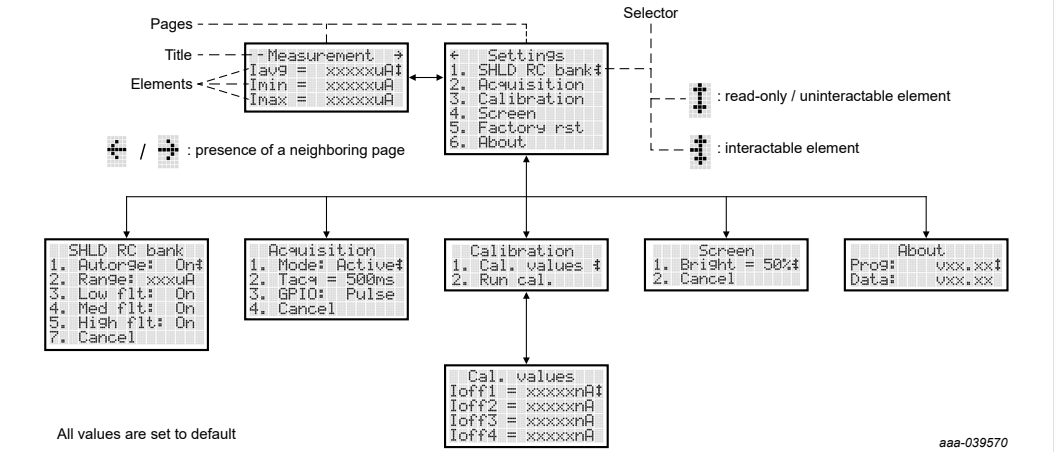


Figure 5. LCD menu structure

By default, the user navigates the menu in normal mode. If an interactable element containing data is pressed, the selector changes into a blinking cursor and edit mode is activated.

Table 2. Menu inputs guide

Input	Normal mode	Edit mode (blinking cursor)
Up / Down 	Navigate through elements on the page (circularly).	Navigate through the values of the elements (circularly).
Left / Right 	Navigate through neighboring pages.	
Back 	Save changes and load the parent page.	Cancel changes in the element and switch back to normal mode.

Table 2. Menu inputs guide*...continued*

Input	Normal mode	Edit mode (blinking cursor)
Press A	Interact with the selected element: If it contains data, switch to edit mode. Else, run its special action.	Apply changes in the element and switch back to normal mode (Note: Changes are not yet saved).

6.2 I²C sensor emulation

In order to allow for Freedom Sensor Toolbox (CE) integration and / or control from another MCU, the reference design is accessible through a standard I²C interface, at address *0Eh*.

The reference design at address *0Eh* provides user access to a register map which mimics the behavior of any standard NXP sensor, as specified in Table 3.

When using the I²C interface with another I²C sensor, ensure that *J13* and *J14* are set to different *SDA* and *SCL* pins than the pins used by the sensor (for example, *SDA0* and *SCL0* on the reference design, *SDA1* and *SCL1* on the sensor shield).

Table 3. Register map

Name	Type	Address	Factory reset value	Description
STATUS_REG	R	00h	04h	Status register
IDD_AVG_FLT1	R	01h	X	Average current measurement value (float representation)
IDD_AVG_FLT2	R	02h	X	
IDD_AVG_FLT3	R	03h	X	
IDD_AVG_FLT4	R	04h	X	
IDD_MIN_FLT1	R	05h	X	Min current measurement value (float representation)
IDD_MIN_FLT2	R	06h	X	
IDD_MIN_FLT3	R	07h	X	
IDD_MIN_FLT4	R	08h	X	
IDD_MAX_FLT1	R	09h	X	Max current measurement value (float representation)
IDD_MAX_FLT2	R	0Ah	X	
IDD_MAX_FLT3	R	0Bh	X	
IDD_MAX_FLT4	R	0Ch	X	
ACQ_TIME_MS1	R	0Dh	F4h	Acquisition time (unsigned int representation)
ACQ_TIME_MS2	R	0Eh	01h	
WHO_AM_I	R	0Fh	C4h	Device identification register
PROG_REV_MAJOR	R	10h	X	Major program revision
PROG_REV_MINOR	R	11h	X	Minor program revision
DATA_REV_MAJOR	R	12h	X	Major flash data revision
DATA_REV_MINOR	R	13h	X	Minor flash data revision
ACQ_TIME	R/W	14h	01h	Acquisition time selection

Table 3. Register map...*continued*

Name	Type	Address	Factory reset value	Description
RC_BANK_SHLD	R/W	15h	1Ch	SHLD RC bank configuration
CTRL_REG1	R/W	16h	27h	Control register 1
CTRL_REG2	R/W	17h	00h	Control register 2 (autoclear bits)
OFFSET1_FLT1	R/W	20h	X	SHLD RC bank offset calibration (float representation)
OFFSET1_FLT2	R/W	21h	X	
OFFSET1_FLT3	R/W	22h	X	
OFFSET1_FLT4	R/W	23h	X	
OFFSET2_FLT1	R/W	24h	X	
OFFSET2_FLT2	R/W	25h	X	
OFFSET2_FLT3	R/W	26h	X	
OFFSET2_FLT4	R/W	27h	X	
OFFSET3_FLT1	R/W	28h	X	
OFFSET3_FLT2	R/W	29h	X	
OFFSET3_FLT3	R/W	2Ah	X	
OFFSET3_FLT4	R/W	2Bh	X	
OFFSET4_FLT1	R/W	2Ch	X	
OFFSET4_FLT2	R/W	2Dh	X	
OFFSET4_FLT3	R/W	2Eh	X	
OFFSET4_FLT4	R/W	2Fh	X	

6.2.1 Status register (STATUS_REG)

Table 4. Status register (STATUS_REG) (00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ERROR[2:0]			–	–	SYSMOD	DOWR	DRDY
Reset	0	0	0	X	X	1	0	0
Access	R	R	R	R	R	R	R	R

Table 5. STATUS_REG register field description

Bit	Symbol	Description
7 to 5	ERROR[2:0]	ERROR: Measurement error code.
		000: No error
		001: Max current clipping error
2	SYSMOD	SYSMOD: Current system mode.
		0: Standby mode
		1: Active mode

Table 5. STATUS_REG register field description*...continued*

Bit	Symbol	Description
1	DOWR	DOWR: Data overwritten flag.
		0: Data was not overwritten since last read
		1: Data was overwritten since last read
0	DRDY	DRDY: Data ready flag.
		0: No new data is available for read.
		1: New data is available for read.

6.2.2 Average current measurement value register (float representation) (IDD_AVG_FLT1)

Table 6. Average current measurement value register (float representation) (IDD_AVG_FLT1) (01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_AVG[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.3 Average current measurement value register (float representation) (IDD_AVG_FLT2)

Table 7. Average current measurement value register (float representation) (IDD_AVG_FLT2) (02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_AVG[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.4 Average current measurement value register (float representation) (IDD_AVG_FLT3)

Table 8. Average current measurement value register (float representation) (IDD_AVG_FLT3) (03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_AVG[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.5 Average current measurement value register (float representation) (IDD_AVG_FLT4)

Table 9. Average current measurement value register (float representation) (IDD_AVG_FLT4) (04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_AVG[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 10. IDD_AVG_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OUT_IDD_AVG	Float representation of average current measurement.

6.2.6 Minimum current measurement value register (float representation) (IDD_MIN_FLT1)

Table 11. Minimum current measurement value register (float representation) (IDD_MIN_FLT1) (05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MIN[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.7 Minimum current measurement value register (float representation) (IDD_MIN_FLT2)

Table 12. Minimum current measurement value register (float representation) (IDD_MIN_FLT2) (06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MIN[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.8 Minimum current measurement value register (float representation) (IDD_MIN_FLT3)

Table 13. Minimum current measurement value register (float representation) (IDD_MIN_FLT3) (07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MIN[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.9 Minimum current measurement value register (float representation) (IDD_MIN_FLT4)

Table 14. Minimum current measurement value register (float representation) (IDD_MIN_FLT4) (08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MIN[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 15. IDD_MIN_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OUT_IDD_MIN	Float representation of minimum current measurement.

6.2.10 Maximum current measurement value register (float representation) (IDD_MAX_FLT1)

Table 16. Maximum current measurement value register (float representation) (IDD_MAX_FLT1) (09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MAX[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.11 Maximum current measurement value register (float representation) (IDD_MAX_FLT2)

Table 17. Maximum current measurement value register (float representation) (IDD_MAX_FLT2) (0Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MAX[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.12 Maximum current measurement value register (float representation) (IDD_MAX_FLT3)

Table 18. Maximum current measurement value register (float representation) (IDD_MAX_FLT3) (0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MAX[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.13 Maximum current measurement value register (float representation) (IDD_MAX_FLT4)

Table 19. Maximum current measurement value register (float representation) (IDD_MAX_FLT4) (0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_IDD_MAX[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 20. IDD_MAX_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OUT_IDD_MAX	Float representation of maximum current measurement.

6.2.14 Acquisition time register (unsigned int representation) (ACQ_TIME_MS1)

Table 21. Acquisition time register (unsigned int representation) (ACQ_TIME_MS1) (0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ACQ_TIME_MS[7:0]							
Reset	1	1	1	1	0	1	0	0
Access	R	R	R	R	R	R	R	R

6.2.15 Acquisition time register (unsigned int representation) (ACQ_TIME_MS2)

Table 22. Acquisition time register (unsigned int representation) (ACQ_TIME_MS2) (0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ACQ_TIME_MS[15:8]							
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R

Table 23. ACQ_TIME_MS1:2 register field description

Bit	Symbol	Description
15 to 0	ACQ_TIME_MS	Unsigned int representation of acquisition time.

6.2.16 Device identification register (WHO_AM_I)

Table 24. Device identification register (WHO_AM_I) (0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WHO_AM_I[7:0]							
Reset	1	1	0	0	0	1	0	0
Access	R	R	R	R	R	R	R	R

Table 25. WHO_AM_I register field description

Bit	Symbol	Description
7 to 0	WHO_AM_I	Device identifier, always set to *C4h*.

6.2.17 Major program revision register (PROG_REV_MAJOR)

Table 26. Major program revision register (PROG_REV_MAJOR) (10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_REV_MAJOR[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 27. PROG_REV_MAJOR register field description

Bit	Symbol	Description
7 to 0	PROG_REV_MAJOR	Major program revision.

6.2.18 Minor program revision register (PROG_REV_MINOR)

Table 28. Minor program revision register (PROG_REV_MINOR) (11h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_REV_MINOR[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 29. PROG_REV_MINOR register field description

Bit	Symbol	Description
7 to 0	PROG_REV_MINOR	Minor program revision.

6.2.19 Major flash data revision register (DATA_REV_MAJOR)

Table 30. Major flash data revision register (DATA_REV_MAJOR) (12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DATA_REV_MAJOR[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 31. DATA_REV_MAJOR register field description

Bit	Symbol	Description
7 to 0	DATA_REV_MAJOR	Major data flash revision.

6.2.20 Minor flash data revision register (DATA_REV_MINOR)

Table 32. Minor flash data revision register (DATA_REV_MINOR) (13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DATA_REV_MINOR[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Table 33. DATA_REV_MINOR register field description

Bit	Symbol	Description
7 to 0	DATA_REV_MINOR	Minor data flash revision.

6.2.21 Acquisition time selection register (ACQ_TIME)

Table 34. Acquisition time selection register (ACQ_TIME) (14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	ACQ_TIME[2:0]		
Reset	X	X	X	X	X	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 35. ACQ_TIME register field description

Bit	Symbol	Description
2 to 0	ACQ_TIME	Acquisition time selection.
		000: 100 ms
		001: 500 ms
		010: 1 s
		011: 2 s
		100: 3 s

6.2.22 SHLD RC bank configuration register (RC_BANK_SHLD)

Table 36. SHLD RC bank configuration register (RC_BANK_SHLD) (15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	–	–	–	HIGH_FLT	MED_FLT	LOW_FLT	RANGE[1:0]	
Reset	X	X	X	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 37. RC_BANK_SHLD register field description

Bit	Symbol	Description
4	High filtering capacitor enable	10 µF decoupling capacitor enable.
		0: Disconnected
		1: Connected
3	Medium filtering capacitor enable	1 µF decoupling capacitor enable.
		0: Disconnected
		1: Connected
2	Low filtering capacitor enable	100 nF decoupling capacitor enable.
		0: Disconnected
		1: Connected
1 to 0	R	Shunt resistor selection.
		00: 5 mA
		01: 1 mA
		10: 200 µA
		11: 40 µA

6.2.23 Control register 1 (CTRL_REG1)

Table 38. Control register 1 (CTRL_REG1) (16h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	–	BRIGHTNESS[2:0]			GPIO[1:0]		AUTORGE	ACTIVE
Reset	X	0	1	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 39. CTRL_REG1 register field description

Bit	Symbol	Description
6 to 4	BRIGHTNESS	LCD module brightness selection.
		000: 0 %
		001: 25 %
		010: 50 %
		011: 75 %
		100: 100 %
3 to 2	GPIO	GPIO pin mode selection.
		00: Disabled
		01: Pulse (generates a fixed-width pulse whenever new data is ready)
		10: DRDY interrupt (stays high until at least one of the current measurement registers are read)

Table 39. CTRL_REG1 register field description*...continued*

Bit	Symbol	Description
1	AUTORGE	Auto-range mode enable.
		0: Fixed range
		1: Auto range
0	ACTIVE	Operating mode selection.
		0: Standby
		1: Active

6.2.24 Control register 2 (autoclear bits) (CTRL_REG2)

Table 40. Control register 2 (autoclear bits) (CTRL_REG2) (17h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	DEFAULT	RESET	CALIB
Reset	X	X	X	X	X	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 41. CTRL_REG2 register field description

Bit	Symbol	Description
2	DEFAULT	Factory settings (autoclear bit).
		0: Do nothing
		1: Load factory settings
1	RESET	Software reset (autoclear bit).
		0: Do nothing
		1: Perform a software reset
0	CALIB	Run calibration (autoclear bit).
		0: Do nothing
		1: Run a calibration procedure

6.2.25 SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT1)

Table 42. SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT1) (20h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET1[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.26 SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT2)

Table 43. SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT2) (21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET1[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.27 SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT3)

Table 44. SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT3) (22h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET1[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.28 SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT4)

Table 45. SHLD RC bank offset 1 calibration register (float representation) (OFFSET1_FLT4) (23h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET1[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 46. OFFSET1_FLT4 register field description

Bit	Symbol	Description
31 to 0	OFFSET1	Float representation of offset calibration for the first shunt resistor

6.2.29 SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT1)

Table 47. SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT1) (24h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET2[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.30 SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT2)

Table 48. SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT2) (25h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET2[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.31 SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT3)

Table 49. SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT3) (26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET2[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.32 SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT4)

Table 50. SHLD RC bank offset 2 calibration register (float representation) (OFFSET2_FLT4) (27h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET2[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 51. OFFSET2_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OFFSET2	Float representation of offset calibration for the second shunt resistor.

6.2.33 SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT1)

Table 52. SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT1) (28h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET3[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.34 SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT2)

Table 53. SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT2) (29h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET3[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.35 SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT3)

Table 54. SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT3) (2Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET3[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.36 SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT4)

Table 55. SHLD RC bank offset 3 calibration register (float representation) (OFFSET3_FLT4) (2Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET3[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 56. OFFSET3_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OFFSET3	Float representation of offset calibration for the third shunt resistor.

6.2.37 SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT1)

Table 57. SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT1) (2Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET4[7:0]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.38 SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT2)

Table 58. SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT2) (2Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET4[15:8]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.39 SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT3)

Table 59. SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT3) (2Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET4[23:16]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.40 SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT4)

Table 60. SHLD RC bank offset 4 calibration register (float representation) (OFFSET4_FLT4) (2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFFSET4[31:24]							
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 61. OFFSET4_FLT1:4 register field description

Bit	Symbol	Description
31 to 0	OFFSET4	Float representation of offset calibration for the fourth shunt resistor.

6.3 Other interfaces

As stated in Section 2, the UAMP-SENSOR reference design embeds other communication channels that are not yet implemented in firmware:

- The onboard USB connector (*J1*) connects to the USB data lines of the K22F. The connection to the data lines enables the creation of highly optimized firmware and software using the USB stack, or through a simple virtual serial port.
- The UART-to-Bluetooth module header (*J8*) can be used to send data wirelessly. With a battery connected on *J2*, the UART-to-Bluetooth module could allow for hostless and wireless data logging.

7 UAMP SENSOR firmware

7.1 Prerequisites

The following prerequisites should be completed prior to launching the UAMP Sensor firmware project.

- Availability of supported sensor toolbox eval sensor kit (FRDMKL25-A8471 and/or FRDM-K22F-AGMP03).
- Recommended toolchain/IDE i.e. MCUXpresso IDE is installed on the development PC.
- Segger J-Link Windows drivers are installed on the development PC.
- FRDM-K22F MCUXpresso SDK (with FreeRTOS included) is downloaded and installed on MCUXpresso IDE.

7.2 Project archive

The complete firmware source code is provided as an MCUXpresso project archive. The zip container can simply be imported into the workspace through the MCUXpresso IDE import wizard.

The exact content of the archive is shown in Figure 6. Note the firmware binary is available in the bin folder.

In order to customize and debug the firmware, project has to be rebuilt to generate the debug folder and files. User shall also create a Debug Configuration associated to the debug probe of choice.

Finally, the 10-pin JTAG/DBM cable of the debug tool is inserted into RD-UAMP board J3 connector to flash and debug the on-board Kinetis K22F MCU.

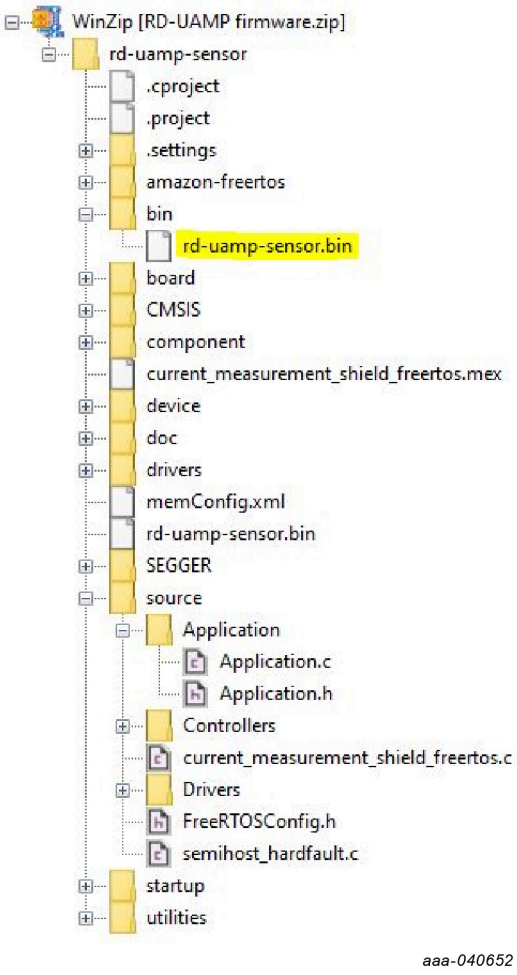


Figure 6. Firmware project archive content

7.3 Firmware structure

The RD-UAMP firmware is implemented as 3 layers, application, controllers, and drivers, detailed in Figure 7.

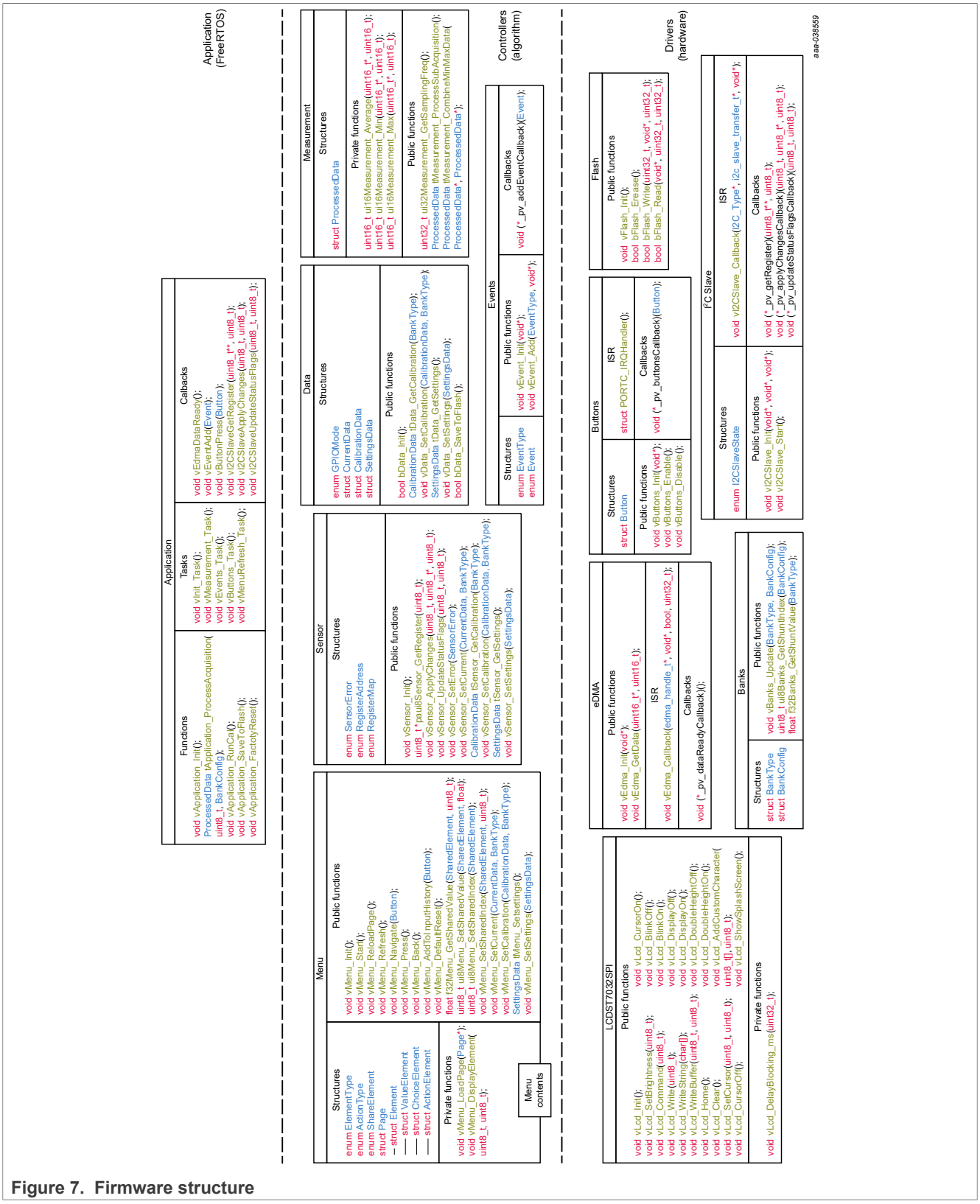


Figure 7. Firmware structure

8 STB-CE custom GUI

8.1 High-level description

The RD-UAMP-SENSOR reference design can be used with existing NXP sensor demo kits such as FRDM-KL25-A8471 and FRDM-K22F-AGMP03. The RD-UAMP board is inserted as per Figure 4, and acts as an interposer between the Kinetis Freedom board and the sensor shield board. Once the 3 boards are stacked, the demo kit is used in the exact same way as it is without RD-UAMP-SENSOR board, which means it is connected to the computer through the OpenSDA USB port as usual.

The RD-UAMP-SENSOR reference design supports existing NXP sensor demo kits such as FRDM-KL25-A8471 and FRDM-K22F-AGMP03. The RD-UAMP board is inserted as shown in Figure 4 between the Kinetis Freedom board and the sensor shield board. After stacking the boards as shown, connect the demo kit with the RD-UAMP-SENSOR board to the computer through the OpenSDA USB port.

The reference design emulates a simple current sensor with I^2C replica interface. The reference design is controlled and exercised by the host MCU of the Freedom board. After simple customization of the main sensor demonstration GUI, the RD-UAMP serves as a secondary sensor to visualize current measurements and settings.

The STB-CE archive content, shown in Figure 8, provides all files and packages needed to install and run FRDM-KL25-A8471 and FRDM-K22F-AGMP03 custom GUI.

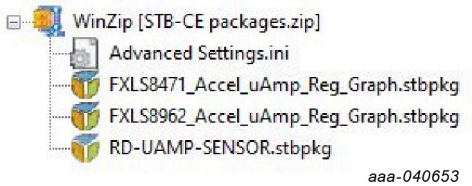


Figure 8. STB-CE packages archive content

8.2 Sensor toolbox installation

Download and install the Sensor Evaluation and Visualization Software for the Freedom Sensor Toolbox - Community Edition. Additional design tools may be downloaded from the Documentation and Development Tools tab

Custom GUIs for RD-UAMP are not part of the official STB-CE demos. Users customizing their application should copy the **Advanced Settings.ini** file from archive into **C:\Program Files (x86)\NXP\Freedom Sensor Toolbox (CE)\Configuration** default directory. This advanced settings file provides users the ability to manually select and launch the desired demo GUI.

Warning: *This advanced setting enables "Create Your Own GUI" mode in the STB-CE. NXP recommends using this mode only for selecting and launching uAmp Sensor custom GUI as described in the next steps. Using "Create Your Own GUI" mode in the STB-CE for any other purpose is not supported by NXP.*

8.3 Import of stbpkg packages

After the successful STB-CE installation, import all three packages from the archive by double-clicking them.

- **RD-UAMP-SENSOR.stbpkg**: This package contains the RD-UAMP sensor plugin for STB-CE. It defines RD-UAMP current sensor register map and data stream.
- **FXLS8471_Accel_uAmp_Reg_Graph.stbpkg**: This package is based on FXLS8471 official demo GUI (**FXLS8471 Accelerometer Demo** project). The package adds the current sensor measurement real-time graph, main settings and complete register map as a third tab.
- **FXLS8962_Accel_uAmp_Reg_Graph.stbpkg**: This package is based on **FXLS8962 Accelerometer Demo** official demo GUI and adds similar, previously mentioned features.

8.4 Run the custom demo GUI

This section explains how to use the **FXLS8471 Accel uAmp Reg Graph** GUI. The **FXLS8471 Accel uAmp Reg Graph** exercises the RD-UAMP-SENSOR associated with FRDM-KL25-A8471 demo kit.

Prior to use of the custom GUI, the Freedom board firmware must be updated in order for the KL25Z host MCU to communicate with and control the RD-UAMP current sensor. Figure 9 illustrates the firmware update procedure. The firmware update needs to be performed once and applicable for all.

1. After launching the STB-CE application, click “Create Your Own GUI”.
2. Under the Tools menu, select "Firmware Downloader".
3. Browse the firmware binary file as indicated.
4. Select the USB drive associated with the Freedom board.
5. Click the "Download" button and wait and follow GUI instructions.

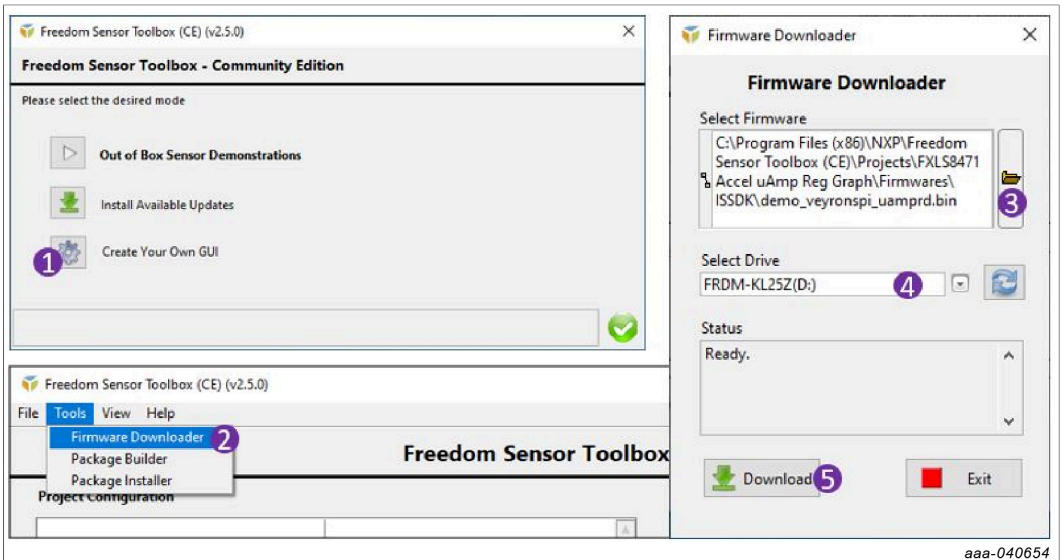


Figure 9. Freedom demo kit FW update

After the firmware update, restart the STB-CE application. Click “Create Your Own GUI”. However, at this time, select the desired Project Name and launch it. Refer to Figure 10.

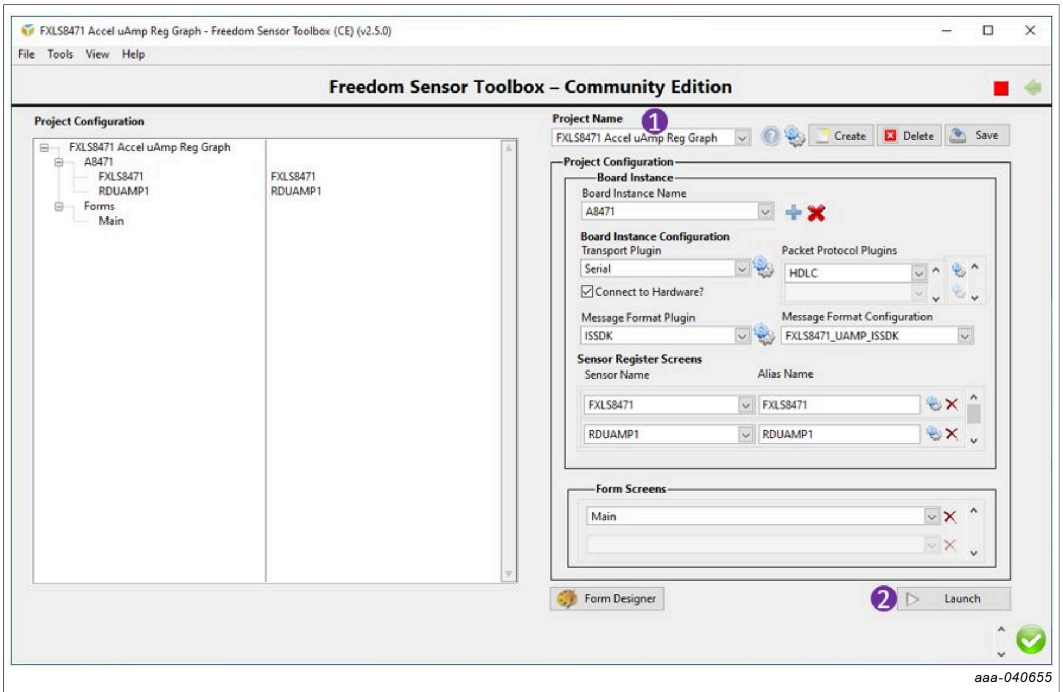


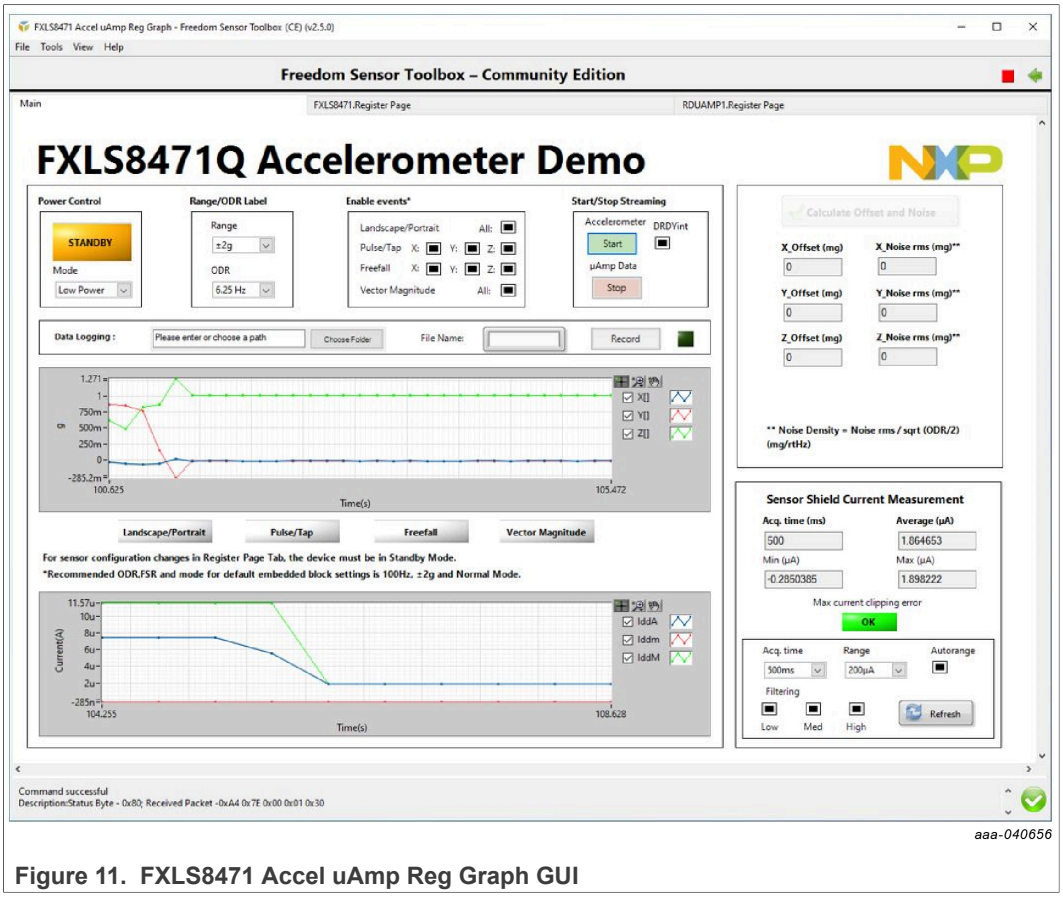
Figure 10. Custom GUI manual selection and Launch

The custom GUI main tab (Figure 11) includes most of the parent (official) GUI features and adds the RD-UAMP specifics:

- Graph vs. time of current sensor data (average, min and max) and their numerical values
- Main current sensor settings (acquisition time, range, filtering)

The data streams of both sensors (accelerometer and current meter) are started and stopped using their individual buttons.

The current sensor plot corresponds to the change in FXLS8471 consumption when transitioning from active mode to standby mode.



aaa-040656

Figure 11. FXLS8471 Accel uAmp Reg Graph GUI

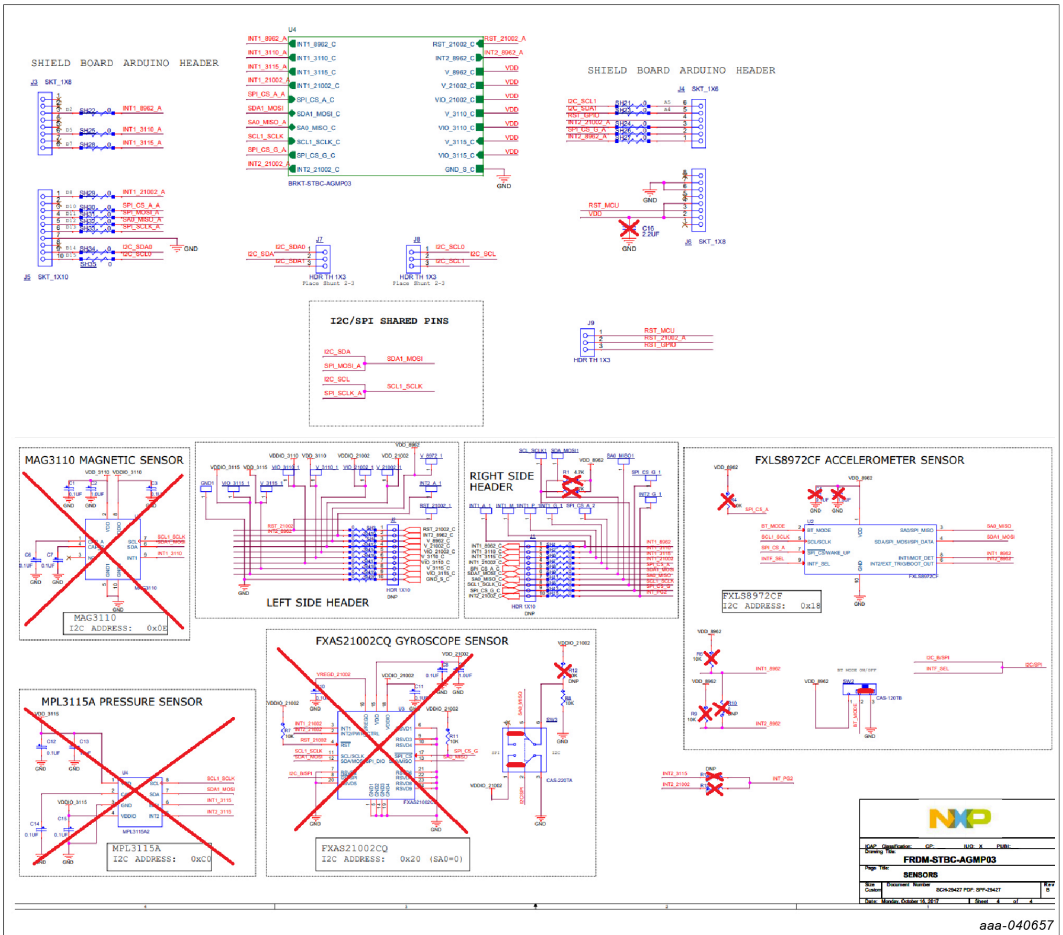
8.5 AGMP03 sensor shield modifications

The procedure presented in Section 8.4 also applies to FXLS8962 demo kit. Consequently, assuming that names of files and folders are transposed to this alternate sensor demo kit, updating the FRDM-K22F firmware and running the custom GUI is straightforward.

NXP recommends an important hardware modification to the demo kit shield. Besides the FXLS8962 sensor, the AGMP03 shield includes several additional sensors. As a result, the measured current on the shield corresponds to the total current of all sensors and does not reflect the standalone FXLS8962 current.

To eliminate the extra sensor consumption, remove all AGMP03 components not specifically needed for the FSLS8962 operation. All components marked with a red "X" in Figure 12 may be removed.

Note: *The jumpers on J7 and J8 are removed, and the SW2 and SW3 positions are indicated. In this case, FXLS8962 is used with BT_MODE=GND and SPI interface.*



aaa-040657

Figure 12. AGMP03 components to be removed

9 Legal information

9.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Bluetooth — the Bluetooth wordmark and logos are registered trademarks owned by Bluetooth SIG, Inc. and any use of such marks by NXP Semiconductors is under license.

Tables

Figures

Contents