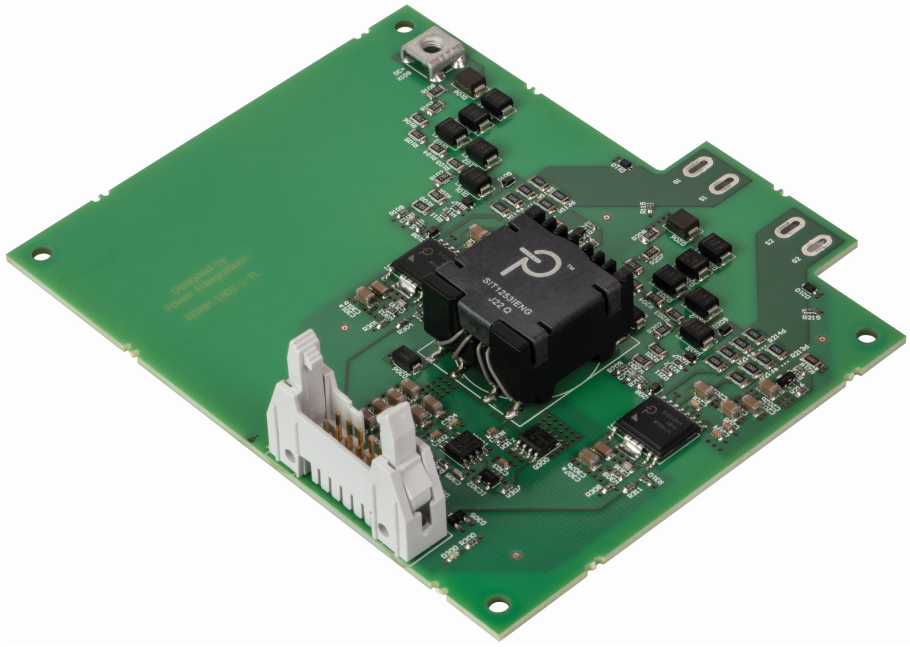
General Purpose Base Board for SCALE-iDriver™ SIC1182K

Application	General purpose drives, UPS, PV power and others
Specification	• Suitable for Half-bridge SiC-MOSFET power modules in 62mm housing • Up to 800V DC-link voltage • Electrical Interface • Short Circuit Detection • Advanced Active Clamping • Source-Controller
Author	Application Engineering Gate Drivers
Document Number	RDHP-1901
Revision[1]	A.2



[1] The letter refers to the hardware revision. The number refers to the documentation revision.

Scope

This application proposal provides a circuit design for a general purpose base board for driving various SiC-MOSFET power modules.

Main features of the design are:

- Suitable for SiC-MOSFET power modules in 62mm housing with a maximum blocking voltage of 1200 V
- Two channels for half-bridge modules
- Short Circuit Detection
- Advanced Active Clamping
- Electrical command inputs and status outputs
- 0 V/5 V command input logic
- 0 V/5 V status output logic
- Minimum pulse suppression
- 5 V supply voltage
- Single PCB solution with soldered-in gate driver IC
- Adjustable Source Controller

Intellectual Property Licensing

The design proposal, products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations.

A complete list of Power Integrations patents may be found at https://www.power.com/.

Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

Application Conditions

The design is proposed for the following application conditions:

- general purpose applications
- SiC-MOSFET power modules
- Up to 8 A peak current
- Up to 1.3 W per channel
- Ambient Temperature: -40… 85°C

Design Description

In addition to the following design description, reference to datasheet of the gate driver SIC1182K is recommended.

Equivalent Circuit

As an overview the equivalent circuit of the design RDHP-1901 is shown in Figure 1.

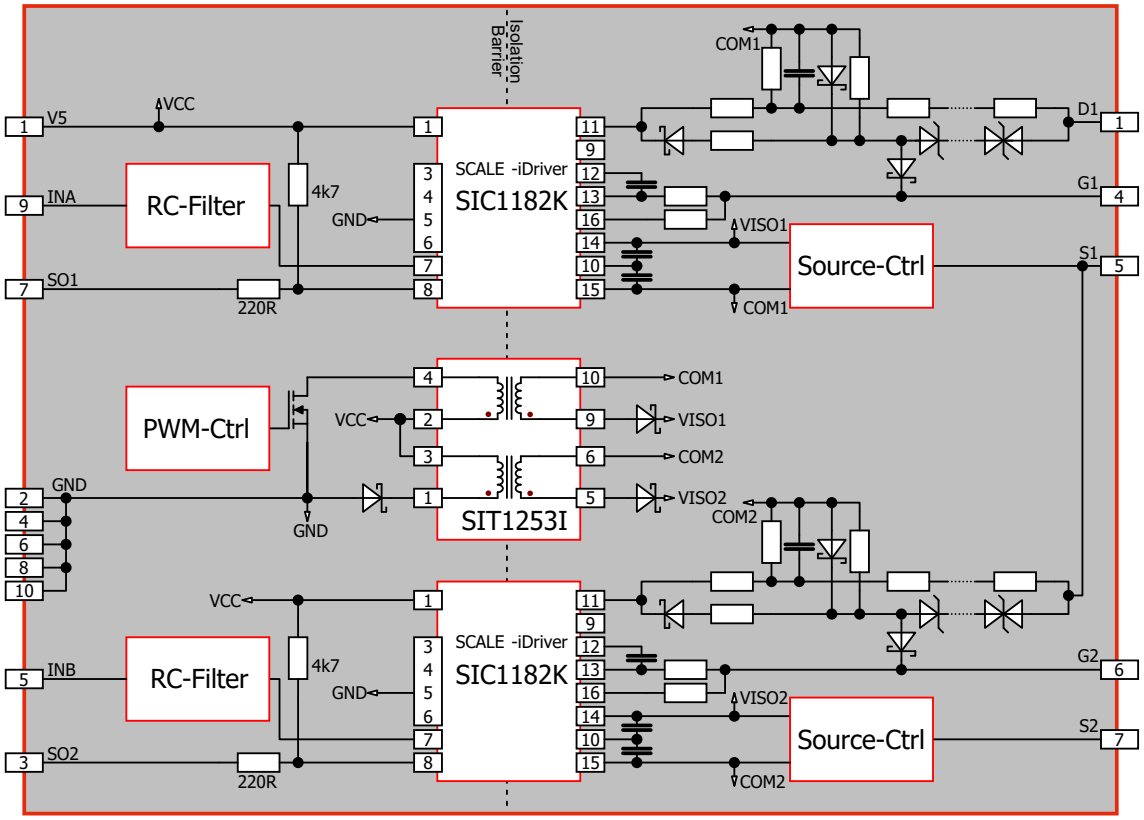


Figure 1: Equivalent Circuit of RDHP-1901

Gate Resistors

Gate resistor values are not explicitly given as they depend on the power module used and on the application. Gate resistors of SMD (size 1206) package can be selected. Their position is depicted in Figure 2.

Turn-On Gate Resistors		Turn-Off Gate Resistors	
Channel	**SMD Package**	**Channel**	**SMD Package**
1	R113a … R113d	1	R114a … R114d
2	R213a … R213d	2	R214a … R214d

The gate resistors must be determined and assembled by the user.

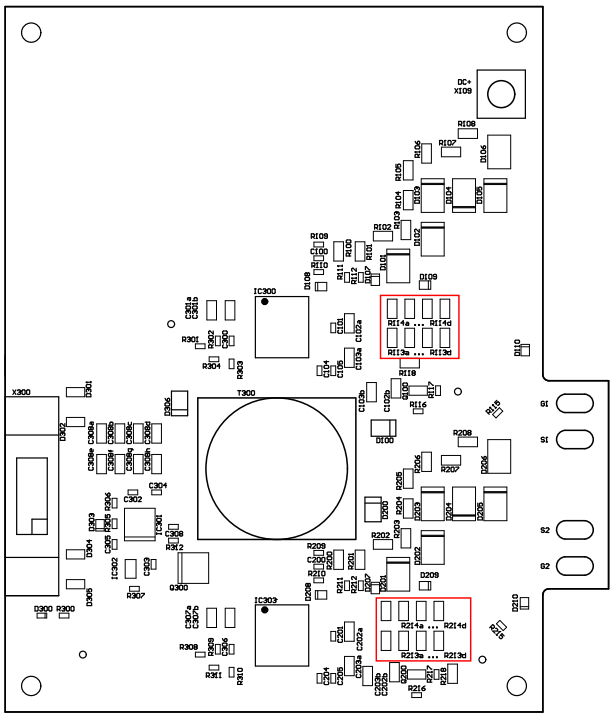


Figure 2: Position of Gate Resistors

Short Circuit Detection

The SIC1182K gate driver IC from Power Integrations provides a sense input for monitoring short-circuit conditions of the power semiconductor. This design offers a short circuit detection function using a resistor network. A assembly variant of implementation tested with Wolfspeed CAS300M12BM2 is described in the following table:

Channel	Resistor Chain	Timing Resistor	Timing Capacitor	Decoupling Resistor
1	R100 … R108	R109	C100	R110
	270 kΩ each	180 kΩ	N.A.	100 kΩ
2	R200 … R208	R209	C200	R210
	270 kΩ each	180 kΩ	N.A.	3.3 kΩ

All mentioned components as shown in Figure 3 can be changed to meet the desired behavior of the short circuit detection.

- R100 … R108 and R200 … R208 are dimensioned for 1200 V power semiconductors and can be decreased according to data sheet of SIC1182K when using lower voltage ranges.
- Increasing R109 and R209 accelerates the SC detection time and lowers the detection threshold voltage.
- Increasing C100 and C200 increases the short circuit detection time but avoids false tripping and weakens the Active Clamping efficiency if implemented.
- Decreasing R110 and R210 helps to avoid false tripping of the short circuit detection.

The details of the short circuit detection function are described in the corresponding data sheet of the gate driver.

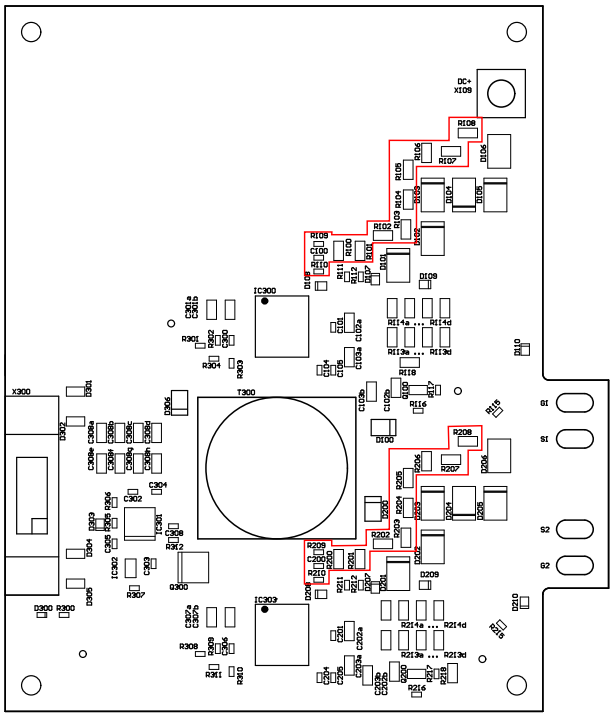


Figure 3: Position of components for Short Circuit Detection

Advanced Active Clamping

Active clamping is a technique designed to partially turn on the power semiconductor in case the voltage across the device exceeds a predefined threshold. The power semiconductor is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the Collector/Drain through transient voltage suppressor (TVS) diodes to the gate. This design proposal supports Power Integrations Advanced Active Clamping realized by the SNS pin of the SIC1182K based on the following principle.

When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. At the same time the turn-on MOSFET of the SIC1182K is supplying (additionally to the TVS diodes) a controlled gate current to keep the power semiconductor in the active region. This feature called Advanced Active Clamping is mainly integrated in the secondary side of the SIC1182K.

A assembly variant as shown in Figure 4 of implementation tested with Wolfspeed CAS300M12BM2 is described in the following table:

Channel (x)	**TVS Chain**	**TVS, bidirectional**
1 and 2	Dx01 … Dx05	Dx06
	Littelfuse P6SMB150A-E3	Vishay P6SMB150CA

Here the theoretical voltage limitation level is set to 900 V for a power semiconductor in the 1200 V-class. This value has to be changed accordingly when lower voltage classes are used.

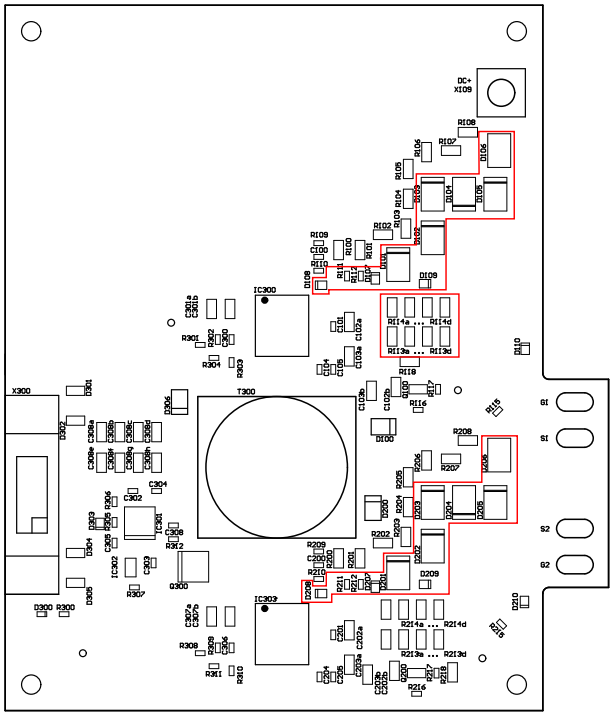


Figure 4: Position of components for Advanced Active Clamping

Minimum Pulse Suppression

This design possesses a minimum pulse suppression with a time constant τ of typically 99 ns. If required the setting can be changed by adjusting C300 and C306 which are depicted in Figure 5. The time constants are given by the following equations.

$$\tau_1 = 99\,\Omega \cdot \text{C300} \quad (1)$$

$$\tau_2 = 99\,\Omega \cdot \text{C306} \quad (2)$$

Recommended values of C300 and C306 are in the range of 1 nF (τ_x = 99 ns) to 3.3 nF (τ_x = 327 ns), depending on the actual application conditions.

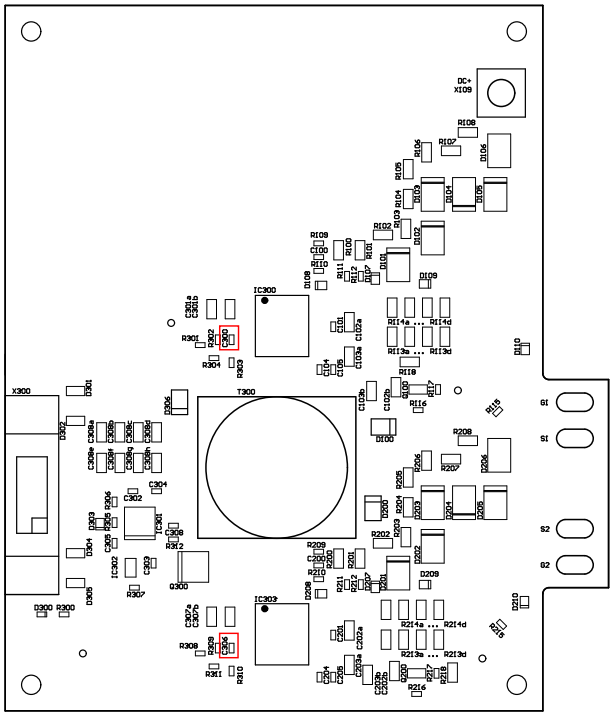


Figure 5: Position of Capacitors for the Minimum Pulse Suppression

Blocking Time

During the blocking time, which is set to typically 10 µs, the SIC1182K ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver IC's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

For further details refer to the data sheet of the gate driver SIC1182K.

Source Controller

In order to realize the appropriate gate switching voltage levels an external source controller in addition to the SIC1182K is used. The following voltage levels are provided:

- Positive Rail ($V_{VISO-Source}$): 20 V (controlled)
- Negative Rail ($V_{Source-COM}$): -5 V (load dependent)

The positive rail is controlled by the help of a shunt regulator TL431BFDT by NXP. The regulated voltage is calculated with equation 3 using V_{ref} =2495 mV and I_{ref} =2 µA.

$$V_{VISO-Source} = V_{ref} \cdot \left(1 + \frac{Rx16}{Rx17}\right) + I_{ref} \cdot Rx16 \quad (3)$$

In the proposed design the resistors like highlighted in Figure 6 are set to the following values:

- Rx17=1.3 kΩ
- Rx16=9.1 kΩ
- Rx18=680 Ω (series resistor)

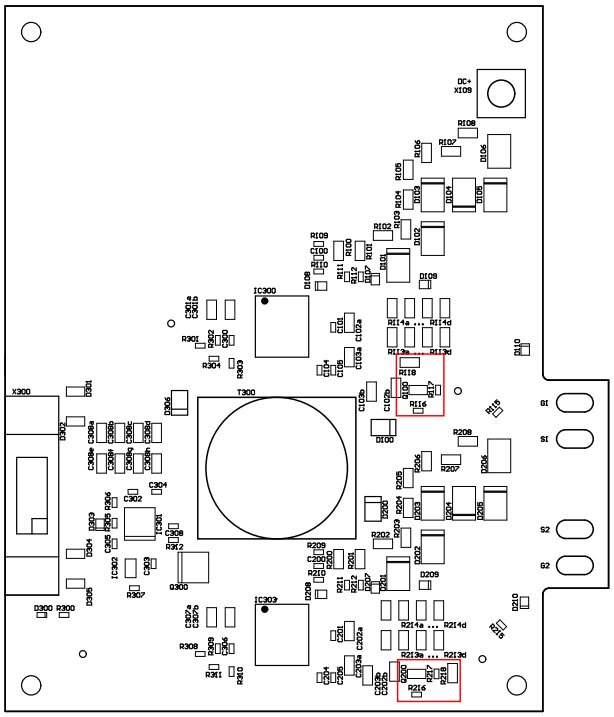


Figure 6: Position of Capacitors for the Minimum Pulse Suppression

Interfaces

The position of the interfaces of RDHP-1901 can be taken from Figure 7.

Electrical Interfaces

X300		
Pin	**Designation**	**Description**
1	V5	15 V-Power Supply (refernced to GND)
2	GND	Ground
3	SO2	Status Output, Channel 2
4	GND	Ground
5	INB	Command Input, Channel 2
6	GND	Ground
7	SO1	Status Output, Channel 1
8	GND	Ground
9	INA	Command Input, Channel 2
10	GND	Ground
X400		
4	G1	Gate of Top Switch
5	S1	Source of Top Switch
6	G2	Gate of Bottom Switch
7	S2	Source of Bottom Switch
X109		
1	DC+	Drain/Collector of Top Switch, positive DC-Link Connection for 2-Level-Application

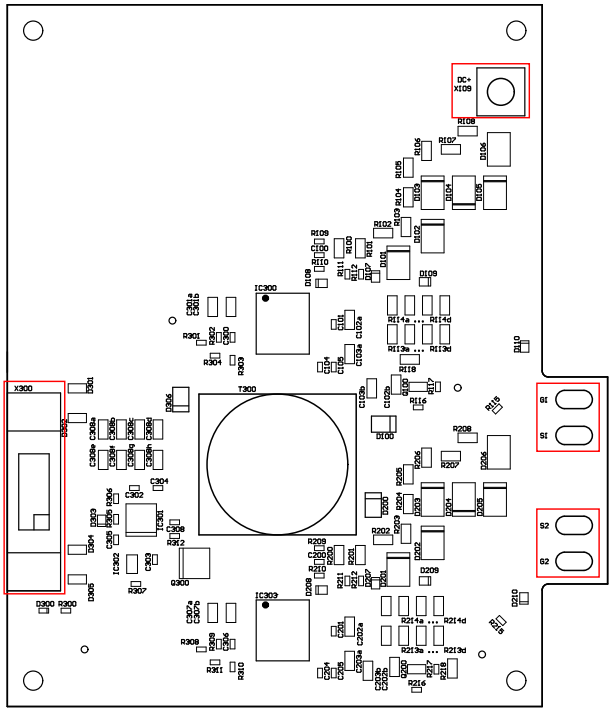


Figure 7: Position of Interfaces

CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, assembly drawing, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

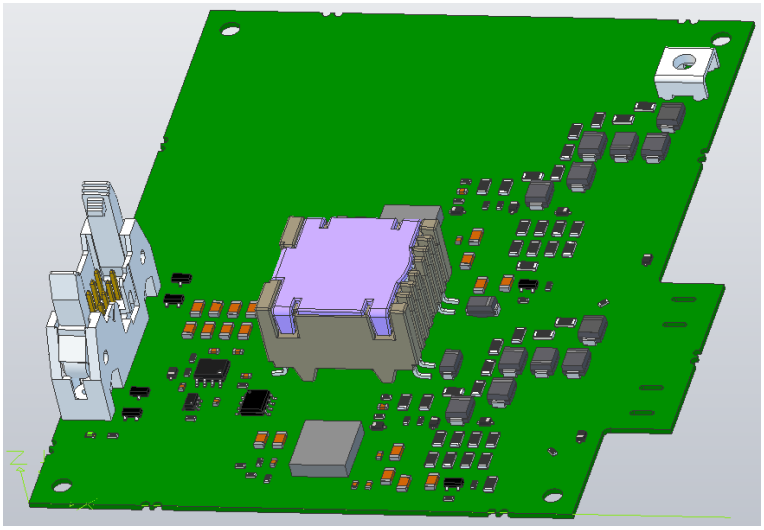


Figure 8: 3D-View on RDHP-1901

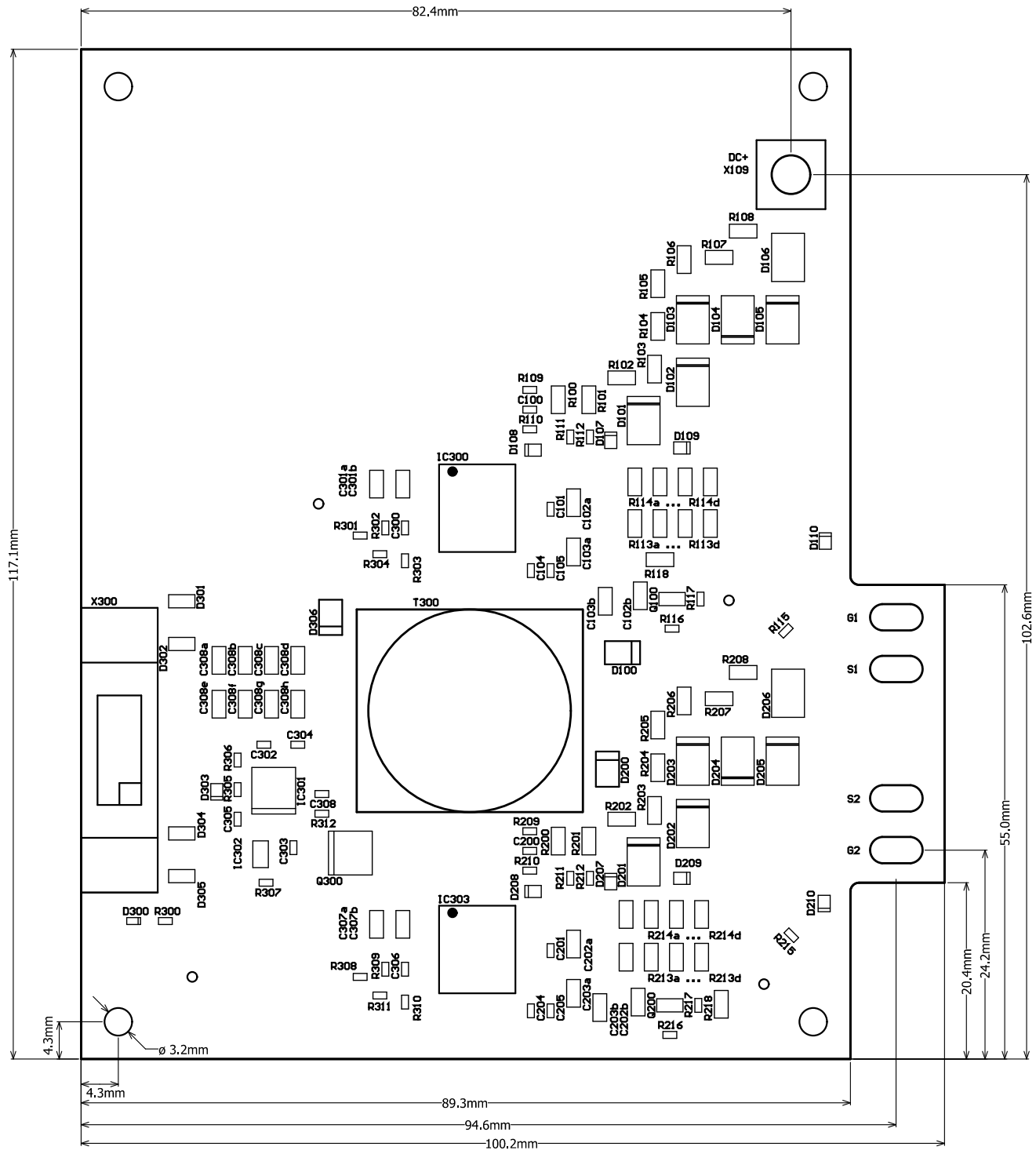
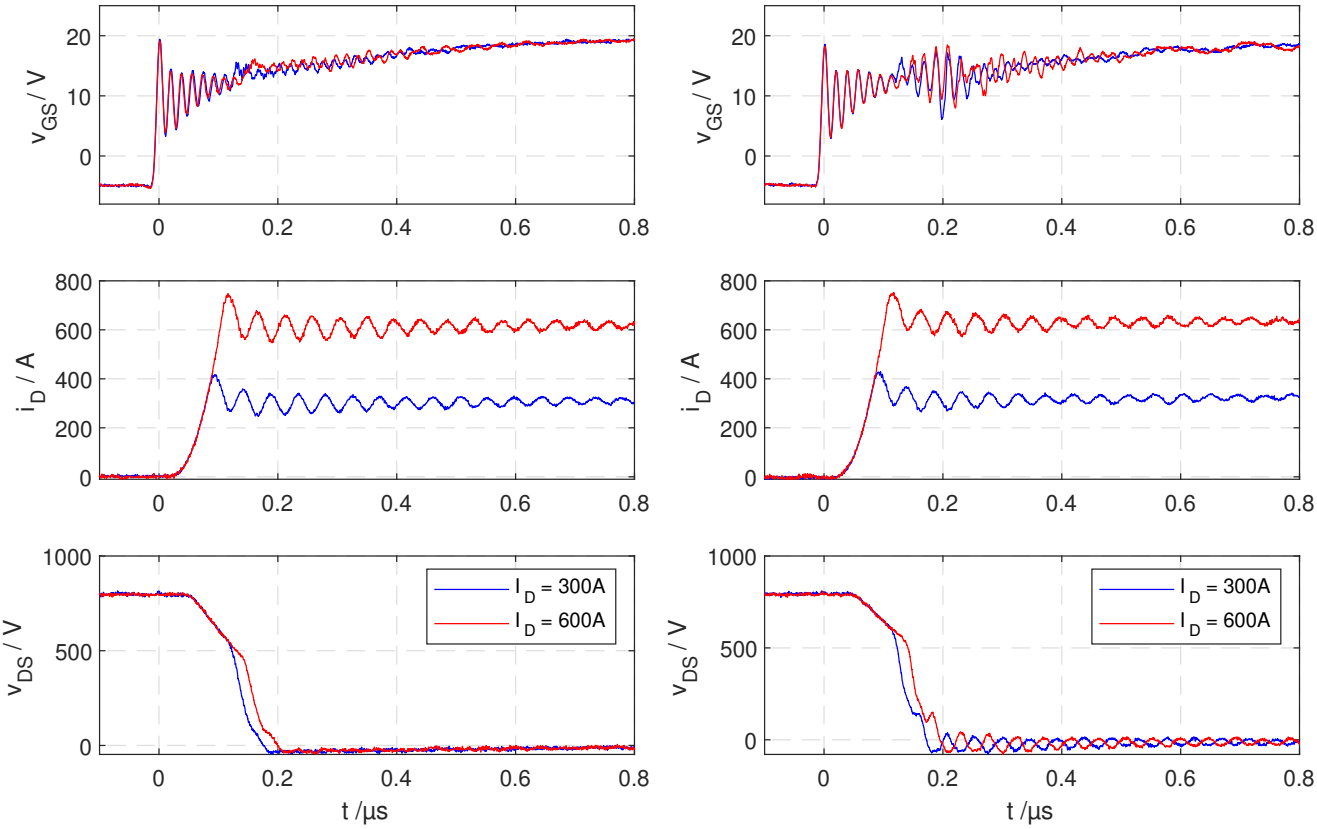


Figure 9: Assembly Drawing of RDHP-1901

Switching Characteristics

Turn-On and Turn-Off Behavior

The measurement examples shown with the SiC power module Wolfspeed CAS300M12BM2 ($R_{G,ON}$ =2.5 Ω and $R_{G,OFF}$ =2.5 Ω) as depicted in Figure 10 and 11 were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of 800 V. The adjusted load current is either nominal current (300 A) or twice nominal current (600 A).



(a) Bottom Channel (b) Top Channel

Figure 10: Turn-On Behavior at V_{DC} =800 V

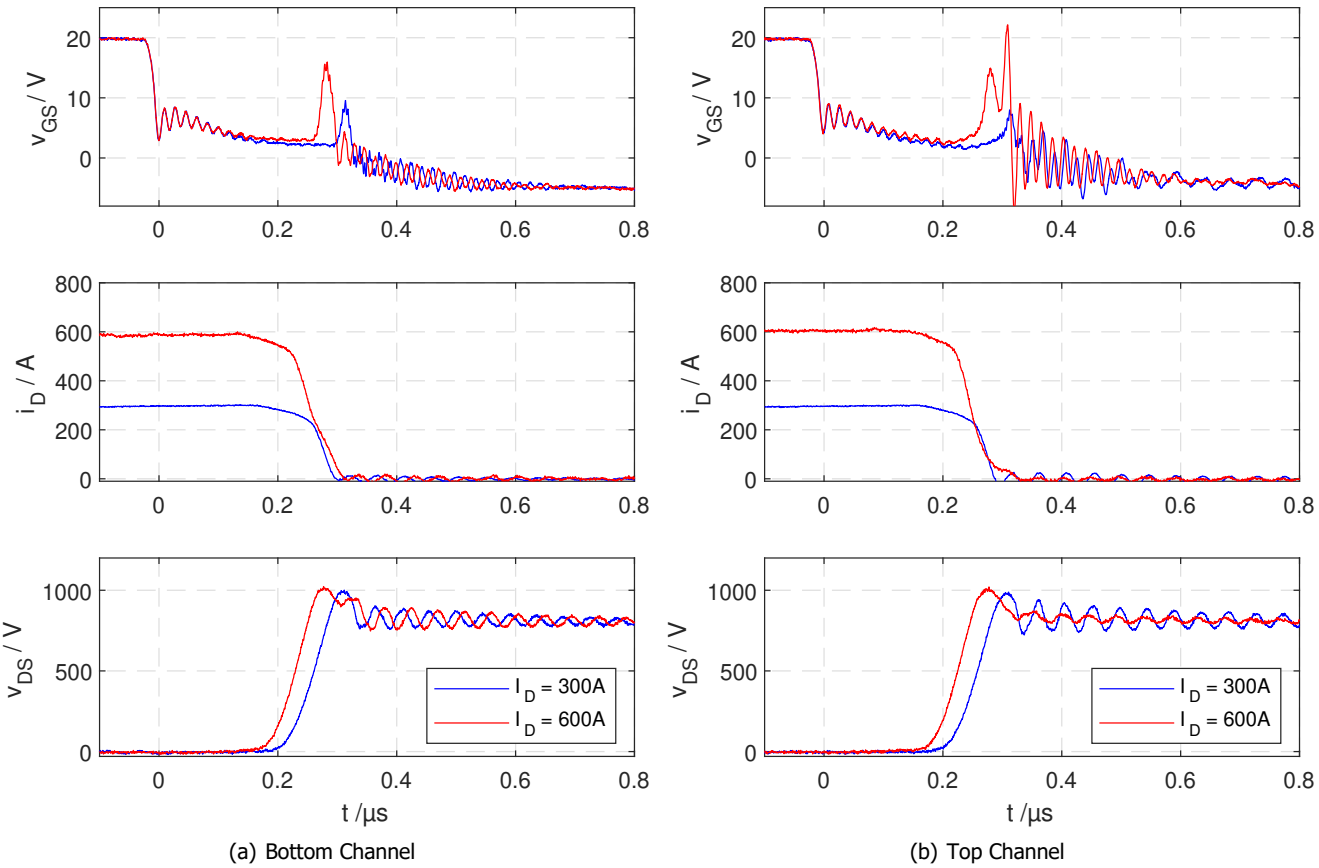
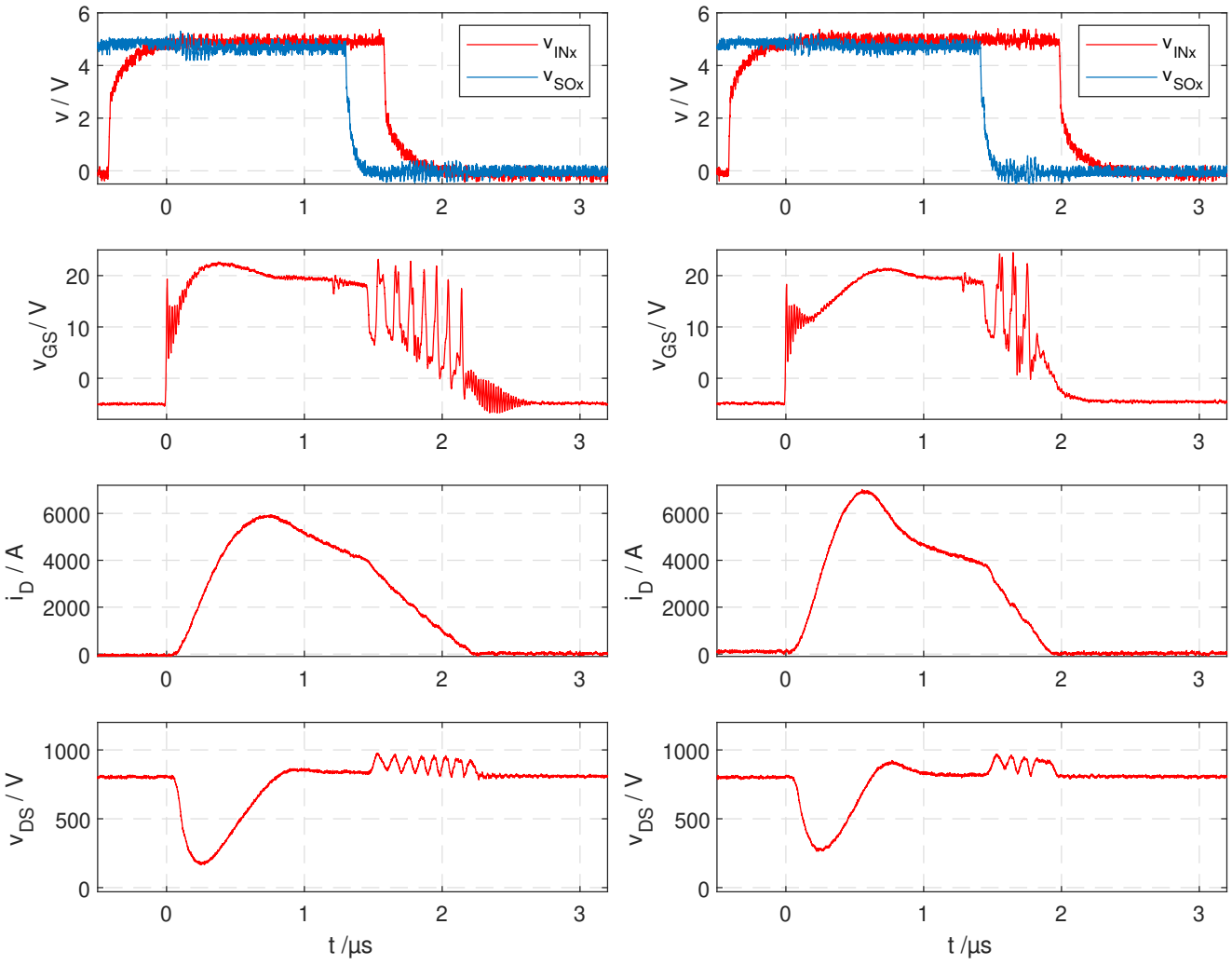


Figure 11: Turn-Off Behavior at V_{DC} = 800 V

Short Circuit Behavior

The measurement examples shown with the SiC power module Wolfspeed CAS300M12BM2 ($R_{G,ON}$ =2.5 Ω and $R_{G,OFF}$ =2.5 Ω) as depicted in Figure 12 were carried at room temperature with an initial DC-link voltage of 800 V.



(a) Bottom Channel (b) Top Channel

Figure 12: Short Circuit Behavior at V_{DC} =800 V

Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /1/.

References

/1/ Application Note AN-0902, Avoiding ESD with CONCEPT Drivers, Power Integrations

History

Date	Version	Changes
2019-04-04	A.1	Initial Version
2019-09-10	A.2	Pinning corrected in Figure 1, History added

Technical Support

Power Integrations provides expert help with your questions and problems:

Website http://www.power.com/igbt-driver/go/support

Email igbt-driver.support@power.com

Quality

The obligation to high quality is one of the central features laid down in the mission statement of Power Integrations. Our total quality management system assures state-of-the-art processes throughout all functions of the company, certified by ISO9001:2008 standards.

Legal Disclaimer

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user.

The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Power Integrations provides expert help with your questions and problems:

Website http://www.power.com/igbt-driver/go/support

Email igbt-driver.support@power.com