Title	***Reference Design Report for a 2.5 W Universal Input, Non-Isolated Buck Converter with Zero Crossing Detection Using LinkSwitch™-TNZ LNK3307D***
Specification	90 VAC – 300 VAC Input; 5 V / 500 mA Output
Application	Home Building Automation & IoT
Author	Applications Engineering Department
Document Number	RDR-866
Date	June 3, 2021
Revision	1.0

Summary and Features

- 5 V / 500 mA output for wireless (WiFi, NBIoT etc.) and relay power
- Low cost and component count buck converter using off-the-shelf inductor
- Compact solution 1.25" x 1.25" x 0.6"
- AC zero crossing signal output
- Optimized for <10 dB audible noise performance
- No-load input power <50 mW
- Excellent output voltage line regulation (<2% 5 V_{TYP})
- Reduced dissipation during output short-circuit fault
- Low output voltage ripple <100 mV_{PK-PK}
- >6 dB conducted EMI margin

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

1 Introduction

This engineering report describes a non-isolated buck converter power supply with an input line Zero Crossing Detection (ZCD) output signal. The nominal output is 5 V, 500 mA across the input range of 90-300 VAC. The PSU is powered by the LinkSwitch-TNZ IC controller.

The LinkSwitch-TNZ family of ICs combine power conversion with lossless generation of AC zero crossing signal used typically for system clock and timing functions. The device incorporates a 725 V power MOSFET, oscillator, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and input overvoltage protection circuitry onto a monolithic IC. Designs using the highly integrated LinkSwitch-TNZ ICs are more flexible than discrete implementations reducing component count by 40% or higher.

The key design goal is low cost, low audible noise and compact form factor intended for wireless (WiFi, NBIoT etc.) and relay power.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, performance and test data.

Figure 1 – Populated Circuit Board, Top View.

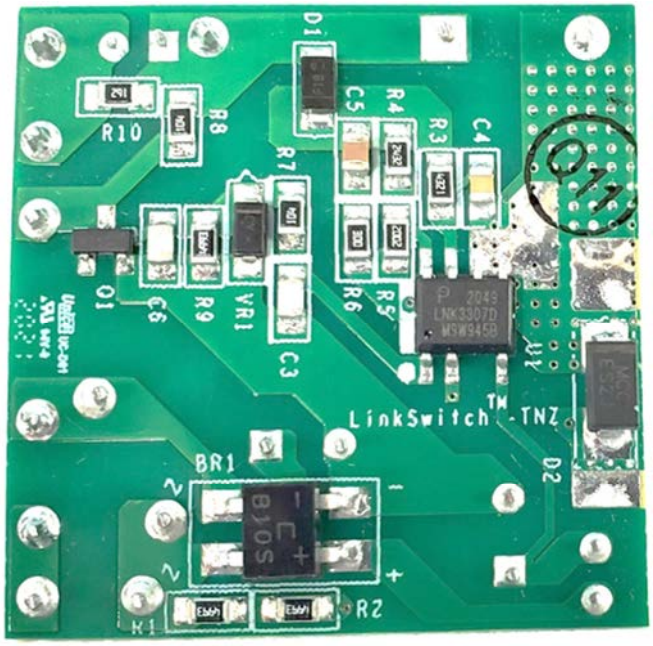


Figure 2 – Populated Circuit Board, Bottom View.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		300	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				50	mW	
Output						
Output Voltage	V_{OUT}		5		V	
Output Current	I_{OUT}		500		mA	
Output Ripple Voltage	V_{RIPPLE}			100	mV	Full Load Condition.
Rated Output Power	P_{OUT}		2.5		W	
Efficiency						
Full Load	η	65%				Full Load.
Environmental						
Conducted EMI		CISPR22B / EN55022B Load Floating				6 dB Margin Using Resistive Load.
Line Surge						
Combination Wave				1	kV	Combination Wave: 2 Ω.
Ring Wave				2.5	kV	Ring Wave: 12 Ω.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

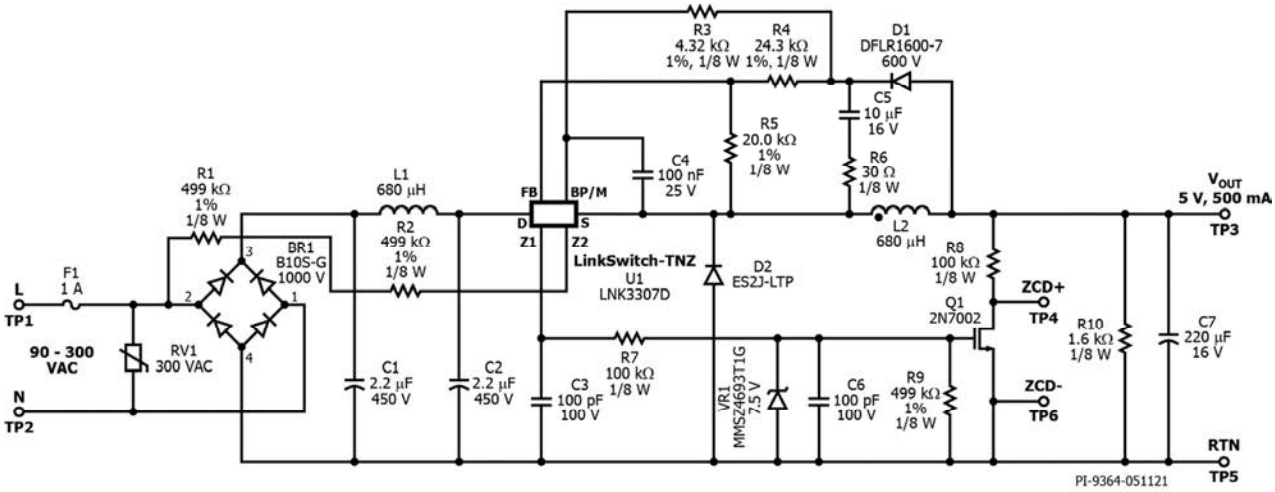


Figure 3 – Schematic.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

4 Circuit Description

4.1 *Input Stage*

Fuse F1 provides safety protection in case of component failure in the power supply circuitry. Varistor RV1 limits the voltage to protect the circuitry during line transient voltage surge events. The bridge rectifier diode BR1 converts AC input to DC voltage by full wave rectification. Bulk capacitors C1, C2 and differential inductor L1 form a Pi filter to minimize bulk ripple voltage and provide differential mode EMI noise filtering.

To improve conducted EMI, power inductor L2 must be placed away from the input side to reduce switching noise coupling. The ZCD line sense resistor R1 and R2 are very high impedance components connected directly to the input side. These resistors must be placed away from the IC or close to the input side to prevent coupling of switching noise.

4.2 *LinkSwitch-TNZ Circuit Operation*

The power supply circuit is a high-side buck converter topology where the power MOSFET inside U1 (LinkSwitch-TNZ) is connected at the positive bulk rail. The main buck converter circuitry comprises of U1, freewheeling diode D2, buck inductor L2 and output capacitor C7. When the MOSFET internal to LinkSwitch-TNZ U1 turns on, the current through the inductor L2 starts to ramp up producing an opposing voltage across its terminal. With respect to the input voltage, the opposing voltage across inductor L2 reduces the output voltage that is delivered to the load. At this point, the freewheeling diode D2 is reverse bias. When U1 MOSFET turns off, the voltage across inductor L2 commutates forward biasing the freewheeling diode D2. The current through inductor L2 starts to ramp down supporting the current flow to the load.

Capacitor C3 with a value of 100 nF sets the current limit to Standard mode. At power-up, the IC is initially powered from the DRAIN (D) pin. The 5V regulator internal to the IC, charges the BYPASS (BP) pin capacitor C3 to power the IC. When the MOSFET turns on, the external bias resistor R3 charges the BP pin capacitor C3 easing up the powering of LinkSwitch-TNZ. The bias voltage must be higher than the BP pin voltage to effectively help power the LinkSwitch-TNZ. For a 5 V output application, adding resistor R6 in series with bias capacitor C5 increases the output voltage at no-load, lowering the no-load input power. Bias resistor R3 must be optimized with respect to the bias voltage to deliver the best efficiency and minimal no-load input power. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than I_{S1}. For the best full-load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than the I_{S2} Max value.

During normal operation, the switching of the power MOSFET is controlled by the FEEDBACK pin through LinkSwitch-TNZ On/Off control engine. MOSFET switching is terminated when a current greater than I_{FB} (49 µA) is delivered into this pin. The feedback voltage is sampled by resistors R4 and R5 across the bias supply voltage, which

track the output voltage. R6 is added in series with C5 to reduce ripple voltage and audible noise.

Pre-load resistor R10 limits the output voltage during a no-load condition.

4.3 *Zero Crossing Detection Circuit*

The LinkSwitch-TNZ IC integrates a low power consumption Zero Cross Detection circuit with Z1 and Z2 as Zero-Detect pins. Z2 is connected to one of the input AC lines through sense resistors R1 and R2, while Z1 forms the ZCD signal output. The Zero Cross Detection circuit internal to the IC senses the high-voltage AC input via R1 and R2 and drives the external ZCD signal generator circuit. For conducted EMI consideration, R1 and R2 which are high-impedance components must be connected near the input line terminal or away from the IC to minimize noise coupling.

During the input AC positive half-cycle with respect to NEUTRAL, Z1 and Z2 allow current flow to drive MOSFET Q1 at the on-state, pulling down the ZCD voltage to GND. During the negative half-cycle of the input AC, Z1 and Z2 block the current flow turning off Q1. At this point, resistor R8 pulls up the ZCD voltage equal to the output voltage. Zener diode VR1 protects Q1 from high voltage stress. Resistor R9 discharges residual gate voltage stored from Q1 parasitic capacitances and C6 to turn off the MOSFET Q1 completely.

Passive components C3, C6 and R7 provide noise filtering to deliver a clean ZCD signal. These capacitors are sized for minimal effect to the delay of the ZCD signal.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

5 PCB Layout

Material: FR4
Copper: 2 oz

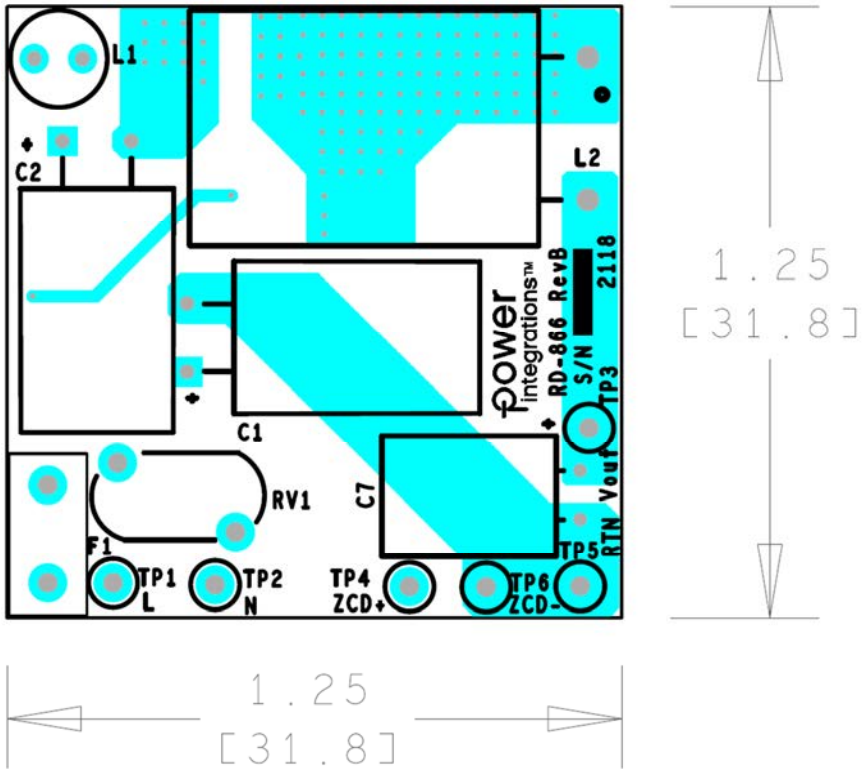


Figure 4 – Top Side.

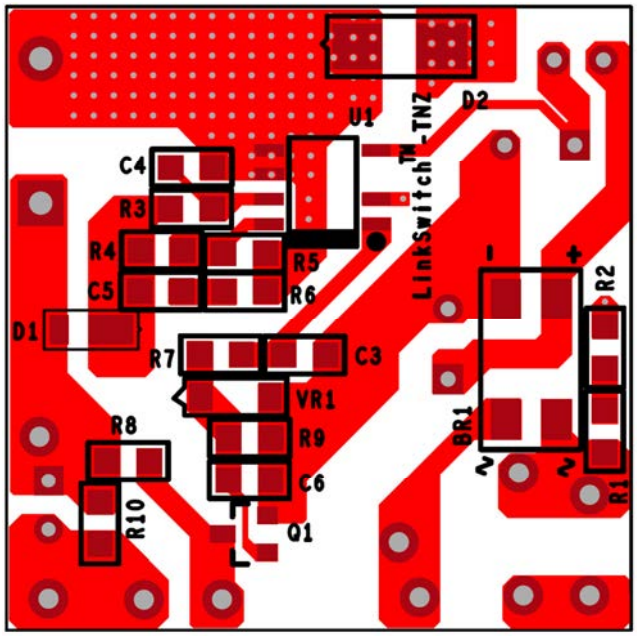


Figure 5 – Bottom Side.

6 Bill of Materials

6.1 *Electrical Parts*

Item	Ref Des	Qty	Description	Mfg Part Number	Manufacturer
1	BR1	1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	C1 C2	2	2.2 µF, 450 V, Electrolytic, (8 x 11.5)	UVK2W2R2MPD1TD	Nichicon
3	C3 C6	2	100 pF, 100 V, Ceramic, COG, 0805	C0805C101J1GACTU	Kemet
4	C4	1	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
5	C5	1	10 µF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
6	C7	1	220 µF, ±20%, 16 V, Electrolytic, Gen. Purpose, 2000 Hrs @ 105°C, (6.3 x 9)	A750EK227M1CAAE016	Nichicon
7	D1	1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes Inc
8	D2	1	600 V, 2 A, Superfast, 35 ns, DO-214AC, SMA	ES2J-LTP	Micro Commercial
9	F1	1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
10	L1	1	680 µH, 0.25 A, 5.5 x 10.5 mm	SBC1-681-251	Tokin
11	L2	1	680 µH, 0.8 A, 20%	RL-5480-4-680	Renco
12	Q1	1	60 V, 115 mA, SOT23-3	2N7002-7-F	Diodes Inc
13	R1 R2 R9	3	RES, 499 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4993V	Panasonic
14	R3	1	RES, 4.32 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4321V	Panasonic
15	R4	1	RES, 24.3 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2432V	Panasonic
16	R5	1	RES, 20.0 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
17	R6	1	RES, 30 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ300V	Panasonic
18	R7 R8	2	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
19	R10	1	RES, 1.6 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ162V	Panasonic
20	RV1	1	300 VAC, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
21	U1	1	LinkSwitch-TNZ, SO8	LNK3307D	Power Integrations
22	VR1	1	DIODE, ZENER, 7.5 V, ±5%, 500 mW, SOD123	MMSZ4693T1G	ON Semi

6.2 *Miscellaneous Part*

Item	Part Reference	QTY	Description	Mfg Part Number	Manufacturer
1	TP1 TP5 TP6	3	Test Point, BLK, Miniature THRU-HOLE MOUNT	Keystone	5001
2	TP2	1	Test Point, WHT, Miniature THRU-HOLE MOUNT	Keystone	5002
3	TP3	1	Test Point, RED, Miniature THRU-HOLE MOUNT	Keystone	5000
4	TP4	1	Test Point, BLUE, Miniature THRU-HOLE MOUNT	Keystone	5117

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

7 PI Expert Design Spreadsheet

1	ACDC_LinkSwitchTNZ_ Buck_032321; Rev.0.1; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-TNZ Buck
2	ENTER APPLICATION VARIABLES					
3	LINE VOLTAGE RANGE			Custom		AC line voltage range
4	VACMIN	90.00		90.00	V	Minimum AC line voltage
5	VACMAX	305.00	Info	305.00	V	The maximum AC line voltage is too high
6	fL			60.00	Hz	AC mains frequency
7	LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
8	VOUT	5.00		5.00	V	Output voltage
9	IOUT	0.500		0.500	A	Average output current
10	EFFICIENCY_ESTIMATED			0.80		Efficiency estimate at output terminals
11	EFFICIENCY_CALCULATED			0.69		Calculated efficiency based on real components and operating point
12	POUT			2.50	W	Continuous output power
13	CIN	4.40		4.40	uF	Input capacitor
14	VMIN			87.7	V	Valley voltage of the rectified minimum AC line voltage
15	VMAX			431.3	V	Peak voltage of the maximum AC line voltage
16	INPUT STAGE RESISTANCE	0		0	Ohms	Input stage resistance in ohms (includes thermistor, filtering components, etc)
17	PLOSS_INPUTSTAGE			0.000	W	Maximum input stage loss
21	**ENTER LINKSWITCH-TNZ VARIABLES**					
22	OPERATION MODE			MCM		Mostly continuous mode of operation
23	CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
24	XCAP REQUIRED	NO		NO		Select whether an X-capacitor is required or not
25	PACKAGE			SO-8C		Device package
26	DEVICE SERIES	LNK3307		LNK3307		Generic LinkSwitch-TNZ device
27	DEVICE CODE			LNK3307D		Required LinkSwitch-TNZ device
28	ILIMITMIN			0.725	A	Minimum current limit of the device
29	ILIMITTYP			0.780	A	Typical current limit of the device
30	ILIMITMAX			0.835	A	Maximum current limit of the device
31	RDSON			12.90	ohms	Primary switch on-time drain to source resistance at 100degC
32	FSMIN			62000	Hz	Minimum switching frequency
33	FSTYP			66000	Hz	Typical switching frequency
34	FSMAX			70000	Hz	Maximum switching frequency
35	BVDSS			725	V	Device breakdown voltage
52	**BUCK INDUCTOR PARAMETERS**					
53	INDUCTANCE_MIN			6120	uH	Minimum design inductance required for current delivery
54	INDUCTANCE_TYP	6800		6800	uH	Typical design inductance required for current delivery
55	INDUCTANCE_MAX			7480	uH	Maximum design inductance required for current delivery
56	TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
57	DC RESISTANCE OF INDUCTOR			2.0	ohms	DC resistance of the buck inductor
58	FACTOR_KLOSS			0.50		Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%)
59	IRMS_INDUCTOR			0.533	A	Maximum inductor RMS current
60	PLOSS_INDUCTOR			0.568	W	Maximum inductor losses
64	**FREEWHEELING DIODE PARAMETERS**					
65	VF_FREEWHEELING			0.70	V	Forward voltage drop across the

						freewheeling diode
66	PIV_RATING			600.0	V	Peak inverse voltage rating of the freewheeling diode
67	TRR			30	ns	Reverse recovery time of the freewheeling diode
68	PIV_CALCULATED			539.2	V	Computed peak inverse voltage across the freewheeling diode
69	IRMS_DIODE			0.529	A	Maximum diode RMS current
70	PLOSS_DIODE			0.356	W	Maximum freewheeling diode loss
71	RECOMMENDED DIODE			BYV26C		Recommended freewheeling diode
75	**BIAS/FEEDBACK PARAMETERS**					
76	VF_BIAS			0.70	V	Forward voltage drop of the bias diode
77	RBIAS			2490	Ohms	Bias resistor (connected across FB and S pin). Results into IFB_BIAS value of 803.213 uA
78	RBP			N/A	Ohms	No BP pin resistor required when output voltage is lower than 5.2V
79	CBP			0.1	uF	BP pin capacitor
80	RFB			3480	Ohms	Feedback resistor
81	CFB			10	uF	Feedback capacitor
82	C_SOFTSTART			N/A	uF	No soft-start capacitor required
83	PLOSS_FEEDBACK			0.004	W	Maximum feedback component losses

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

8 Performance Data

Electrical tests are done at room temperature otherwise specified.

8.1 *Full Load Efficiency vs. Input Line Voltage*

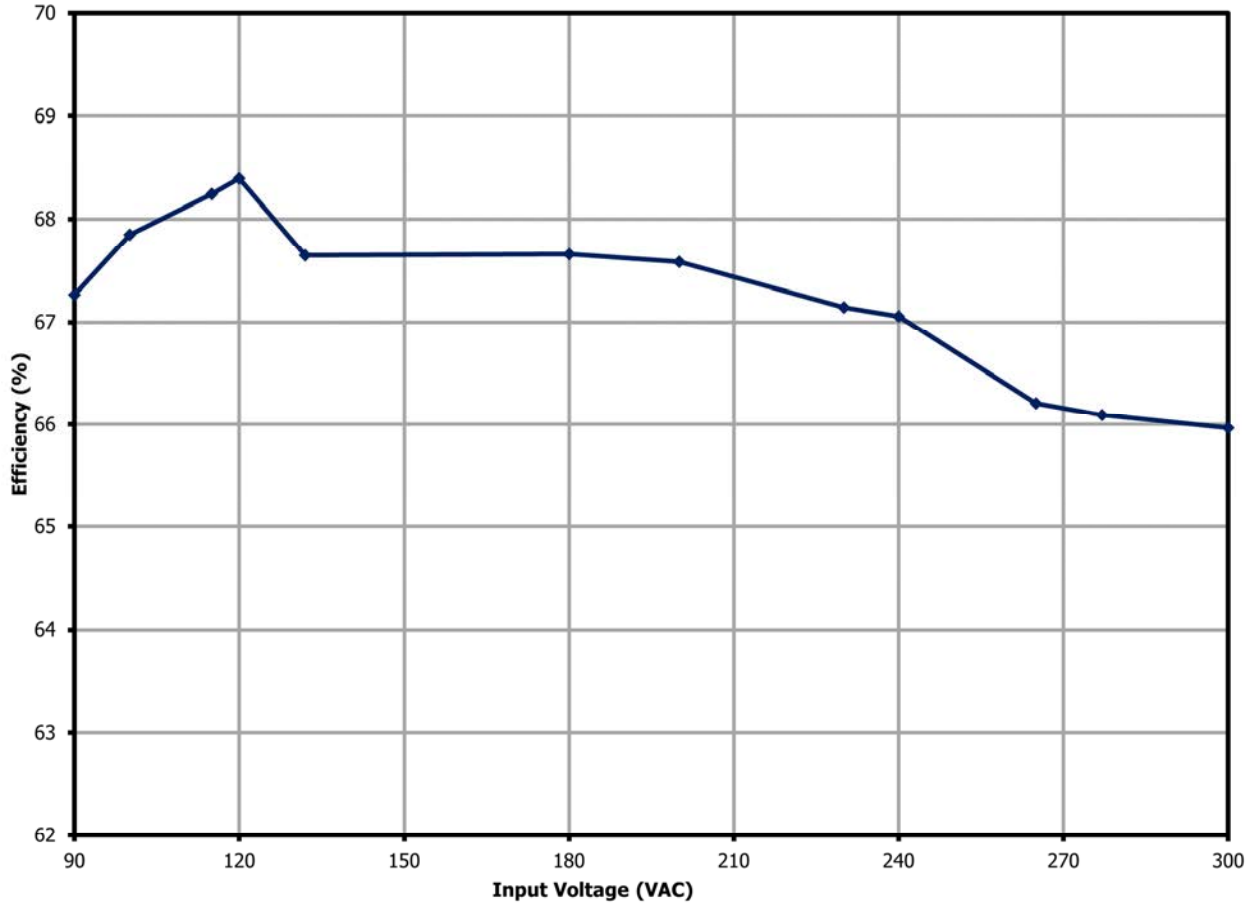


Figure 6 – Efficiency vs. Line Voltage.

8.2 *Efficiency vs. Load*

Measured using an E-load at CC mode loading Set-up. Output voltage is measured at the PCB side output terminal.

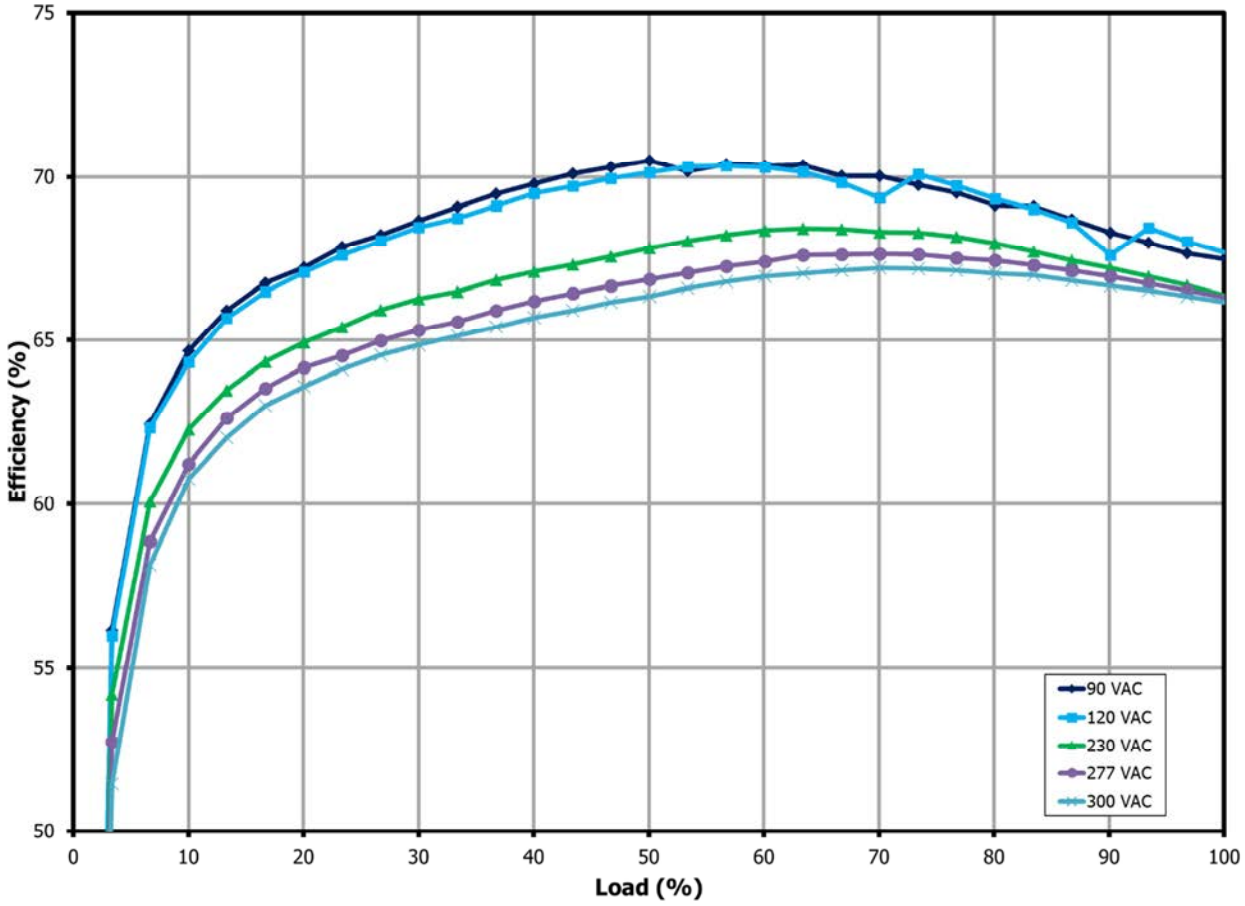


Figure 7 – Efficiency vs. Load.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

8.3 *No-Load Input Power*

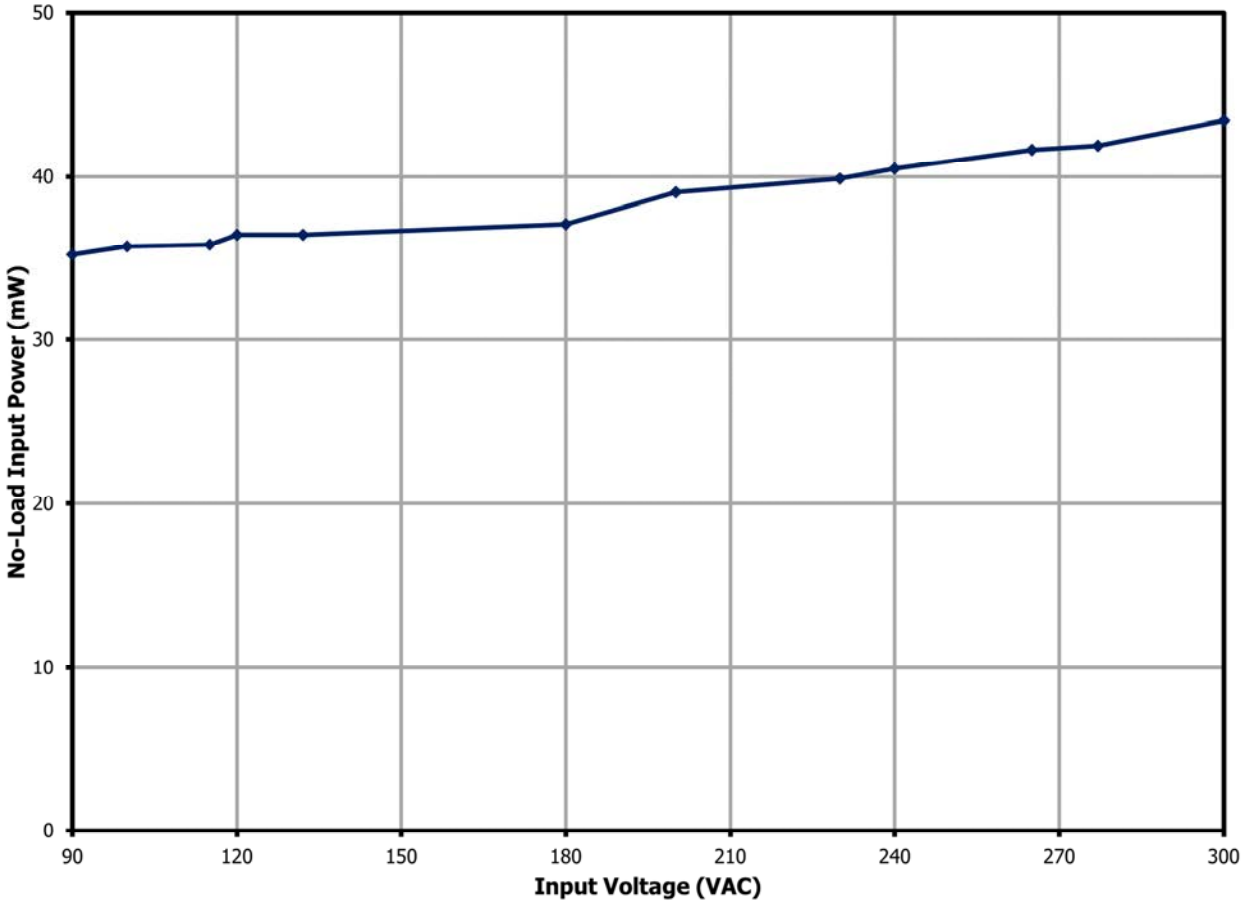


Figure 8 – No Load Input Power vs. Input Line Voltage.

8.4 *Line and Load Regulation*

8.4.1 Line Regulation

Measured using an E-load at CC mode loading set-up. Output voltage is measured at the PCB side output terminal.

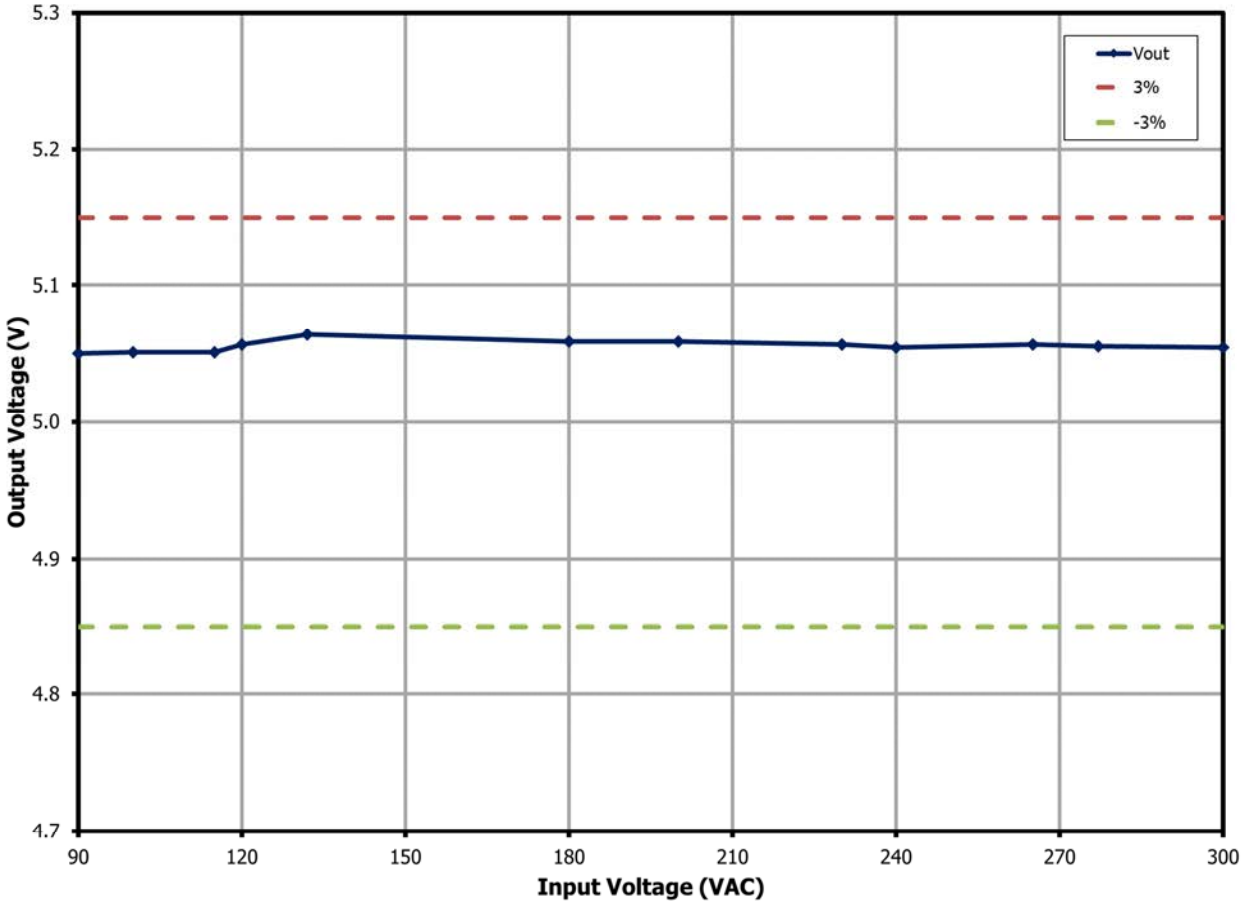


Figure 9 – Output Voltage vs Input Voltage at Full Load.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

8.4.2 Load Regulation

Measured using an E-load at CC mode loading set-up. Output voltage is measured at the PCB side output terminal.

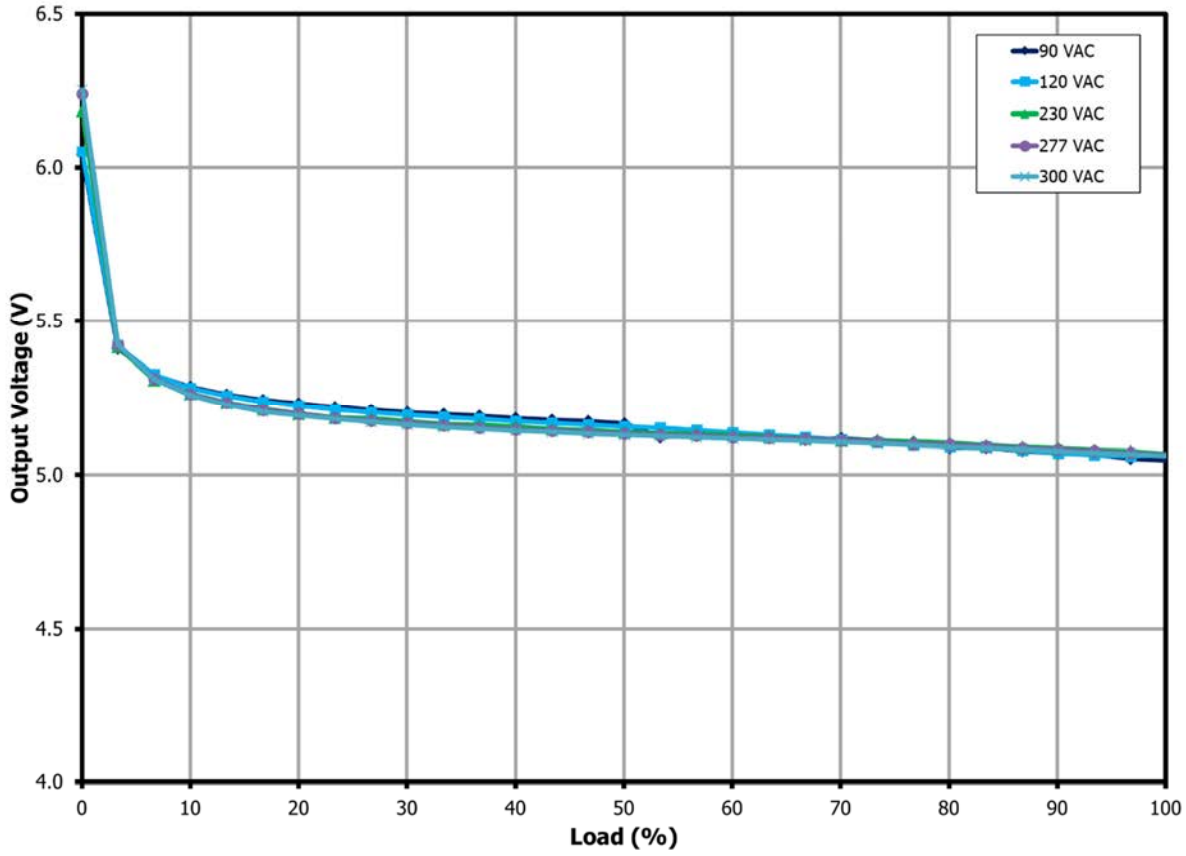


Figure 10 – Output Voltage vs Load.

9 Electrical Test Data

9.1 *Full Load Line Regulation and Efficiency*

Input		Input Measurement			Output Measurement				
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
90	60	89.97	69.64	3.76	5.05	500.55	2.53	1.00	67.26
100	60	100.00	63.46	3.73	5.05	500.36	2.53	1.02	67.85
115	60	115.01	57.15	3.70	5.05	500.45	2.53	1.02	68.25
120	60	119.99	55.56	3.70	5.06	500.45	2.53	1.13	68.39
132	60	131.99	52.77	3.75	5.06	500.55	2.53	1.28	67.65
180	60	180.00	43.74	3.74	5.06	500.36	2.53	1.17	67.66
200	50	199.96	39.75	3.75	5.06	500.45	2.53	1.17	67.58
230	50	229.96	36.97	3.77	5.06	500.45	2.53	1.13	67.14
240	50	239.99	36.16	3.77	5.05	500.45	2.53	1.08	67.06
265	50	264.96	34.61	3.82	5.06	500.45	2.53	1.13	66.21
277	60	276.99	35.10	3.83	5.06	500.36	2.53	1.11	66.10
300	60	300.06	33.86	3.84	5.05	500.55	2.53	1.08	65.97

9.2 *No-Load Regulation and Standby Power*

Input		Input Measurement			
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)
90	60	89.97	2.39	0.035	6.03
100	60	100.00	2.16	0.036	6.04
115	60	115.01	1.98	0.036	6.02
120	60	119.99	1.93	0.036	6.05
132	60	131.98	1.75	0.036	6.03
180	60	179.99	1.41	0.037	6.07
200	50	199.96	1.32	0.039	6.09
230	50	229.96	1.17	0.040	6.16
240	50	240.00	1.15	0.041	6.14
265	50	264.97	1.05	0.042	6.18
277	60	276.99	0.97	0.042	6.15
300	60	300.05	0.88	0.043	6.18

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

10 Waveforms

10.1 *Output Voltage Ripple*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 10 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

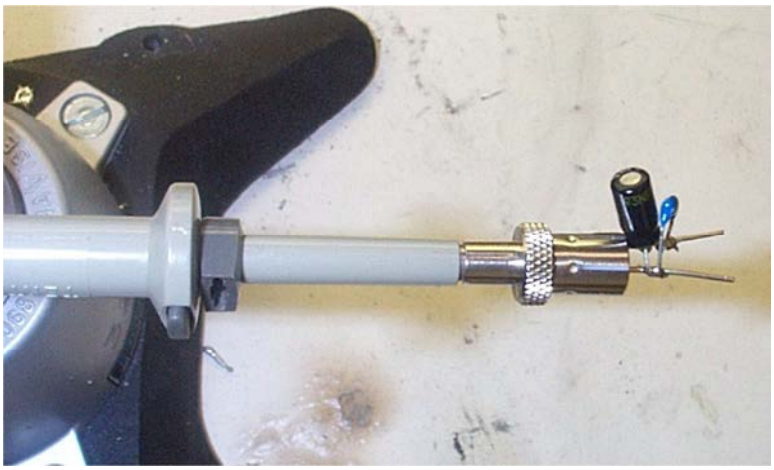


Figure 11 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.1.1 Output Ripple Voltage Test Data

Input Voltage (V)	Line Frequency (Hz)	Ripple Voltage (V_{P-P})		
		100% Load	50% Load	25% Load
90	60	64	96	93
115	60	66	107	98
230	50	68	132	124
265	50	88	150	129
277	60	84	155	130
300	60	92	161	134

10.1.2 Output Ripple Voltage Waveform at Full Load

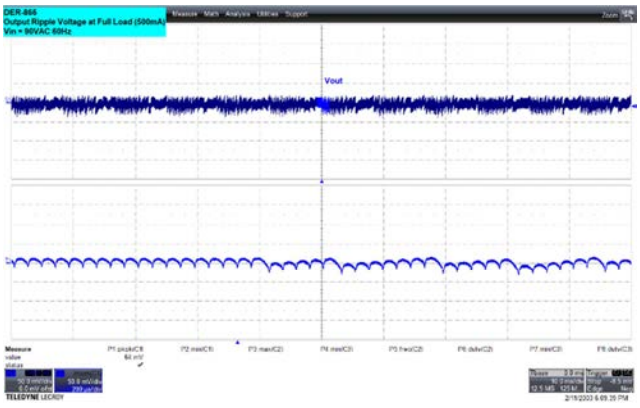


Figure 12 – 90 VAC 60 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 64 mV.

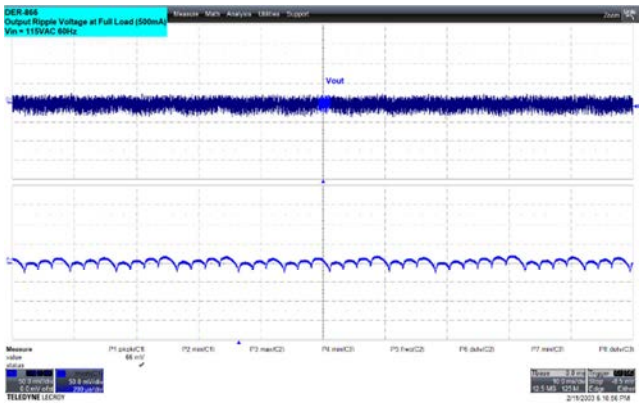


Figure 13 – 115 VAC 60 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 66 mV.

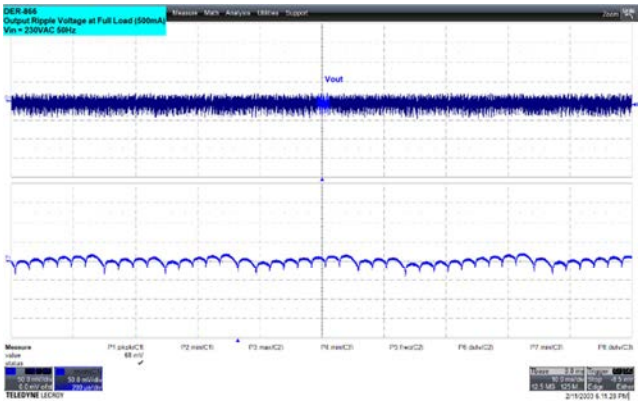


Figure 14 – 230 VAC 50 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 68 mV.

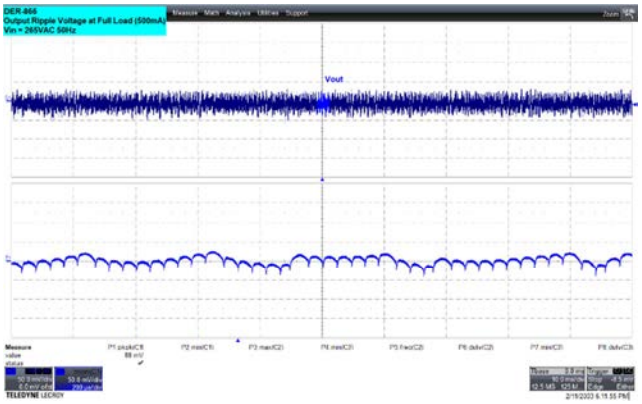


Figure 15 – 265 VAC 50 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 88 mV.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

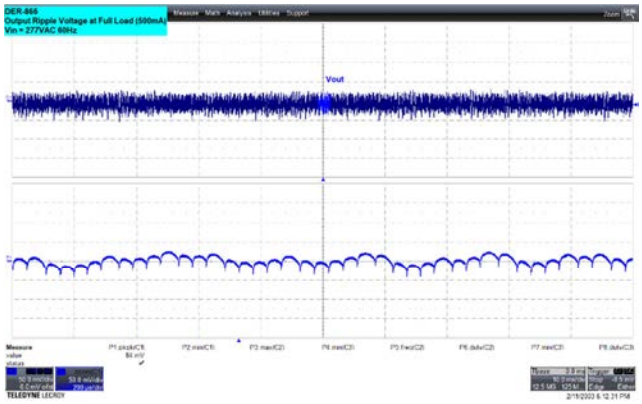


Figure 16 – 277 VAC 60 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 84 mV.

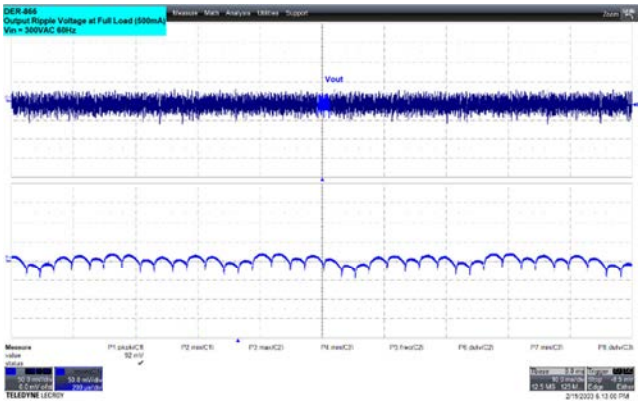


Figure 17 – 265 VAC 50 Hz.
Condition: 5 V, 500 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 92 mV.

10.1.3 Output Ripple Voltage Waveform at 50% Load

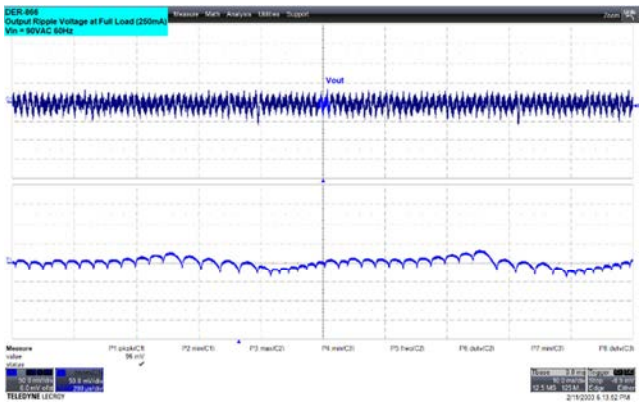


Figure 18 – 90 VAC 60 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 96 mV.

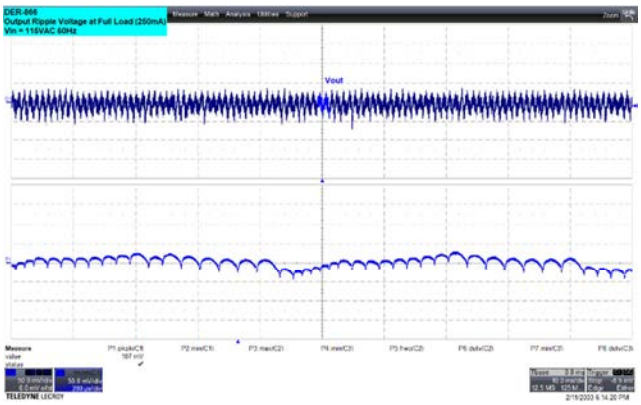


Figure 19 – 115 VAC 60 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 107 mV.

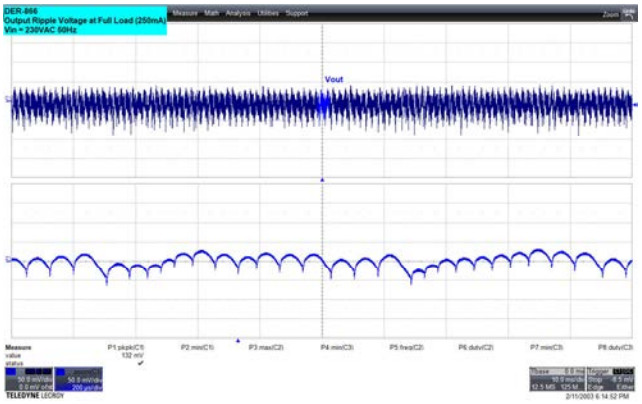


Figure 20 – 230 VAC 50 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 132 mV.

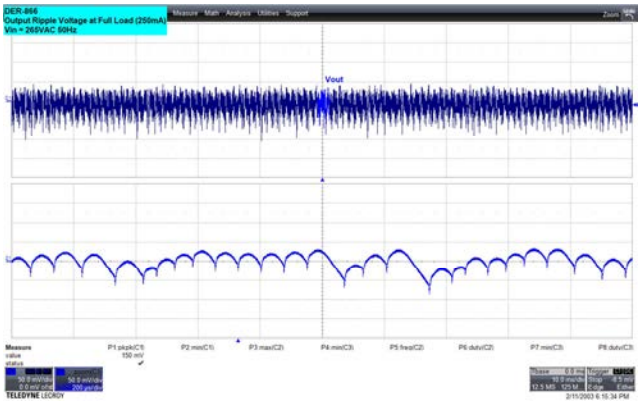


Figure 21 – 265 VAC 50 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 150 mV.

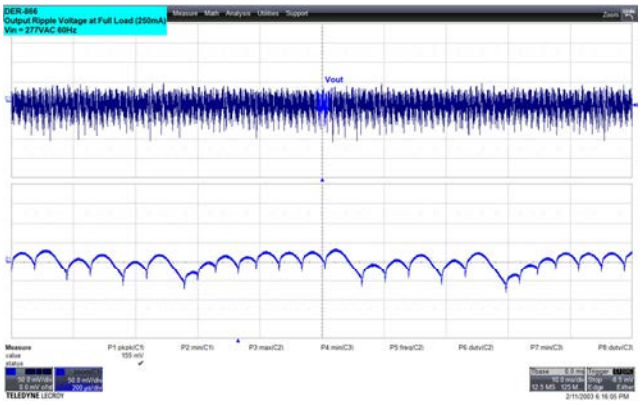


Figure 22 – 277 VAC 60 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 155 mV.

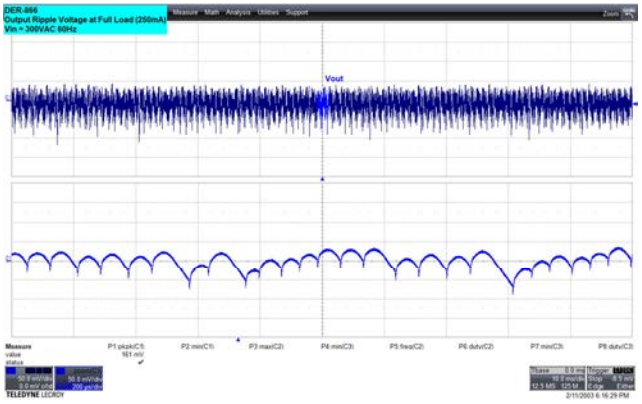


Figure 23 – 300 VAC 60 Hz.
Condition: 5 V, 250 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 161 mV.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

10.1.4 Output Ripple Voltage Waveform at 25% Load

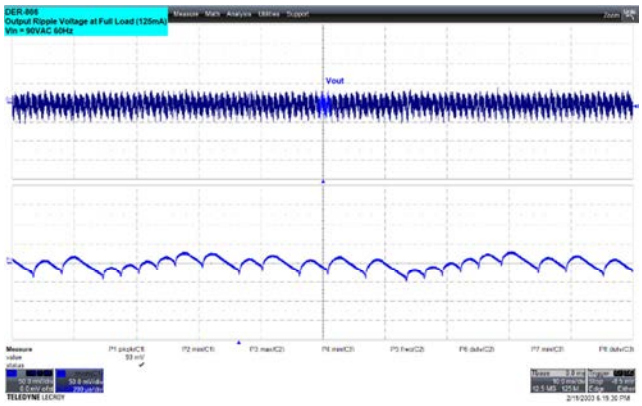


Figure 24 – 90 VAC 60 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 93 mV.

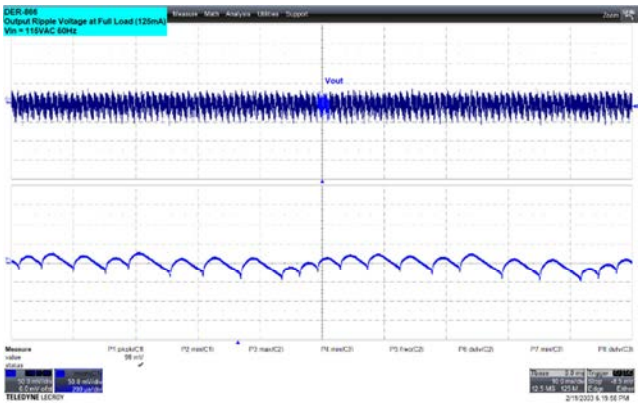


Figure 25 – 115 VAC 60 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 98 mV.

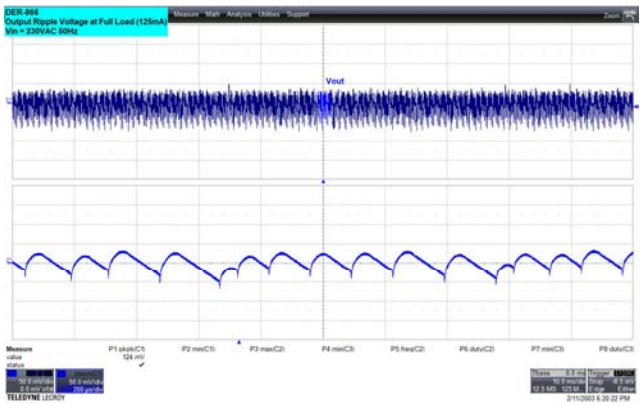


Figure 26 – 230 VAC 50 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 124 mV.

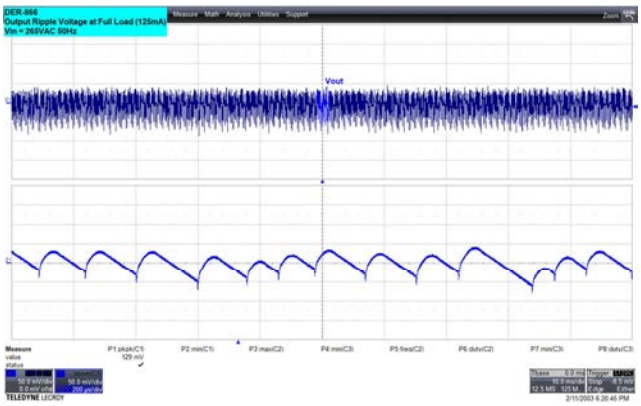


Figure 27 – 265 VAC 50 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 129 mV.

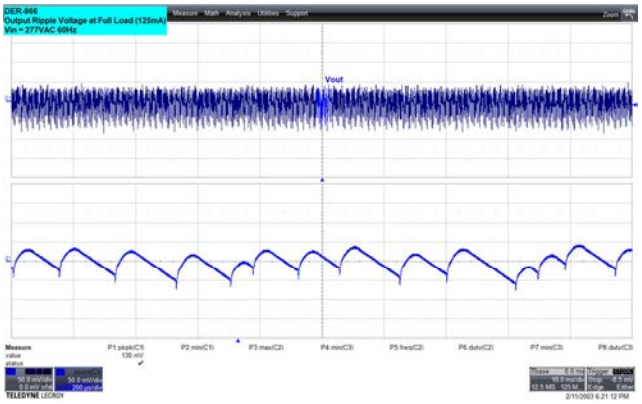


Figure 28 – 277 VAC 60 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 130 mV.

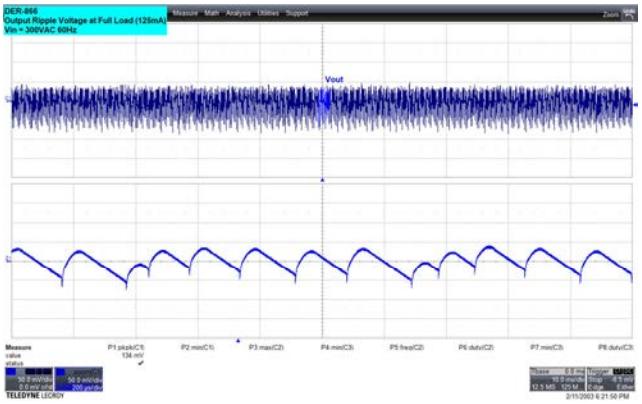


Figure 29 – 300 VAC 60 Hz.
Condition: 5 V, 125 mA.
V_{RIPPLE}, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{RIPPLE(PK-PK)}$: 134 mV.

10.2 ***Start-up Profile***

Tested using an E-load set at CC mode.

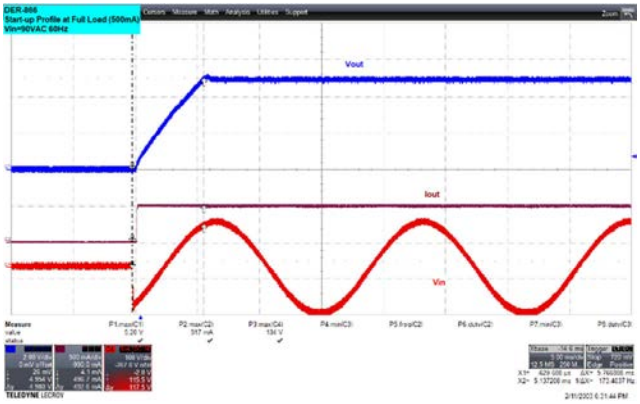


Figure 30 – 90 VAC 60 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 100 V / div.
Rise Time: 5.8 ms.

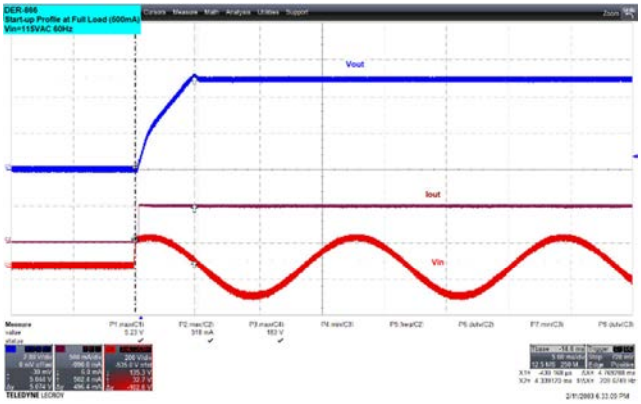


Figure 31 – 115 VAC 60 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 200 V / div.
Rise Time: 4.8 ms.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

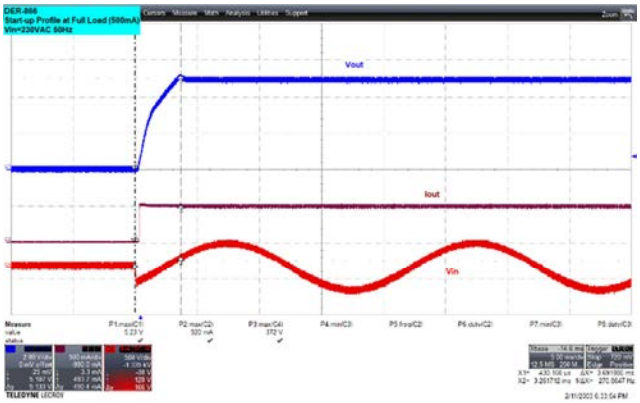


Figure 32 – 230 VAC 50 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 500 V / div.
Rise Time: 3.7 ms.

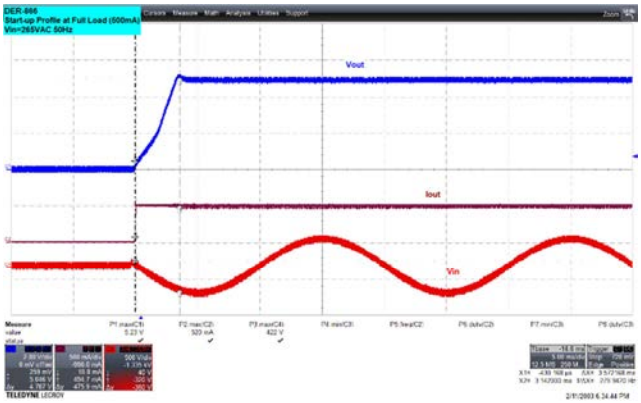


Figure 33 – 265 VAC 50 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 500 V / div.
Rise Time: 3.6 ms.

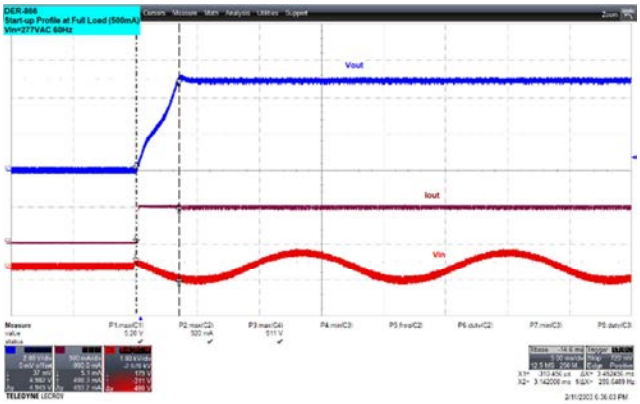


Figure 34 – 277 VAC 60 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 1 kV / div.
Rise Time: 5.8 ms.

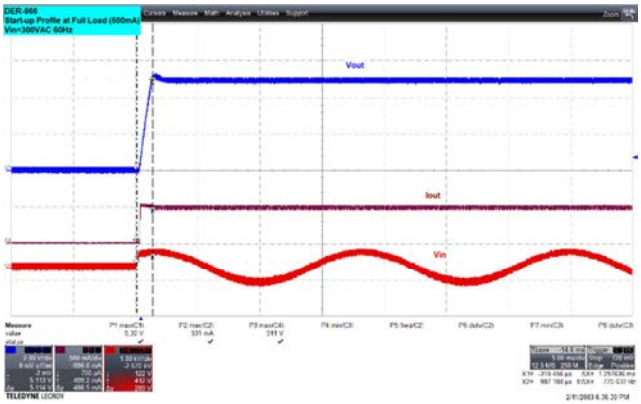


Figure 35 – 300 VAC 60 Hz, 500 mA Load.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Middle: I_{OUT}, 500 mA / div.
Lower: V_{OUT}, 1 kV / div.
Rise Time: 4.8 ms.

10.3 *Drain Voltage and Current Waveforms at Normal Operation*

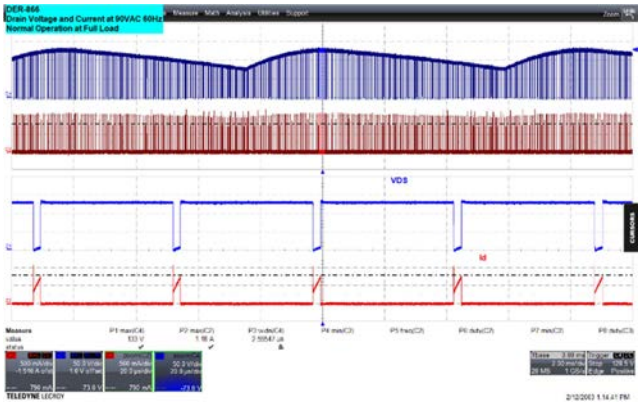


Figure 36 – 90 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 50 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 133 V.
$I_{DS(MAX)}$: 1.18 A.

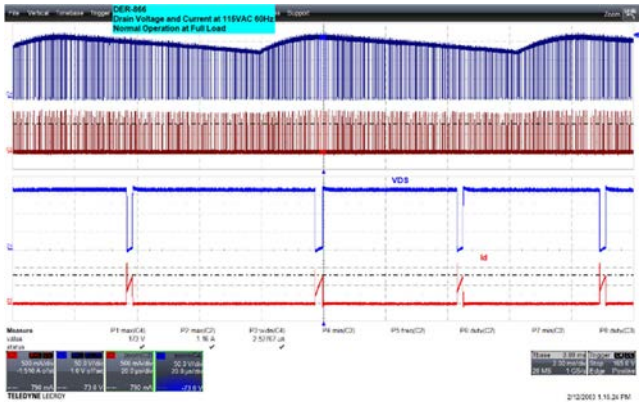


Figure 37 – 115 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 50 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 173 V.
$I_{DS(MAX)}$: 1.16 A.

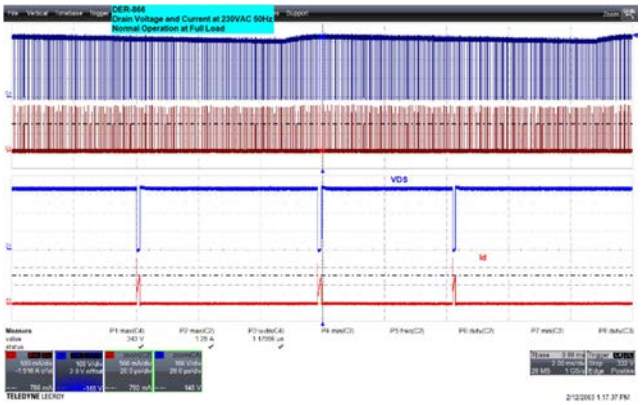


Figure 38 – 230 VAC 50 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 343 V.
$I_{DS(MAX)}$: 1.29 A.

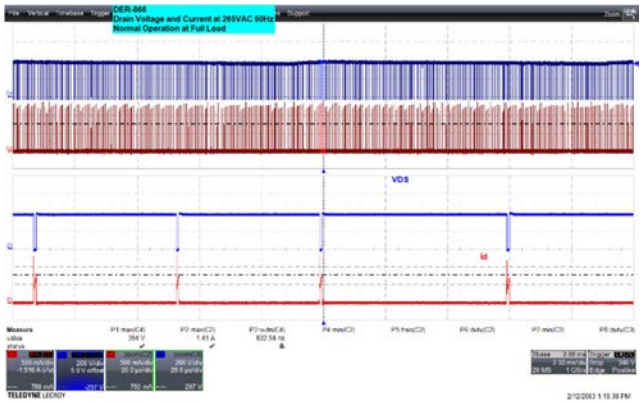


Figure 39 – 265 VAC 50 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 394 V.
$I_{DS(MAX)}$: 1.41 A.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

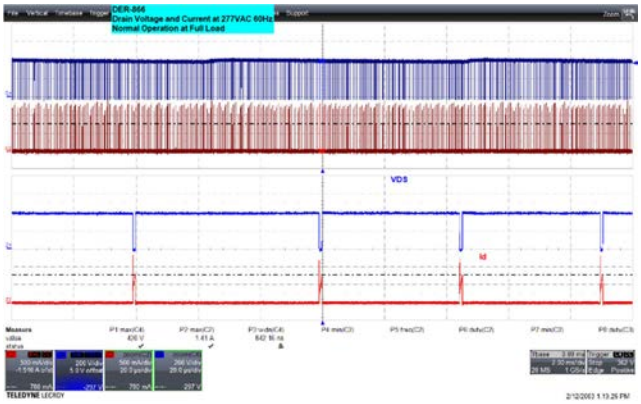


Figure 40 – 277 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 200 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 420 V.
$I_{DS(MAX)}$: 1.41 A.

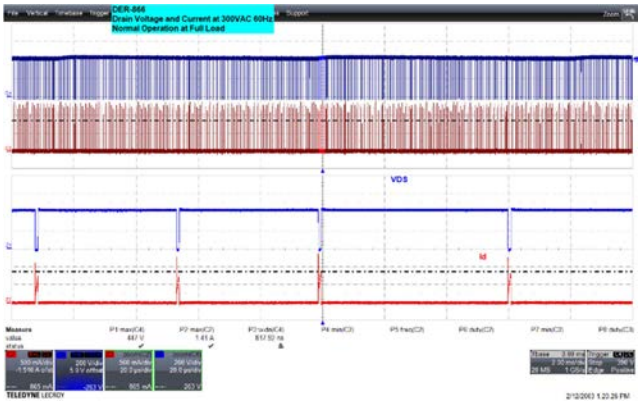


Figure 41 – 300 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: V_{DS}, 200 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(MAX)}$: 447 V.
$I_{DS(MAX)}$: 1.41 A.

10.4 *Drain Voltage and Current Waveforms at Start-up Operation*

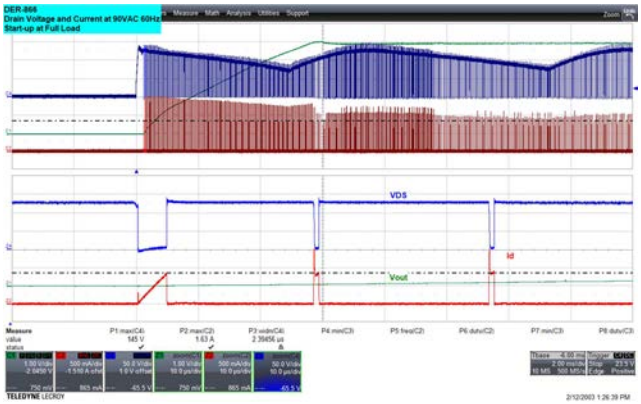


Figure 42 – 90 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 50 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 145 V.
$I_{DS(MAX)}$: 1.62 A.

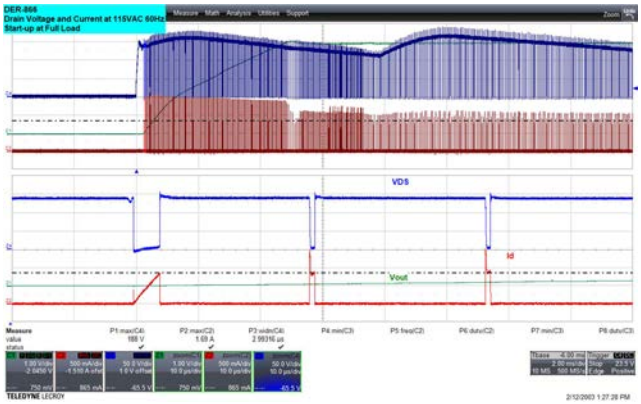


Figure 43 – 115 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 50 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 188 V.
$I_{DS(MAX)}$: 1.69 A.

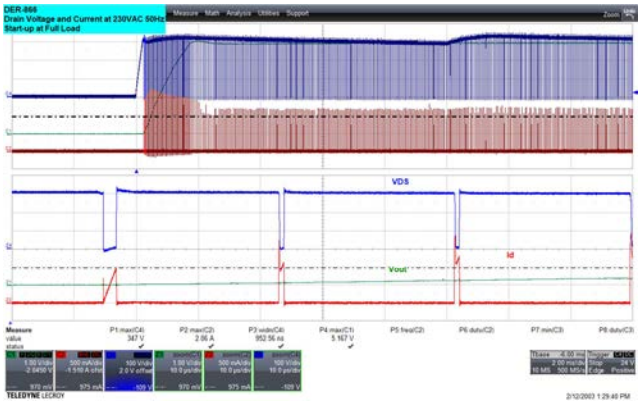


Figure 44 – 230 VAC 50 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 347 V.
$I_{DS(MAX)}$: 2.06 A.

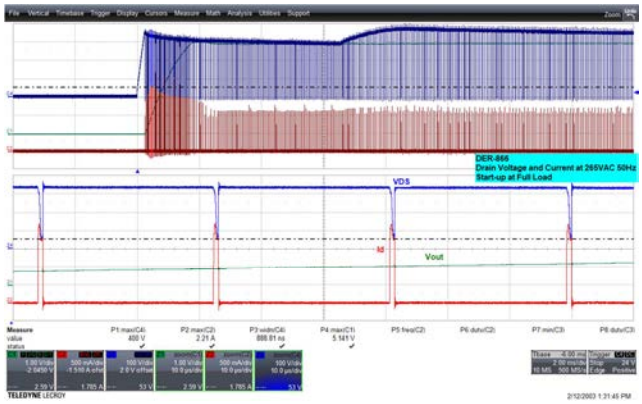


Figure 45 – 265 VAC 50 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 400 V.
$I_{DS(MAX)}$: 2.21 A.

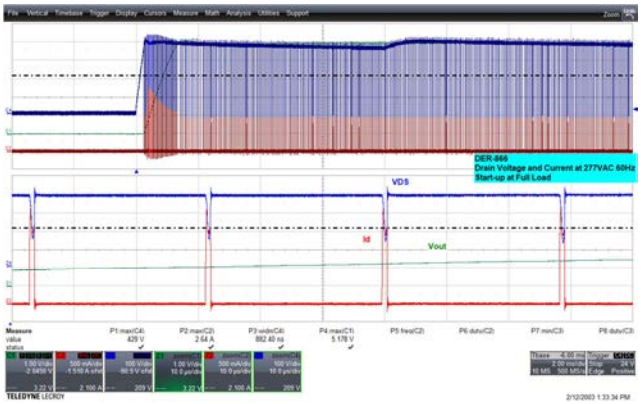


Figure 46 – 277 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 429 V.
$I_{DS(MAX)}$: 2.64 A.

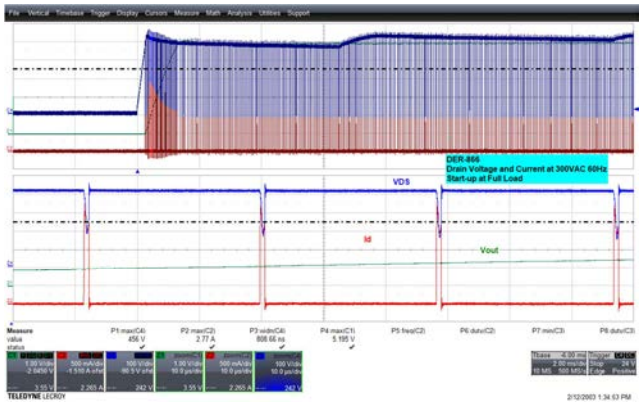


Figure 47 – 300 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_{DS}, 100 V / div., 2 ms / div.
Lower: I_{DS}, 500 mA / div.
Zoom in: 10 µs / div.
$V_{DS(MAX)}$: 456 V.
$I_{DS(MAX)}$: 2.77 A.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

10.5 *Freewheeling Diode Voltage and Current Waveform at Normal Operation*

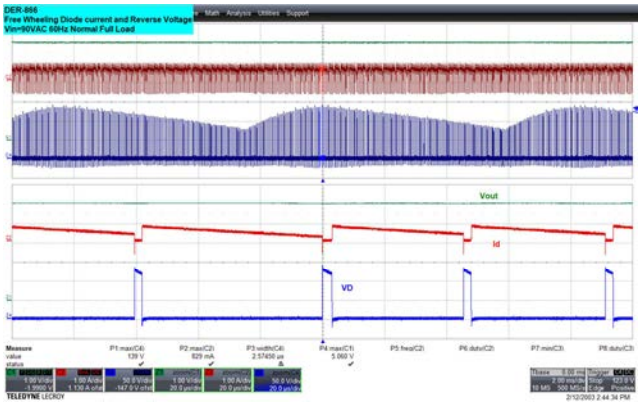


Figure 48 – 90 VAC 60 Hz, 500 mA.
Normal at Full Load.
Upper: V_D, 50 V / div., 2 ms / div.
Lower: I_D, 1 A / div.
Zoom in: 20 µs / div.
$V_{D(MAX)}$: 139 V.
$I_{D(MAX)}$: 0.829 A.

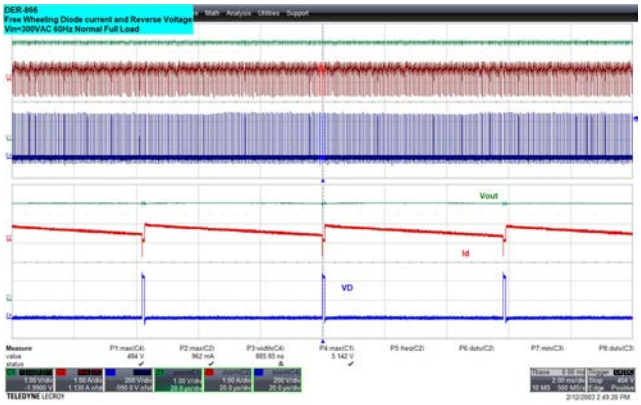


Figure 49 – 300 VAC 60 Hz, 500 mA.
Normal at Full Load.
Upper: V_D, 200 V / div., 2 ms / div.
Lower: I_D, 1 A / div.
Zoom in: 20 µs / div.
$V_{D(MAX)}$: 484 V.
$I_{D(MAX)}$: 0.962 A.

10.6 *Freewheeling Diode Voltage and Current Waveform at Start-up Operation*

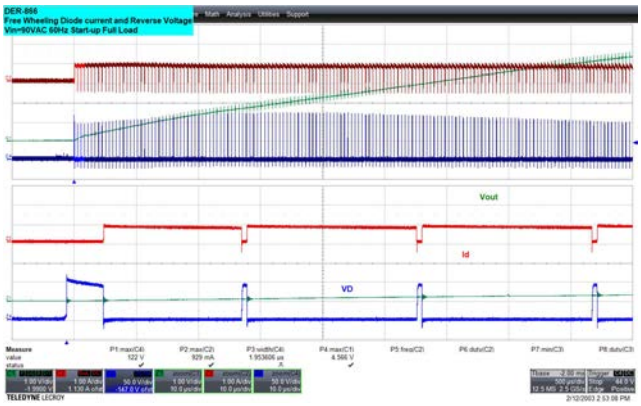


Figure 50 – 90 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_D, 50 V / div., 500 µs / div.
Lower: I_D, 1 A / div.
Zoom in: 20 µs / div.
$V_{D(MAX)}$: 122 V.
$I_{D(MAX)}$: 0.929 A.

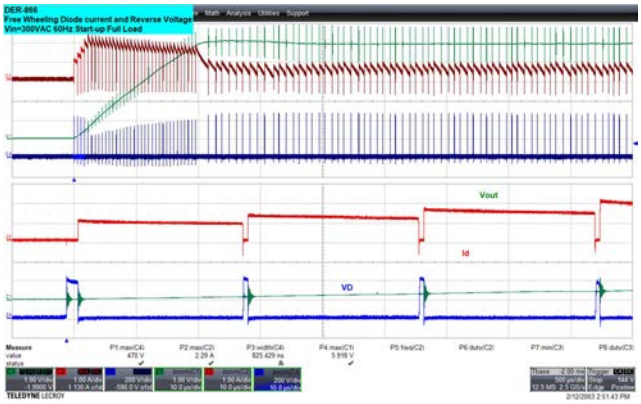


Figure 51 – 115 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: V_D, 200 V / div., 500 µs / div.
Lower: I_D, 1 A / div.
Zoom in: 10 µs / div.
$V_{D(MAX)}$: 470 V.
$I_{D(MAX)}$: 2.29 A.

10.7 ***Dynamic Load Response***

Tested using an e-load set at 50 Hz, 50 % duty cycle and slew rate of 0.08 mA/s.

Voltage Overshoot and Undershoot During Dynamic Loading

10-100%, 50 Hz Dynamic Load Response						
V_{OUT}	**Voltage Overshoot / Undershoot (V)**					
	90 VAC 60 Hz	**115VAC 60 Hz**	**230 VAC 50 Hz**	**265 VAC 50 Hz**	**277 VAC 60 Hz**	**300 VAC 60 Hz**
$V_{OUT(MAX)}$	5.4	5.4	5.4	5.4	5.4	5.4
$V_{OUT(MIN)}$	4.95	4.84	4.81	4.77	4.68	4.8
50-100%, 50 Hz Dynamic Load Response						
V_{OUT}	**Voltage Overshoot / Undershoot (V)**					
	90 VAC 60 Hz	**115 VAC 60 Hz**	**230 VAC 50 Hz**	**265 VAC 50 Hz**	**277 VAC 60 Hz**	**300 VAC 60 Hz**
$V_{OUT(MAX)}$	5.26	5.26	5.25	5.25	5.25	5.25
$V_{OUT(MIN)}$	4.87	4.86	4.82	4.84	4.84	4.82

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

10.7.1 10-100% 50 Hz Dynamic Load

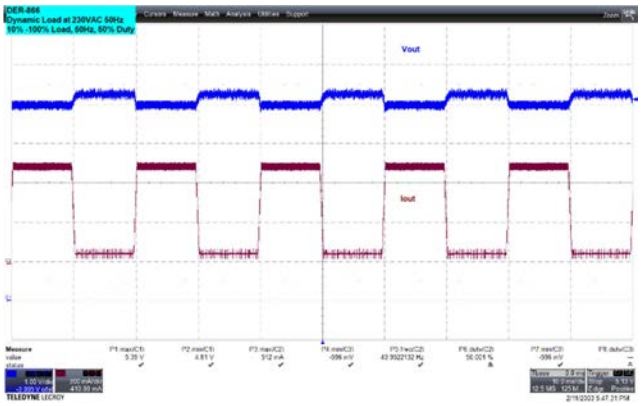


Figure 52 – 90 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.81 V.

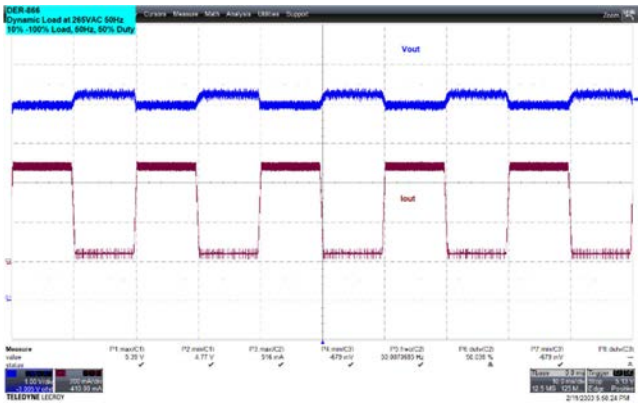


Figure 53 – 115 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.77 V.

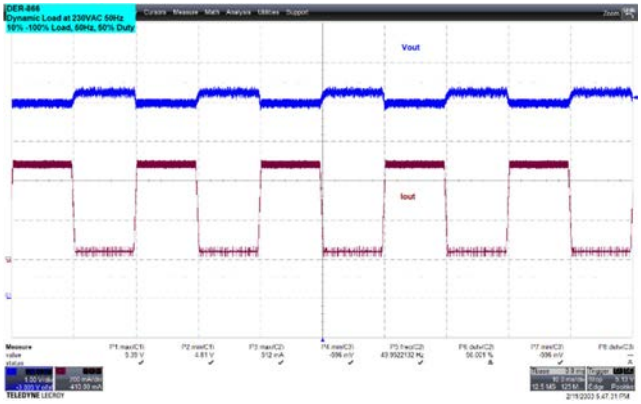


Figure 54 – 230 VAC 50 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.81 V.

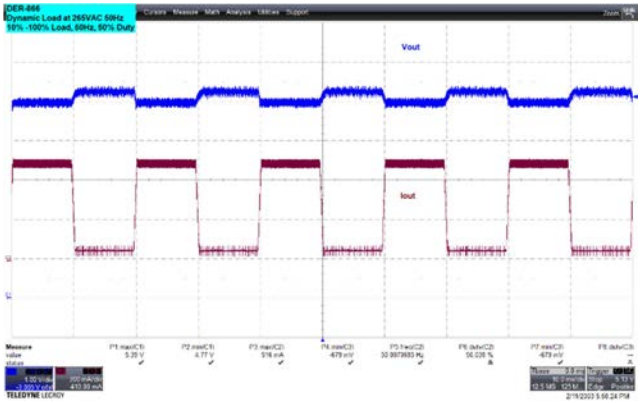


Figure 55 – 265 VAC 50 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.77 V.

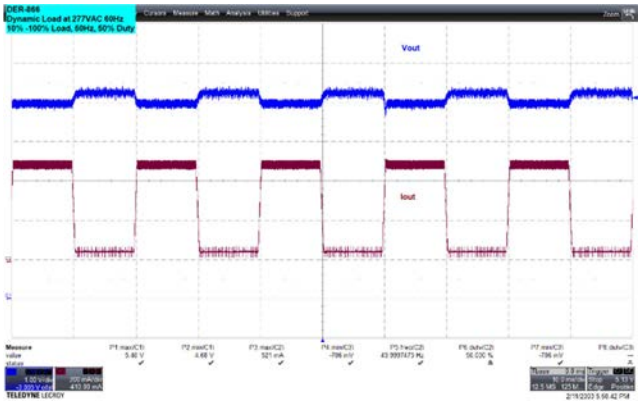


Figure 56 – 277 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.4 V.
$V_{OUT(MIN)}$: 4.68 V.

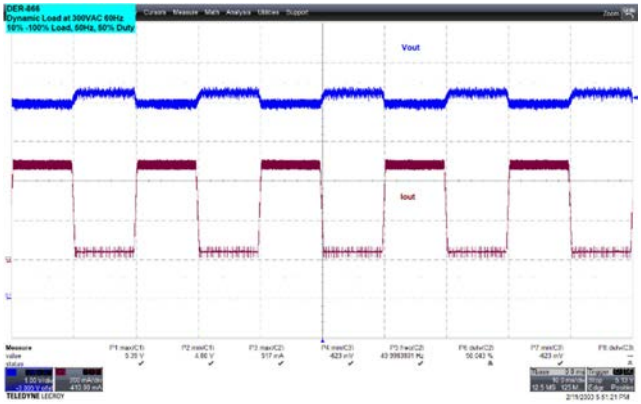


Figure 57 – 300 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.8 V.

10.7.2 50-100% 50 Hz Dynamic Load

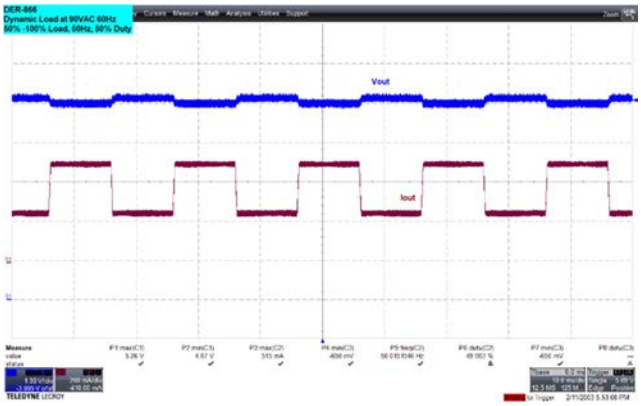


Figure 58 – 90 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.26 V.
$V_{OUT(MIN)}$: 4.87 V.

Figure 59 – 115 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.26 V.
$V_{OUT(MIN)}$: 4.86 V.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

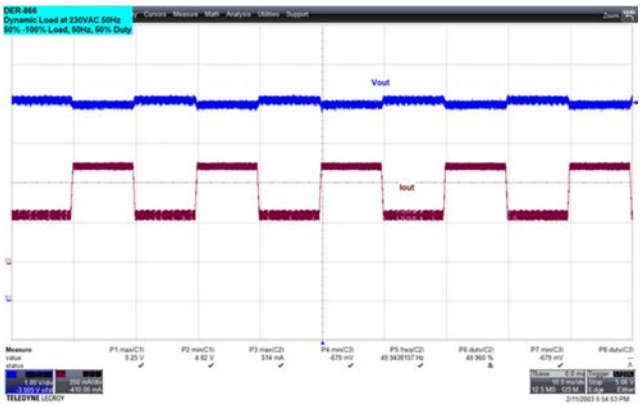


Figure 60 – 230 VAC 50 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.82 V.

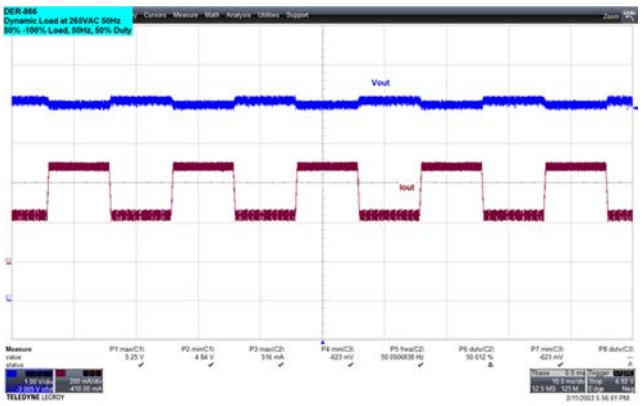


Figure 61 – 265 VAC 50 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.84 V.

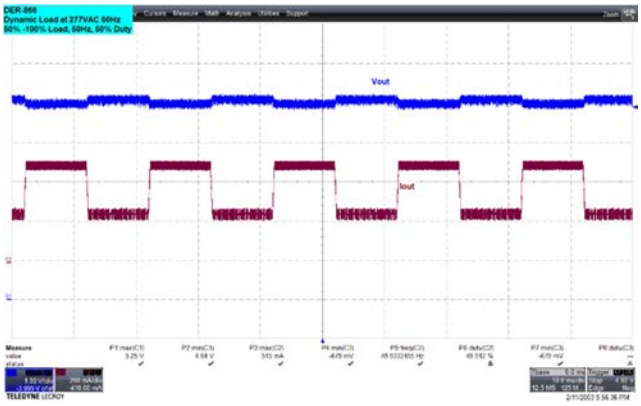


Figure 62 – 277 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.84 V.

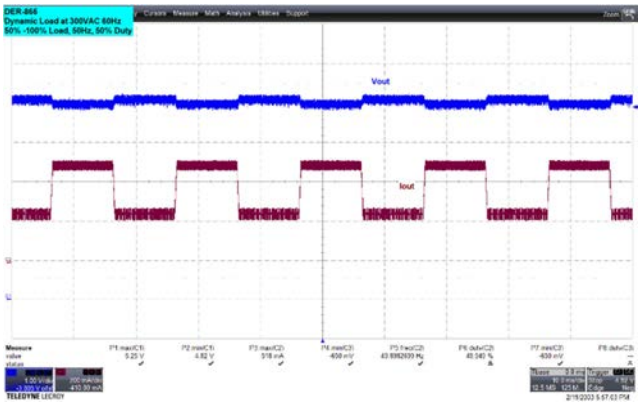


Figure 63 – 300 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: V_{OUT}, 1 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.82 V.

10.8 *Output Short-Circuit Protection*

Short the main output (5 V) and monitor I_{DS}, output voltage, and output current. The first time fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

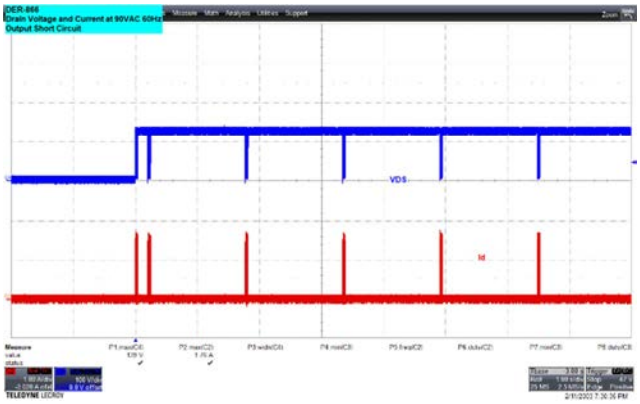


Figure 64 – 90 VAC 60 Hz, Output Short.
Upper: V_{DS}, 100 V / div.
Middle: I_{DS}, 1 A / div., 1 s / div.
$V_{DS(MAX)}$: 139 V.
$I_{DS(MAX)}$: 1.75 A.

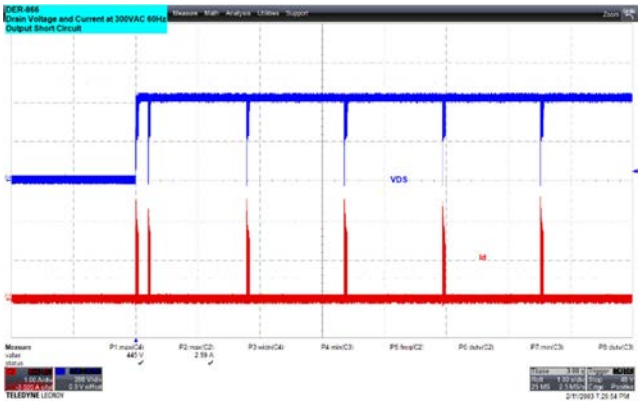


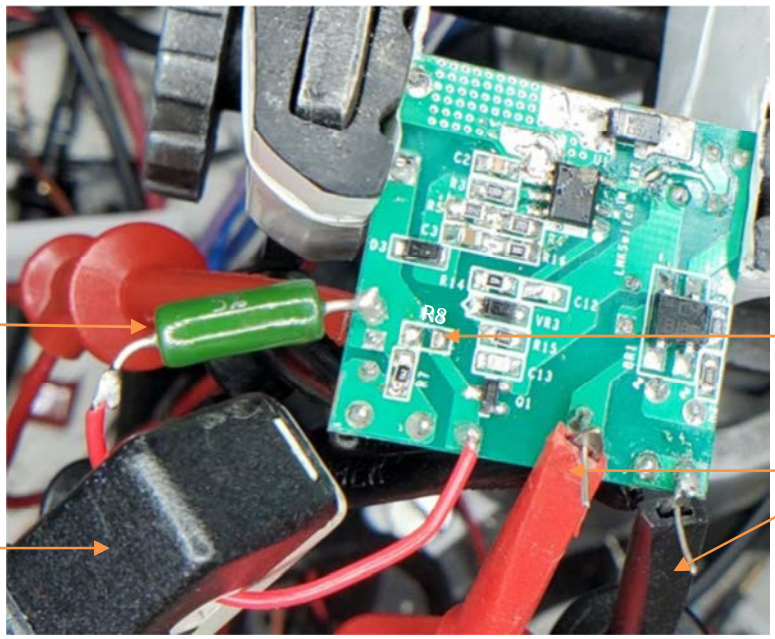
Figure 65 – 300 VAC 60 Hz, Output Short.
Upper: V_{DS}, 200 V / div.
Middle: I_{DS}, 1 A / div., 1 s / div.
$V_{DS(MAX)}$: 445 V.
$I_{DS(MAX)}$: 2.59 A.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

10.9 *Zero Crossing Detection Measurement*

The ZCD signal is sensitive to common mode noise introduced by voltage probes or other sources. Following are specific guidelines in probing and measuring the ZCD signal without compromising its signal integrity.

10.9.1 Current Measurement Set-up (Recommended Set-up)



R8 – use 100Ω axial resistor to mount the current probe easily

R8 – remove

Differential Voltage Probe- connected to AC input terminal

Current Probe – Must be place away from the IC or away from PCB

Figure 66 – ZCD Signal using Current Measurement Set-up.

For ZCD current measurement set-up, the following steps are recommended for bench testing procedure:

- Use 10 Ω fixed resistor load instead of an E-load.
- Remove SMD resistor R8 and replace with 100 Ω axial resistor using a small wire to mount the current probe easily. Lower the resistance value if needed to increase the resolution.
- Place current probe away from the IC or PCB as shown in above figure.
- Use differential voltage probe to monitor the input voltage. Using voltage probe could distort the ZCD signal due to ground connection.

10.9.1.1 ZCD Signal Waveforms Using Current Measurement

ZCD Waveforms gathered at full load (5 V 500 mA)

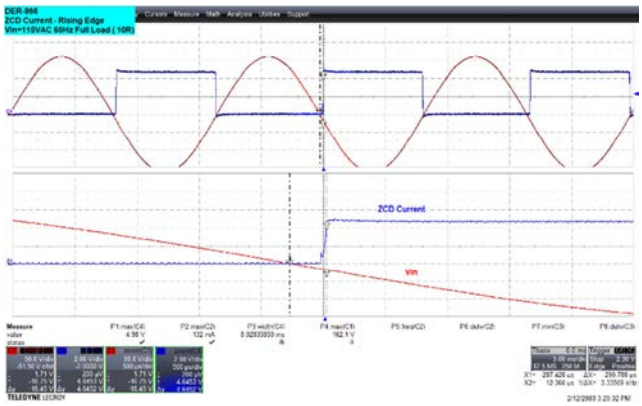


Figure 67 – 115 VAC 60 Hz.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 300 µs.

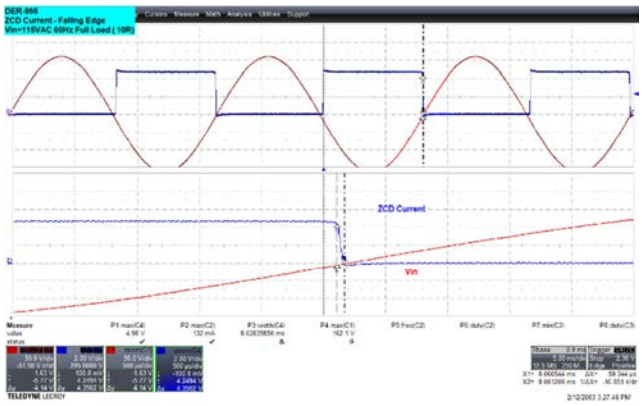


Figure 68 – 1115 VAC 60 Hz.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 100 µs.

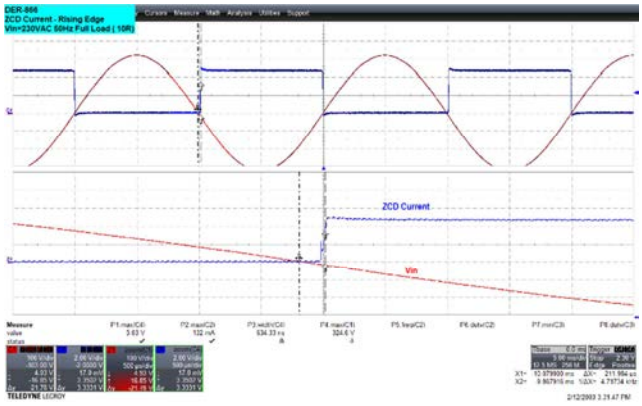


Figure 69 – 230 VAC 50 Hz.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 212 µs.

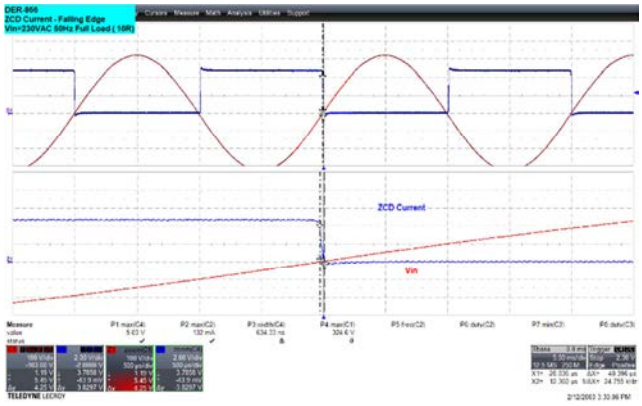


Figure 70 – 230 VAC 50 Hz.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 40.4 µs.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

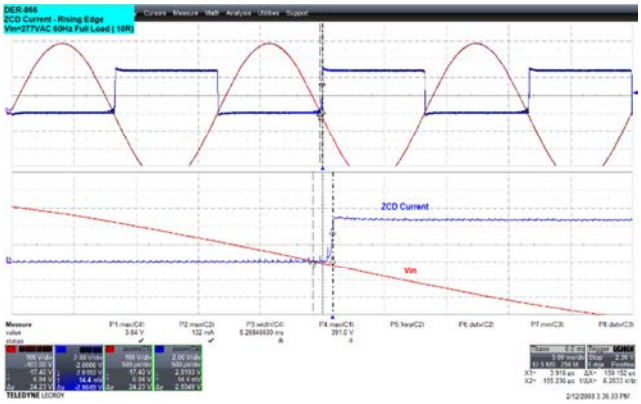


Figure 71 – 277 VAC Input.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 159.2 µs.

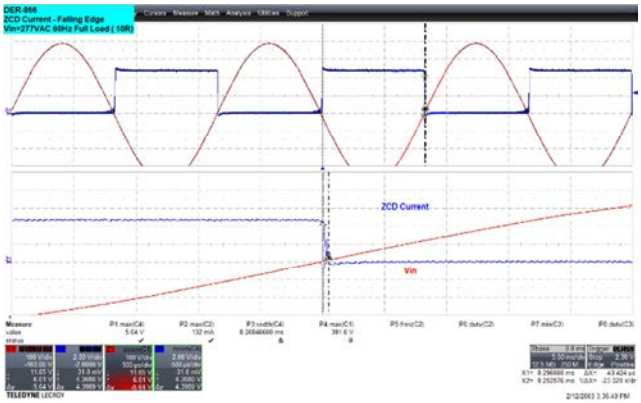


Figure 72 – 277 VAC Input.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 43.4 µs.

10.9.2 ZCD Voltage Measurement Set-up (Alternative Set-up)

Figure 73 – ZCD Voltage Measurement Set-up.

As an alternate set-up, the ZCD voltage can be measured using the following recommendations:

- Connect input directly to AC mains line – do not use an electronic AC source
- Make sure that the oscilloscope ground (earth) line is connected
- Use differential voltage probes
- Use fixed resistor load instead of using e-load

10.9.2.1 ZCD Voltage Waveforms

10.9.2.1.1 ZCD Waveforms Gathered at No-Load Condition

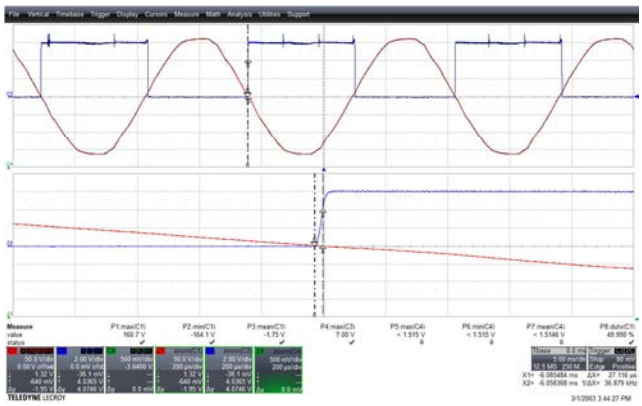


Figure 74 – 100 VAC Input, No-Load.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 27.16 µs.

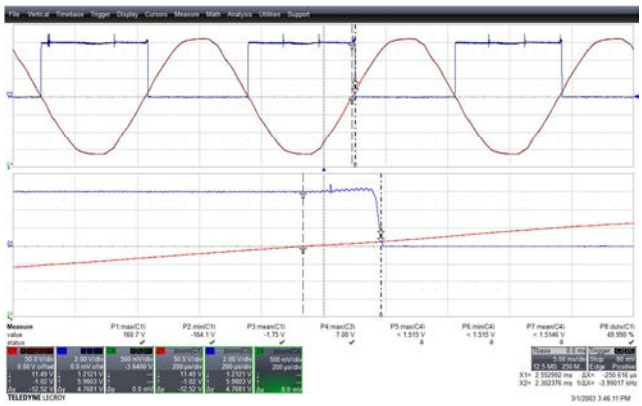


Figure 75 – 100 VAC Input, No-Load.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 251 µs.

10.9.2.1.2 ZCD Waveforms Gathered at Full Load (5 V 500 mA)

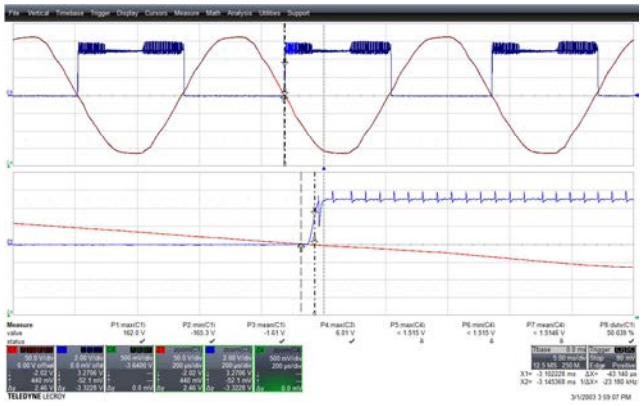


Figure 76 – 100 VAC Input, No-Load.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 23 µs.

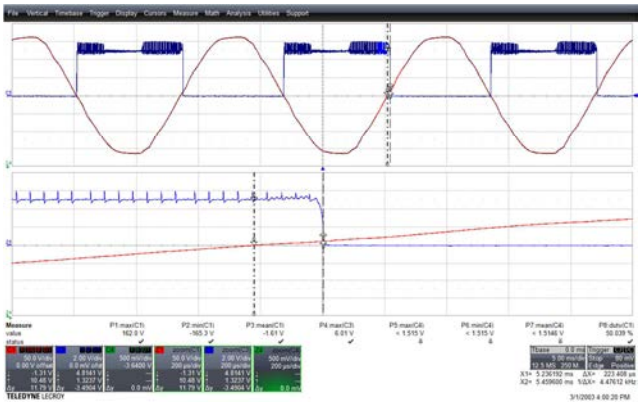


Figure 77 – 100 VAC Input, No-Load.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 223 µs.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

11 Thermal Performance at Room Temperature

Thermal measurement done at room temperature.

11.1 *Set-up*

Open frame unit in vertical position was placed inside the acrylic box to eliminate the effect of ambient air flow. FLIR camera was used to measure components case temperature.

Figure 78 – Thermal Test Set-up Picture.

11.2 *Thermal Test Data Based from IR Thermal Camera Scan*

Component	Temperature(°C)					
	90 V 60 Hz	**115 V 60 Hz**	**230 V 50 Hz**	**265 V 50 Hz**	**277 V 60 Hz**	**300 V 60 Hz**
U1 - LNK3307D	67.1	71.4	78.4	76.5	76	76.2
D2 - Freewheeling Diode	71.3	73.3	77.5	76.5	76.6	77.1
L4 - Buck Inductor	61.3	59.6	68.1	66.5	68.2	68.3

11.3 *Thermal Scan*

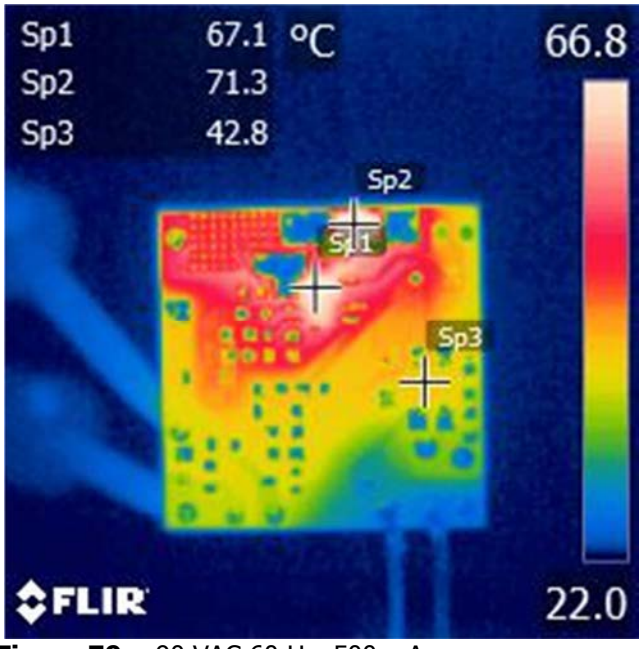


Figure 79 – 90 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 67.1 ºC.
SP2: D2 – 71.3 ºC.

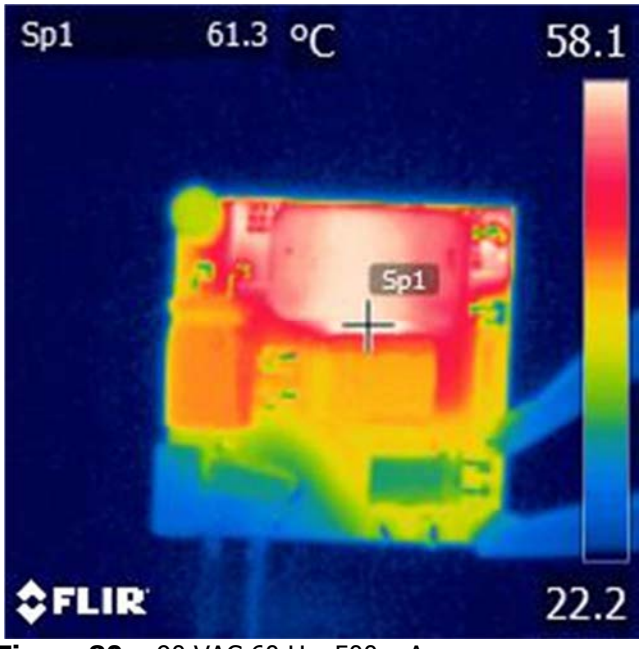


Figure 80 – 90 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 61.3 ºC.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

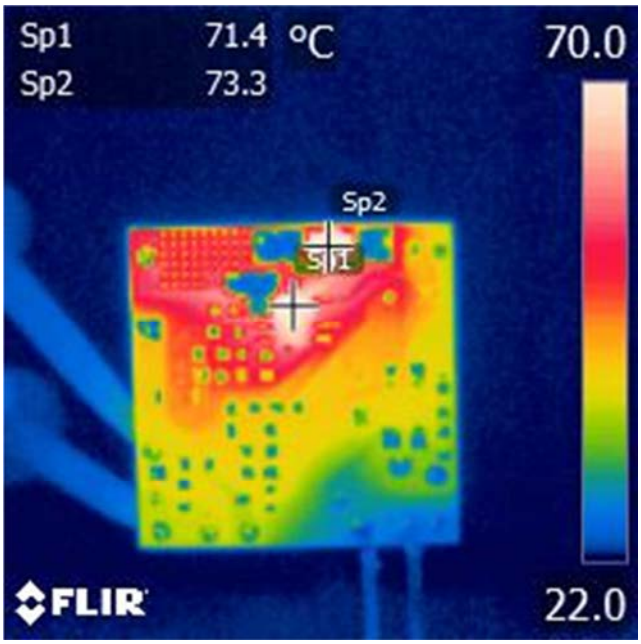


Figure 81 – 115 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 71.4 ºC.
SP2: D2 – 73.3 ºC.

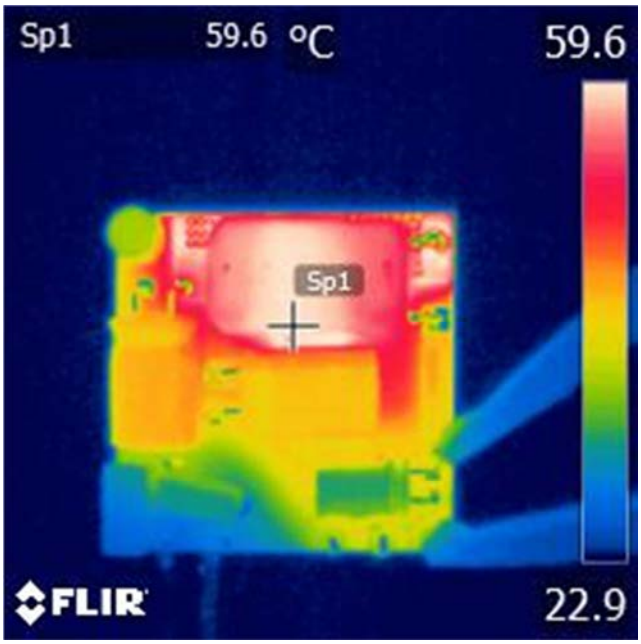


Figure 82 – 115 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 59.6 ºC.

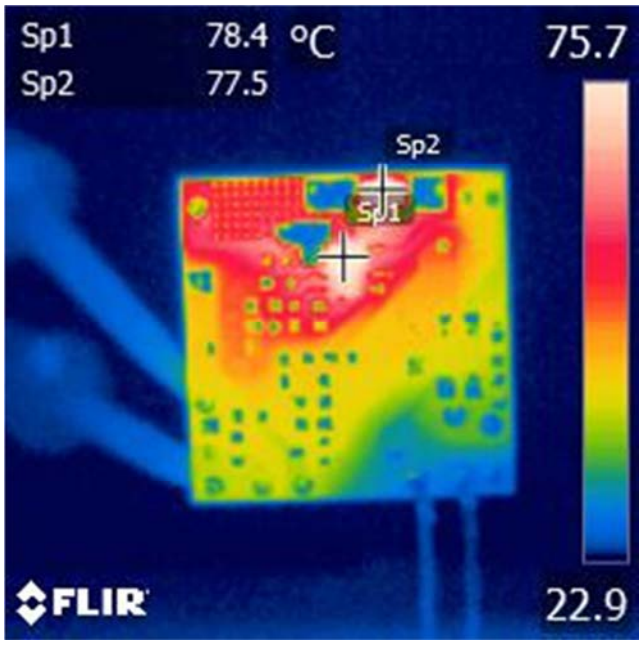


Figure 83 – 230 VAC 50 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 78.4 ºC.
SP2: D2 – 77.5 ºC.

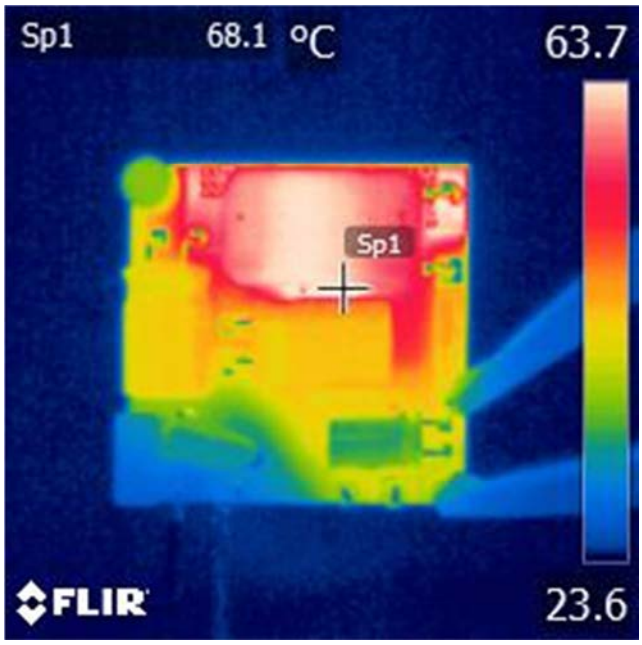


Figure 84 – 230 VAC 50 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.1 ºC.

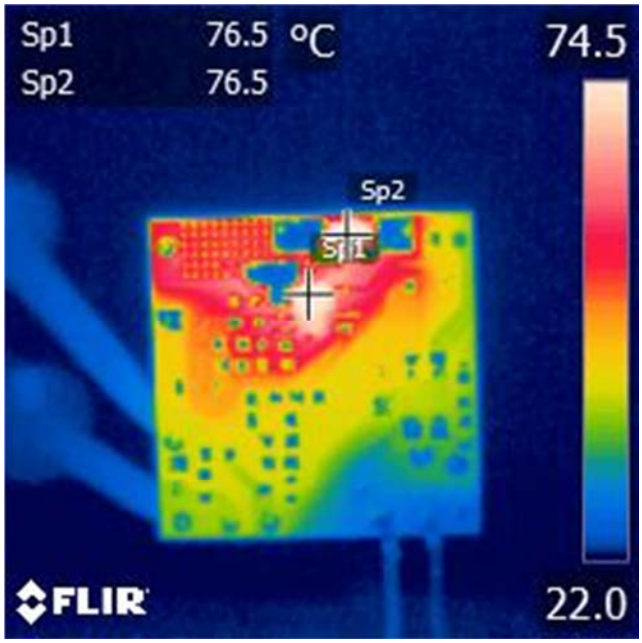


Figure 85 – 265 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76.5 ºC.
SP2: D2 – 76.5 ºC.

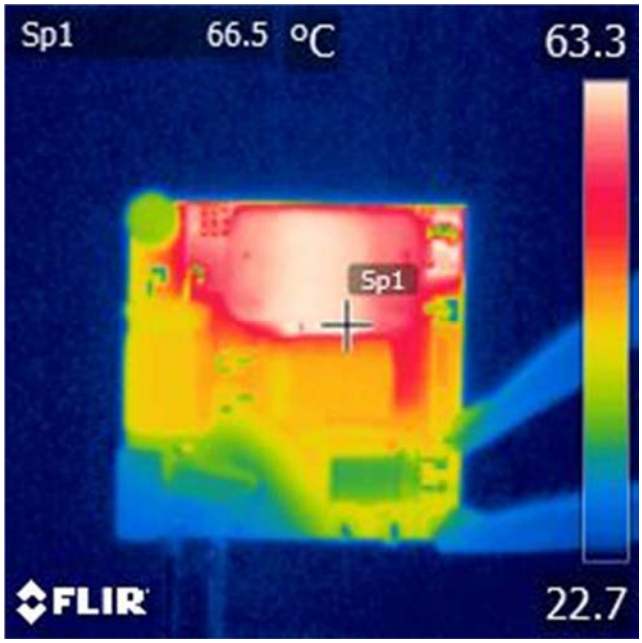


Figure 86 – 265 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 66.5 ºC.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

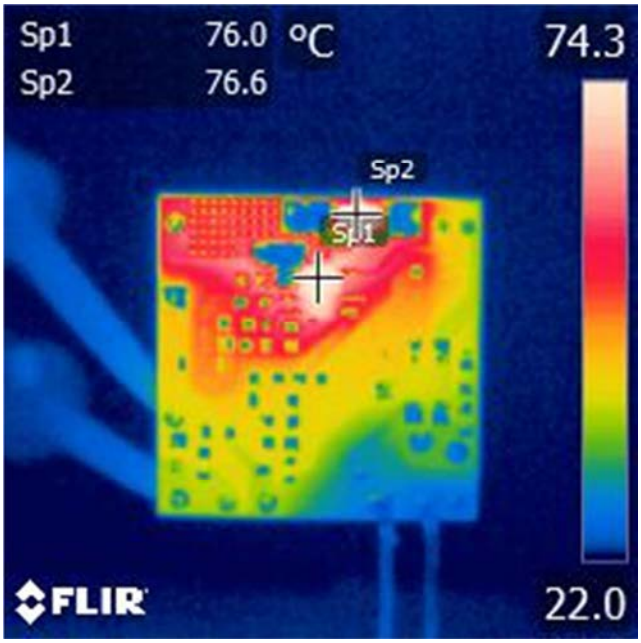


Figure 87 – 277 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76 ºC.
SP2: D2 – 76.6 ºC.

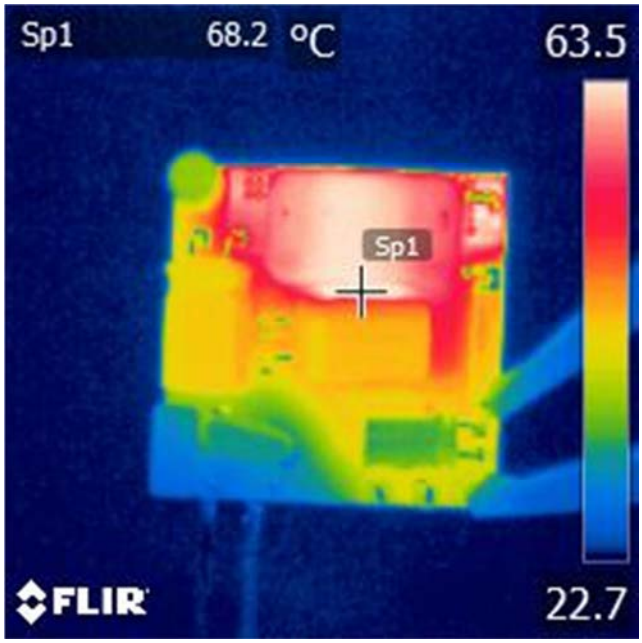


Figure 88 – 277 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.2 ºC.

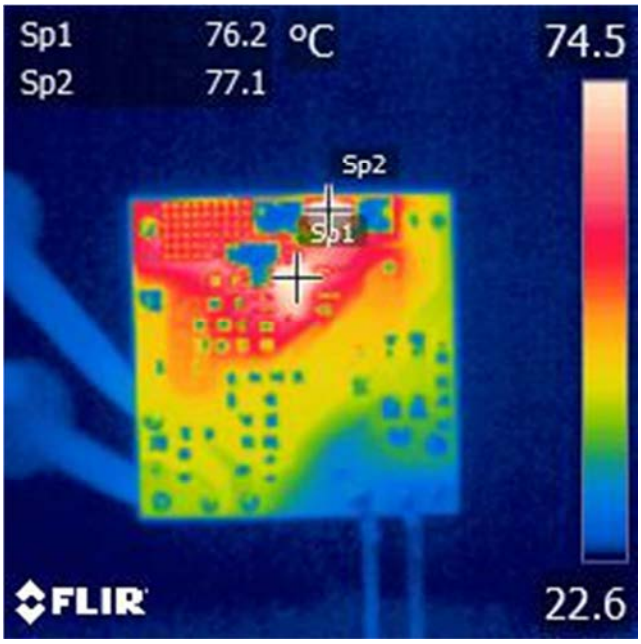


Figure 89 – 300 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76.2 ºC.
SP2: D2 – 77.1 ºC.

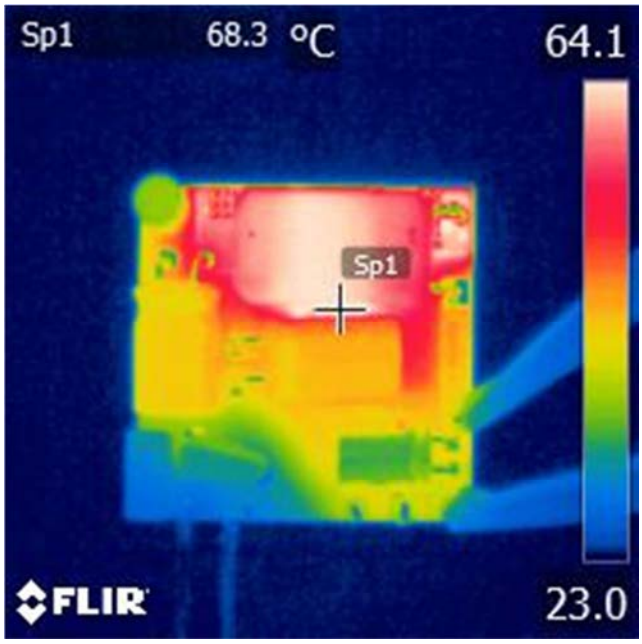


Figure 90 – 300 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.3 ºC.

12 Conducted EMI

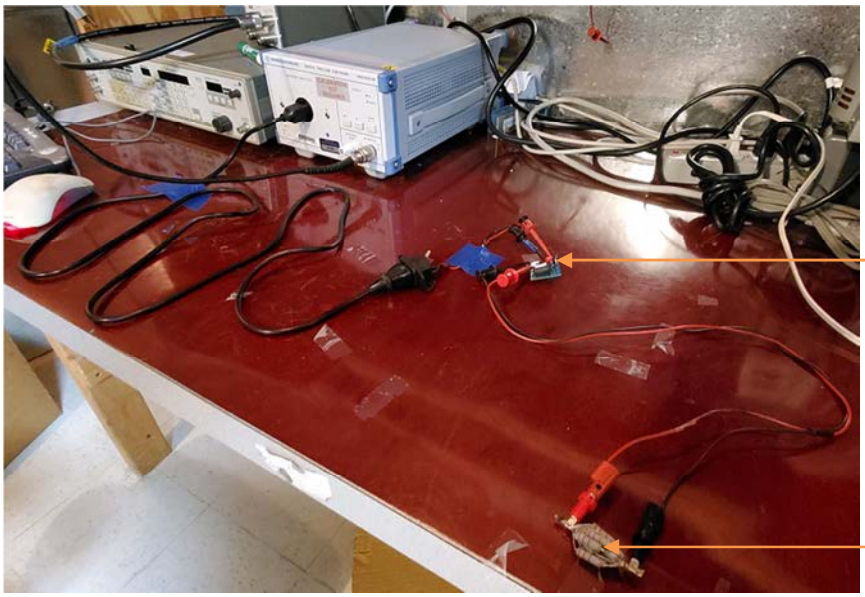


Figure 91 – Conducted EMI Set-up Picture.

12.1 *Test Set-up Equipment*

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. 10 Ω resistor load.
4. Variac input voltage source set at 115 VAC and 230 VAC.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

12.2 ***Conducted Emission Scan***

Unit passed conducted EMI EN55022 limit with >10 dB uV margin at low line and > 6 dBuV at high line.

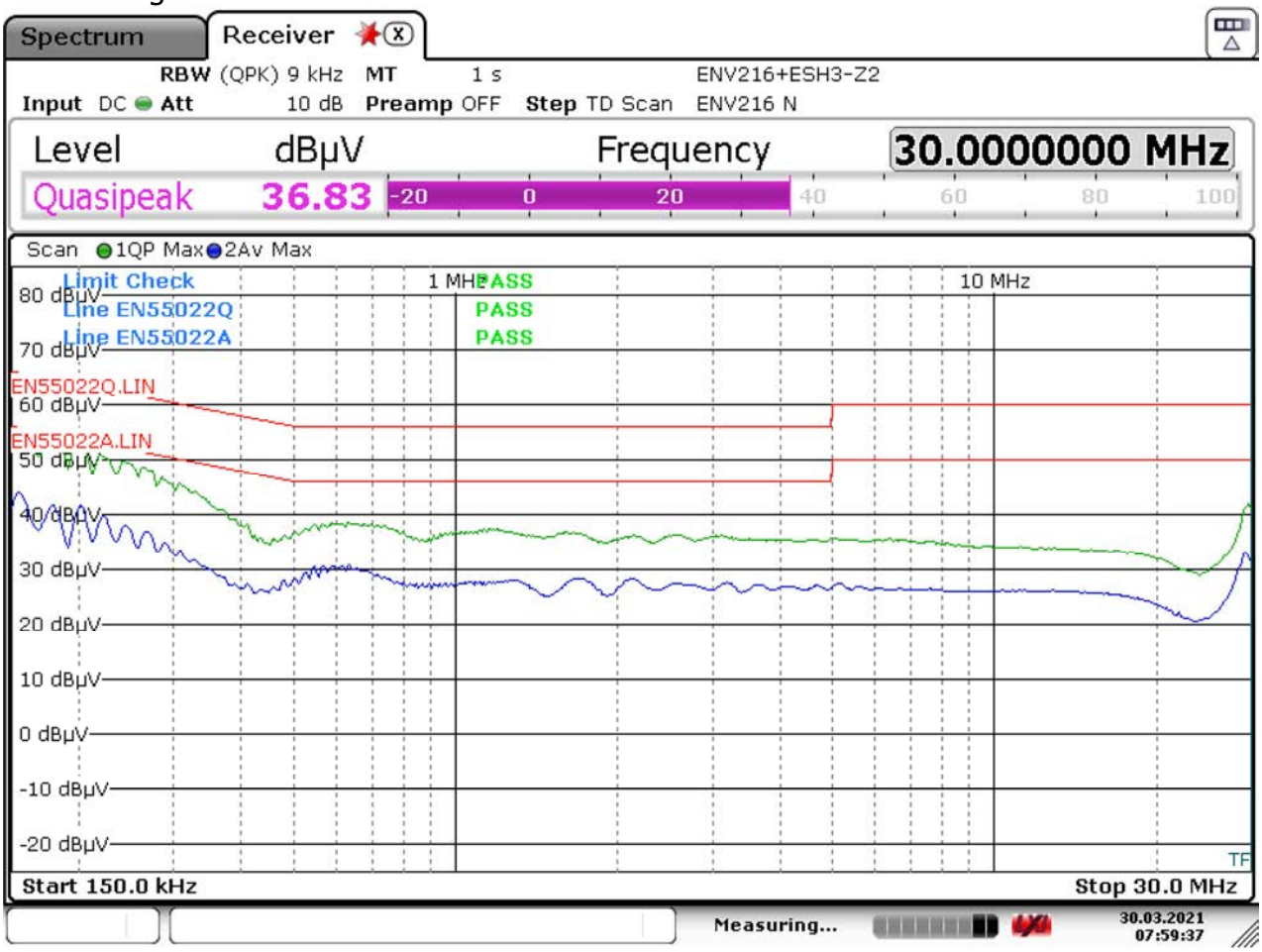


Figure 92 – Conducted EMI Scan at 115 VAC.

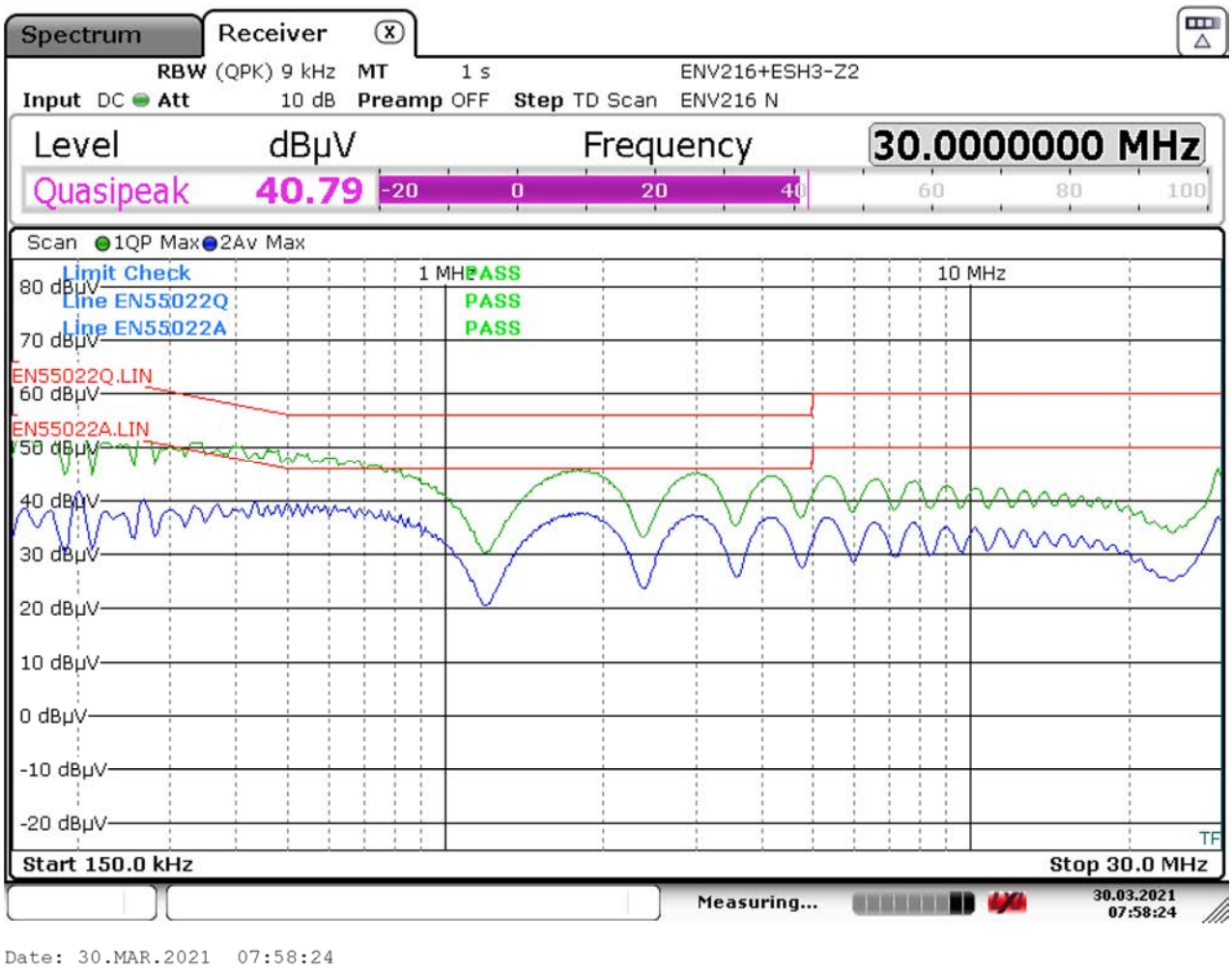


Figure 93 – Conducted EMI Scan at 230 VAC.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

13 Line Surge

13.1 *Combination Wave Surge*

The unit was subjected to ±1000 V, combination wave surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

13.2 *Ring Wave Surge*

The unit was subjected to ±2500 V, combination wave surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
+2500	230	L to N	180	Pass
-2500	230	L to N	180	Pass
+2500	230	L to N	270	Pass
-2500	230	L to N	270	Pass

14 Audible Noise

The LNK3307D IC has a built-in state machine to minimize audible noise at light load condition. The current limit is automatically reduced at light load condition to minimize power inductor vibration. To reduce audible noise further, an off-the-shelf dog-bone or barrel type inductor is recommended. Horizontal mounting helps minimize PCB vibration that may amplify audible noise. Adding hot melt type glue around the power inductor L2 helps reduce audible noise at light load condition but will slightly increase audible noise at full load.

14.1 *Audible Noise Test Set-up*

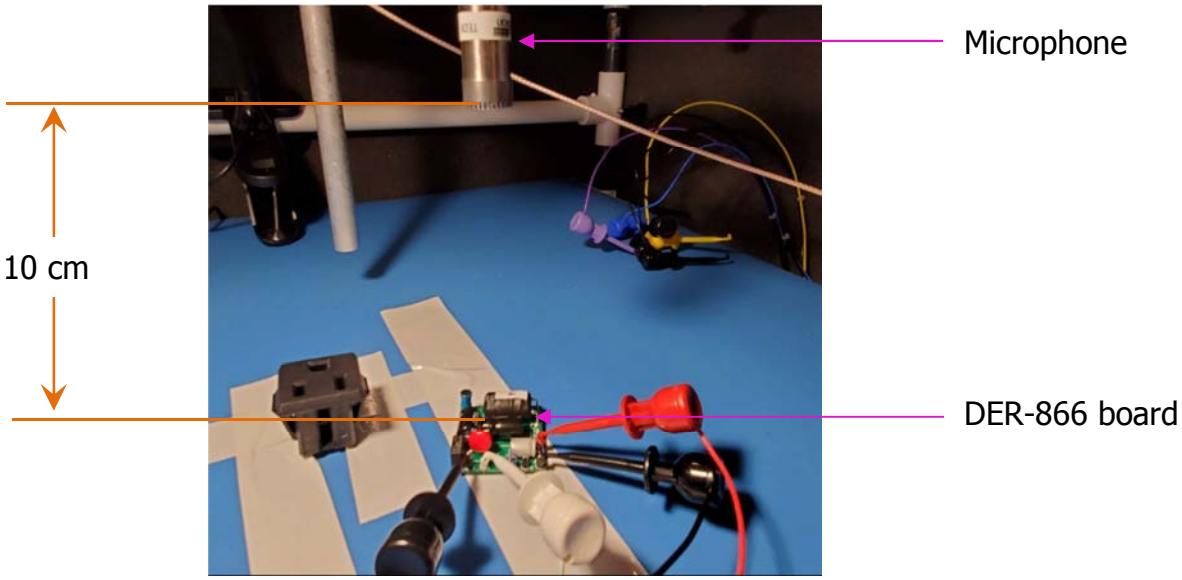


Figure 94 – Audible Noise Measurement Set-up Pictures.

Glue application points
Location 1: L2
Location 2: Between L2 and C1
Glue material: Digikey Part no:
SDL4062-ND

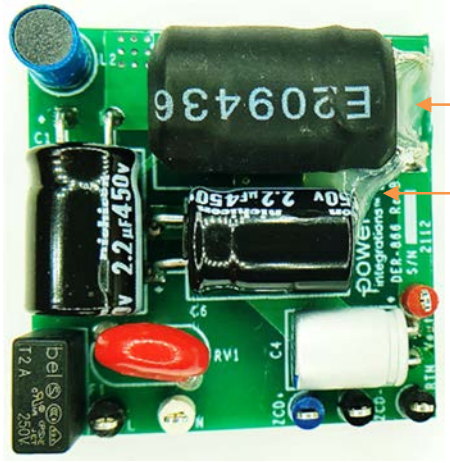


Figure 95 – Glue Point Locations.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

14.2 ***Audible Noise Measurements***

Audible noise measured from full load to no-load.

14.2.1 Audible Noise with No Glue Applied on the Board

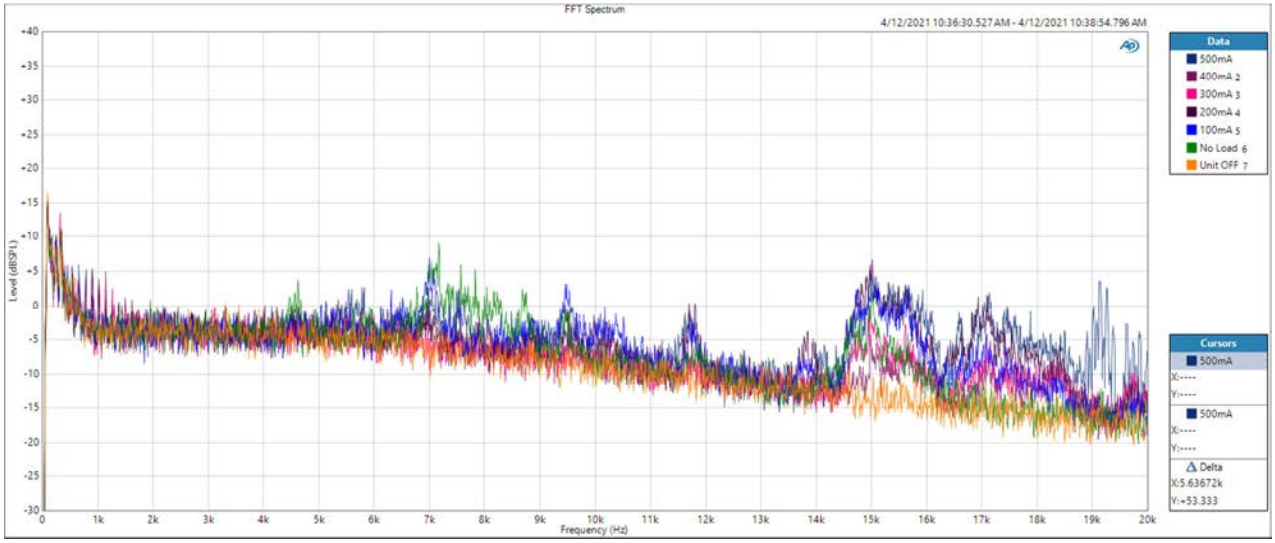


Figure 96 – Audible Noise Measurements at 120 VAC.

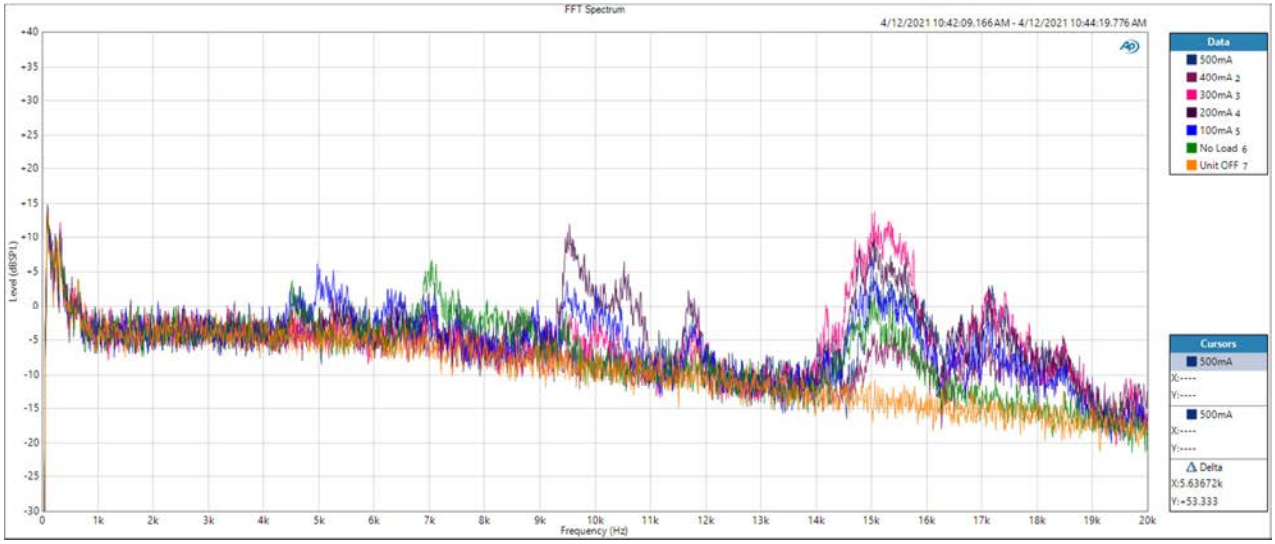


Figure 97 – Audible Noise Measurements at 230 VAC.

14.2.2 Audible Noise with Glue Applied on the Board

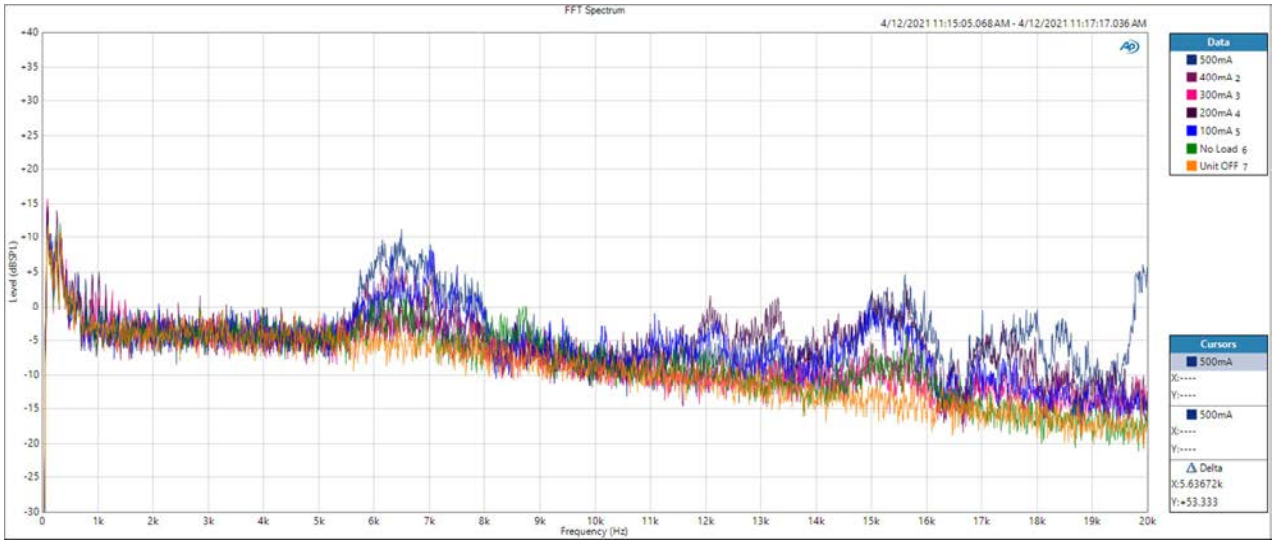


Figure 98 – Audible Noise Measurements at 120 VAC.

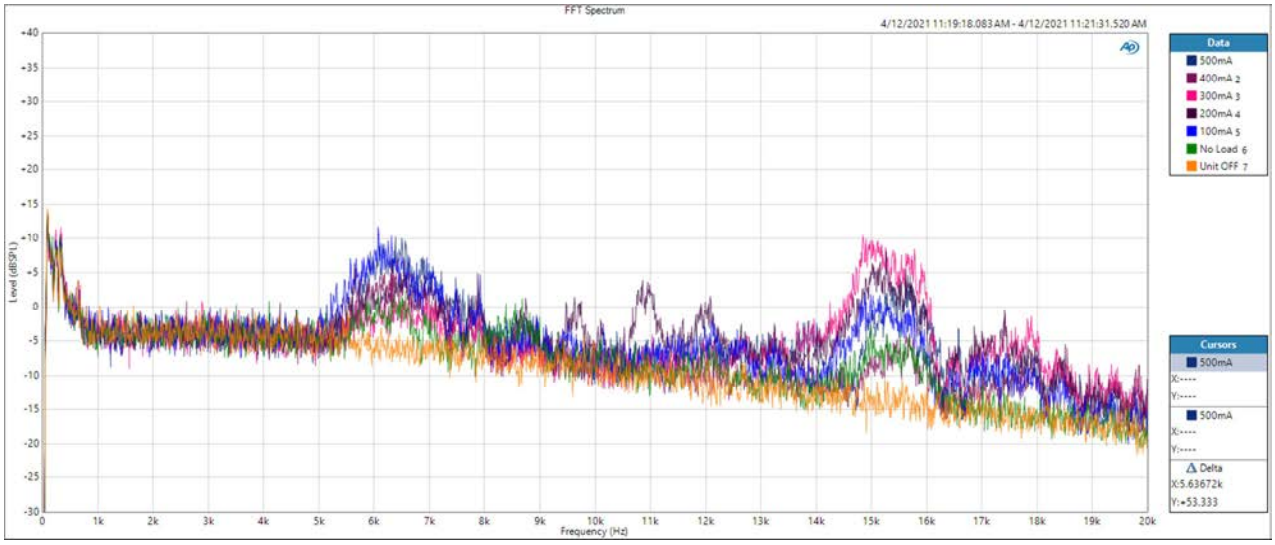


Figure 99 – Audible Noise Measurements at 230 VAC.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
03-Jun-21	MGM	1.0	Initial Release.	Apps & Mktg