Title	***Reference Design Report for a 30 W 1-Phase Inverter Using BridgeSwitch™ BRD1260C***
Specification	270 VDC – 365 VDC Input; 30 W Continuous Inverter Output Power, 0.22 A Continuous Motor RMS Current
Application	High-Voltage Single-Phase BLDC Motor
Author	Applications Engineering Department
Document No.	RDR-873
Date	March 23, 2021
Revision	1.2

Summary and Features

- BridgeSwitch – high-voltage half-bridge motor driver
  - Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- Single-phase inverter design for high-voltage BLDC applications using BRD1260C
- Highly compact design with an inverter size of 25 x 30 mm
- Inverter efficiency up to 95% in trapezoidal control scheme
- <100 ºC package temperature at 65 ºC ambient with no external heat sink
- Fully self-biased operation – no auxiliary power supply needed on the BridgeSwitch devices
- Supports low-side external-bias operation for low no-load input power requirement
- Integrated high-side and low-side cycle-by-cycle current limit on each BridgeSwitch devices
- Device over-temperature protection
- High-voltage bus monitor with four undervoltage threshold and one overvoltage threshold
- Instantaneous phase current output signal on each BridgeSwitch devices
- Single wire status update communication bus
- External system sensing input

Power Integrations, Inc.
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 (408) 414-9200 Fax: +1 (408) 414-9201
www.power.com

Table of Contents

Important Note:
During operation, the design example board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

1 Introduction

This document is an engineering report describing a 0.22 A_{RMS}, 30 W, up to 95% efficient compact single-phase inverter design for a high-voltage single-phase brushless DC (BLDC) motor using BridgeSwitch™ motor driver IC.

The inverter stage is implemented using two fully integrated BridgeSwitch (BRD1260C) devices in a full-bridge inverter configuration. BridgeSwitch driver IC comes in a small footprint surface mount InSOP-24C package with exposed pads that enable heat sinking through PCB allowing a small form factor solution with few components.

The board incorporates a simple control interface to the external controller facilitating the inverter control inputs and the BridgeSwitch additional features including a system sensing input, instantaneous phase current output and a single wire status update communication bus. In addition, an optional input for low-side device external-bias operation is provided for low no load input power requirement.

This document contains the inverter specifications, circuit schematic, bill of materials, printed circuit board layout, the inverter performance, inverter manual and the bench test set-up.

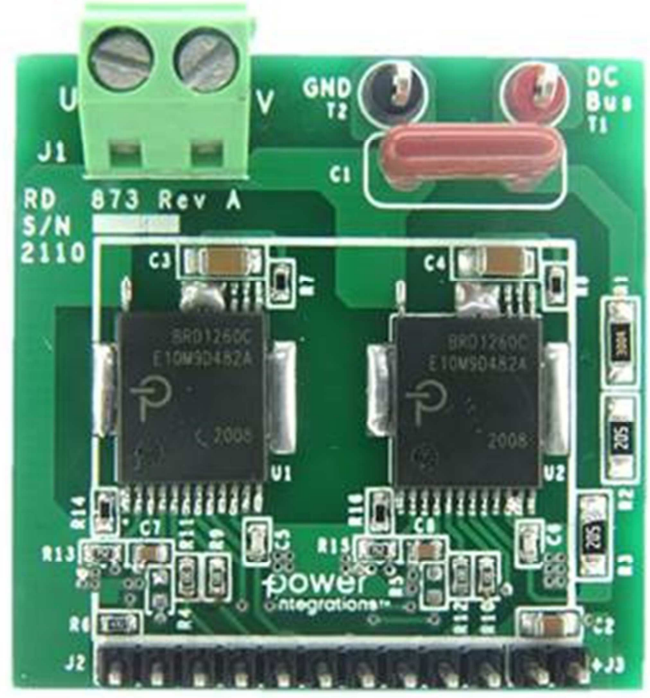

Figure 1 – Populated Circuit Board Photograph, Top.

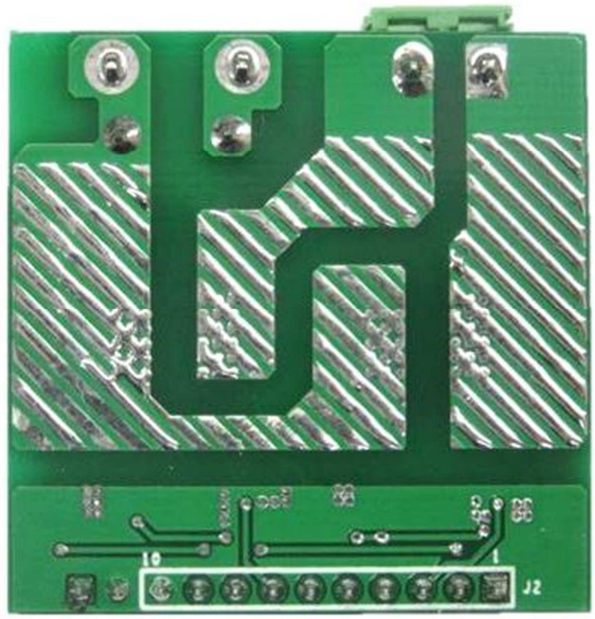

Figure 2 – Populated Circuit Board Photograph, Bottom.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

2 Inverter Specification

The table below provides the electrical specification of the single-phase inverter design.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	270	310	365	V	High-Voltage DC Bus.
Power	P_{IN}		31.4		W	Inverter Input Power.
Output						
Power	P_{OUT}		30		W	Inverter Output Power.
Motor Current	$I_{MOT(RMS)}$		0.22		A	Continuous RMS Current.
Motor Output Speed	ω		1000		RPM	Motor Speed at 30 W Inverter Output Power.
PWM Carrier Frequency	F_{PWM}		18		kHz	High-side PWM Control Frequency.
Efficiency						
Full load	ζ		95.5		%	30 W Inverter Output Power in External-Supply Operation.
Environmental						
Ambient Temperature	T_{AMB}	-20	25	65	°C	Free Convection
Device Case Temperature	$T_{PACKAGE}$			100	°C	0.22 A_{RMS} Motor Current in Self-Supplied Operation with BridgeSwitch BRD1260C.
DC Bus Sensing[1]						
OV Threshold	V_{OV}		422		V	Reported Through Status Communication Bus.
1st UV Threshold	V_{UV100}		247		V	
2nd UV Threshold	V_{UV85}		212		V	
3rd UV Threshold	V_{UV60}		177		V	
4th UV Threshold	V_{UV55}		142		V	
Overcurrent Protection[2]						
Internal HS / LS FREDFET Over-current Threshold	I_{OC}		0.7		A	BridgeSwitch BRD1260C. Default Current Limit.

Notes:
[1] Externally programmable through SM pin sensing resistor
[2] Externally programmable through XL/XH pin resistors (0.7 A default current limit at 44.2 kΩ)

Table 1 – Inverter Specification.

3 Schematic

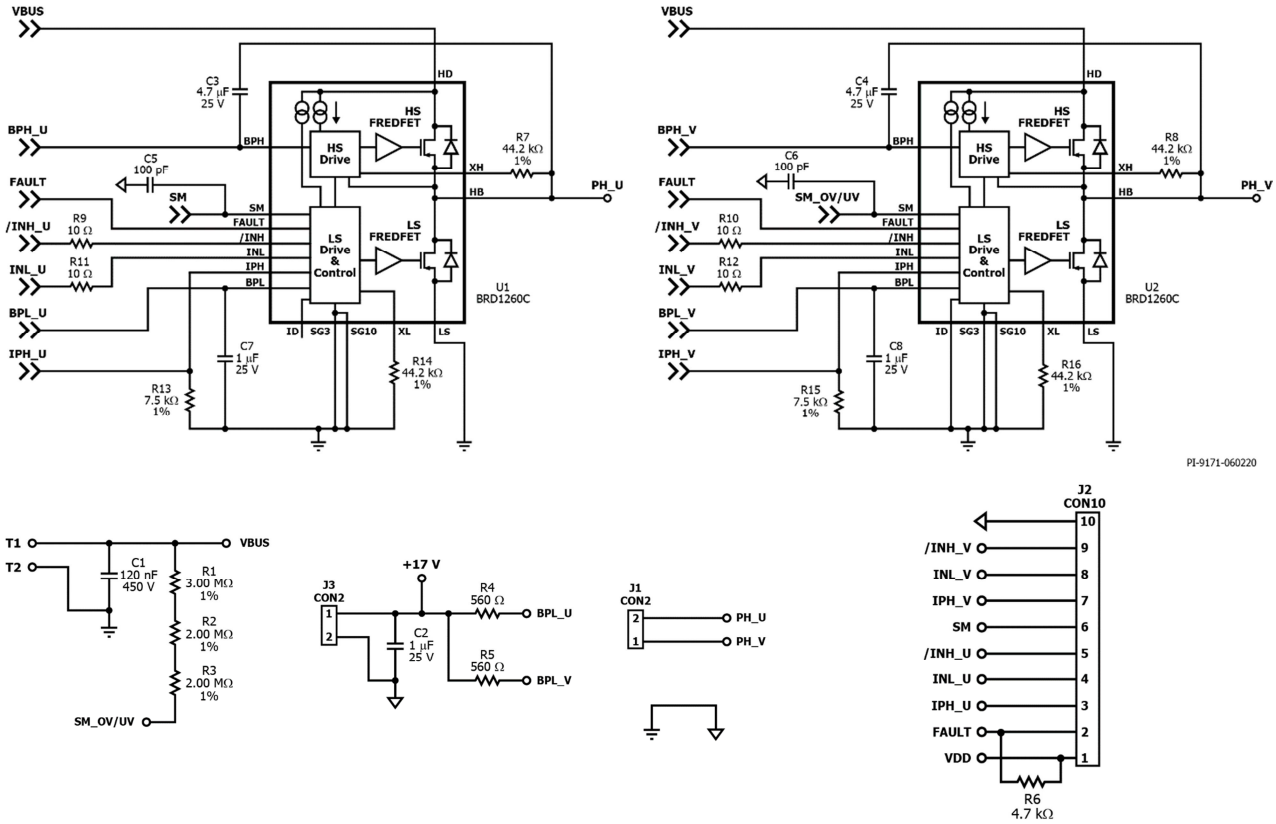

Figure 3 – BridgeSwitch Single Phase Inverter Schematic.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

4 Circuit Description

The schematic in Figure 3 shows a single-phase inverter in full-bridge configuration employing two BRD1260C devices. The circuit enables driving a high-voltage, single winding single-phase brushless DC (BLDC) motor from a DC input voltage. BridgeSwitch integrates two N-channel 600 V rated power FREDFETs, gate drivers and controllers into a low profile surface mount package IC. The power FREDFETs feature ultra-soft, fast recovery diodes ideally suited for hard switched inverter drives. Both drivers are fully self-supplied eliminating the need for an external power supply for the design. The board signal interface provides access to the inverter control inputs as well as facilitating BridgeSwitch additional features including a system sensing input, instantaneous phase current output and a single wire status update communication bus. An optional device power supply input allows low-side external bias operation for applications that require a very low inverter no load input power.

BridgeSwitch has device internal fault protection and system-level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two-level thermal overload protection. System level monitoring includes high-voltage DC bus sensing with multi-level undervoltage thresholds and one overvoltage threshold as well as driving external sensors such as a thermistor for system temperature monitoring. This design example employs a DC bus sensing on one device and provides a system sense input on another device. Half-bridge phase current (low-side FREDFET instantaneous current) information is provided through its instantaneous phase current output IPH pin. A single-wire open-drain bus communicates all detected fault or status change conditions.

4.1 *High-Voltage Input*

The high-voltage DC input and power ground connects to the input terminals T1 and T2 respectively. Capacitor C1 provides the local decoupling of the high-voltage DC link input provided externally to the inverter board.

4.2 *Single-Phase Inverter Stage*

The two BridgeSwitch devices (BRD1260C) U1 and U2 form the single-phase inverter in full-bridge configuration. The half-bridge point of each device connects to a single winding single-phase high-voltage BLDC motor.

4.2.1 Self-Supply Operation

Capacitors C7 and C8 provide self-supply decoupling for the integrated low-side controller and gate driver for device U1 and U2 respectively. Internal high-voltage current sources recharge them as soon as the voltage level starts to dip. Capacitors C3 and C4 provide self-supply decoupling for the integrated high-side controller and gate driver for device U1 and U2 respectively.

Internal high-voltage current sources recharge them whenever the half-bridge point of the respective device drops to the low-side source voltage level (i.e. the low-side FREDFET turns on).

4.2.2 Control Inputs

Control input signals INL_U, /INH_U, INL_V and /INH_V, control the switching state of the integrated high side and low side power FREDFETs. These control input signals interface to the system microcontroller through pins 4, 5, 8 and 9 of the signal interface connector J2 and are compatible with 3.3 V and 5 V CMOS logic levels. Series gate resistors R11, R9, R12, and R10 maintain the signal integrity of the control input signals.

4.2.3 Cycle-by-Cycle Current Limit

Resistors R14, R7, R16, and R8 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. The selected value of 44.2 kΩ sets it to 100% of the default level. The default current limit, $I_{LIM(DEF)}$ = 0.7 A (typical) at di/dt = 250 mA/μS with BRD1260C. The FAULT pin reports any detected device overcurrent fault condition to the system MCU via the status communication bus.

4.2.4 Instantaneous Phase Current Information

Each BridgeSwitch device provides instantaneous phase current information of the low-side power FREDFET Drain to Source current through its IPH pin output across resistors R13 and R15 respectively. With BRD1260C, the IPH pin output gain is 400 μA/A, which translates into a 3 V signal per 1 A drain current with the selected value of 7.5 kΩ. The respective IPH pin output signals IPH_U and IPH_V of device U1 and U2 are available on the pin 3 and 7 of the signal interface connector J2.

4.2.5 System Undervoltage and Overvoltage Monitoring and Protection

BridgeSwitch U2 monitors the DC bus voltage through resistors R1, R2, and R3. Their combined resistance of 7 MΩ sets the undervoltage thresholds to 247 V, 212 V, 177 V, and 142 V. The set bus overvoltage threshold is 422 V. Capacitor C6 provides an optional high frequency noise decoupling at the SM pin. The FAULT pin reports any detected bus voltage fault condition to the system MCU via the status communication bus.

4.2.6 External System Sense Input

BridgeSwitch U1 provides a system sense input via its SM pin, which can be connected externally, for example to an external thermistor as a system temperature sense. Capacitor C5 provides an optional high frequency noise decoupling at the SM pin. The FAULT pin reports a system fault condition (the current threshold on SM pin was reached) to the system MCU via the status communication bus. The system sense input is available on the pin 6 of connector J2.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

4.2.7 Status Communication Bus

Each BridgeSwitch will report any detected internal and system fault through the status communication bus (FAULT bus) located on pin 2 of connector J2. The two FAULT pins of each BridgeSwitch device are tied together in a single wire bus using a pull-up resistor (i.e. 10 kΩ) to VDD supply. The pull-up supply (VDD) for the open-drain fault output is available on the pin 1 of connector J2.

4.2.8 Device ID

Each BridgeSwitch device assigns itself a unique device ID by configuring its ID pin connection: device U1 ID pin floating (60 µs t_{ID}) and device U2 ID pin shorted to SG (80 µs). The device ID supports status communication bus arbitration and enables communicating the physical location of a detected fault to the system microcontroller (refer to the status communication section in the data sheet).

4.3 ***Microcontroller Interface***

A 10-position connector header J2 interfaces the single-phase inverter stage to the system microcontroller for the control inputs, instantaneous phase current information, external system sense input and the status communication bus.

4.4 ***External Device Supply***

The circuit also provides an external bias option to supply the integrated low-side and gate controller of each BridgeSwitch devices from a single input rail (17 VDC recommended) through J3 connector. The optional external bias operation addresses low inverter no load input power requirement in some applications. Capacitor C2 provides local decoupling of the external DC supply. Resistors R4 and R5 limit the external supply current on the BPL pin of the respective BridgeSwitch devices. These resistors must be depopulated when operating in self-supply mode to prevent BPL voltage threshold interactions.

4.5 ***Single-Phase Output Connector***

The respective half-bridge output of the BridgeSwitch device U1 and U2 connect to the single-phase high-voltage BLDC motor through the connector J1.

5 Printed Circuit Board Layout

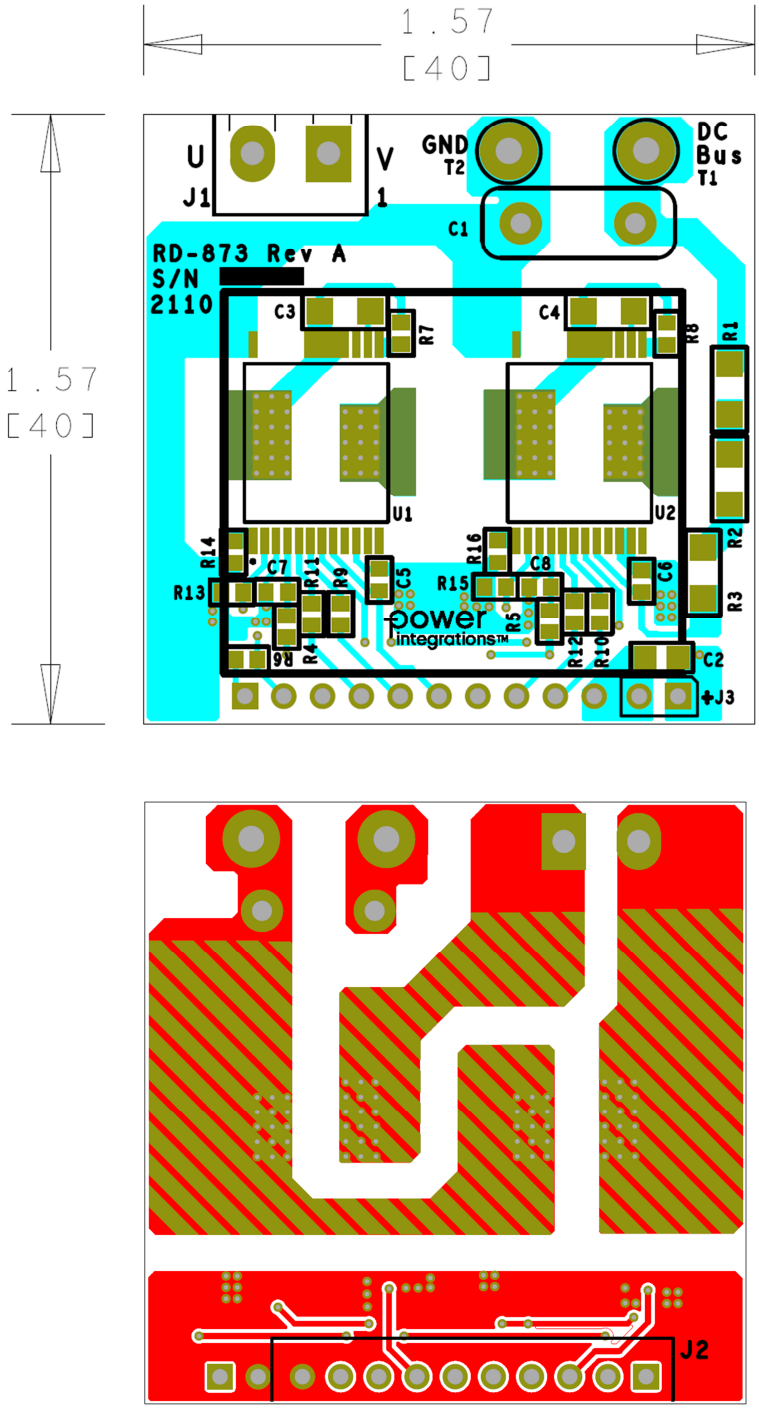

Figure 4 – Printed Circuit Board Layout Top and Bottom View.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	120 nF, 450 VDC, Film, 5%, RADIAL	ECW-FD2W124J4	Panasonic
2	1	C2	1 µF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
3	2	C3, C4	4.7 µF, 35 V, Ceramic, X5R, 1206	GCM31CR71E475KA55L	Murata
4	2	C5, C6	100 pF, 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
5	2	C7, C8	1 µF, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
6	1	J1	2 Position (1 x 2) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	1715022	Phoenix Contact
7	1	J2	10 Position (1 x 10) header, 0.1 pitch, Vertical	22-28-4100	Molex
8	1	J3	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-28-4020	Molex
9	1	R1	RES, 3 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3004	Rohm
10	2	R2, R3	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
11	2	R4, R5	RES, 560 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ561V	Panasonic
12	1	R6	RES, 4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
13	4	R7, R8, R14, R16	RES, 44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422V	Panasonic
14	4	R9, R10, R11, R12	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
15	2	R13, R15	RES, 7.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
16	1	T1	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone
17	1	T2	Test Point, RED,THRU-HOLE MOUNT	5011	Keystone
18	2	U1, U2	BridgeSwitch, Full Featured, Continuous Rated Current 0.22 A (RMS)	BRD1260C	Power Integrations

Table 2 – Bill of Materials.

7 Performance Data

This section presents the performance data gathered on the RDR-873 inverter board. The performance data presented were taken with the inverter operating using the test setup and motor control algorithm detailed in Appendix 8.3 and Appendix 8.6. The inverter operates at nominal test conditions with the BridgeSwitch devices in self-supply mode unless noted otherwise. For external supply mode, the inverter is supplied by a 17 VDC external DC supply through the input connector, J3. All measurements were performed at room ambient temperature.

In addition, the use of complementary PWM mode with BridgeSwitch is demonstrated with RDR-873 and described in Appendix 8.7. This unique device feature provides additional benefits such as reduced micro-controller pin count and simplified PCB layout.

7.1 *Start-up Operation*

Figure 4 and 5 shows the inverter start-up waveforms captured on one BridgeSwitch device (U2). Figure 5 depicts the low-side and high-side BYPASS pin voltages of BridgeSwitch device during start-up sequence. Figure 6 depicts the motor phase current, PWM control signals (INL and \INH) and the half-bridge voltage.

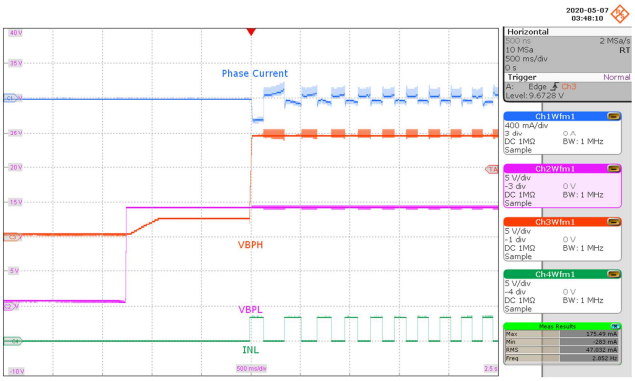

Figure 5 – BPL and BPH-pin Voltages at Start-Up
First: I_{MOTOR}, 400 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 500 ms / div.

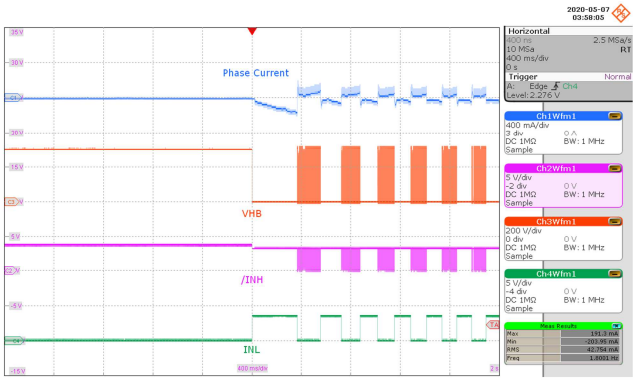

Figure 6 – Motor Start-up Waveforms
First: I_{MOTOR}, 400 mA / div.
Second: V_{HB}, 200 V / div.
Third: V_{INL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 400 ms / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.2 *Steady-State Operation*

Figure 7 to 10 depict the motor phase current and half-bridge voltage signals during steady state operation.

7.2.1 Phase Currents During Steady-State

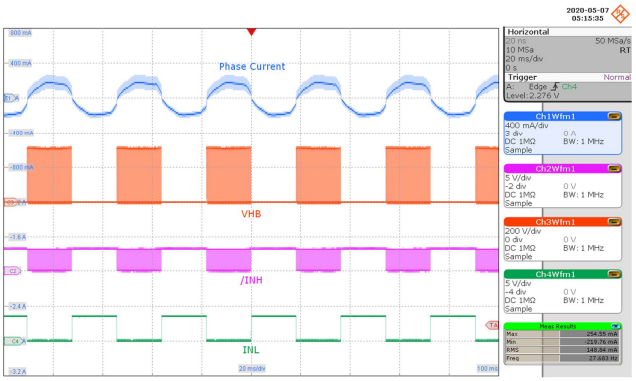

Figure 7 – At 15 W Inverter Output Power.
$I_{MOTOR, RMS}$: 148 mA.
First: I_{MOTOR}, 400 mA / div.
Second: V_{HB}, 200 V / div.
Third: $V_{/INH}$, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 20 ms / div.

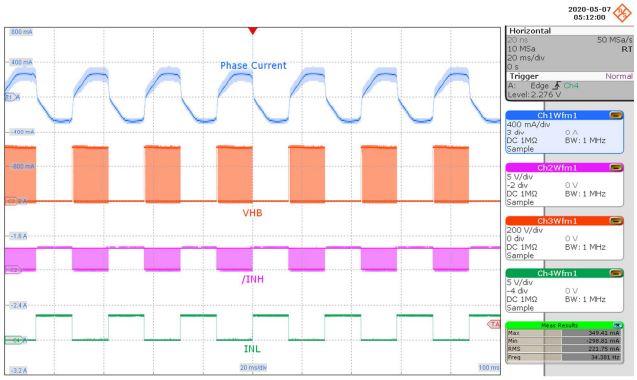

Figure 8 – At 30 W Inverter Output Power.
$I_{MOTOR, RMS}$: 220 mA.
First: I_{MOTOR}, 400 mA / div.
Second: V_{HB}, 200 V / div.
Third: $V_{/INH}$, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 20 ms / div.

7.2.2 Half-Bridge Voltage Signals During Steady-State

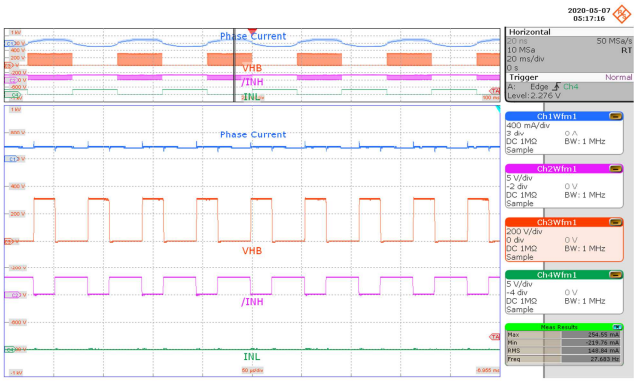

Figure 9 – At 15 W Inverter Output Power.
$I_{MOTOR, RMS}$: 148 mA.
First: I_{MOTOR}, 400 mA / div.
Second: V_{HB}, 200 V / div.
Third: $V_{/INH}$, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 50 µs / div.

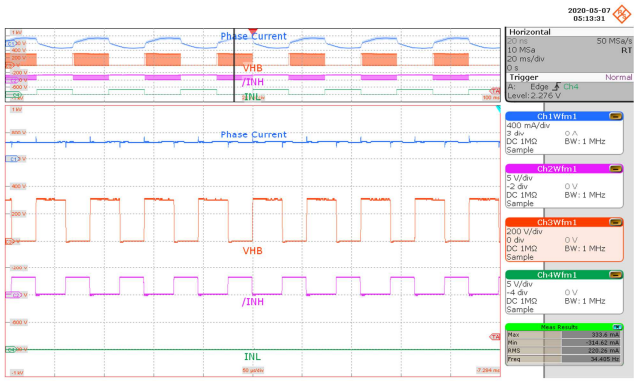

Figure 10 – At 30 W Inverter Output Power.
$I_{MOTOR, RMS}$: 148 mA.
First: I_{MOTOR}, 400 mA / div.
Second: V_{HB}, 200 V / div.
Third: V_{INL}, 5 V / div.
Fourth: $V_{/INH}$, 5 V / div.
Time Scale: 50 µs / div.

7.2.3 /INH and INL Input Signals During Steady-State

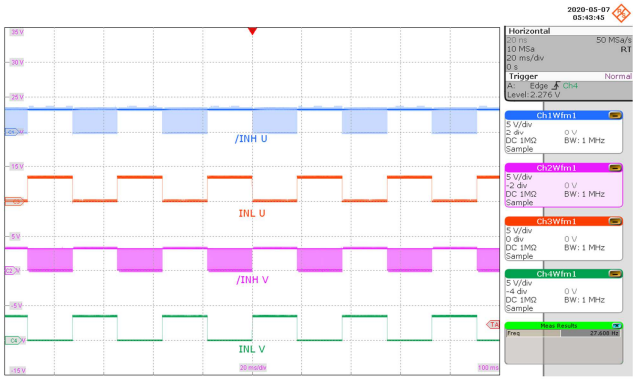

Figure 11 – At 15 W Inverter Output Power.
Motor Speed : 800 RPM
First: $V_{/NH\_U}$, 5 V / div.
Second: V_{INL_U}, 5 V / div.
Third: $V_{/INH\_V}$, 5 V / div.
Fourth: V_{INL_V}, 5 V / div.
Time Scale: 20 ms / div.

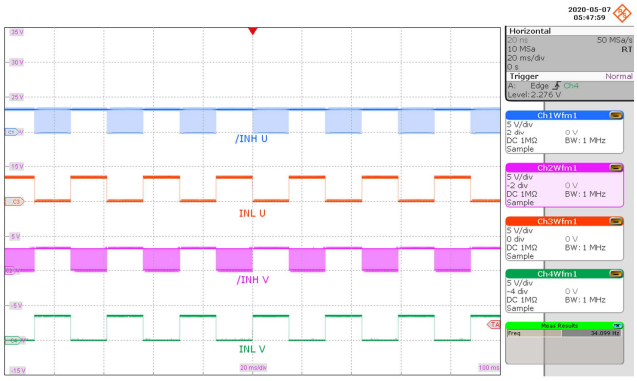

Figure 12 – At 30 W Inverter Output Power.
Motor Speed : 1000 RPM
First: $V_{/INH\_U}$, 5 V / div.
Second: V_{INL_U}, 5 V / div.
Third: $V_{/INH\_V}$, 5 V / div.
Fourth: V_{INL_V}, 5 V / div..
Time Scale: 20 ms / div.

7.2.4 BYPASS Pin Voltage Signals During Steady-State

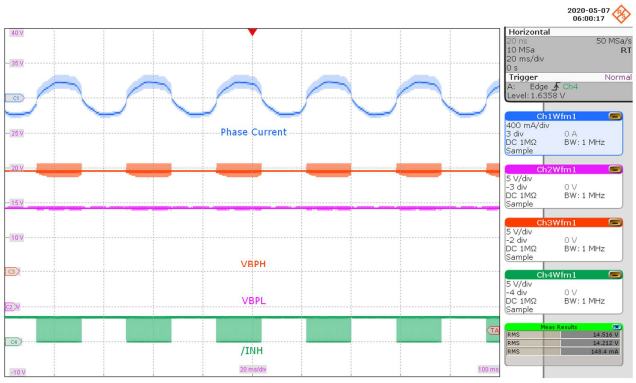

Figure 13– At 15 W Inverter Output Power.
First: I_{MOTOR}, 400 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 20 ms / div.

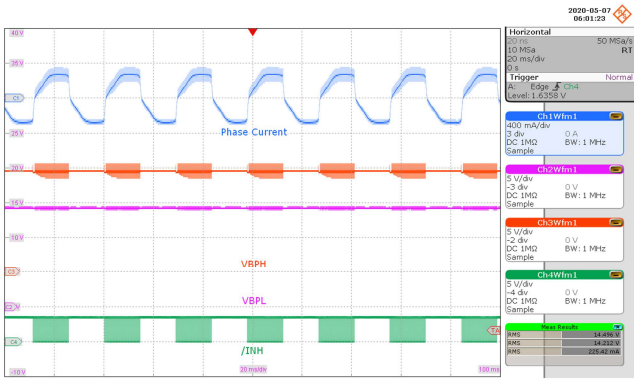

Figure 14– At 30 W Inverter Output Power.
First: I_{MOTOR}, 400 mA / div.
Second: V_{BPH}, 5 V / div.
Third: V_{BPL}, 5 V / div.
Fourth: V_{INL}, 5 V / div.
Time Scale: 20 ms / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.2.5 Phase Current Information Signal (IPH)

Figure 15 to Figure 16 depict the phase current waveform of device U2 and the corresponding phase current output signal available on pins 3 and 7 of connector J2.

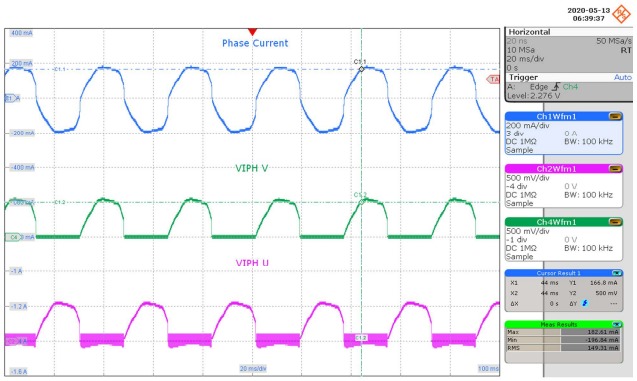

Figure 15 – At 15 W Inverter Output Power.
First: I_{MOTOR}, 200 mA / div.
Second: V_{IPH_V}, 1 V / div.
Third: V_{IPH_U}, 1 V / div.
Time Scale: 20 ms / div.

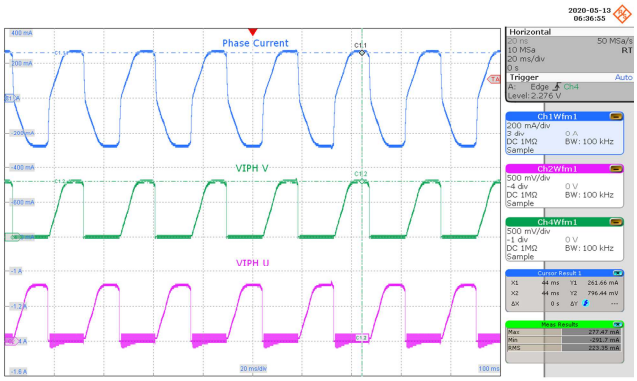

Figure 16 – At 30 W Inverter Output Power.
First: I_{MOTOR}, 200 mA / div.
Second: V_{IPH_V}, 1 V / div.
Third: V_{IPH_U}, 1 V / div.
Time Scale: 20 ms / div.

7.2.6 FREDFET Drain-voltage Slew Rate at Full Load

Figure 17 and Figure 18 depict low-side FREDFET Drain voltage slew rates at turn-on and turn-off at 30 W inverter output power respectively.

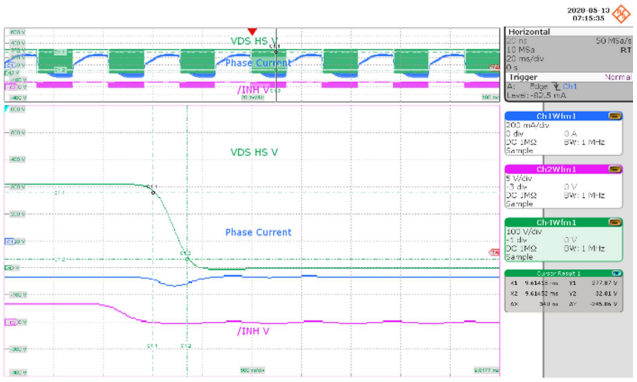

Figure 17 – High-Side FREDFET Turn-On.
Turn-On Voltage Slew Rate: 0.72 V / ns.
Upper: I_{MOTOR}, 200 mA / div.
Middle: $V_{DS\text{-}HS\_V}$, 100 V / div.
Lower: $V_{/INH\_V}$, 5 V / div., 20 ms/div.
Zoom: 50 ns / div.

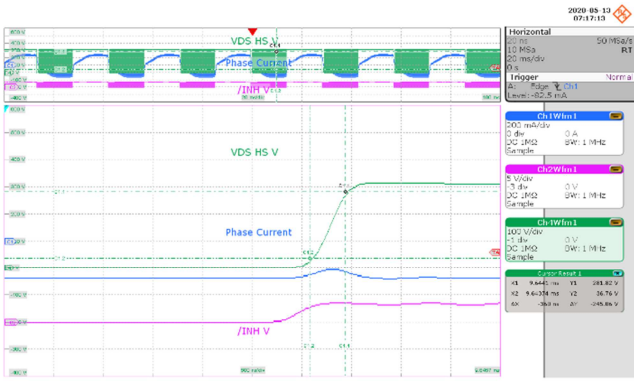

Figure 18 – High-Side FREDFET Turn-Off.
Turn-Off Voltage Slew Rate: 0.68 V / ns.
Upper: I_{MOTOR}, 200 mA / div.
Middle: $V_{DS\text{-}HS\_V}$, 100 V / div.
Lower: $V_{/INH\_V}$, 5 V / div., 20 ms /div.
Zoom: 500 ns / div.

7.3 *Thermal Performance*

Figure 19 and Figure 20 depicts the open case board thermal scan of the inverter board in self-supply operation at 15 W and 30 W inverter output power, respectively, taken at room ambient temperature.

Figure 19 – Thermal Scan at 15 W Inverter Output in Self-Supply Operation.

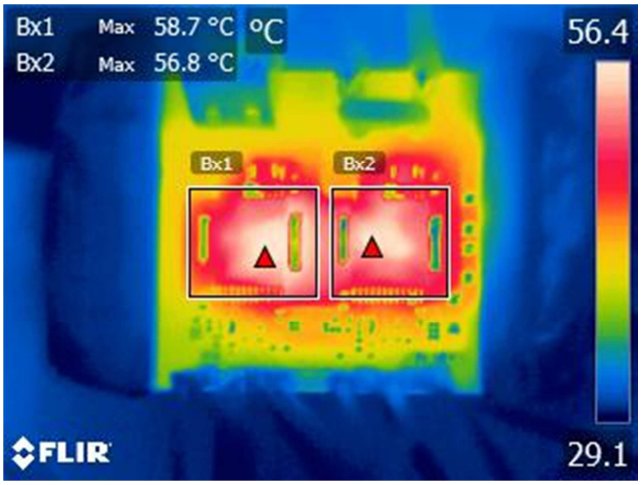

Figure 20 – Thermal Scan at 30 W Inverter Output in Self-Supply Operation.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Figure 21 and Figure 22 depicts the open case board thermal scan of the inverter board while supplied externally (17 VDC applied to external supply input, J3) at 15 W and 30 W inverter output power, respectively, taken at room ambient temperature.

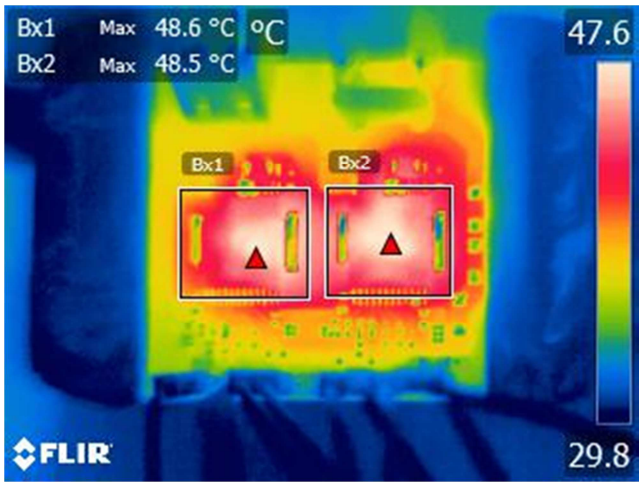

Figure 21 – Thermal Scan at 15 W Inverter Output in External-Supply Operation.

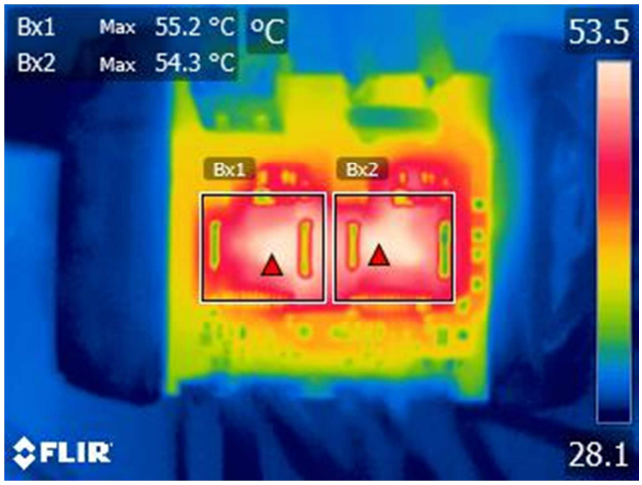

Figure 22 – Thermal Scan at 30 W Inverter Output in External-Supply Operation.

Figure 23 summarizes the device average case temperature rise above ambient with the inverter operating in self-supply and external supply mode.

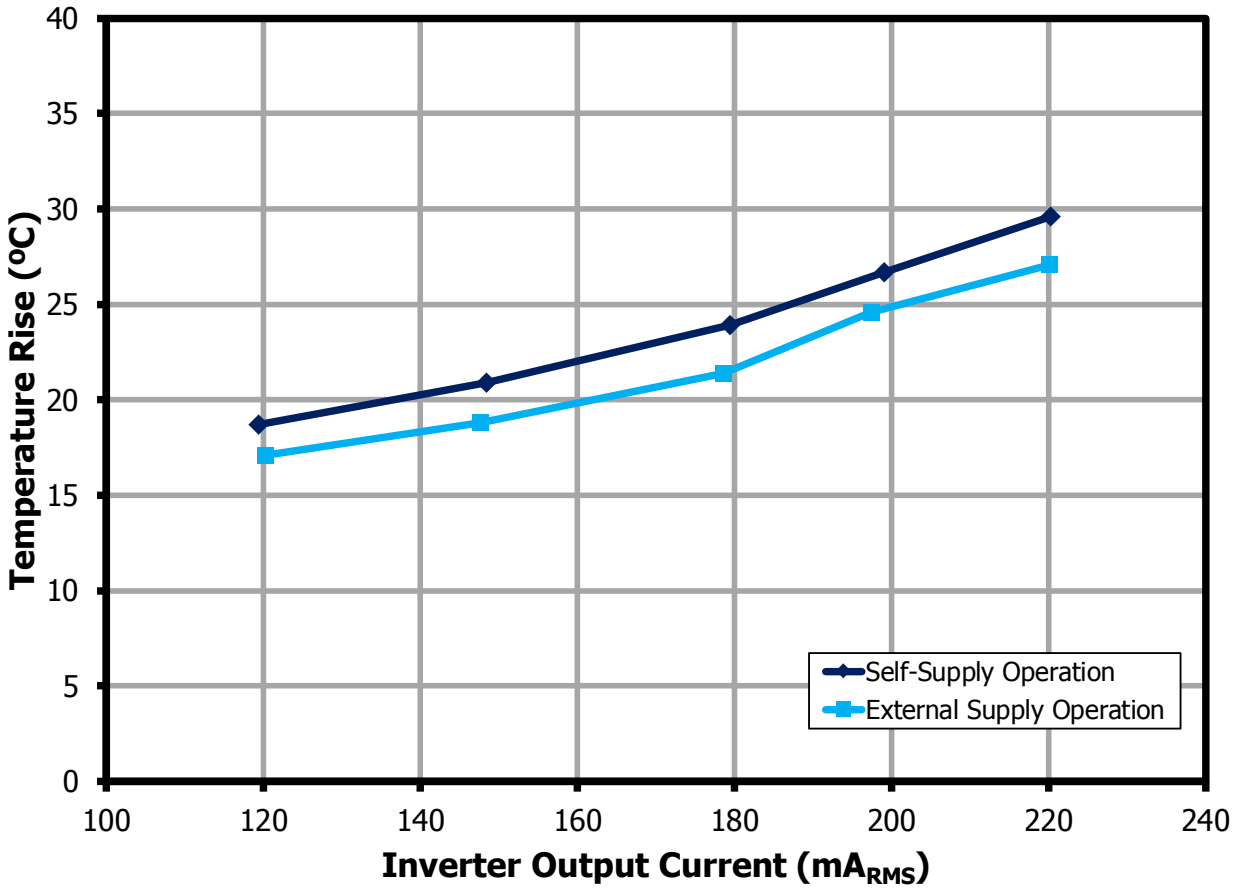

Figure 23 – Device Average Case Temperature Rise.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.4 *No-Load Power Consumption*

Figure 24 depicts the inverter no-load input power consumption measured across the input line voltage with the inverter operating in self-supply and external supply mode.

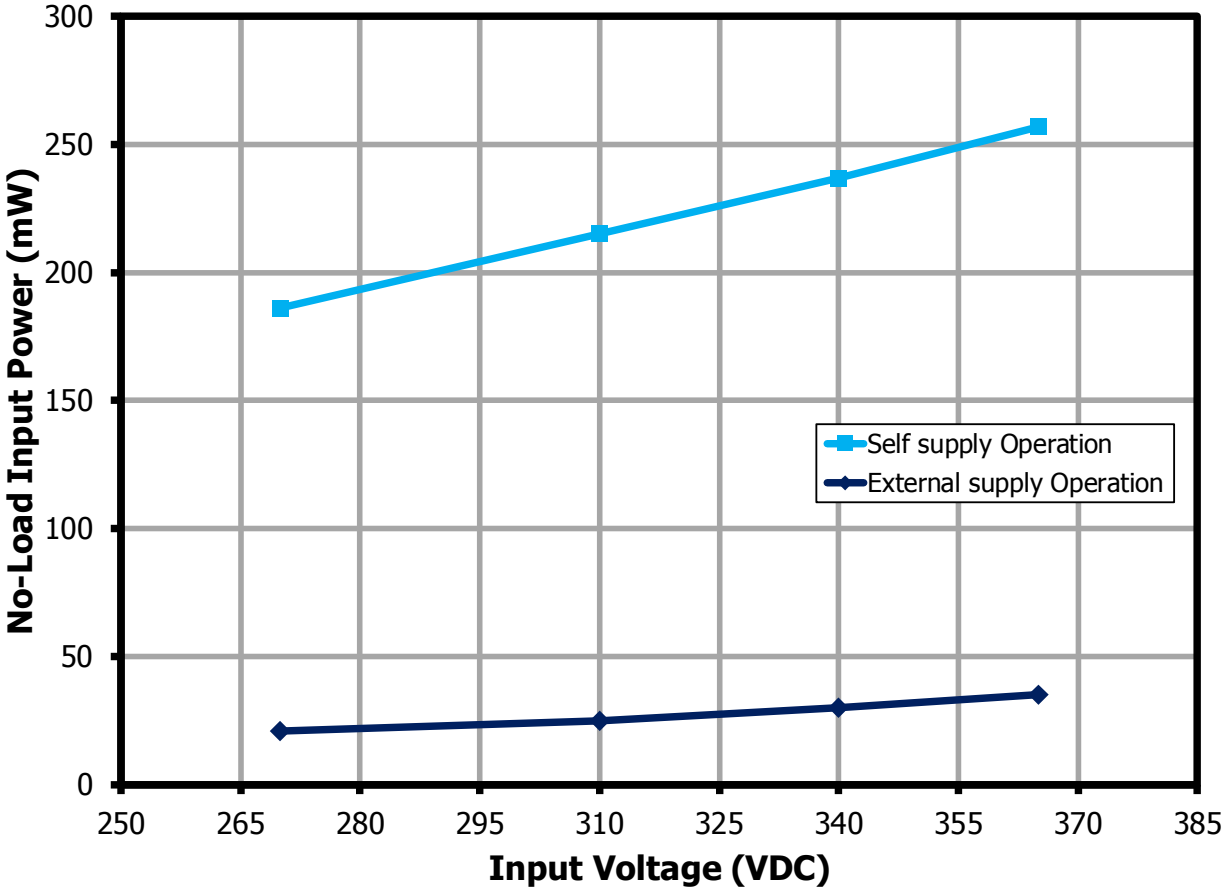

Figure 24 – No-Load Input Power.

7.5 *Efficiency*

Figure 25 depicts the inverter efficiency versus output power. Table 3 and 4 shows the efficiency data described in this graph.

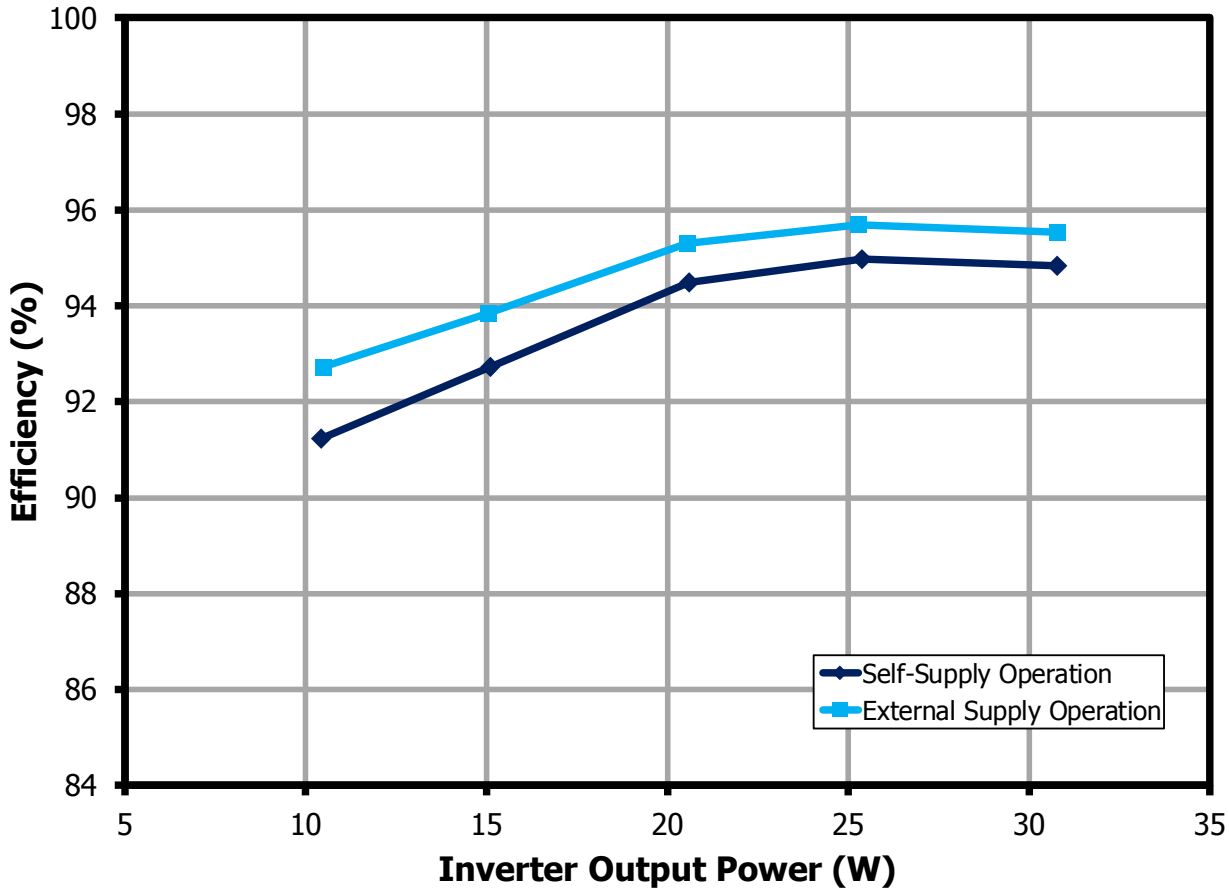

Figure 25 – Inverter Efficiency.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Table 3 provides the efficiency data with the inverter operating in self-supply mode.

Input DC Voltage	Speed	DC Input Power	Motor RMS Current	Inverter Output Power	Inverter Efficiency
(V)	(RPM)	(W)	(mA)	(W)	(%)
310	726	11.432	119.36	10.43	91.24
310	822	16.275	148.39	15.091	92.73
310	908	21.794	177.2	20.594	94.49
310	971	26.72	198.06	25.377	94.97
310	1034	32.46	220.3	30.786	94.84

Table 3 – Self-supply Inverter Efficiency Data.

Table 4 provides the efficiency data with the inverter operating in external-supply mode.

Input DC Voltage	Speed	DC Input Power	Motor RMS Current	Inverter Output Power	Inverter Efficiency
(V)	(RPM)	(W)	(mA)	(W)	(%)
310	726	11.308	120.21	10.484	92.71
310	823	16.044	147.73	15.056	93.84
310	904	21.574	178.62	20.559	95.30
310	971	26.41	197.38	25.27	95.68
310	1037	32.22	220.09	30.779	95.53

Table 4 – External-supply Inverter Efficiency Data.

7.6 *Device and System Level Protection and Monitoring*

This section demonstrates the device integrated and system-level protection and monitoring feature. Each device communicates its status including device or system level fault through the status communication bus (FAULT bus). The status communication bus is available through pin 2 of connector J2 (open-drain pin that connects to an external VDD pull-up supply).

7.6.1 Device Level Protection

7.6.1.1 Over Current Protection

Figure 26 and Figure 27 depict the integrated current limit function at device U2 (phase V) and the associated status update reported on the FAULT bus during motor overload condition. In this demonstration, a lower current limit was selected to limit the inverter peak output power to 40 W.

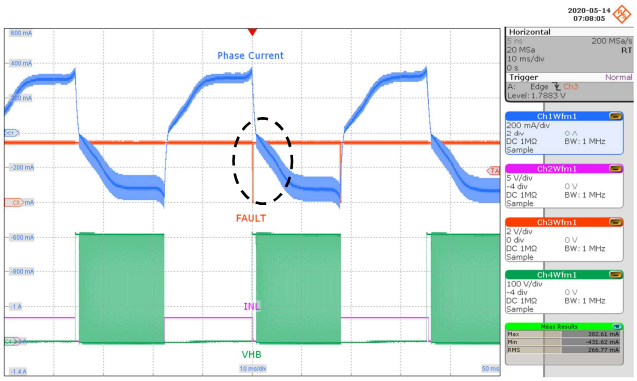

Figure 26 – Over-current - Motor Overload.
Peak Current: 0.38 A R_{XL}: 57.6 kΩ.
First: I_{MOTOR}, 200 mA / div.
Second: V_{FAULT}, 2 V / div.
Third: V_{HB_V}, 100 V / div.
Fourth: V_{INL_V}, 5 V / div.
Time Scale: 10 ms / div.

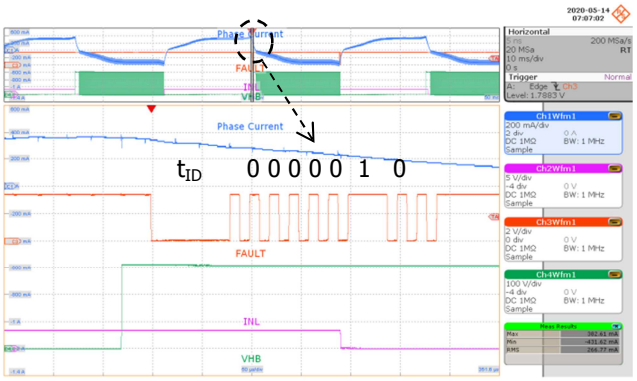

Figure 27 – LS FET Over-current Fault Status.
Status Update: 000 00 1 0 (LS OC)
Upper: I_{MOTOR}, 200 mA / div.
Middle: V_{FAULT}, 2 V / div.
Third: V_{HB_V}, 100 V / div.
Fourth: V_{INL_V}, 5 V / div., 10 ms / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Consequently, Figure 28 and Figure 29 depict the integrated current limit function at device U1 (phase U) and the associated status update reported on the FAULT bus during overload condition.

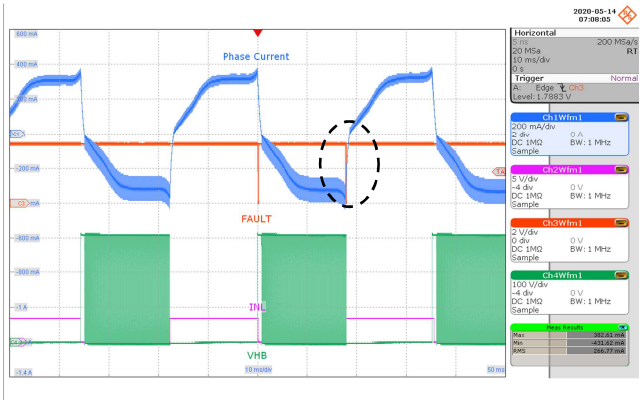

Figure 28 – Over-current - Motor Overload.
Peak Current: 0.38 A R_{XL}: 57.6 kΩ.
First: I_{MOTOR}, 200 mA / div.
Second: V_{FAULT}, 2 V / div.
Third: V_{HB_V}, 100 V / div.
Fourth: V_{INL_V}, 5 V / div.
Time Scale: 10 ms / div.

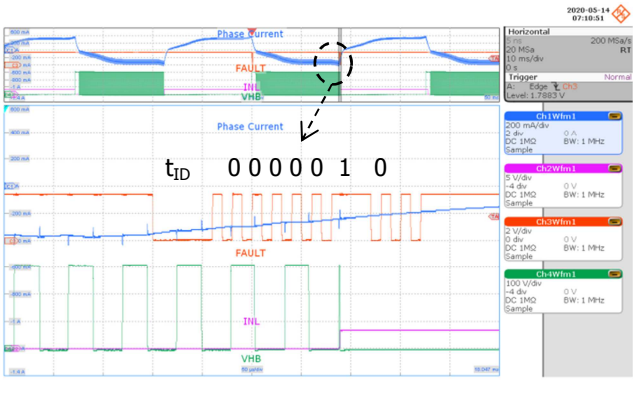

Figure 29 – LS FET Over-current Fault Status.
Status Update: 000 00 1 0 (LS OC)
Upper: I_{MOTOR}, 200 mA / div.
Middle: V_{FAULT}, 2 V / div.
Third: V_{HB_V}, 100 V / div.
Fourth: V_{INL_V}, 5 V / div., 10 ms / div.
Zoom: 50 µs / div..

7.6.1.2 Over Temperature Protection

Figure 30 and 31 depict the low-side FREDFET over-temperature warning (OTW) and shutdown (OTP) function and the associated status update reported on the FAULT bus during an over-temperature shutdown test. A localized external heat source applied to the device package forced the temperature rise while the inverter operating at full load condition.

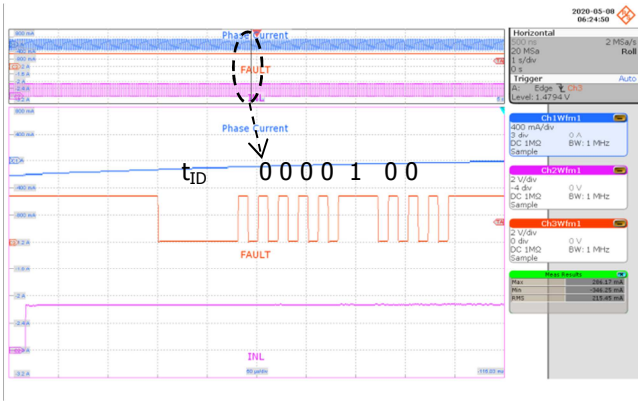

Figure 30 – Temperature Warning, Phase V.
Status Update: 000 01 0 0 (OTW).
Upper: I_{MOTOR}, 400 mA / div.
Middle: V_{FAULT}, 2 V / div.
Lower: V_{INL_V}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

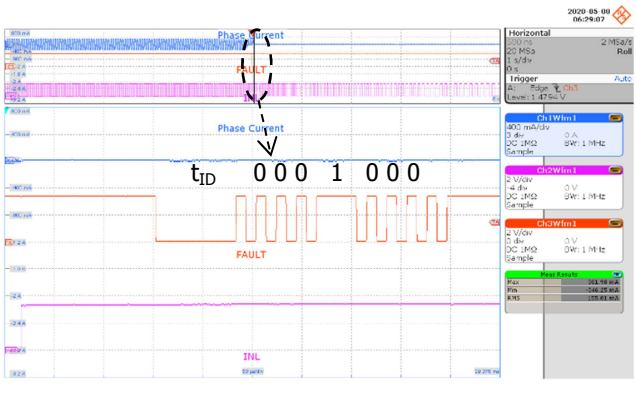

Figure 31 – Thermal Shutdown, Phase V.
Status Update: 000 10 0 0 (OTP).
Upper: I_{MOTOR}, 400 mA / div.
Middle: V_{FAULT}, 2 V / div.
Lower: V_{INL_V}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.6.2 System Level Monitoring

7.6.2.1 Undervoltage (UV)

The test results shown in Figures 32 to 35 demonstrate the integrated HV bus UV monitoring function and status reporting through the status communication bus. Device U2 (Phase V) senses the High-voltage DC input. The input voltage slew rate for all bus monitoring tests is 5 V / ms.

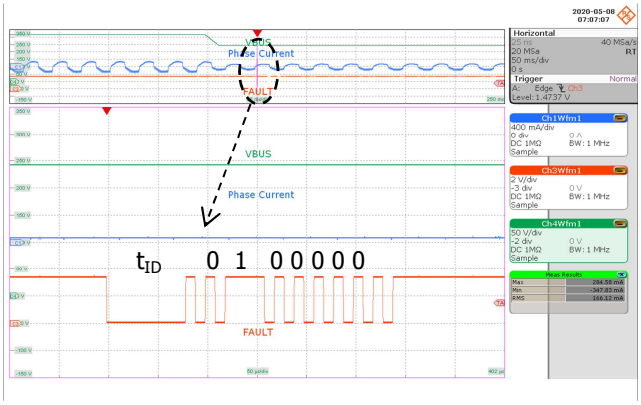

Figure 32 – Bus Sensing - Brown-out.
Bus Voltage Drop 340 to 240 VDC.
Status Update: 010 00 0 0 (UV100).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 50 ms / div.
Zoom: 50 µs / div.

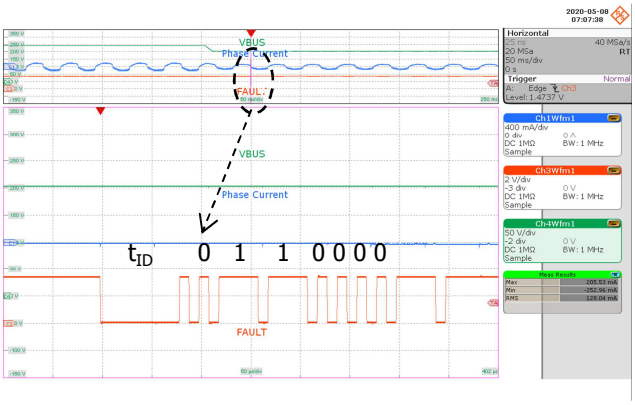

Figure 33 – Bus Sensing - Brown-out.
Bus Voltage Drop 240 to 200 VDC.
Status Update: 011 00 0 0 (UV85).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 50 ms / div.
Zoom: 50 µs / div.

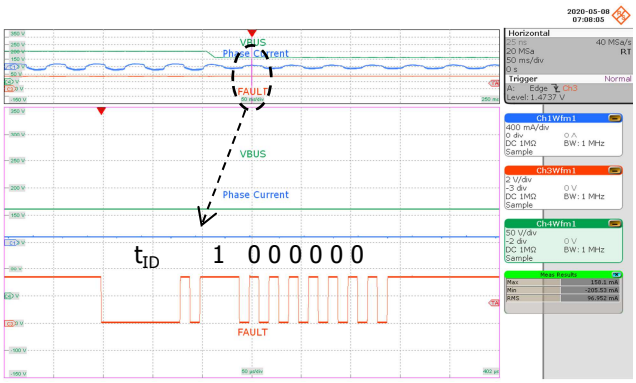

Figure 34 – Bus Sensing - Brown-out.
Bus Voltage Drop 200 to 160 VDC.
Status Update: 100 00 0 0 (UV70).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 50 ms / div.
Zoom: 50 µs / div.

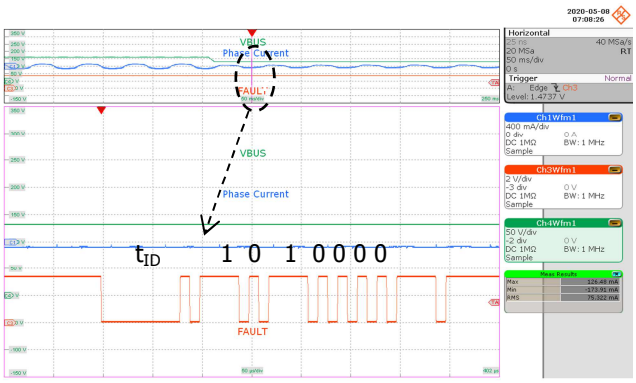

Figure 35 – Bus Sensing - Brown-out.
Bus Voltage Drop 160 to 130 VDC.
Status Update: 101 00 0 0 (UV55).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 50 ms / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.6.2.2 Overvoltage (OV)

Figure 36 and Figure 37 illustrate the HV bus OV monitoring feature. Device U2 (Phase V) stops switching and reports the OV fault condition as soon as the bus voltage exceeds the set OV threshold (422 V with 7 MΩ). Switching resumes after the bus voltage level drops again below the detection threshold minus the hysteresis.

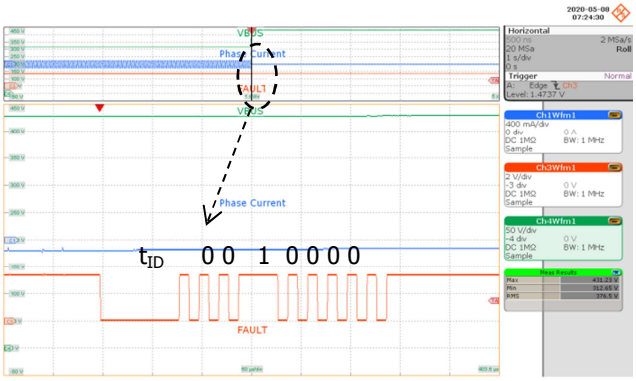

Figure 36 – Bus Sensing - OV Threshold Fault.
Bus Voltage Rise 340 to 430 VDC.
Status Update: 001 00 0 0 (OV).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div

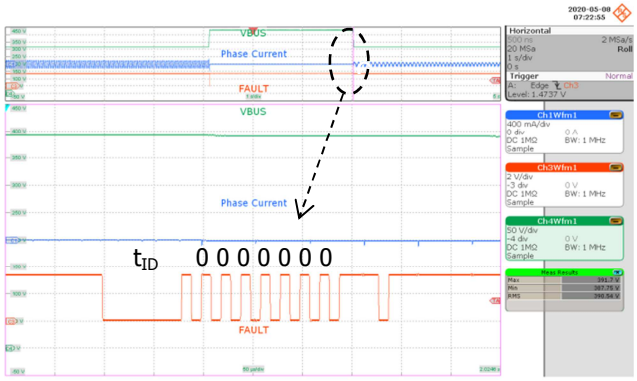

Figure 37 – Bus Sensing - OV Threshold Cleared.
Bus Voltage Drop 430 to 340 VDC.
Status Update: 000 00 0 0 (OV Cleared).
Upper: V_{BUS}, 50 V / div.
Middle: I_{MOTOR}, 400 mA / div.
Lower: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div

7.6.2.3 System Over Temperature

Figure 38 and Figure 39 illustrate the system-level temperature monitoring function via the external system sense input, SM (pin 6 of connector J2). For this test, the system temperature is sensed though an external NTC thermistor connected to the SM pin. Figure 38 depicts the status reporting when the system over-temperature threshold was reached while Figure 39 depicts the status reporting when the over-temperature was removed.

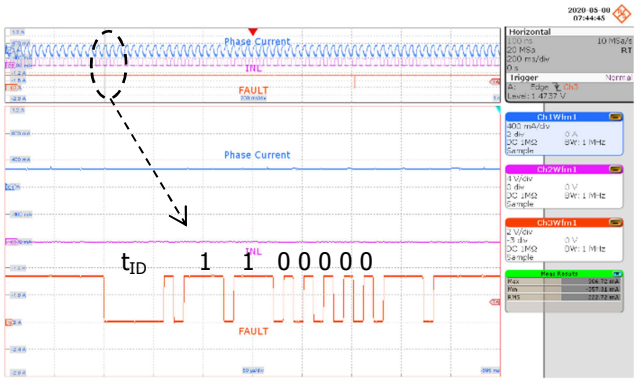

Figure 38 – External Temperature Fault Detected.
Status Update: 011 00 0 0 (System OT)
Upper: I_{MOTOR}, 400 mA / div.
Middle: V_{INL_U}, 4 V / div.
Lower: V_{FAULT}, 2 V / div., 200 ms / div.
Zoom: 50 µs / div

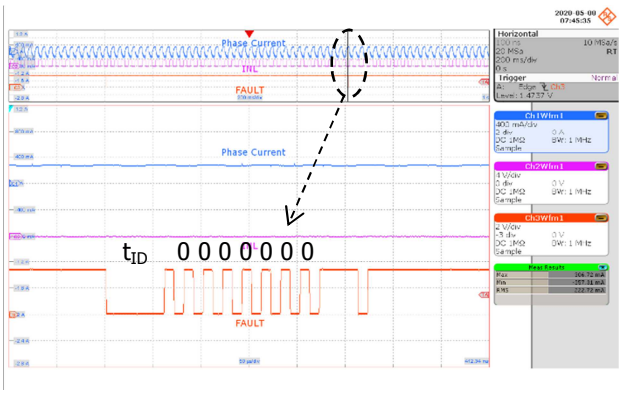

Figure 39 – External Temperature Fault Cleared.
Status Update: 000 00 0 0 (Fault Clear).
Upper: I_{MOTOR}, 400 mA / div.
Middle: V_{INL_U}, 4 V / div.
Lower: V_{FAULT}, 2 V / div., 200 ms / div.
Zoom: 50 µs / div

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.7 *Abnormal Motor Operation Tests*

This paragraph provides the results of the abnormal operation tests performed on the RDR-873 inverter board. The abnormal operation test complies with the abnormal test for appliances with motors as described in IEC 60335-1 standard (safety of household and similar electrical appliances). The abnormal operation tests cover the following:

1. Operation under stalled motor conditions
2. Operation with one motor winding disconnected
3. Running overload test

The test results demonstrate the integrated protection mechanism feature of BridgeSwitch under such abnormal operations without microcontroller intervention for protection. The motor operates at 30 W and 1000 RPM at 310 VDC input voltage for all test cases except for the overload test.

7.7.1 Operation Under Stalled (Motor) Conditions

Figure 40 and Figure 41 depict the motor phase currents and overcurrent fault flag on Phase V device when doing startup with a motor stalled condition. During start up motor stall condition, BridgeSwitch overcurrent protection will engage every restart action of the microcontroller. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. The motor is non-operational during the test with no device or motor damage during or after this test.

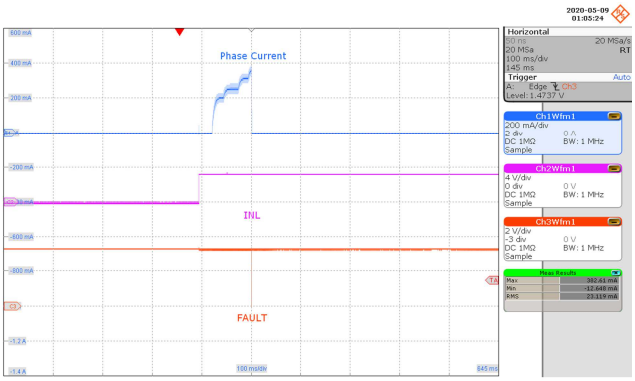

Figure 40 – Motor Stalled at Start-up Condition.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.

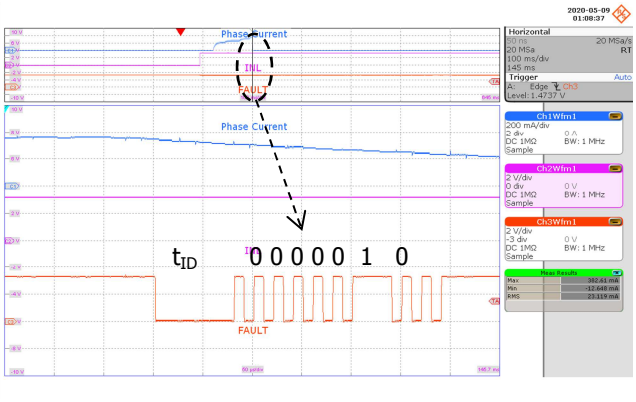

Figure 41 – Fault Flag: 000 00 0 1.
LS Overcurrent, Phase V.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

Figure 42 and 43 depict the motor phase currents and fault flags when the motor is stalled during running operation. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. BridgeSwitch limits the inverter output power to 40 W and reports over-current fault conditions when the motor current exceeds the current limit set point. The motor is non-operational with no device or motor damage during the test or after the fault is removed. With the hall sensor based control used, the microcontroller will stop providing PWM signals once hall signal transitions is lost, this can happen during motor stalled conditions.

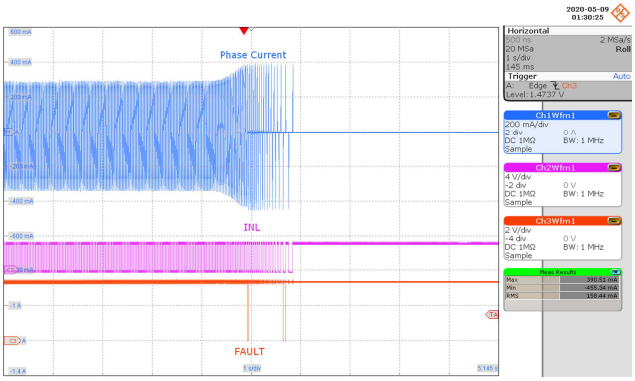

Figure 42 – Motor Stalled at Running Condition.
Multiple Overcurrent Flags Reported.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.

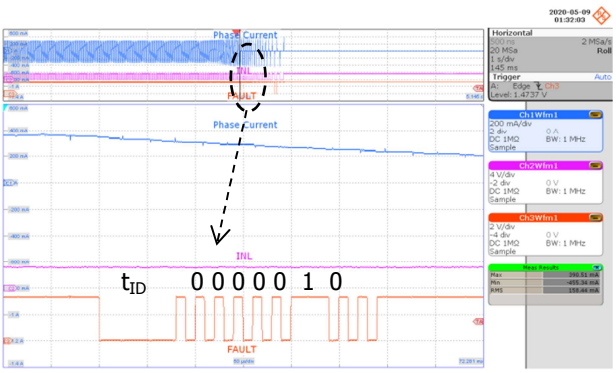

Figure 43 – Fault Flag: 000 00 1 0.
LS overcurrent, Phase V.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

7.7.2 Operation with One Motor Winding Disconnected

Figure 44 and 45 depict the motor phase currents and fault flag during operation with one motor winding disconnected. The motor will stall during this condition with no device and motor damage. BridgeSwitch will report a high-side driver not ready due to high-side bypass-pin supply discharge of the disconnected phase which happens immediately after the phase disconnection. A signal distortion in the FAULT bus signal is a result of the phase winding disconnection.

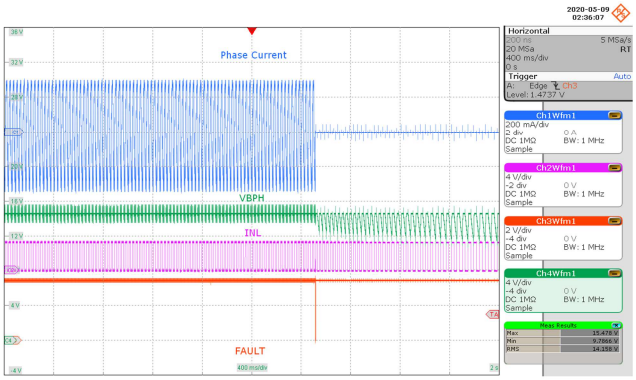

Figure 44 – Phase U Winding Disconnected.
First: I_{MOTOR}, 200 mA / div.
Second: V_{BPH_V}, 4 V / div.
Third: V_{INL_V}, 2V / div.
Fourth: V_{FAULT}, 2 V / div., 1 s / div.

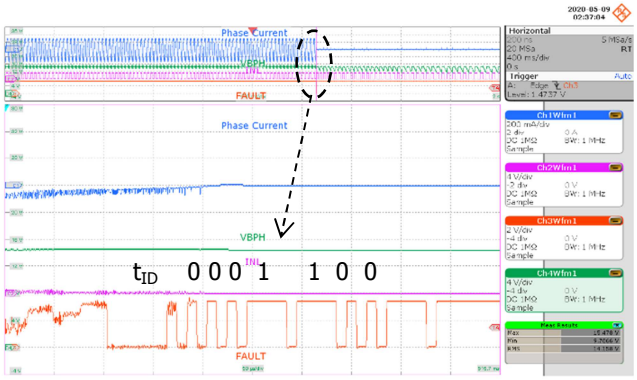

Figure 45 – Fault Flag: 000 11 0 0.
High-side Driver Not Ready, Phase U.
First: I_{MOTOR}, 200 mA / div.
Second: V_{BPH_V}, 4 V / div.
Third: V_{INL_V}, 2V / div.
Fourth: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

7.7.3 Running Overload Test

Figure 46 and Figure 47 depict the motor phase currents and status update flag during a running overload fault condition. During this test, the motor load is increased such that the current through the motor windings increases by 10% and until steady conditions are established. The load is then increased again and the test repeats until the BridgeSwitch protection engages or the motor stalls.

With the motor stalled condition, the inverter is supplied continuously for a period of 10 minutes at the rated voltage. BridgeSwitch overcurrent protection engages and reports overcurrent fault conditions during this condition. The motor operates abnormally during the condition with no device or motor damage during the test.

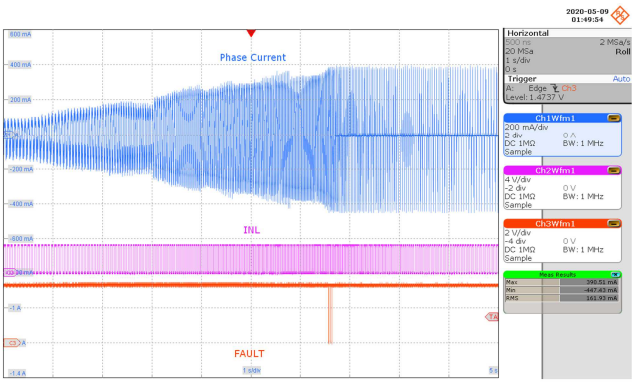

Figure 46 – Running Overload Test.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.

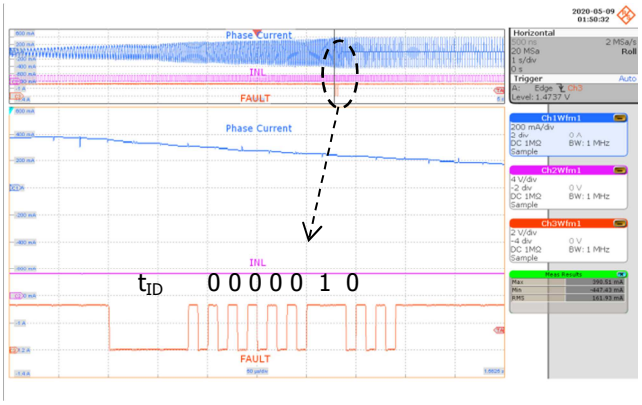

Figure 47 – First Fault Flag: 000 00 1 0.
Low-side Overcurrent, Phase V.
First: I_{MOTOR}, 200 mA / div.
Second: V_{INL_V}, 4 V / div.
Third: V_{FAULT}, 2 V / div., 1 s / div.
Zoom: 50 µs / div.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8 Appendix

8.1 *Inverter Circuit Board Manual*

Figure 48 shows locations and functions of all connectors to and from the inverter board.

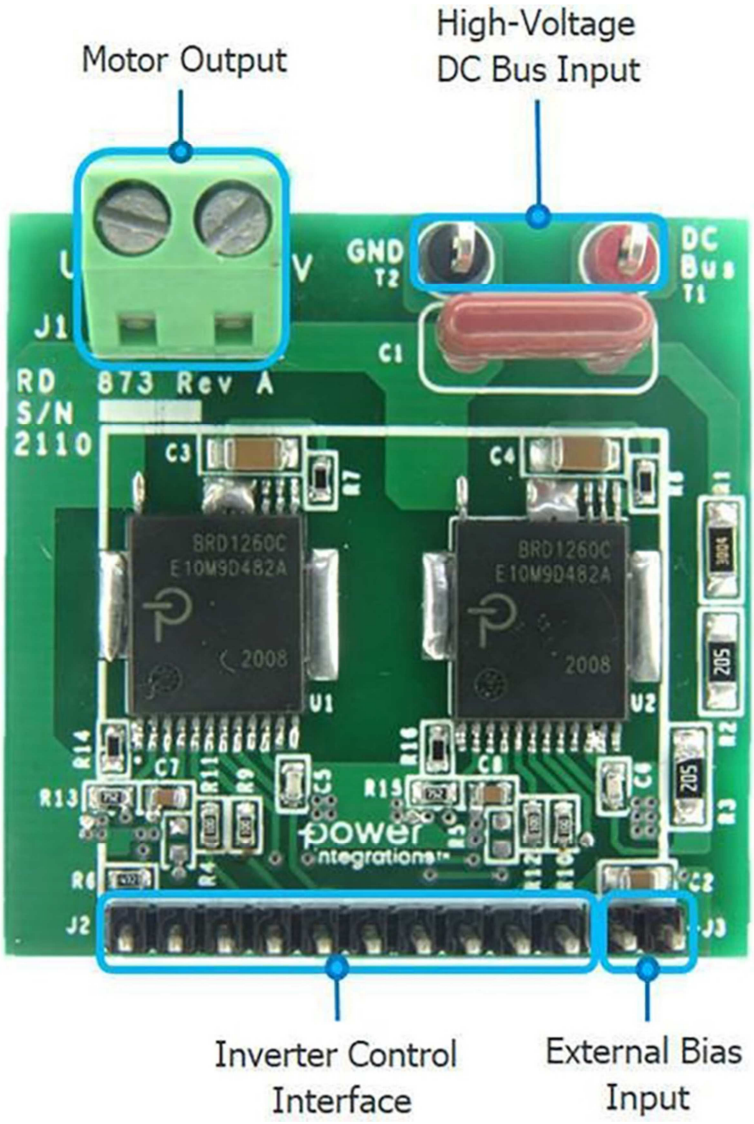

Figure 48 – Inverter Board Connections.

The high-voltage DC bus and the power ground connect to the inverter through two through-hole mount terminals, T1 and T2 respectively.

The single winding motor output connects to a 2-position screw type terminal block, J1. The half-bridge output of device U1 connects to one of its terminal labeled U while the half-bridge output of device U2 connects to the other terminal labeled V.

The inverter control interface which consists of control input signals, system sensing input, instantaneous phase current output and the single wire status update communication bus connect to the test system through 10-position header breakaway connectors, J2. Figure 49 depicts the physical dimensions and pin numbers.

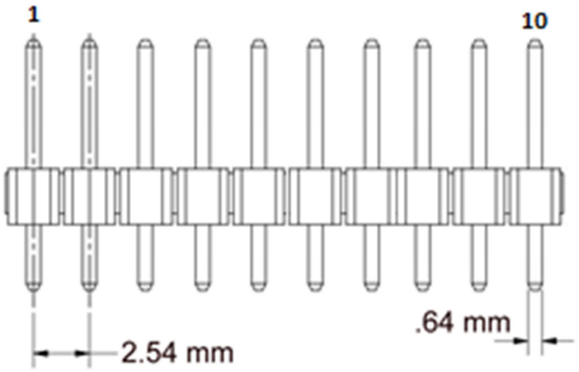

Figure 49 – Inverter Control Interface Connector (J2).

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

Table 5 lists the pin assignments on the inverter control interface connector, J2.

Pin No.	Signal	Type	Comments
1	VDD	Input	Pull-up supply for communication bus, 3.3 V ±5% or 5 V ±5% compatible
2	FAULT	Input/Output	Single wire, bi-directional communication bus (open-Drain architecture)
3	IPH_U	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current of Phase U device (U1), 3 V per 1 A Drain current signal ratio
4	INL_U	Input	Gate drive signal for low-side power FREDFET of Phase U device (U1), active high, 3.3 V or 5 V CMOS compatible
5	/INH_U	Input	Gate drive signal for high-side power FREDFET of Phase U device (U1), active low, 3.3 V or 5 V CMOS compatible
6	SM	Input	External input for system sensing (i.e. can be connected to external thermistor for system temperature monitor via status communication bus)
7	IPH_V	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current of Phase V device (U2), 3 V per 1 A Drain current signal ratio
8	INL_V	Input	Gate drive signal for low-side power FREDFET of Phase V device (U2), active high, 3.3 V or 5 V CMOS compatible
9	/INH_V	Input	Gate drive signal for high-side power FREDFET of Phase V device (U2), active low, 3.3 V or 5 V CMOS compatible
10	Ground	n/a	Reference for connector input and output signals and system microcontroller

Table 5 – Inverter Control Interface Connector Pin Assignments.

The inverter board permits optional external supply operation from a single-rail 17 V DC supply. The external supply input connects to the inverter through a two-position header connector, J3. The positive input should connect to the terminal besides the "+" label on-board. Figure 50 depicts physical dimension of connector J3.

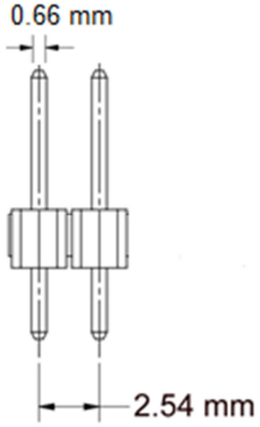

Figure 50 – External Supply Input Connector (J3).

8.2 *Status Word Encoding*

The 7-bit word followed by a parity bit encodes the status communication bus information. Table 6 summarizes encoding of various status updates the device may communicate to the system micro-controller. The status word consists of five blocks with status changes grouped together that cannot occur at the same time. This enables simultaneous reporting of multiple status updates to the system micro-controller without having to take care about fault priorities and a fault-reporting queue.

The last row (7-bit word “000 00 0 0”) encodes Device Ready status and is used to communicate a successful power-up sequence to the system, communicated when a certain fault is cleared and sent it to acknowledge a status request the system MCU in case no fault is present.

FAULT	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
HV bus OV	0	0	1				
HV bus UV 100%	0	1	0				
HV bus UV 85%	0	1	1				
HV bus UV 70%	1	0	0				
HV bus UV 55%	1	0	1				
System thermal fault	1	1	0				
LS Driver not ready[1]	1	1	1				
LS FET thermal warning				0	1		
LS FET thermal shutdown				1	0		
HS Driver not ready[2]				1	1		
LS FET over-current						1	
HS FET over-current							1
Device Ready (no faults)	0	0	0	0	0	0	0

Notes:
1. Includes XL-pin open/short circuit fault, IPH pin to XL pin short circuit, and trim bit corruption
2. Includes HS-to-LS communication loss, V_{BPH} or internal 5 V rail out of range, and XH pin open/short-circuit fault

Table 6 – Status Word Encoding.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.3 *Test Bench Set-up*

Figure 51 depicts the test bench used to gather the performance data presented in this report.

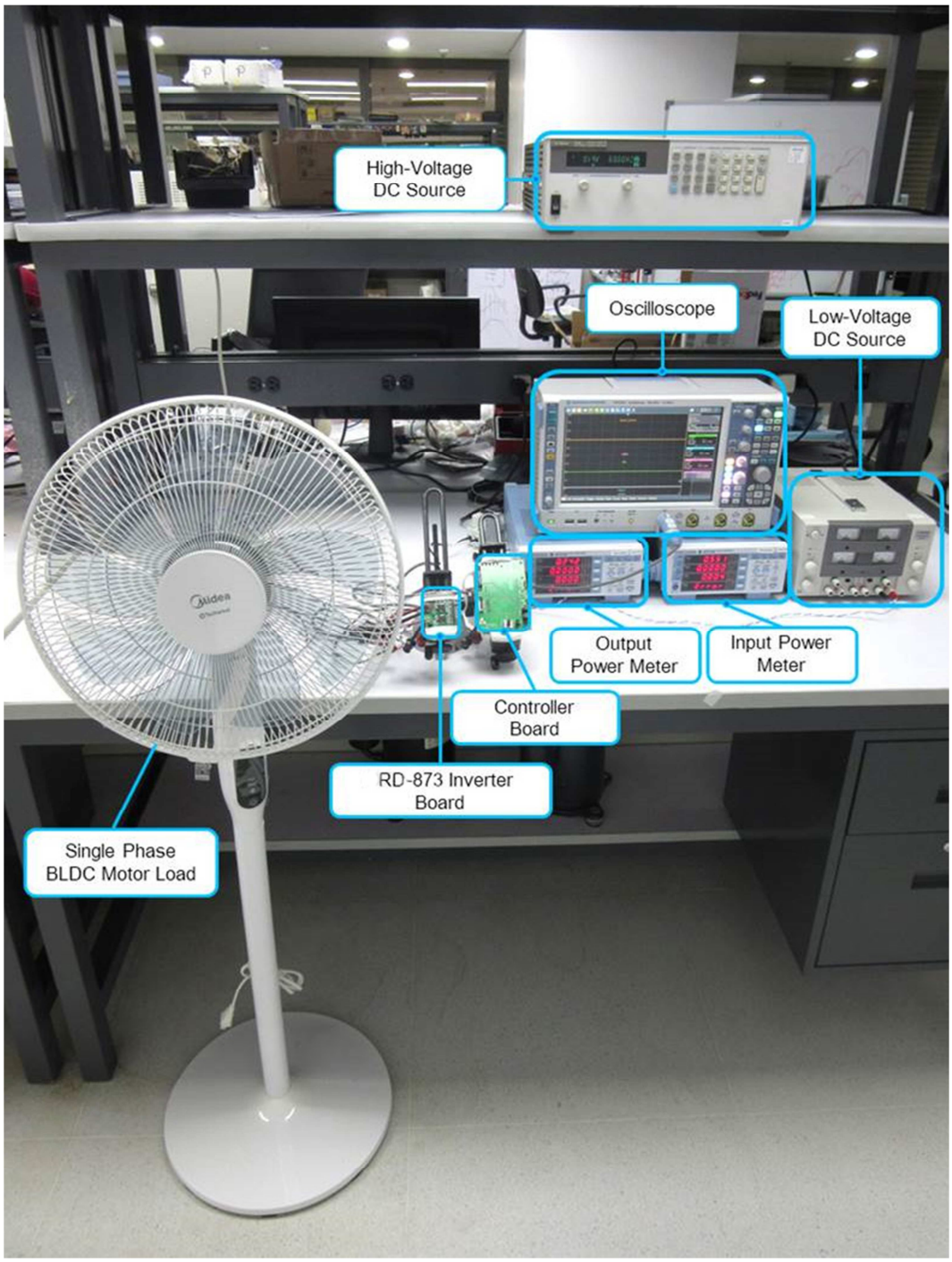

Figure 51 – Test Bench Set-up.

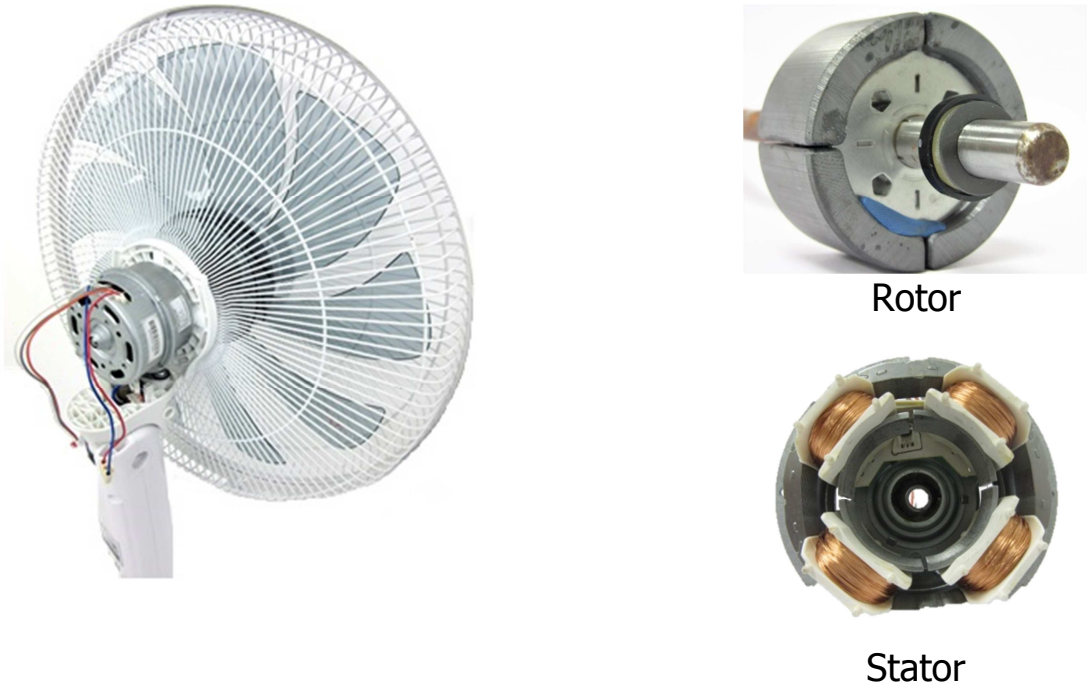

Figure 52 – Single-Phase Motor Load and the Motor Internal Structure.

Table 7 lists the model/specifications for each item in the test bench set-up.

Test Bench Setup Item	Model/Specification
High-voltage DC Source	Keysight 6313B
Low-voltage DC Source	Topward 6303A
Oscilloscope	Rohde & Schwarz RTO-2004 4-channel 600 MHz
Input Power Meter	Yokogawa WT310
Output Power Meter	Yokogawa WT310
Inverter Board	RDR-873
Controller Board	Cypress PSoC 4 Pioneer Kit MCU Board
Single-Phase Motor Load	Midea Electric Fan Motor (FS40-18AR) – Single-Phase BLDC Motor 4-slot, 4-pole, 25 W, 1000 RPM

Table 7 – Test Bench Setup Details.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.4 *Inverter Power Measurements*

The inverter efficiency measurements used the input and output wattmeter connection illustrated in Figure 53 below.

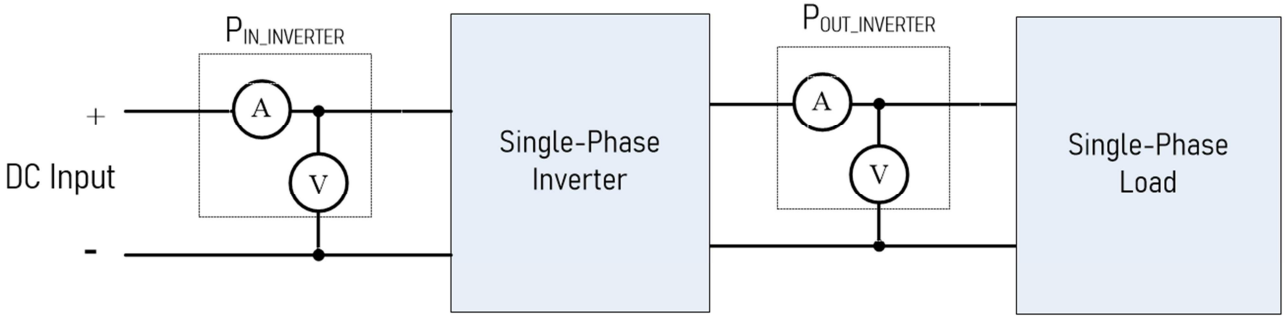

Figure 53 – Inverter Power Measurement Diagram.

8.5 *Current Capability vs. Ambient Temperature*

Figure 54 depicts the continuous RMS current capability of the RDR-873 inverter board running on the same control scheme at 18 kHz high-side PWM frequency with 310 VDC input. The plots show two derating curves with two BRD1260C devices operating either self-supplied or externally supplied at the respective BPL-pins. Each curve details the available continuous RMS current at different board ambient temperatures with a package temperature of 100 °C.

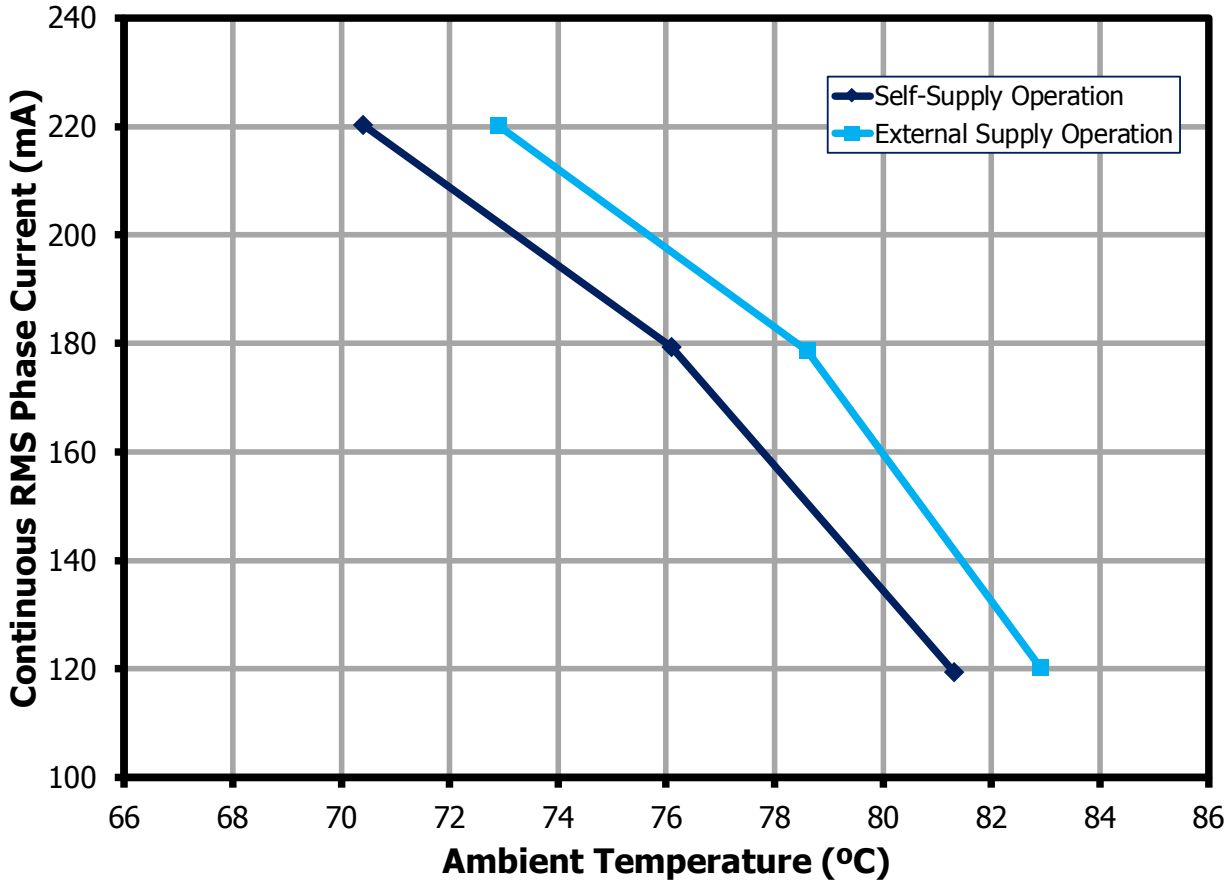

Figure 54 – Current Capability vs. Ambient Temperature (Max. 100 °C Package Temperature).

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.6 *Motor Control Algorithm*

The control algorithm presented in the report is based on a hall sensor commutation control strategy. Alternating current drive is applied to the motor winding during each cycle facilitated through the high-side and low-side switch of the two half-bridges. Consequently, the high-side switch is pulse width modulated at 18 kHz carrier frequency to enable motor speed control. Figure 55 depicts the commutation timing diagram.
(Note: BridgeSwitch low-side control input (INL) is active HIGH and high-side control input (/INH) is active LOW)

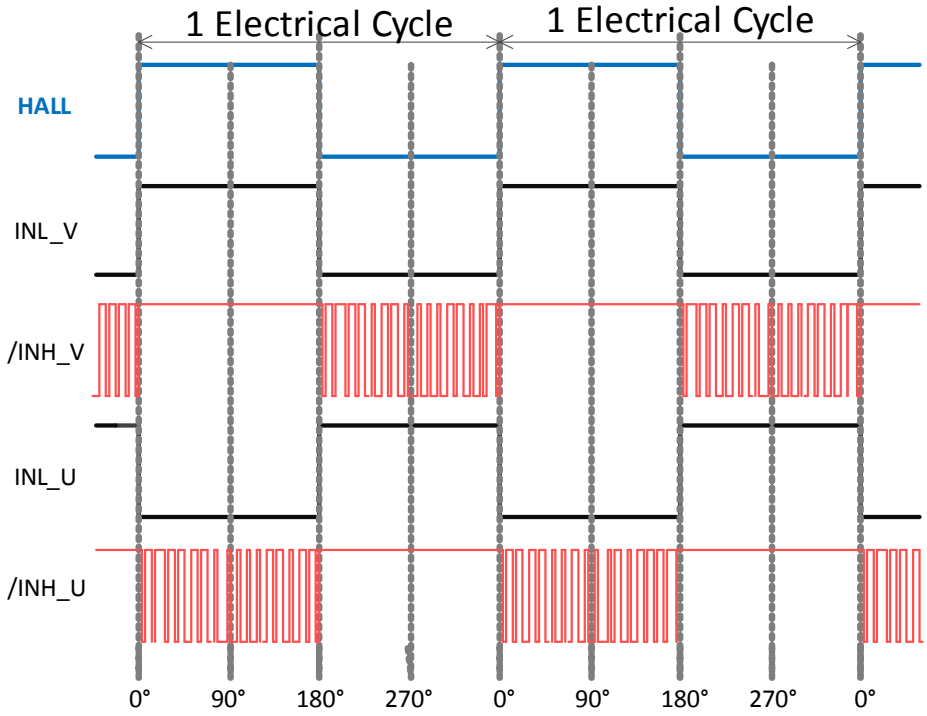

Figure 55 – Motor Control Commutation Timing Diagram.

The PWM control implements a modulation scheme based on the actual motor back-emf shape. Figure 56 depicts the actual back-emf shape of the motor load at the same time , Figure 57 depicts a trapezoidal 12-bit duty cycle pattern applied on the high-side switch during each commutation sequence. In this document, the control algorithm is referred as "trapezoidal control scheme".

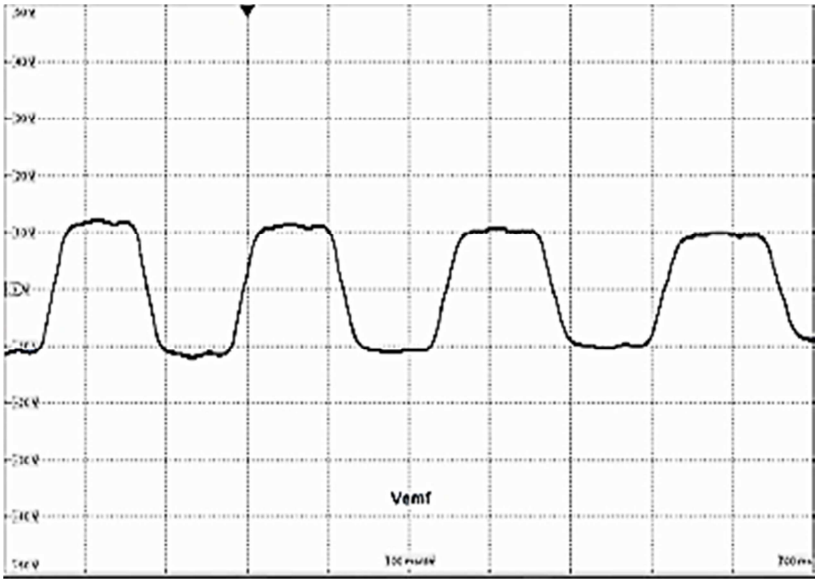

Figure 56 – Actual Motor Load Back-Emf Shape.

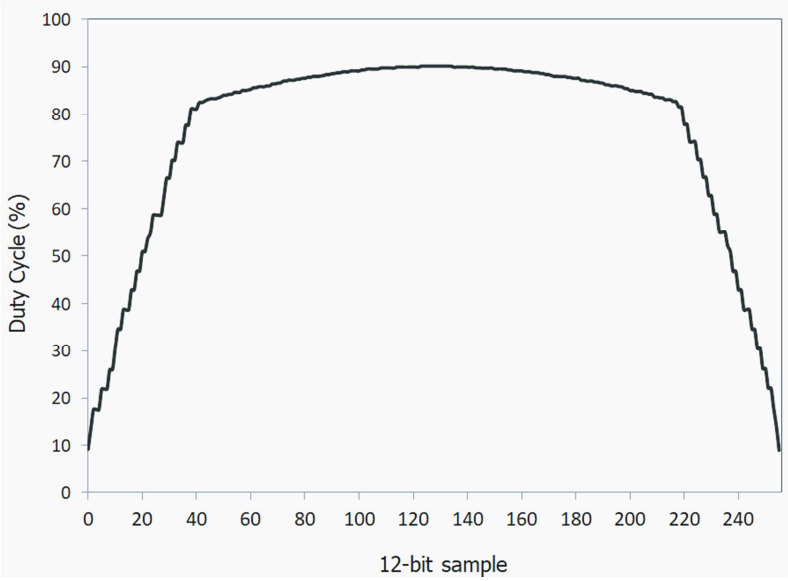

Figure 57 – PWM Duty Cycle Pattern.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

8.7 *Complementary PWM Signal Operation*

BridgeSwitch ICs are well suited for complementary PWM signal operation because of the reverse polarity of the two control inputs. Low-side control input INL is active high and high-side control input /INH is active low. This allows tying both control inputs together and driving them with a single complementary PWM signal. Benefits of such a drive scheme are reduced micro-controller pin count and a simplified PCB layout.

Figure 58 depicts the complementary PWM implementation with BridgeSwitch in a single-phase inverter. Adding an external pull-down resistor R_{PD} in complementary PWM drive mode prevents possible accidental noise induced FREDFET switching. The recommended value is 10 kΩ to 100 kΩ.

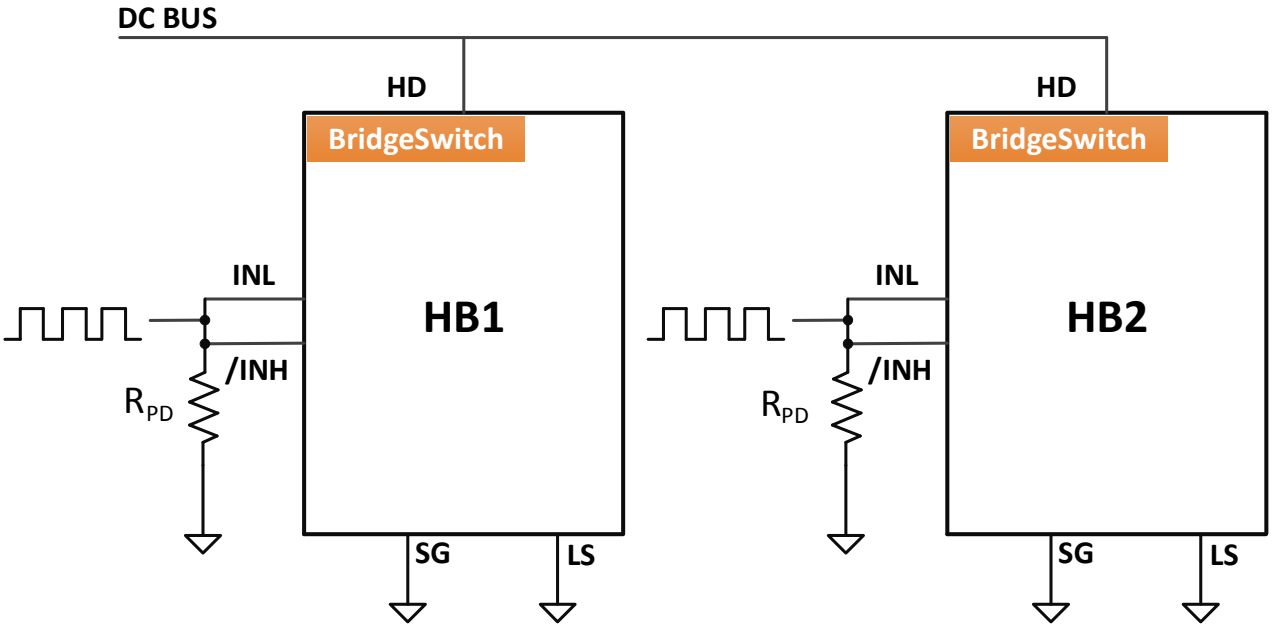

Figure 58 – Complementary PWM Signal Implementation with BridgeSwitch Inverter.

Figure 59 depicts the corresponding complementary PWM control commutation timing diagram where each respective half-bridge INL and /INHs inputs are driven with a single PWM signal. Consequently, Figure 60 and Figure 61 provide the actual complementary PWM mode operation with RDR-873 in trapezoidal control scheme.

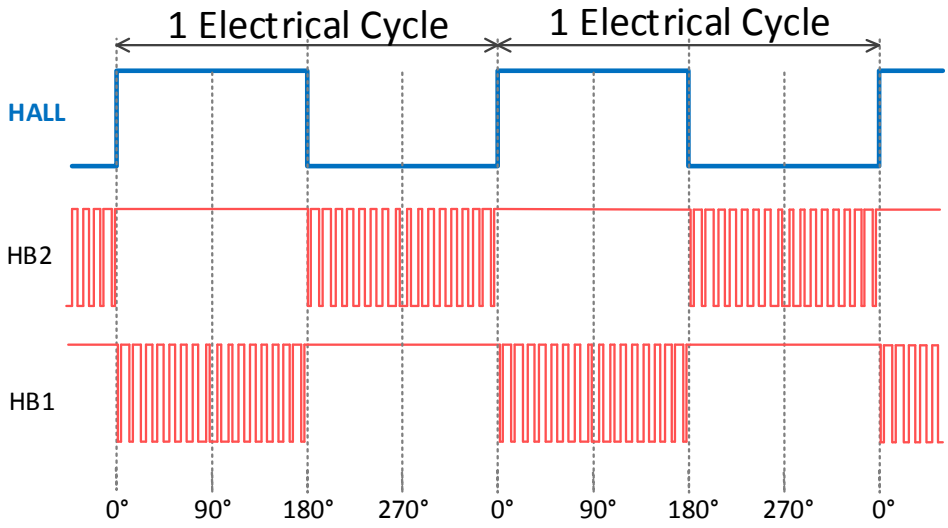

Figure 59 – Complementary PWM Control Commutation Timing Diagram with BridgeSwitch Inverter.

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com

The following waveform plots illustrate the complementary PWM mode operation with the RDR-873 reference design operating at 310 VDC bus and 0.22 A_{RMS} inverter load current. Its respective phase high-side PWM output drives the combined INL and /INH logic input of BridgeSwitch.

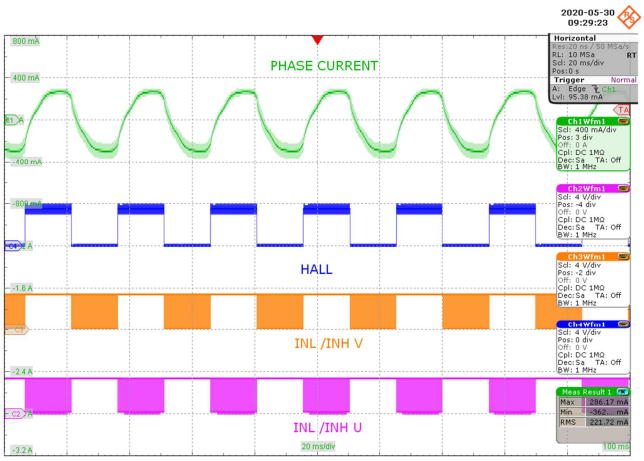

Figure 60 – Control Inputs, Motor Current and Hall Sensor Signal.
First: I_{MOTOR}, 400 mA / div.
Second: V_{HALL}, 4 V / div.
Third: $V_{INL/INH\ V}$, 4 V / div.
Fourth: $V_{INL/INH\ U}$, 4 V / div.
Time Scale: 20 ms / div.

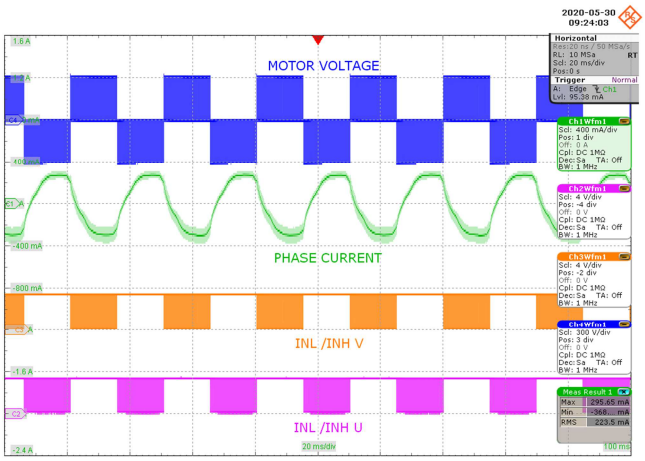

Figure 61 – Control Inputs, Motor Current and Motor Winding Voltage.
First: V_{HB}, 300 V / div.
Second: I_{MOTOR}, 400 mA / div.
Third: $V_{INL/INH\ V}$, 4 V / div.
Fourth: $V_{INL/INH\ U}$, 4 V / div.
Time Scale: 20 ms / div.

9 Revision History

Date	Author	Revision	Description & Changes	Reviewed
23-Mar-21	JHP	1.2	Initial Release	Apps & Mktg

Power Integrations, Inc.
Tel: +1 (408) 414-9200
www.power.com