READ2304G

High Drivability & High Slew Rate, Input Output Full Range, CMOS Dual Operational Amplifier

R03DS0159EJ0100
Rev.1.00
2020.08.20

V_{IO}≤±6mV, SR = 8V/μs , GBW=6MHz

Description

The READ2304G is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40˚C to +105˚C.

Available in ultra-small 8 pins TSSOP and MSOP packages.

Features

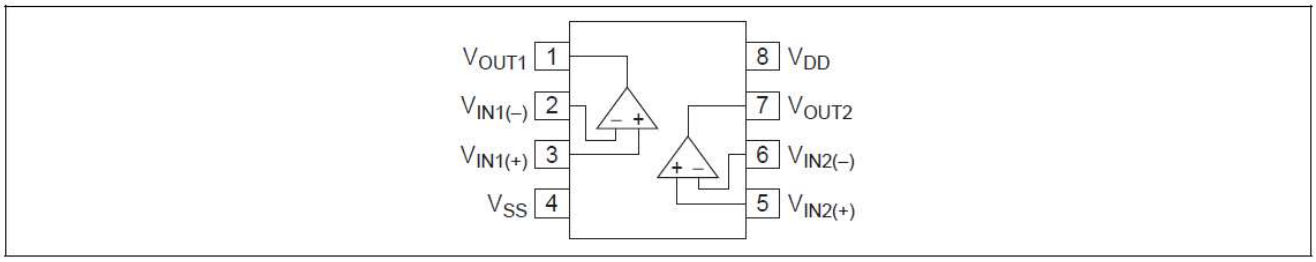
- Low voltage single supply operation — V_{DD} = 2.5V to 5.5V
- Low input offset voltage — V_{IO} ≤ ±6.0mV
- Low input bias current — I_B ≤ (1pA).
- Wide output voltage range — V_{OUT} : V_{SS}+0.1V to V_{DD}-0.1V(@Io=5mA)
- Supply current (per channel) — I_{DD} = 0.75mA Typ.
- High slew rate — SR = 8V/μs Typ.

( ) reference value of design

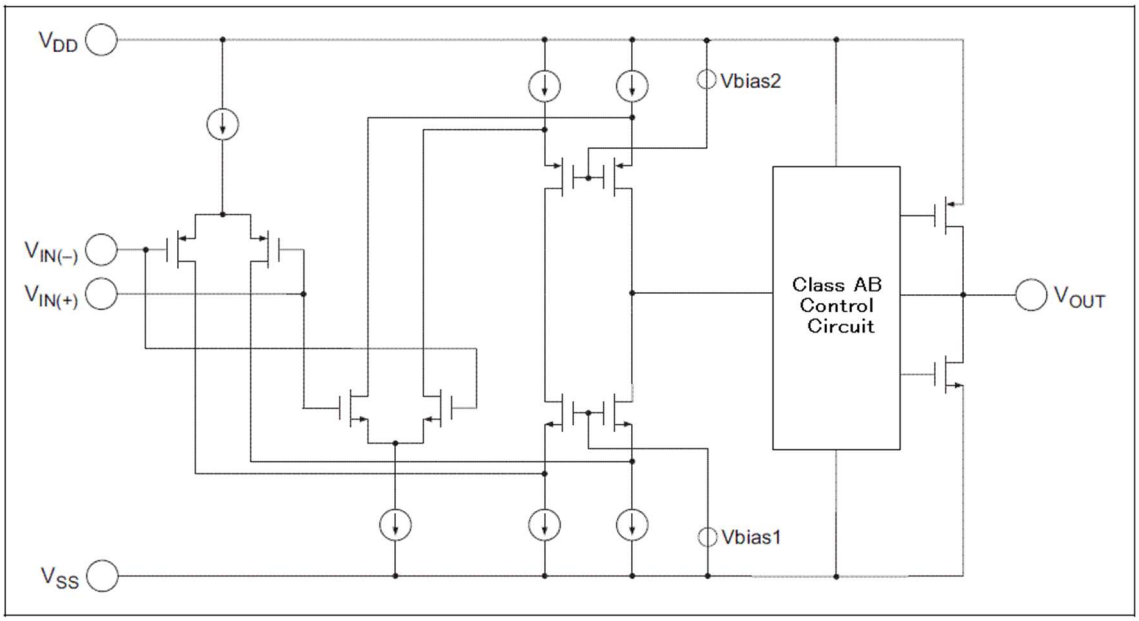
Product Line-up

Type name	Product type quality level	Package
READ2304GSP	High slew rate with Normal quality level	8 pins plastic TSSOP
READ2304GSN	High slew rate with Normal quality level	8 pins plastic MSOP

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T_A=25˚C>

Items	Symbol	Ratings	Unit
Supply voltage Note.1	V_{DD}	-0.3 to +6.5	V
Differential input voltage	V_{ID}	$-V_{DD}$ to $+V_{DD}$	V
Input voltage Note.2	V_I	-0.3 to V_{DD} +0.3	V
Maximum output current	I_O	20	mA
Power dissipation Note.3	P_T	440	mW
Junction temperature	T_j	+150	˚C
Operating temp. range	T_A	-40 to +105	˚C
Storage temp. range	T_{stg}	-55 to +150	˚C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm x 100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ2304GSP: Derate at -5.5 mW/˚C when T_A > 69 ˚C

(Junction – ambient thermal resistance $R_{th(J-A)}$ = 183 ˚C/W)

READ2304GSN: Derate at -4.8 mW/˚C when T_A > 58 ˚C

(Junction – ambient thermal resistance $R_{th(J-A)}$ = 208 ˚C/W)

Electrical Characteristics

<V_{DD}=5V, T_A= +25˚C>

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply voltage	V_{DD} − V_{SS}	2.5		5.5	V	
Input offset voltage	V_{IO}			±6.0	mV	
Input offset current	I_{IO}			(1)	pA	
Input bias current	I_B			(1)	pA	
Output high voltage	V_{OH}	V_{DD}-0.2			V	I_L = 10mA
Output low voltage	V_{OL}			V_{SS}+0.2	V	I_L = 10mA
Voltage gain	A_V	60	90		dB	R_L≥100kΩ
Channel supply current	I_{DD}/ch		0.75	1.5	mA	R_L=∞, I_O=0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}	V	
Gain bandwidth product	GBW		6		MHz	C_L=20pF
Slew rate	SR		8		V/us	C_L=20pF

( ) reference value of design

Notes

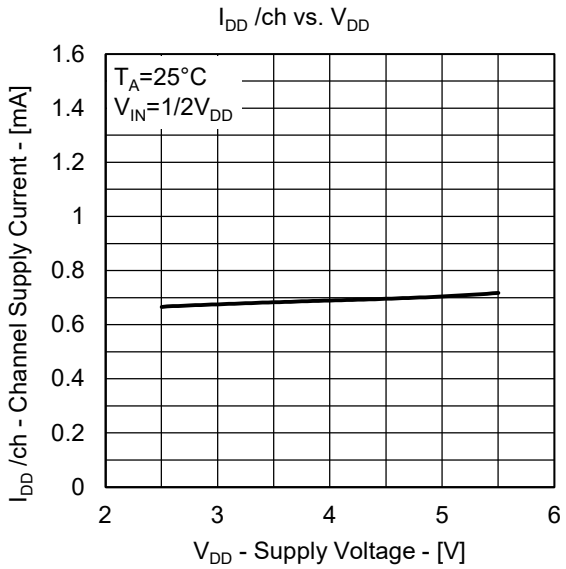
Output terminal: The over-current protection feature is not built in the output terminal of this product.

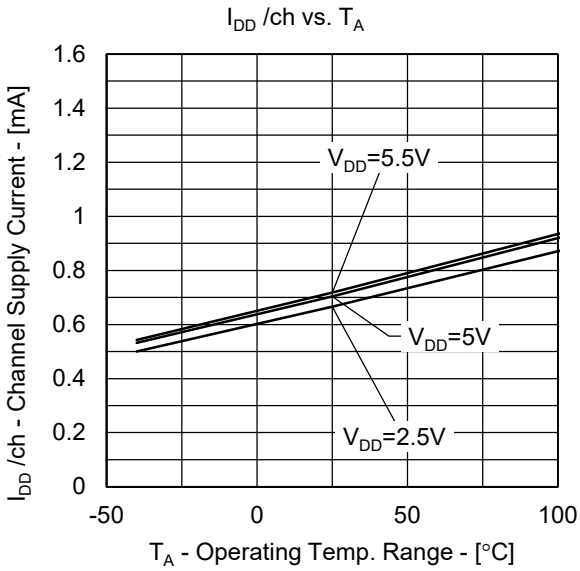
Therefore, please insert resistance to output port.

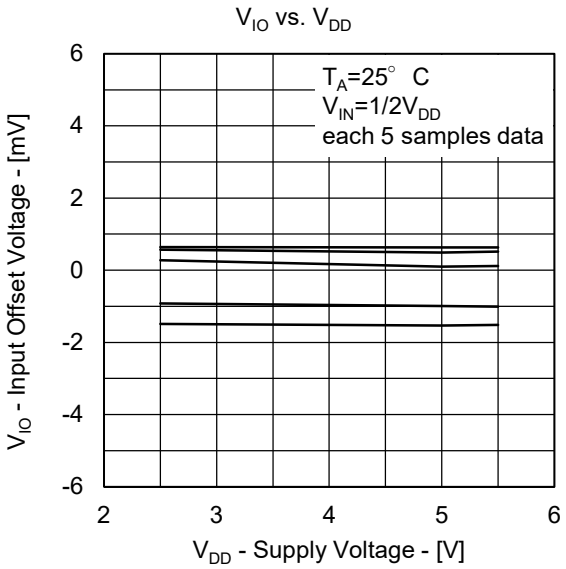
Input offset voltage : The amplifier circuit of the first block of operational amplifier.

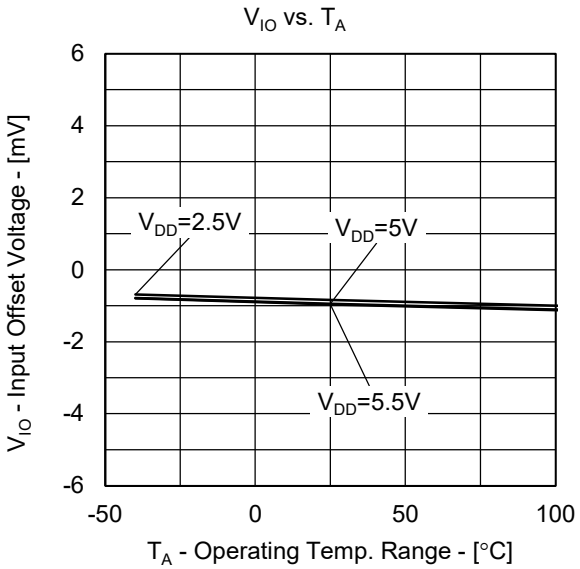
A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply. In case of input voltage of overlap point output port has a minute voltage shift or distortion.

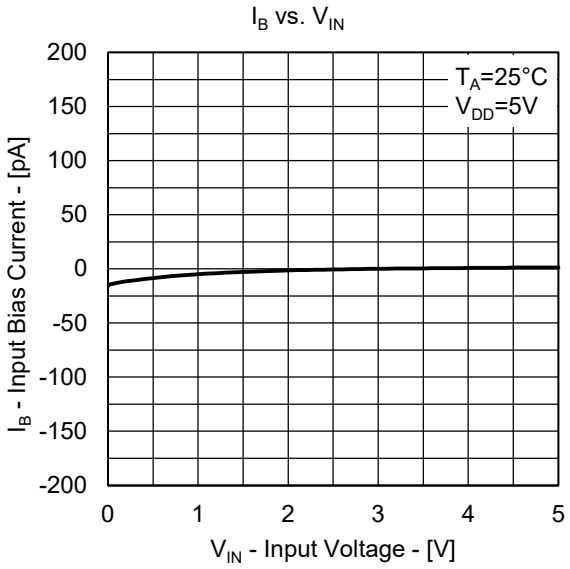
Electrical Characteristics

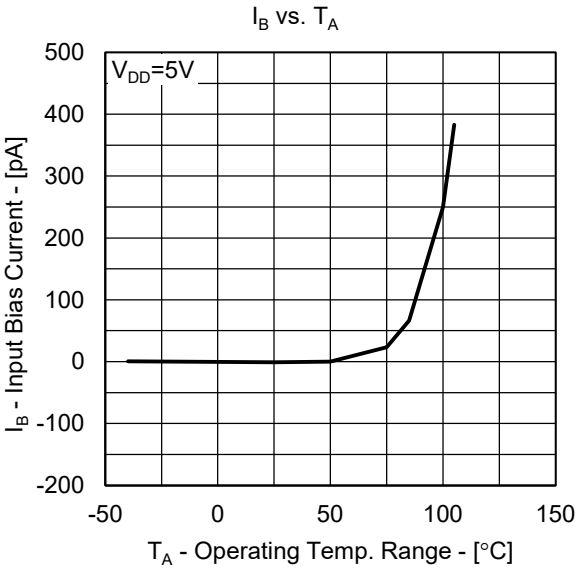


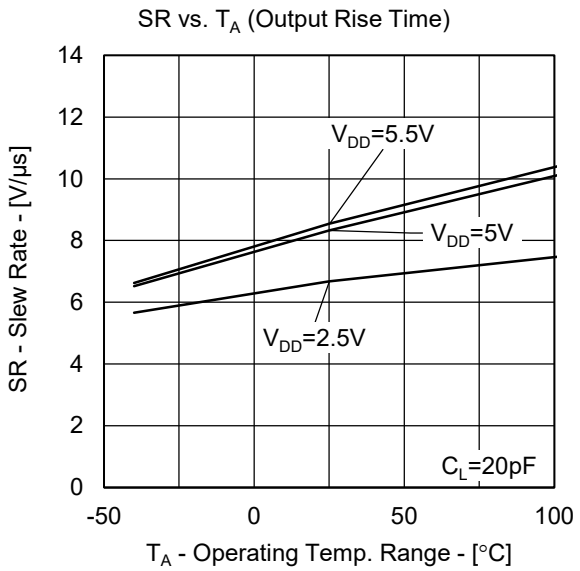


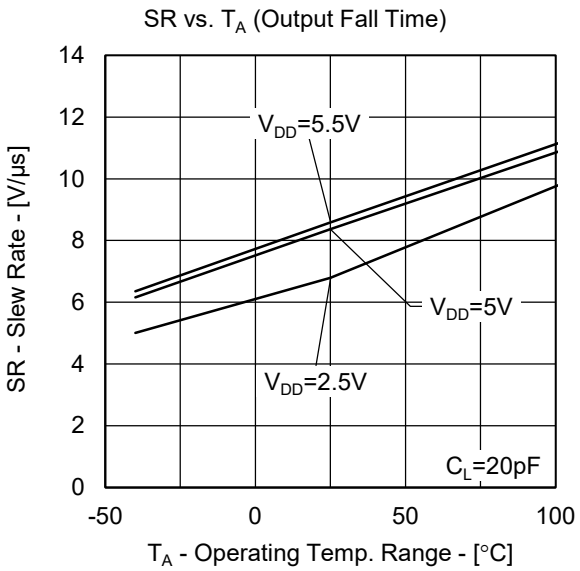









SR vs. T_A (Output Rise Time)
SR - Slew Rate - [V/µs]
T_A - Operating Temp. Range - [°C]
V_{DD}=5.5V
V_{DD}=5V
V_{DD}=2.5V
C_L=20pF
14
12
10
8
6
4
2
0
-50
0
50
100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12
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2
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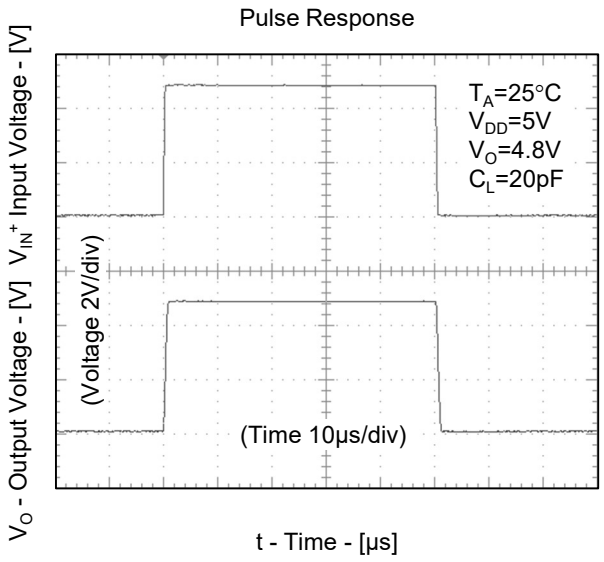
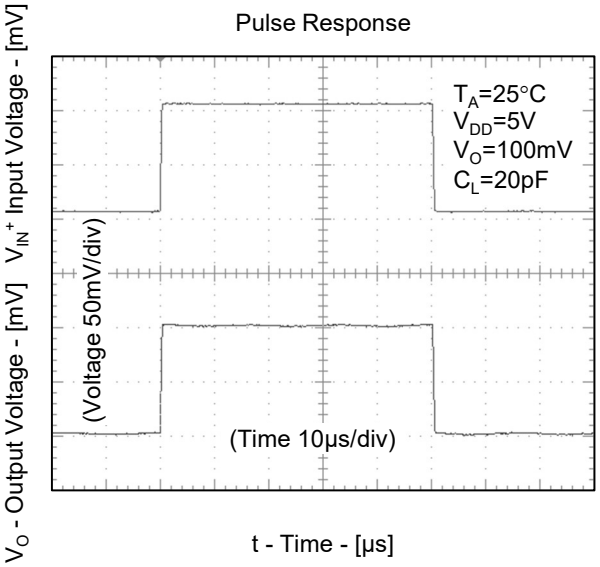
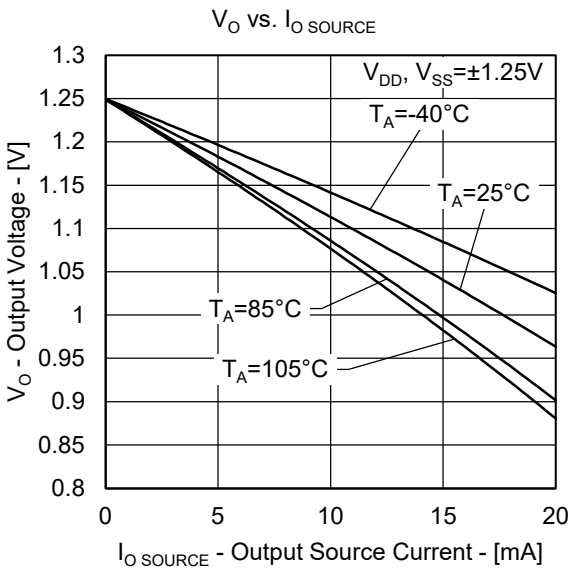
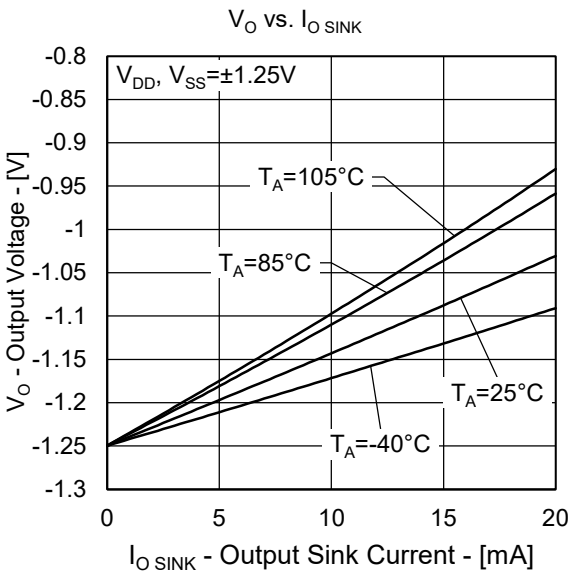
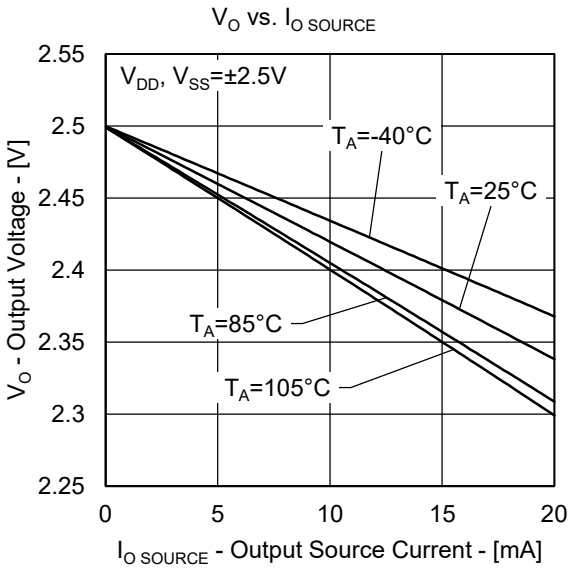
-50
0
50
100

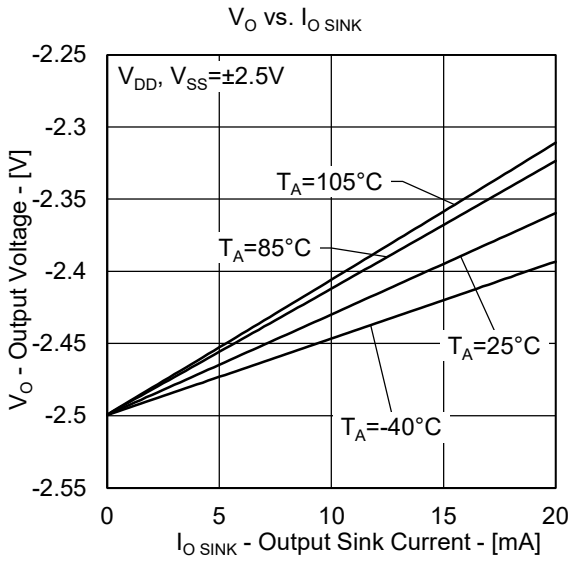

Pulse Response
V_O - Output Voltage - [V] V_{IN}^+ Input Voltage - [V]
(Voltage 2V/div)
(Time 10µs/div)
T_A=25°C
V_{DD}=5V
V_O=4.8V
C_L=20pF
t - Time - [µs]

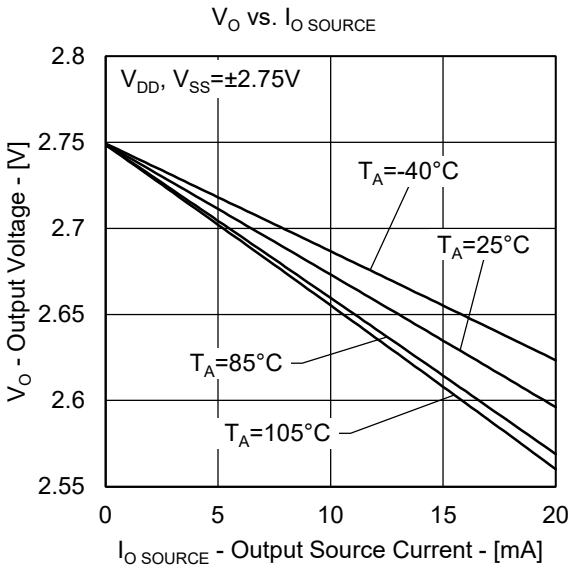

Pulse Response
V_O - Output Voltage - [mV] V_{IN}^+ Input Voltage - [mV]
(Voltage 50mV/div)
(Time 10µs/div)
T_A=25°C
V_{DD}=5V
V_O=100mV
C_L=20pF
t - Time - [µs]

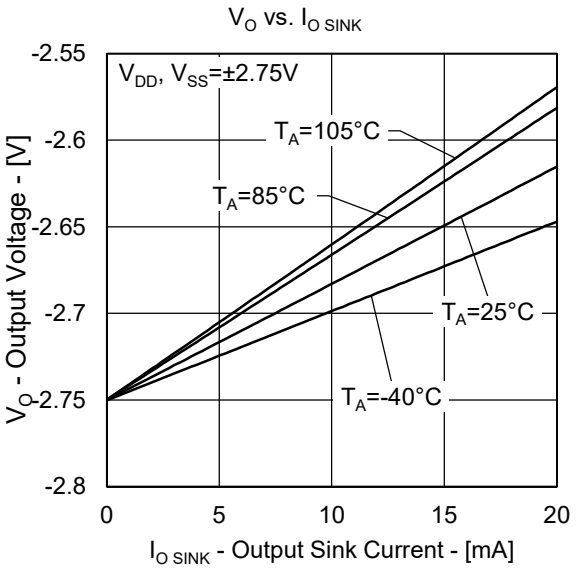

VO vs. IO SOURCE
VDD, VSS=±1.25V
TA=-40°C
TA=25°C
TA=85°C
TA=105°C
VO - Output Voltage - [V]
IO SOURCE - Output Source Current - [mA]

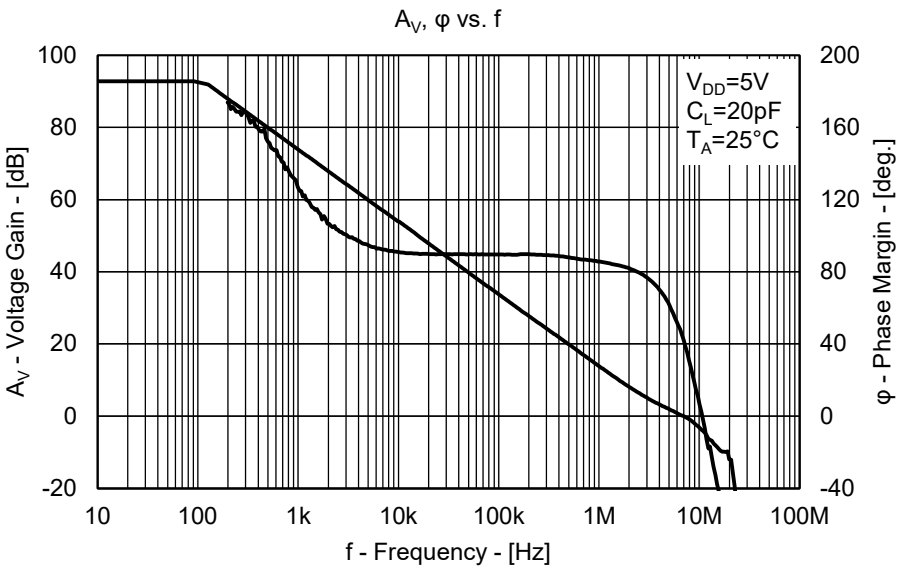

VO vs. IO SINK
VDD, VSS=±1.25V
TA=105°C
TA=85°C
TA=25°C
TA=-40°C
VO - Output Voltage - [V]
IO SINK - Output Sink Current - [mA]

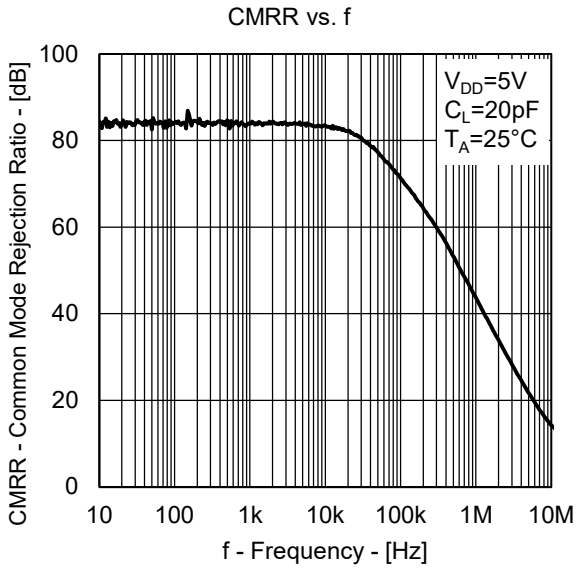

VO vs. IO SOURCE
VDD, VSS=±2.5V
TA=-40°C
TA=25°C
TA=85°C
TA=105°C
VO - Output Voltage - [V]
IO SOURCE - Output Source Current - [mA]

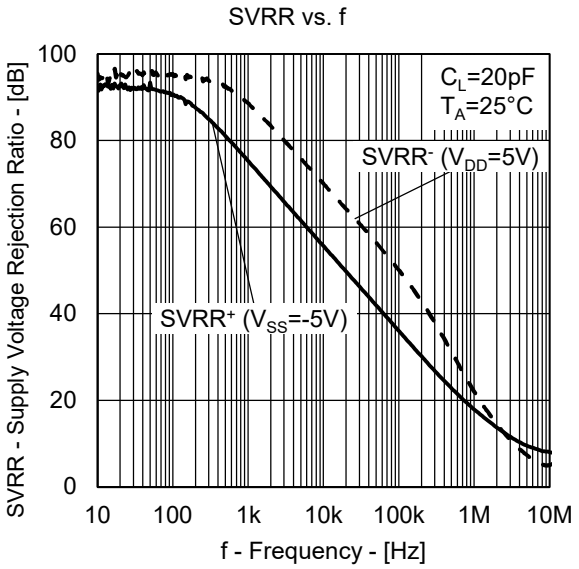

VO vs. IO SINK
VDD, VSS=±2.5V
TA=105°C
TA=85°C
TA=25°C
TA=-40°C
VO - Output Voltage - [V]
IO SINK - Output Sink Current - [mA]

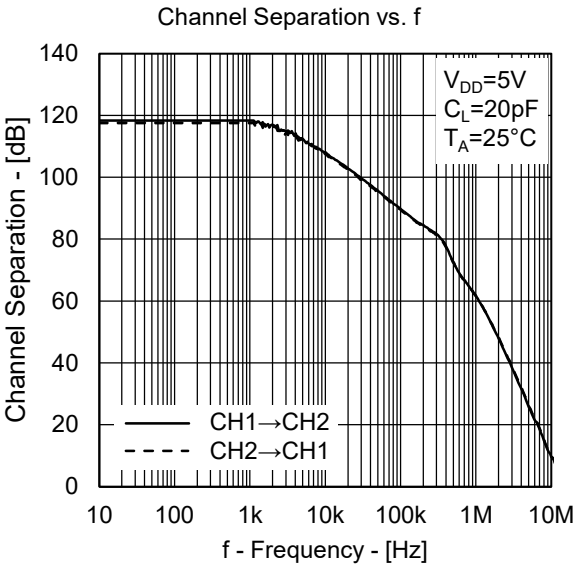

VO vs. IO SOURCE
VDD, VSS=±2.75V
TA=-40°C
TA=25°C
TA=85°C
TA=105°C
VO - Output Voltage - [V]
IO SOURCE - Output Source Current - [mA]

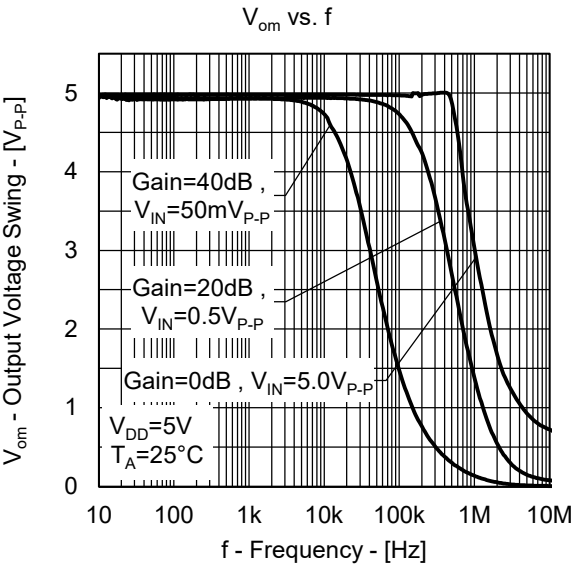

VO vs. IO SINK
VDD, VSS=±2.75V
TA=105°C
TA=85°C
TA=25°C
TA=-40°C
VO - Output Voltage - [V]
IO SINK - Output Sink Current - [mA]


A_V, φ vs. f
V_{DD}=5V
C_L=20pF
T_A=25°C
A_V - Voltage Gain - [dB]
φ - Phase Margin - [deg.]
f - Frequency - [Hz]


CMRR vs. f
V_{DD}=5V
C_L=20pF
T_A=25°C
CMRR - Common Mode Rejection Ratio - [dB]
f - Frequency - [Hz]


SVRR vs. f
C_L=20pF
T_A=25°C
SVRR⁻ (V_{DD}=5V)
SVRR⁺ (V_{SS}=-5V)
SVRR - Supply Voltage Rejection Ratio - [dB]
f - Frequency - [Hz]


Channel Separation vs. f
V_{DD}=5V
C_L=20pF
T_A=25°C
CH1→CH2
CH2→CH1
Channel Separation - [dB]
f - Frequency - [Hz]

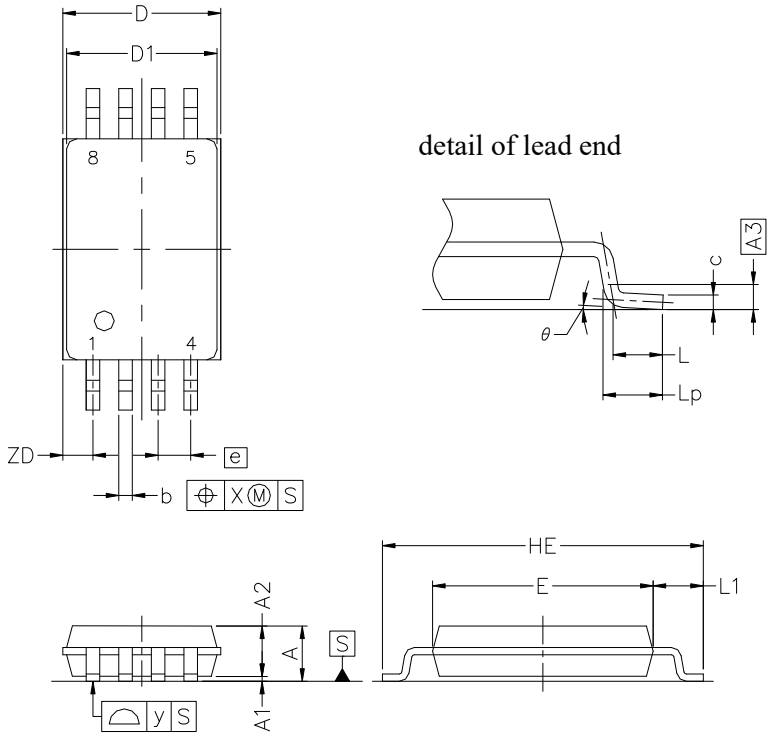

V_{om} vs. f
Gain=40dB , V_{IN}=50mV_{P-P}
Gain=20dB , V_{IN}=0.5V_{P-P}
Gain=0dB , V_{IN}=5.0V_{P-P}
V_{DD}=5V
T_A=25°C
V_{om} - Output Voltage Swing - [V_{P-P}]
f - Frequency - [Hz]

Package Dimensions

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—

Unit:mm



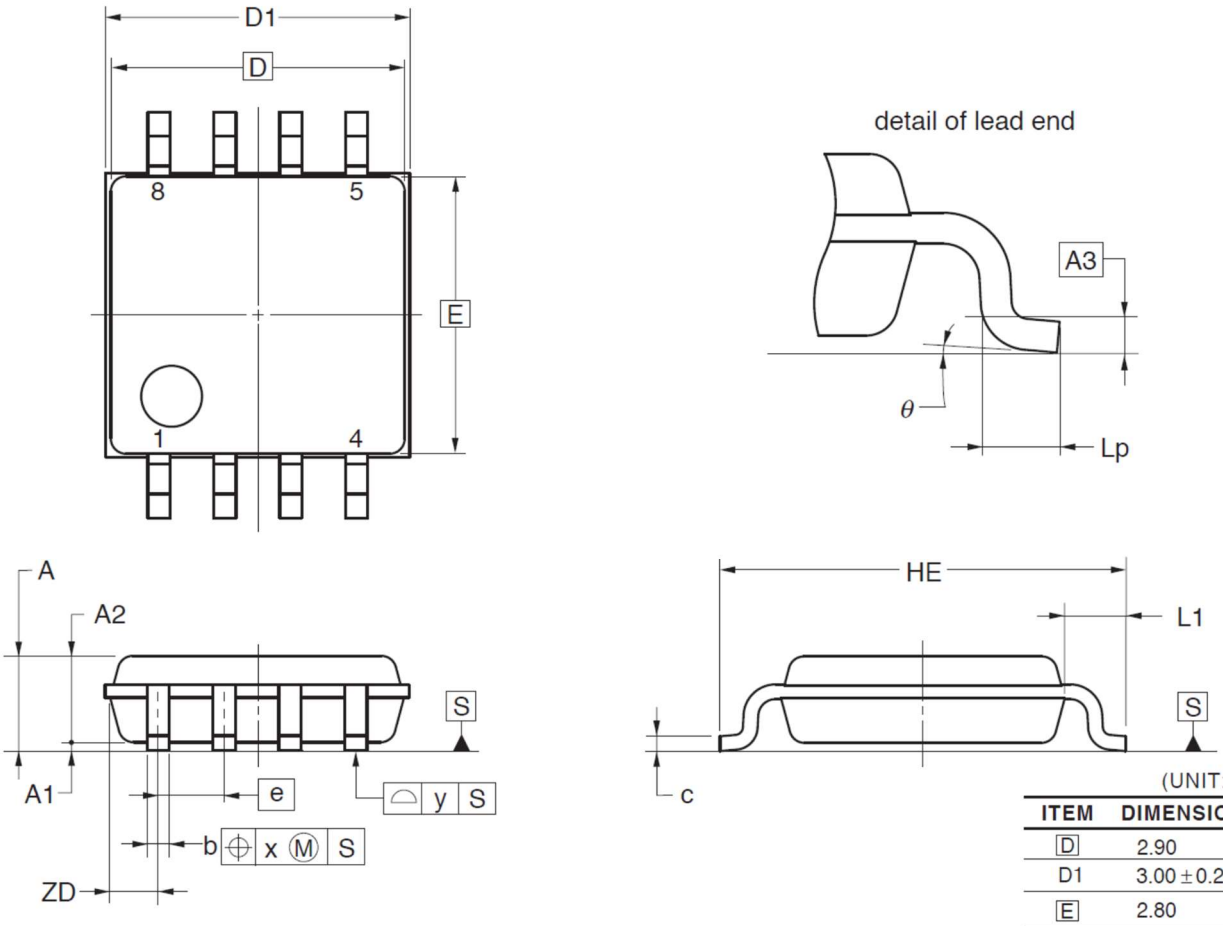
ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 +0.06 -0.05
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
e	0.65
x	0.10
y	0.10
ZD	0.60

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

8-PIN PLASTIC MSOP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-TSSOP8-2.8x2.9-0.65	PTSP0008JF-A	P8MP-65-KAA-1	0.02



(UNIT:mm)

ITEM	DIMENSIONS
D	2.90
D1	3.00 ± 0.20
E	2.80
HE	4.00 ± 0.20
e	0.65
b	0.22 ± 0.05
A	1.03 MAX.
A1	0.08 ± 0.05
A2	0.85 ± 0.05
A3	0.25
L1	0.60 ± 0.20
c	$0.145^{+0.05}_{-0.03}$
Lp	0.37 ± 0.10
x	0.10
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.525

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.