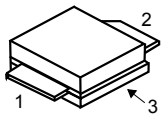
RF2L16080CF2

Datasheet

80 W, 28 V, 1.3 to 1.7 GHz RF power LDMOS transistor



A2

Pin connection	
Pin	**Connection**
1	Gate
2	Drain
3	Source (bottom side)

Product status link
RF2L16080CF2

Product summary	
Order code	RF2L16080CF2
Marking	2L16080
Package	A2
Packing	Tape and reel 13"
Base/bulk quantity	120/120

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF2L16080CF2	1625 MHz	28 V	80 W	18 dB	57%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally input matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European Directive 2002/95/EC

Applications

- Satellite comms
- Telecom
- ISM

Description

The RF2L16080CF2 is a 80 W, 28 V input matched LDMOS FETs, designed for global positioning system and communication/ISM applications with frequencies from 1300 to 1700 MHz. It can be used in class AB, B or C for all typical modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC} (1)	Thermal resistance, junction-to-case	1.0	°C/W

1. *T_C=85 °C, T_J= 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	0B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	65	-		V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 28 V		-	1	µA
		V_{GS} = 0 V, V_{DS} = 50 V		-		
I_{GSS}	Gate-body leakage current	V_{GS} = -6/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 28 V, I_{DS} = 600 µA	1.75	-	2.5	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS}= 1 V, I_{DS}= 700 mA	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 5 A		-	0.9	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS}= 10 V, V_{DS}= 100 mV		-	2.5	A
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, V_{DS}= 100 mV		-	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		1300		1700	MHz
P_{OUT}	Output power	f= 1625 MHz, 1dB compression point		80		W
G_{PS}	Power gain			18		dB
η_D	Drain efficiency			57		%
VSWR	Load mismatch	P_{OUT} = 80 W, all phases			10:1	

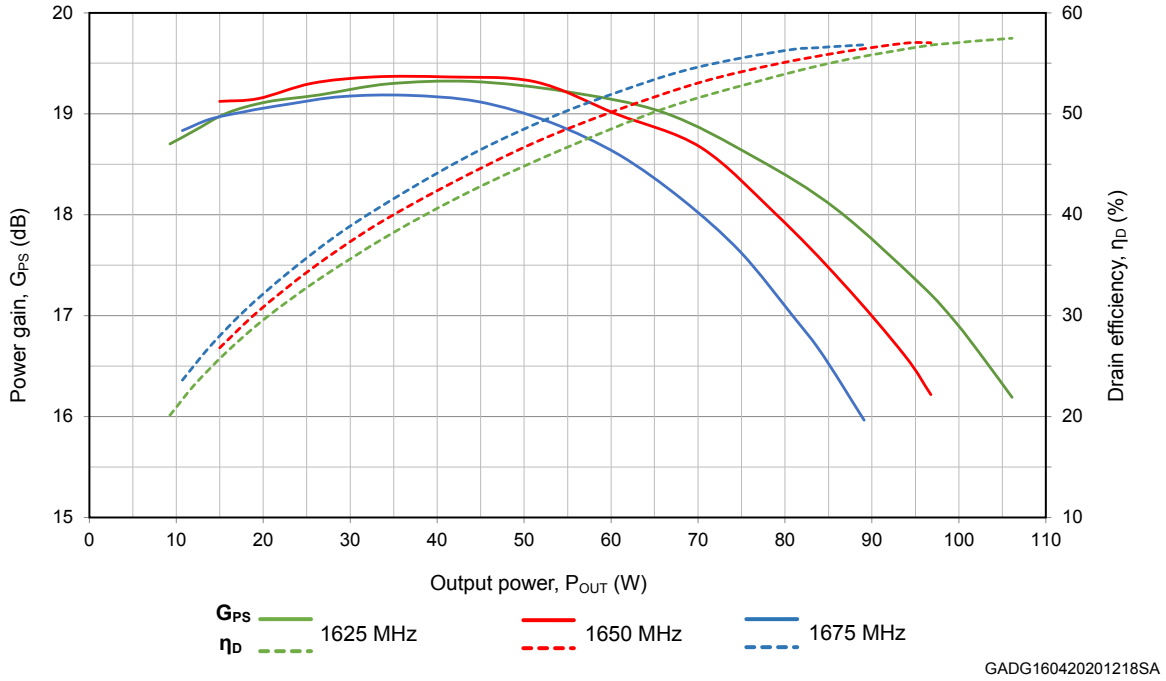
Note: V_{DD} = 28 V, I_{DQ} = 400 mA, pulsed CW, pulse width=20 µs, duty cycle=10%.

3 Typical performances

Table 6. Typical performance (1625 - 1675 MHz)

f (MHz)	P_{1dB} (W)	G_{PS} (dB)	P_{3dB}(W)	η_D @P_{3dB} (%)
1625	81	18.3	105	57
1650	75	18.4	95	57
1675	68	18.2	88	57

Figure 1. Gain and efficiency vs output power (1625 - 1675 MHz)



Note: V_{DD} = 28 V, I_{DQ} = 400 mA, pulsed CW, pulse width=20 µs, duty cycle=10%.

4 Test circuits

Figure 2. **Test circuit layout (1625 - 1675 MHz)**

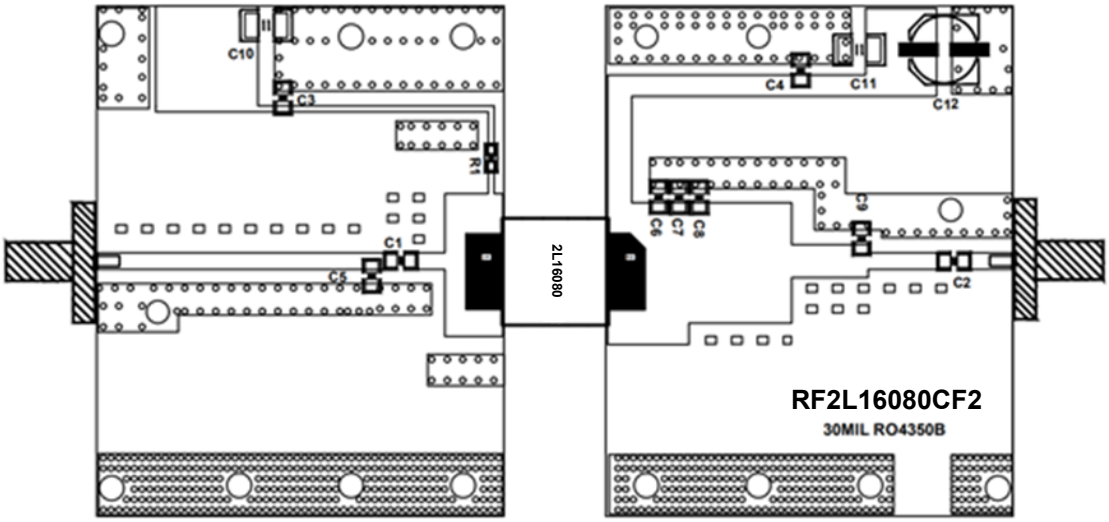


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Figure 3. **Test circuit photo (1625 - 1675 MHz)**

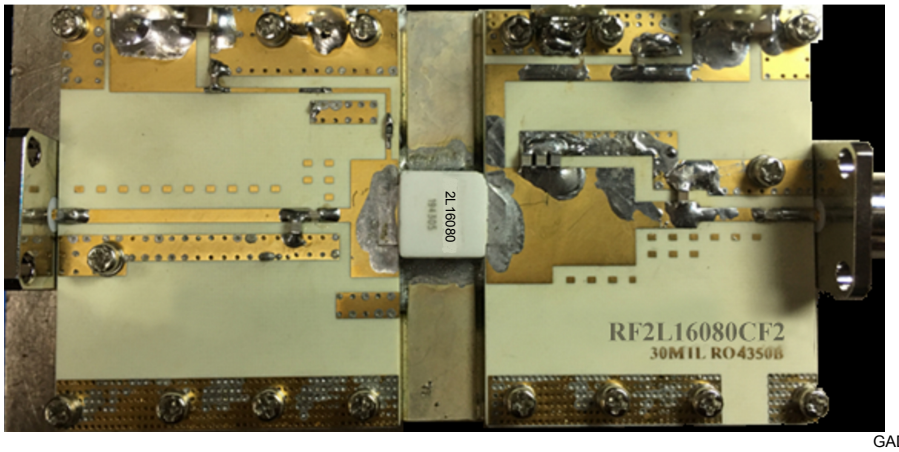

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Table 7. Components list

Component	Value	Size	Reference
C1, C2, C3, C4	27 pF	0805	ATC600F
C5, C6, C7	2 pF	0805	ATC600F
C8	0.5 pF	0805	ATC600F
C9	0.9 pF	0805	ATC600F
C10, C11	10 µF	1210	Ceramic multilayer capacitor
C12	100 µF		Aluminum electrolytic capacitor
R1	10 Ω	0805	Chip resistor
PCB	0.762 mm (.030") thick, ε_r = 3.48, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 A2 package information

Figure 4. A2 package outline

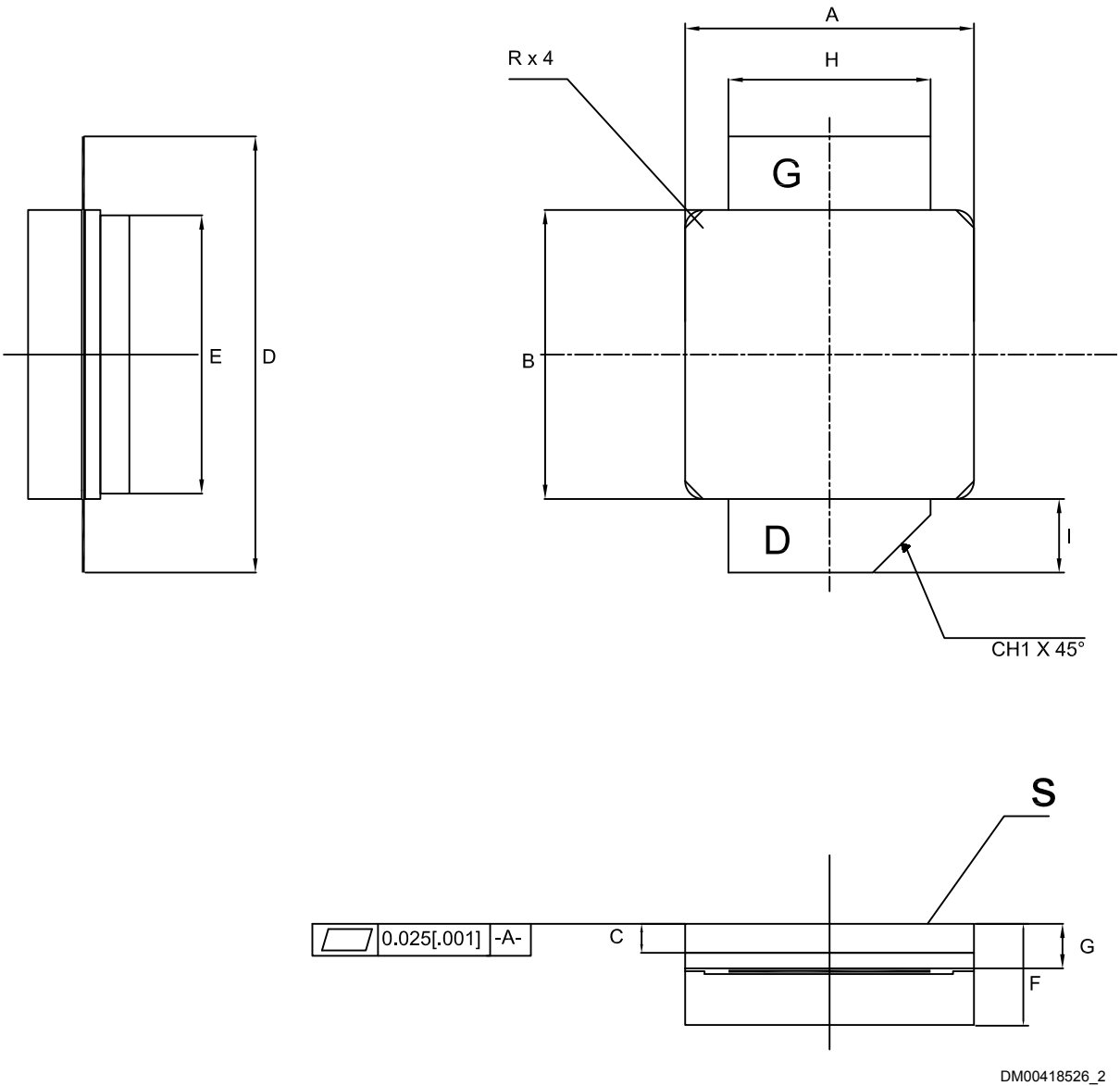
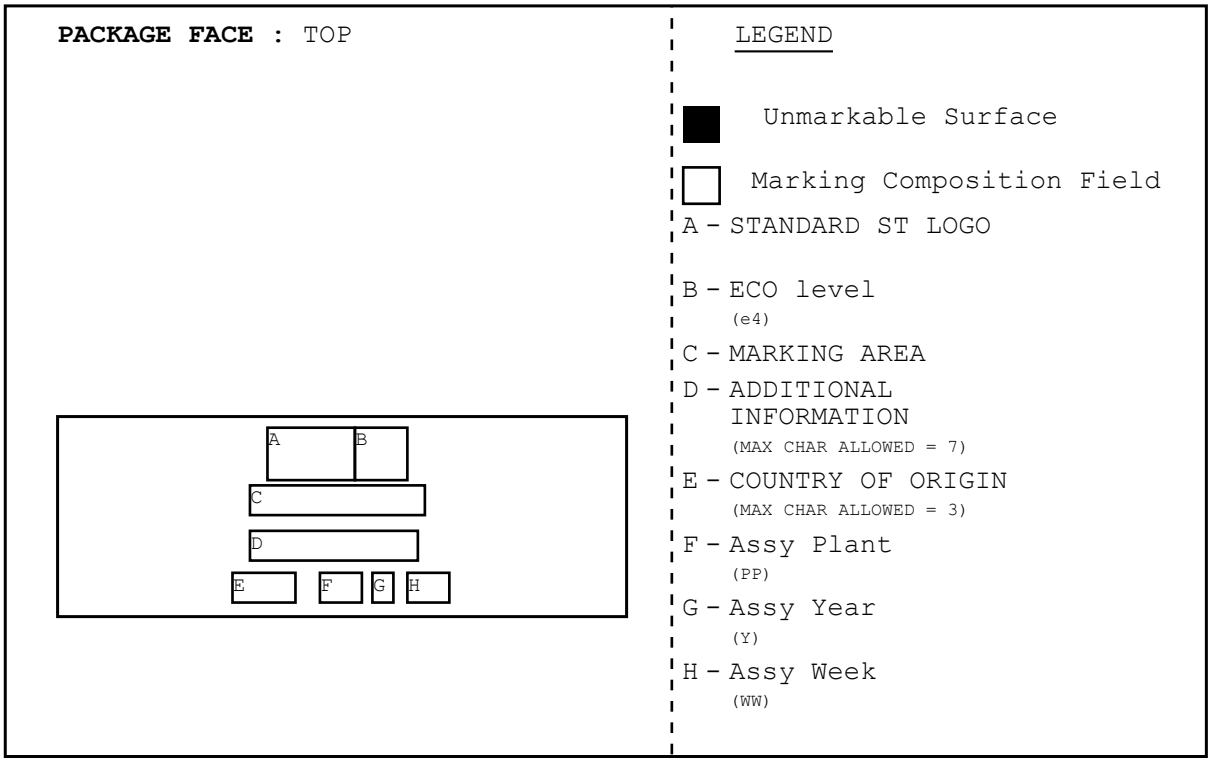


Table 8. **A2 mechanical data**

Symbol	Millimetres		
	Min.	Typ.	Max.
A	10.03	10.16	10.29
B	10.03	10.16	10.29
C	0.89	1.02	1.15
D	15.21	15.34	15.47
E	9.65	9.78	9.91
F	3.43	3.56	3.69
G	1.44	1.57	1.70
H	6.98	7.11	7.24
I	2.08	2.59	3.10
CH1		2.03	
R			0.63

6 Marking information

Figure 5. **Marking composition**



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Revision history

Table 9. **Document revision history**

Date	Version	Changes
04-May-2020	1	First release.
20-Apr-2021	2	Modified efficiency and marking values on cover page. Modified Table 1. Absolute maximum ratings (T_C = 25 °C), Table 2. Thermal data, Table 3. ESD protection, Table 4. Static, Table 5. Dynamic, Figure 1. Gain and efficiency vs output power (1625 - 1675 MHz), Figure 2. Test circuit layout (1625 - 1675 MHz), Figure 3. Test circuit photo (1625 - 1675 MHz) and Table 7. Components list. Added Section 6 Marking information. Minor text changes.

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