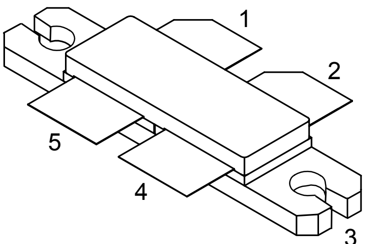
RF3L05200CB4

Datasheet

200 W, 28/32 V, HF to 1 GHz RF power LDMOS transistor



LBB

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF3L05200CB4	650 MHz	28 V	200 W	19 dB	63%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

Applications

- 2-30 MHz HF or short wave communication
- 30-88 MHz ground communication
- 118-140 MHz Avionics
- 136-174 MHz commercial ground communication
- 30-512 MHz Jammer, ground/air communication
- HF to 1000 MHz ISM - instrumentation

Description

The RF3L05200CB4 is a 200 W, 28/32 V, LDMOS FET designed for wideband communication and ISM applications in the frequency range from HF to 1 GHz. It can be used in class AB, B or C for all typical modulation formats.

Product status link
RF3L05200CB4

Product summary	
Order code	RF3L05200CB4
Marking	3L05200
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	36	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}[(1)]	Thermal resistance, junction-to-case	0.35	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	90			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
		V_{GS} = 0 V, V_{DS} = 75 V			1	
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 42 V, I_D = 600 µA	1.75		2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 28 V, I_D = 500 mA		2.9		V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 1 A			275	mV
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV			1	Ω
C_{ISS}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 28 V, f = 1 MHz		106		pF
C_{RSS}	Common source feedback capacitance			1.6		pF
C_{OSS}	Common source output capacitance			40		pF

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				1000	MHz
P_{OUT}	Output power	f = 650 MHz, 2.5 dB compression		200		W
G_{PS}	Power gain			19		dB
η_D	Drain efficiency			63		%
VSWR	Load mismatch	P_{OUT} = 200 W, all phases			10:1	

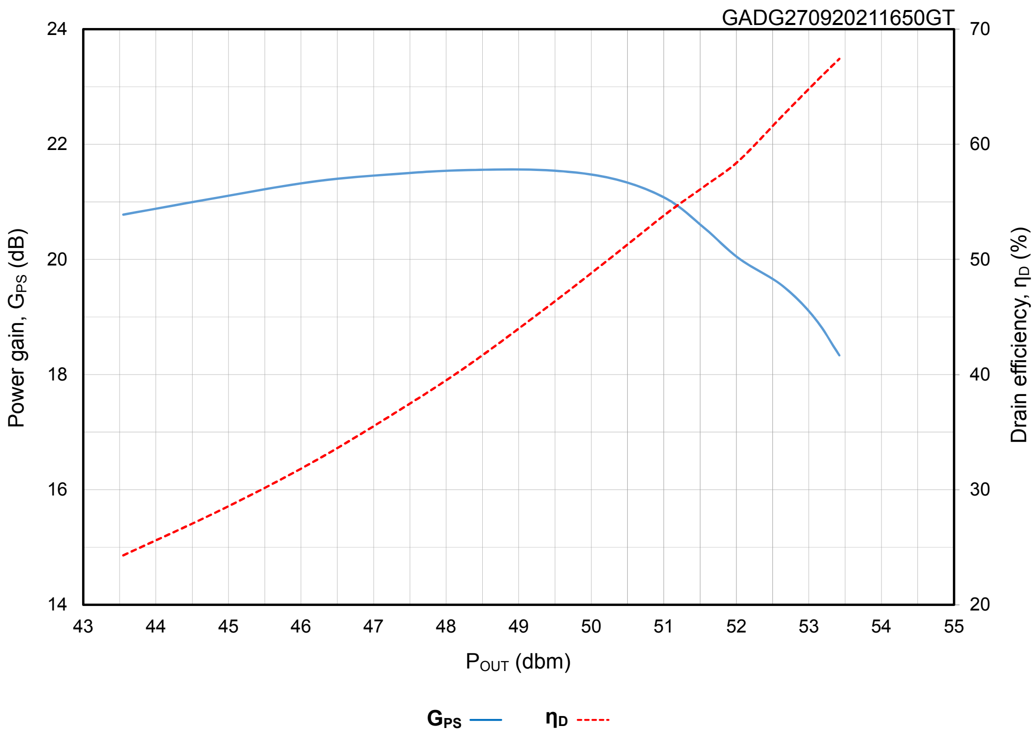
Note: *V_{DD} = 28 V, I_{DQ} = 100 mA, CW test signal.*

3 Typical performances

Table 6. Output power, power gain and drain efficiency vs input power (f = 650 MHz)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D(%)
22.63	43.29	21	3.31	20.66	23
23.65	44.57	29	3.86	20.92	27
24.67	45.81	38	4.48	21.14	30
25.68	46.97	50	5.15	21.29	35
26.69	48.08	64	5.9	21.39	39
27.7	49.13	82	6.7	21.43	44
28.72	50.07	102	7.54	21.35	48
29.71	50.83	121	8.32	21.12	52
30.73	51.47	140	9.07	20.74	55
31.73	51.97	157	9.75	20.24	58
32.74	52.48	177	10.46	19.74	60
33.74	52.95	197	11.11	19.21	63
34.76	53.32	215	11.66	18.56	66

Figure 1. Power gain and drain efficiency versus output power (f = 650 MHz)



Note: V_{DD} = 28 V, I_{DQ} =100 mA, CW test signal.

4 Test circuits

Figure 2. Test circuit layout (f = 650 MHz)

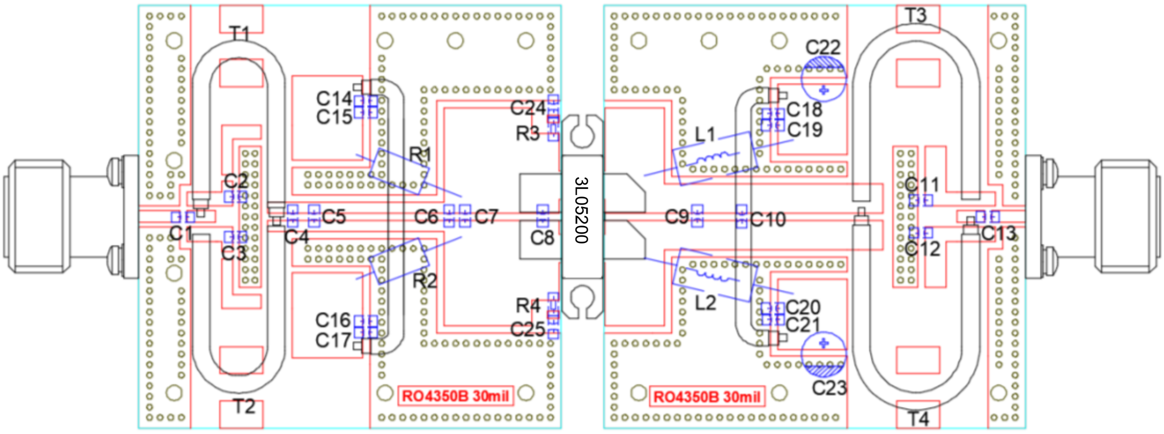


Figure 3. Test circuit photo

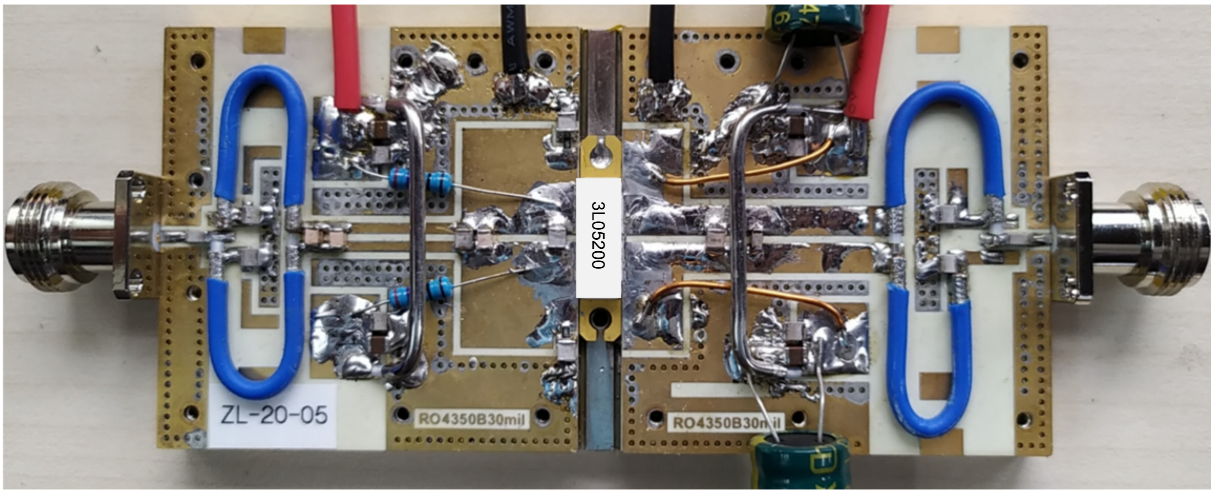


Table 7. Components list

Component	Value	Reference
C1,C13,C15,C16,C19,C20	47 pF	ATC800B
C2,C3,C11,C12,C24,C25	100 pF	ATC800B
C4,C5	2.7 pF	DLC70B
C6,C10	6.8 pF	ATC800B
C7	24 pF	DLC70B
C8	24 pF	ATC800B
C9	18 pF	DLC70B
C14,C17,C18,C21	10 µF	50 V ceramic multilayer capacitor
C22,C23	470 µF	63 V electrolytic capacitor
R1,R2	270 Ω	Metal film resistor
R3,R4	16 Ω	0805 chip resistor
L1,L2	Φ 0.8 mm	Copper wire
T1,T2,T3,T4	25 Ω, line length = 50 mm	SF-086-25
PCB	0.762 mm [0.030''] thick, εr = 3.48, Rogers RO4350B, 1 oz. copper	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 4. LBB package outline

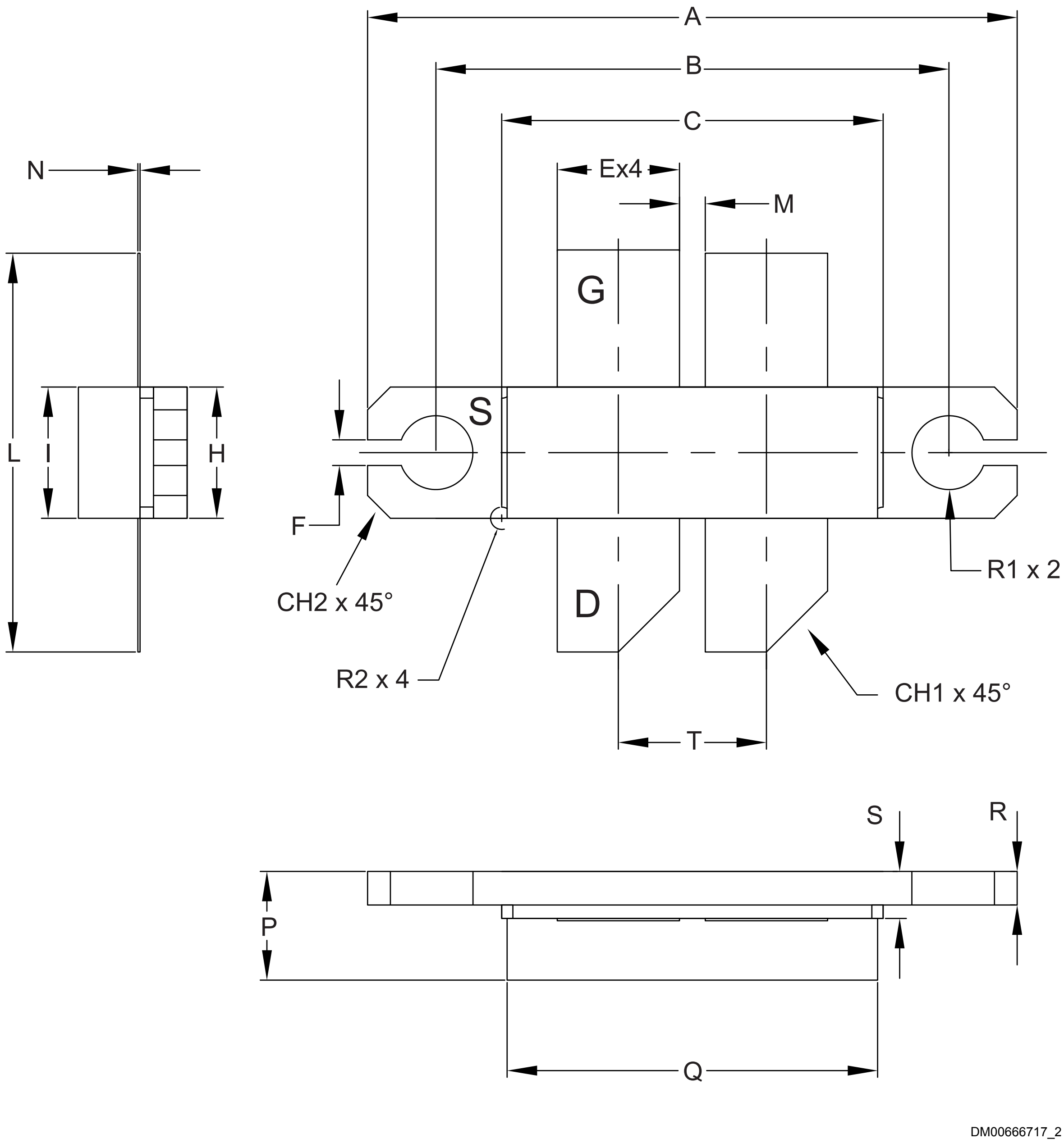
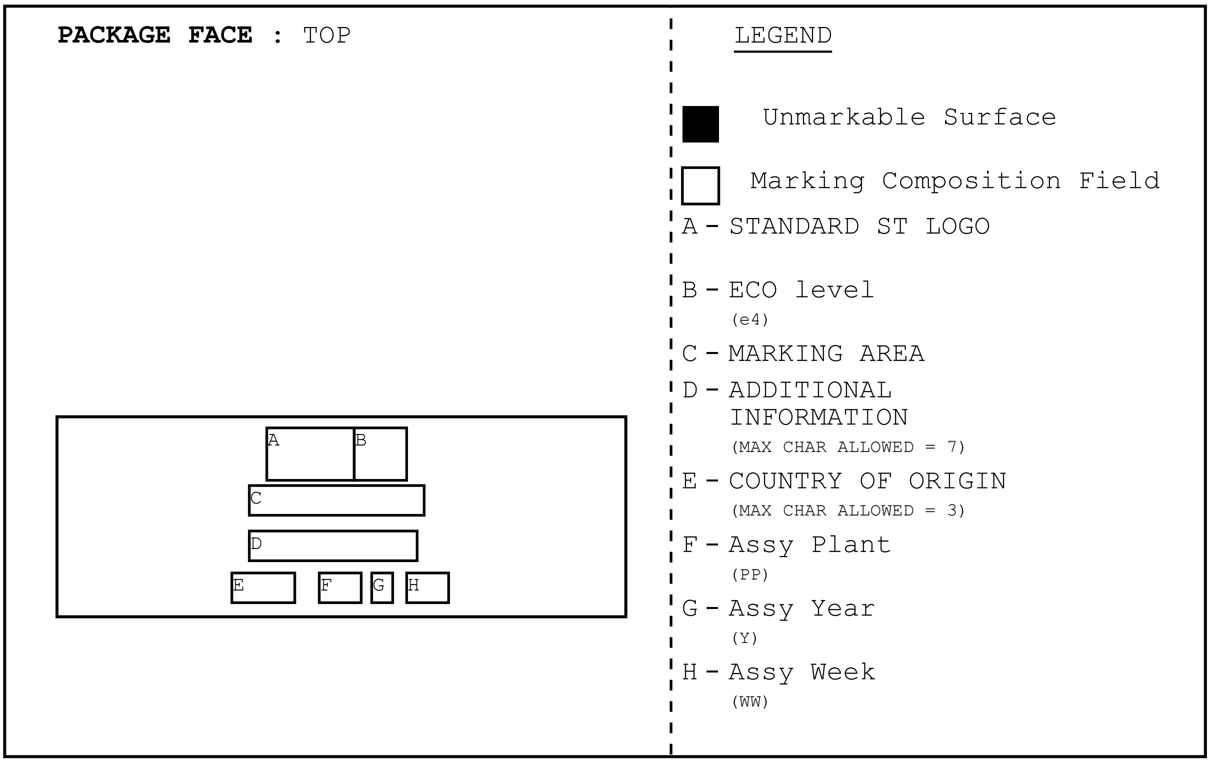


Table 8. LBB mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

5.2 Marking information

Figure 5. Marking composition



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Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Jun-2020	1	First release.
28-Sep-2021	2	Updated title and Device summary in cover page. Updated Section 1 Electrical ratings. Updated Section 2 Electrical characteristics. Updated Figure 1. Power gain and drain efficiency versus output power (f = 650 MHz) Updated Section 4 Test circuit. Added Section 5.2 Marking information. Minor text changes.

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