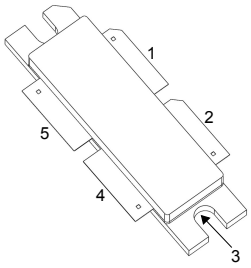
RF4L15400CB4

Datasheet

400 W, 40 V, 1.2 to 1.5 GHz RF power LDMOS transistor



D4E

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Product status link
RF4L15400CB4

Product summary	
Order code	RF4L15400CB4
Marking	4L15400
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF4L15400CB4	1.5 GHz	40 V	400 W	18.5 dB	57%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched pair transistors in push-pull configuration
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European directive 2002/95/EC

Applications

- 1.3 and 1.5 GHz particle accelerator
- L-band radar

Description

The RF4L15400CB4 is a 400 W, 50 V high performance, internally matched LDMOS FET, designed for multiple applications in the frequency range from 1.2 to 1.5 GHz. It is qualified up to 40 V operation.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	42	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.21	°C/W

1. *T_C = 85 °C , P_{OUT} = 300 W CW, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	90	-		V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 42 V		-	1	µA
		V_{GS} = 0 V, V_{DS} = 75 V		-		
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 40 V, I_{DS} = 600 µA	1.75	-	2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 1 V, I_{DS} = 100 mA	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 6 A		-	1	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV		-	2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV		-	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	f = 1.5 GHz, pulsed CW, 1 dB compression	-	400		W
G_{PS}	Power gain		-	18.5		dB
η_D	Drain efficiency		-	57		%
VSWR	Load mismatch	P_{OUT} = 400 W, all phases	-		10:1	

Note: V_{DD} = 40 V, I_{DQ} = 0.1 A, pulse width = 20 µs, duty cycle = 10%.

3 Typical performances

Figure 1. Power gain and drain efficiency vs output power (1480 – 1520 MHz frequency band, I_{DQ} = 100 mA)

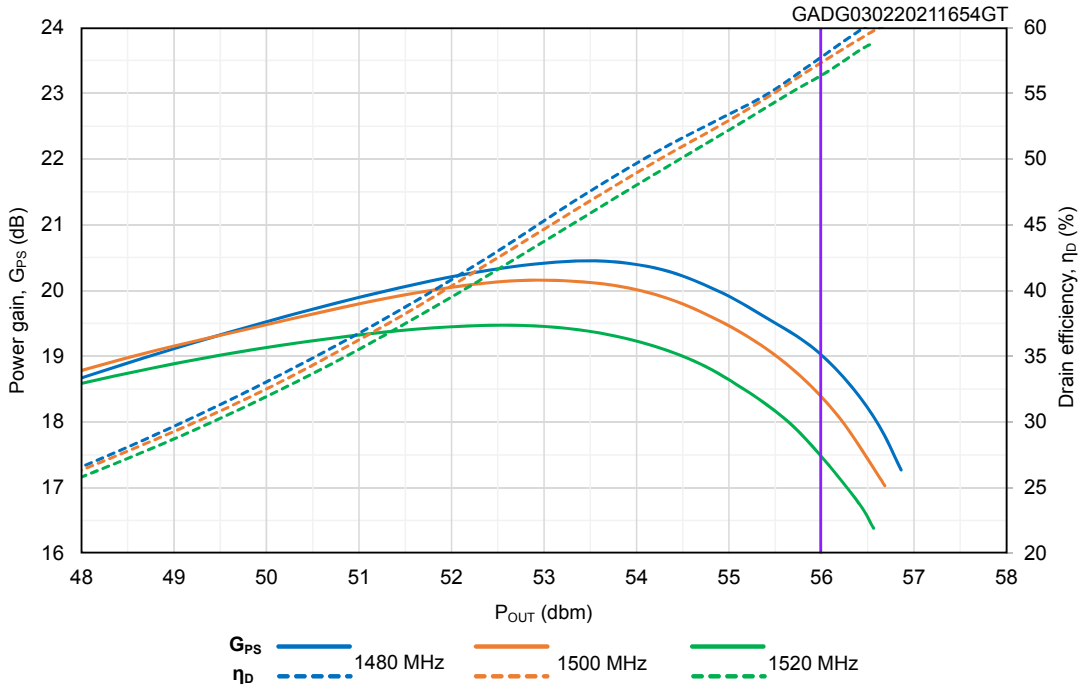
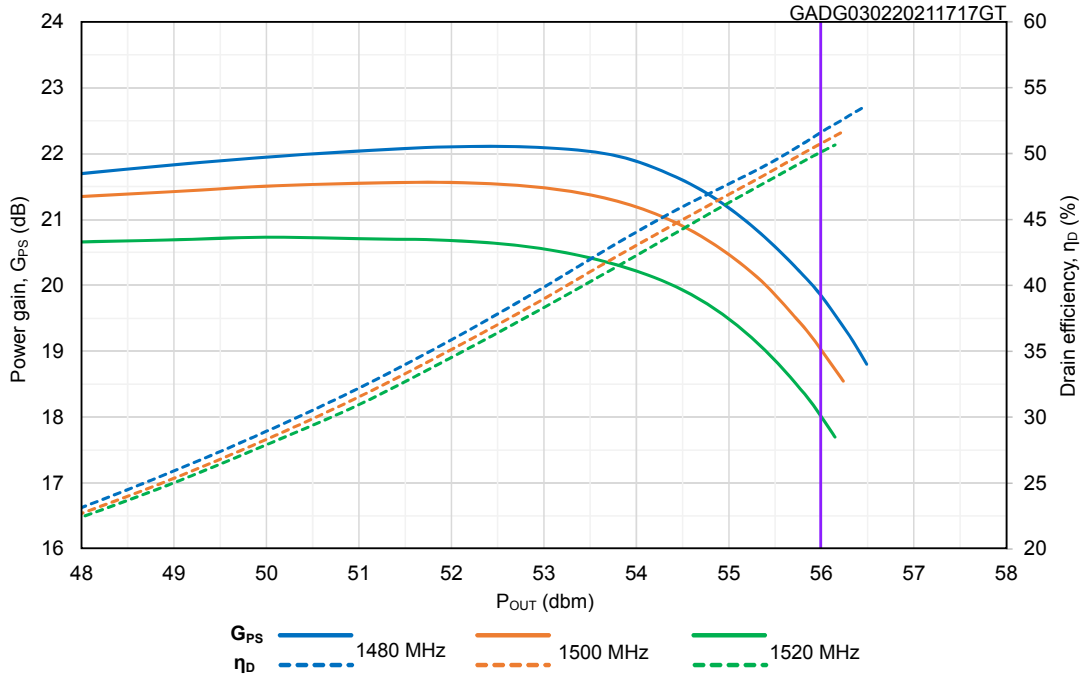
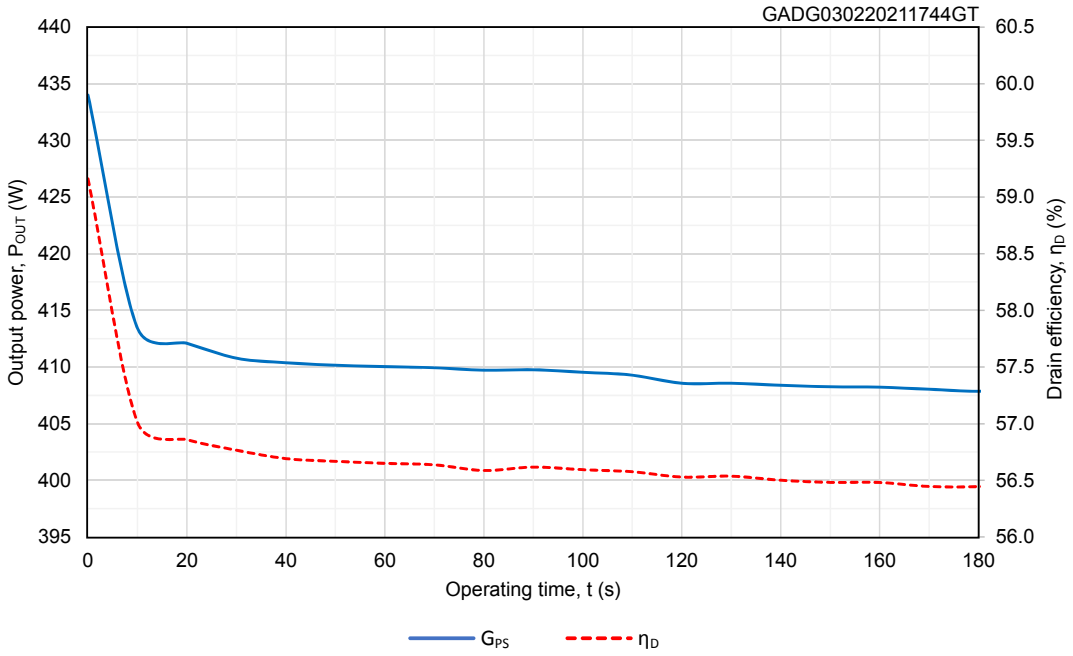


Figure 2. Power gain and drain efficiency vs output power (1480 – 1520 MHz frequency band, I_{DQ} = 1.5 A)



Note: V_{DD} = 40 V, pulsed CW, pulse width = 20 µs, duty cycle = 10%.

Figure 3. Thermal test at 1.5 GHz under standard pulsed conditions



Note: V_{DD} = 40 V, I_{DQ} = 100 mA, pulsed CW, pulse width = 20 µs, duty cycle = 10%.

4 Test circuits

Figure 4. **Test circuit layout**

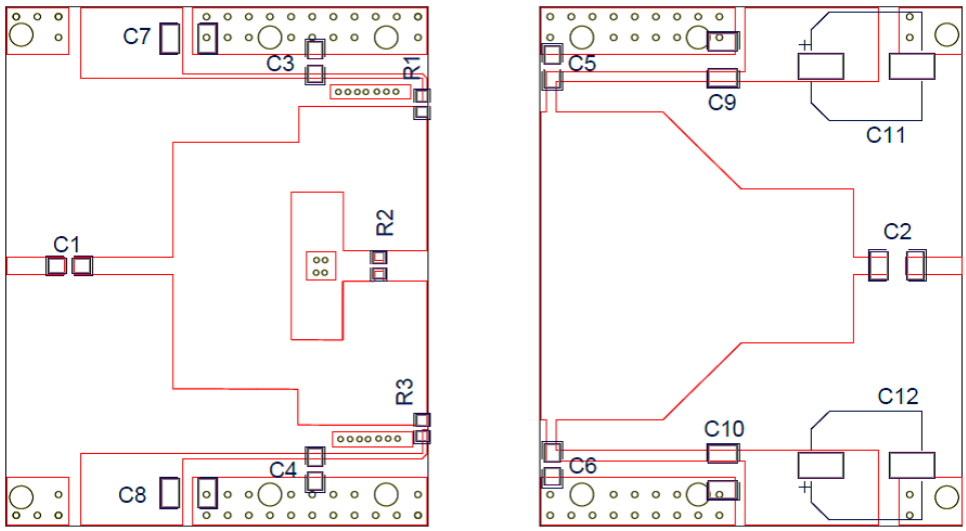


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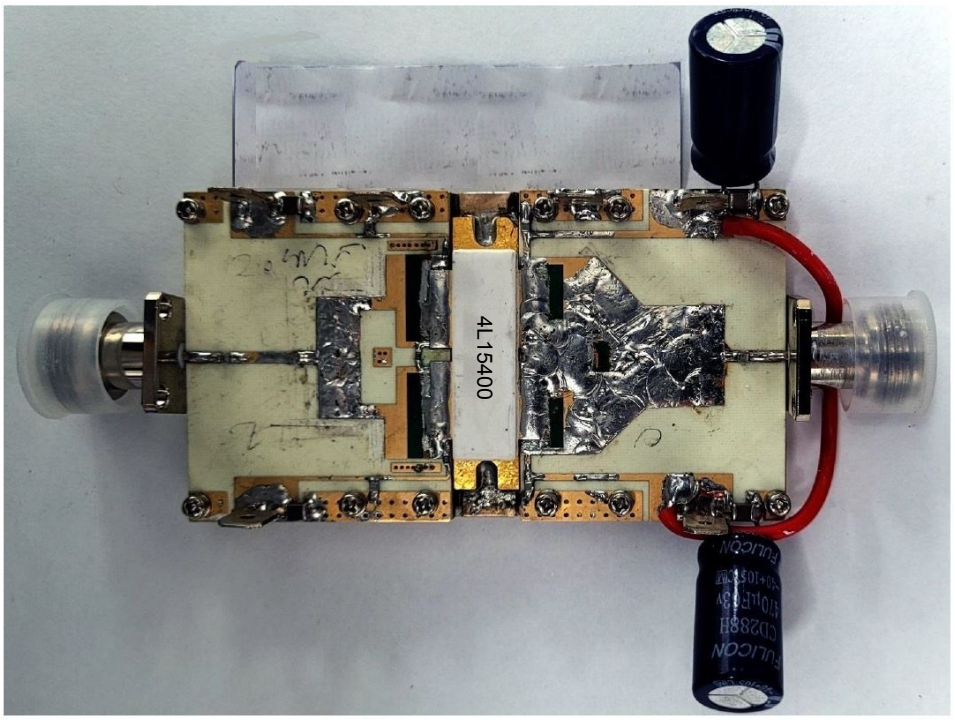
Table 6. **Components list**

Component	Value	Size	Reference
C1	6.8 pF	0805	ATC600F
C2	33 pF	1210	ATC100B
C3, C4, C5, C6	33 pF	0805	ATC600F
C7, C8, C9, C10	10 µF	1210	X7R
C11, C12	100 µF		Aluminium electrolytic capacitor
R1, R2, R3	10 Ω	0603	
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B		

Figure 5. **Test circuit photo**



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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 D4E package information

Figure 6. D4E package outline

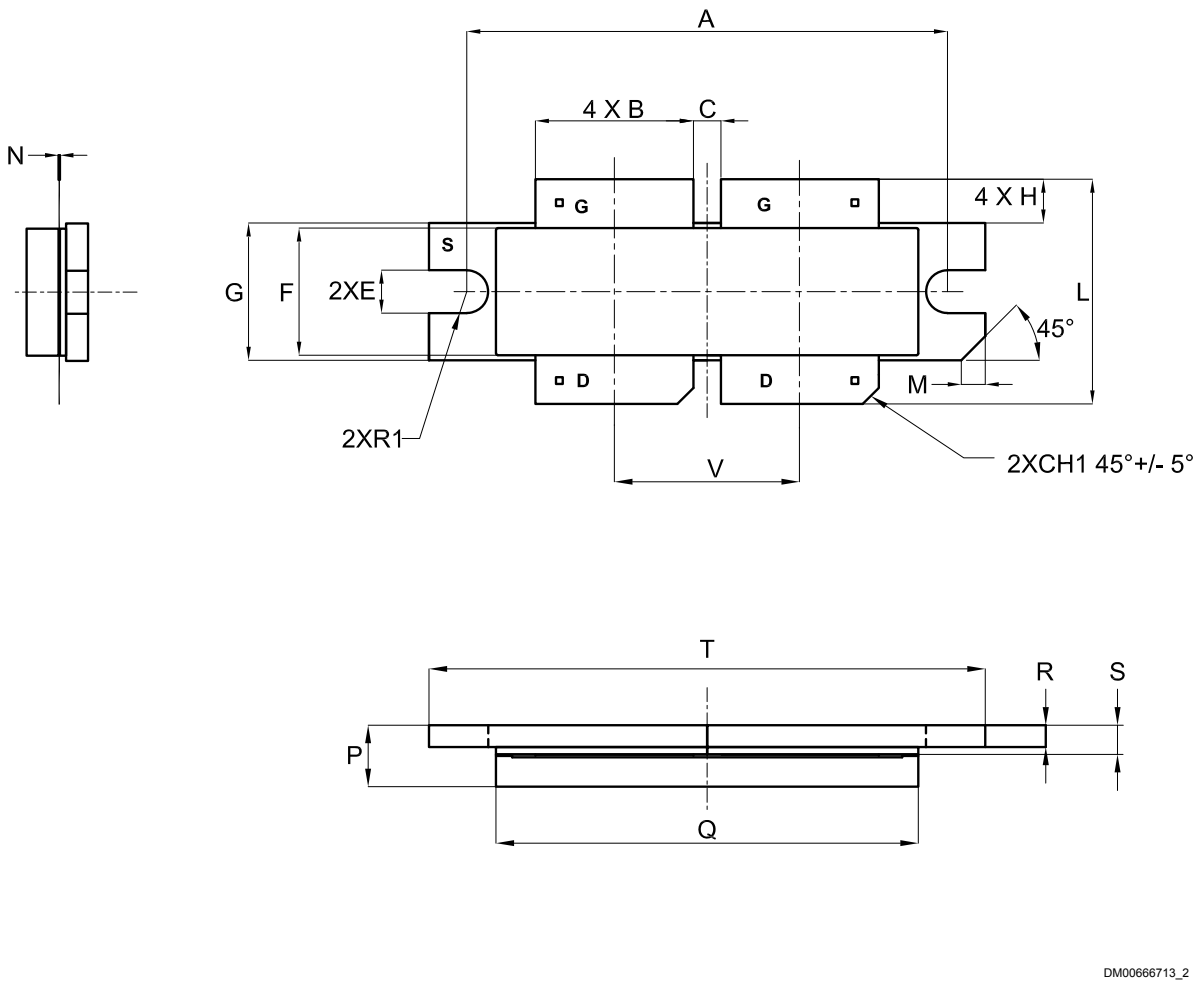
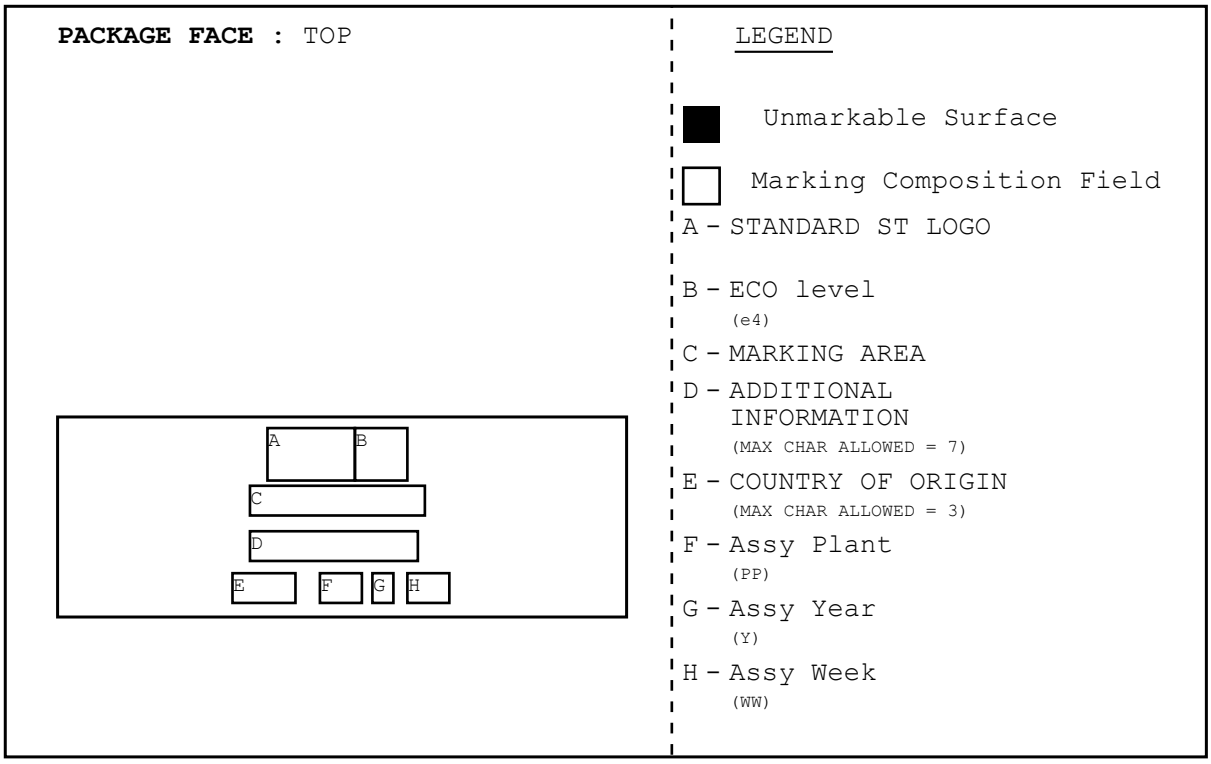


Table 7. **D4E package mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

5.2 Marking information

Figure 7. **Marking composition**



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Revision history

Table 8. **Document revision history**

Date	Revision	Changes
08-Feb-2021	1	First release.
22-Sep-2021	2	Updated Table 1. Absolute maximum ratings (T_C = 25 °C) and Table 3. ESD protection. Updated Table 4. Static (per side). Minor text changes.

Contents