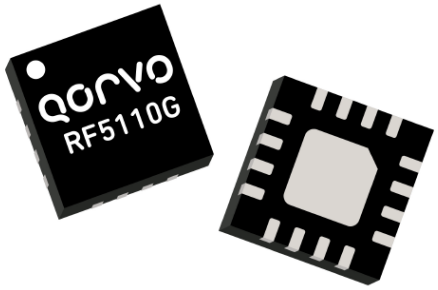
RF5110G

3V General Purpose/GSM Power Amplifier

Product Overview

The RF5110G is a high-power, high-gain, high-efficiency power amplifier. The device is manufactured with an advanced GaAs HBT process. It is designed for use as the final RF amplifier in GSM hand-held equipment in 900 MHz band, and General-Purpose radio application in standard sub-bands from 150 MHz to 960 MHz. An analog on-board power controller provides over 70 dB range of adjustment. Which allows for power down with a voltage equals to the logic “Low” to set the device in standby mode. The RF5110G RF Input is internally matched to 50 Ω. On its RF Output, it can be easily matched externally to obtain optimum power and efficiency for certain applications.



16 Pad 3 x 3 mm QFN Package

Key Features

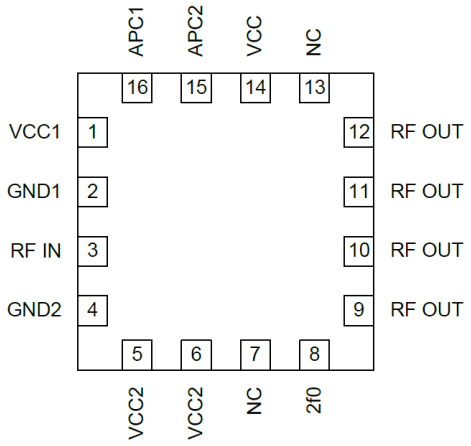
General Purpose:

- Single 2.8 V to 3.6 V Supply
- +32 dBm Output Power
- 53% Efficiency
- 150 MHz to 960 MHz Operation

GSM:

- Single 2.7 V to 4.8 V Supply
- +36 dBm Output Power at 3.6 V
- 32 dB Gain with Analog Gain Control
- 57% Efficiency
- 800 MHz to 950 MHz Operation
- Supports GSM and E-GSM

Functional Block Diagram



Top View

Applications

- FM Radio Applications
  - 150 MHz/220 MHz/450 MHz
  - 865 MHz to 928 MHz
- 3 V GSM Cellular Handsets
- GPRS Compatible

Ordering Information

Part No.	Description
RF5110GTR7	2,500 pieces on a 7” reel (standard)
RF5110GPCK-410	GSM900 Fully Tested Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 °C to +150 °C
Device Voltage (V_{CC}, V_{CC1}, V_{CC2})	-0.5 V to +6.0 V
Control Voltage (V_{APC1}, V_{APC2})	-0.5 V to +3.0 V
Device Current (I_{CC}, I_{CC1}, I_{CC2})	2400 mA
RF Input Power	+13 dBm
Duty Cycle at Max Power	50%

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. This rating specified for GSM operation.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC}, V_{CC1}, V_{CC2})		+3.5		
	+2.7		+4.8(1)	V
			+5.5(1)(2)	V
T_{CASE}	−40		+85	°C
T_J			+150	°C

Note:
1. P_{OUT} < +35 dBm
2. With maximum output load VSWR 6:1

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Output Power	150 MHz		32		dBm
Gain			31.5		dB
Efficiency			53		%
Output Power	220 MHz		32		dBm
Gain			32		dB
Efficiency			52		%
Output Power	450 MHz; V_{CC}, V_{CC1} and V_{CC2} = 3.0 V		32		dBm
Gain			32.5		dB
Efficiency			50.5		%
Output Power	865 MHz to 928 MHz Equals typical at respective frequency corner		32		dBm
Gain		33.0		29.5	dB
Efficiency			49		%

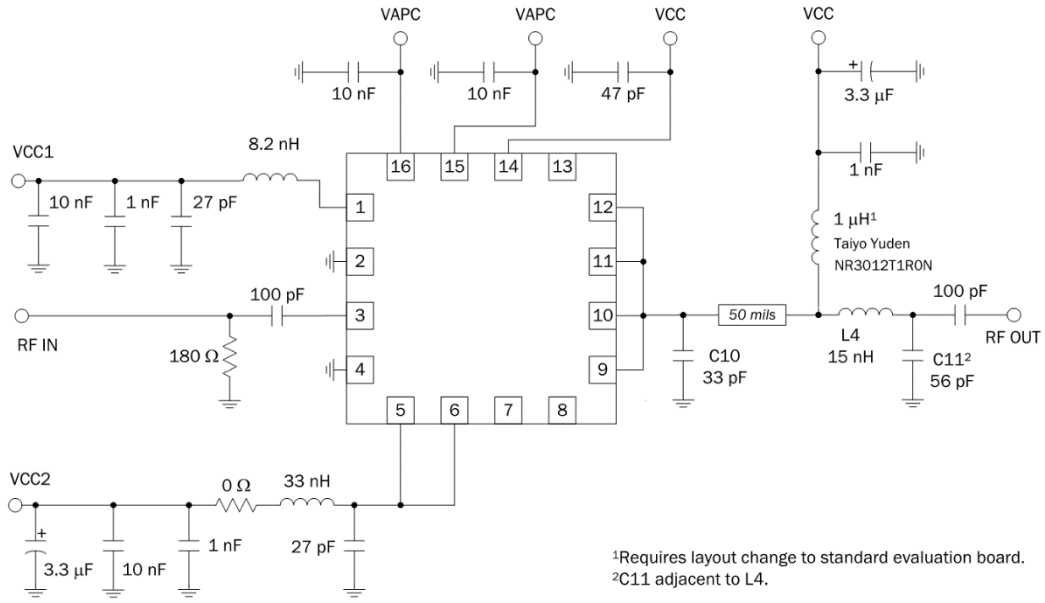
Notes:
1. Test conditions unless otherwise noted: V_{APC1} and V_{APC2} = 2.8 V; V_{CC}, V_{CC1} and V_{CC2} = 3.3 V; Duty Cycle = 100%; Temp = +25 °C; 50 Ω system; Refer to application circuits

Electrical Specifications (continue)

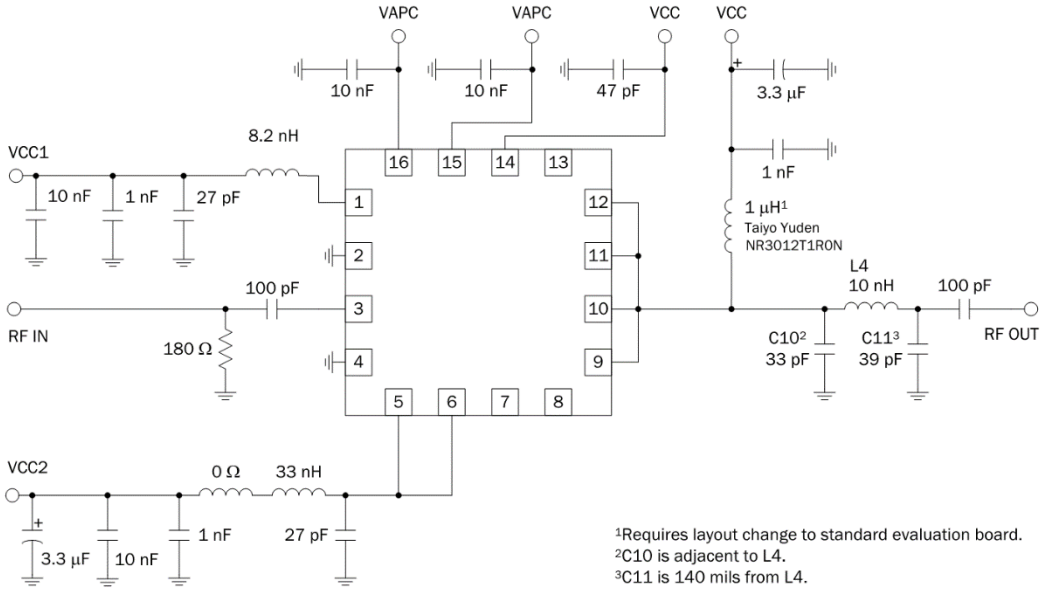
Parameter	Conditions [1]	Min	Typ	Max	Units
Operational Frequency Range		880		915	MHz
Usable Frequency Range	Using different EVB tune	800		950	MHz
Maximum Output Power		33.8	34.5		dBm
	Temp = +60 °C, V_{CC}, V_{CC1} and V_{CC2} = 3.3 V	33.1			dBm
Efficiency	At Maximum Output Power	50	57		%
	P_{OUT} = +20 dBm		12		%
	P_{OUT} = +10 dBm		5		%
Input Power for Max. Output		4.5	7.0	9.5	dBm
Output Noise Power	RBW = 100 KHz; 925-935 MHz; V_{CC}, V_{CC1} and V_{CC2} = 3.3 to 5.0V			-72	dBm
	RBW =100 KHz; 935-960 MHz; V_{CC}, V_{CC1} and V_{CC2} = 3.3 to 5.0V			-81	dBm
Forward Isolation	Standby Mode V_{APC1} and V_{APC2} = 0.3 V, P_{IN} = +9.5 dBm			-22	dBm
Second Harmonic	P_{IN} = +9.5 dBm		-20	-7	dBm
Third Harmonic	P_{IN} = +9.5 dBm		-25	-7	dBm
Non-Harmonic Spurious				-36	dBm
Input Impedance			50		Ω
Optimum Source Impedance	For best noise performance		40 + j10		Ω
Input VSWR	($P_{OUT, MAX}$ - 5 dB) < Pout < $P_{OUT.MAX}$			2.5:1	
	P_{OUT} < ($P_{OUT.MAX}$ - 5 dB)			4.0:1	
Output Load VSWR, Stability	Spurious < -36dBm, RBW=100KHz V_{APC1} and V_{APC2} from 0.3 V to 2.6 V	8:1			
Output Load VSWR, Ruggedness	No damage	10:1			
Output Load Impedance	Load Impedance presented at RF OUT pad		2.6 – j1.5		Ω
Power Control “ON” Voltage	V_{APC1}, V_{APC2}; Maximum P_{OUT}	2.6			V
Power Control “OFF” Voltage	V_{APC1}, V_{APC2}; Minimum P_{OUT}	0.2	0.5		V
Gain Control Range	V_{APC1} and V_{APC2} from 0.2 V to 2.6 V	75			dB
Gain Control Slope	P_{OUT} from -10 dBm to +35 dBm	5	100	150	dB/V
APC Input Capacitance	DC to 2 MHz			10	pF
APC Input Current	V_{APC1} and V_{APC2} = 2.8V		4.5	5	mA
	V_{APC1} and V_{APC2} = 0 V			25	µA
Turn ON/OFF Time	V_{APC1} and V_{APC2} from 0 V to 2.8V			100	ns
Device Current (I_{CC}, I_{CC1}, and I_{CC2})	At Maximum Output Power		2		A
	Quiescent, P_{IN} < -30dBm	15	200	335	mA
	Standby Mode, P_{IN} < -30dBm		1	10	µA
	Standby Mode, P_{IN} < -30dBm, Temp = +85°C		1	10	µA
Thermal Resistance	CW Mode, Junction to Case		25.6		°C/W

Notes:
1. Test conditions unless otherwise noted: V_{APC1} and V_{APC2} = 2.8 V; V_{CC}, V_{CC1} and V_{CC2} = 3.6 V; P_{IN} = +4.5 dBm; Pulse Width = 1731 µs; Duty Cycle = 37.5%; Temp = +25 °C; 50 Ω system; Refer to RF5110GPCK-410 GSM900 evaluation board circuit.

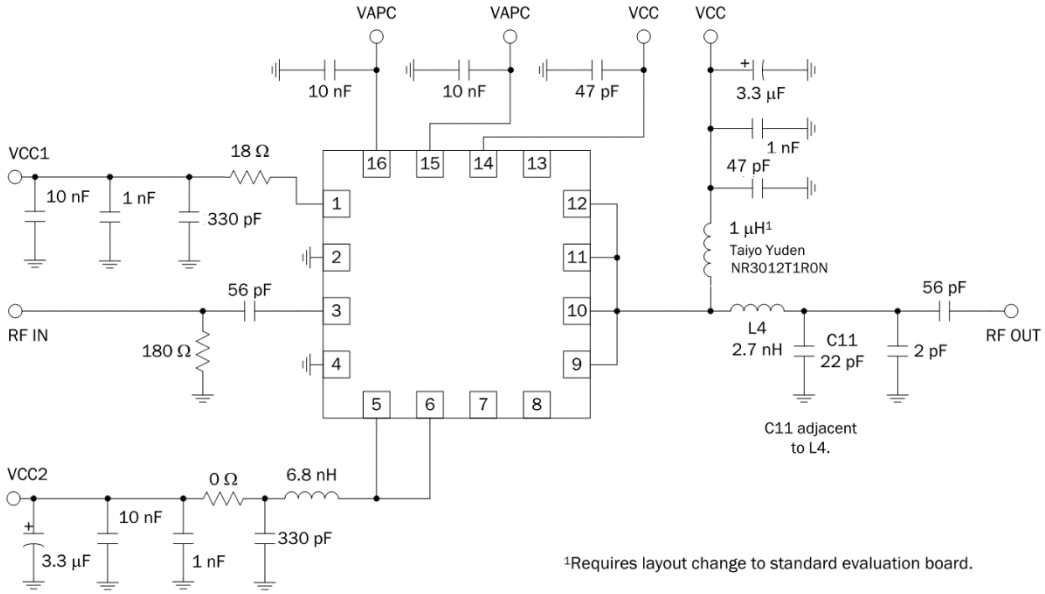
150 MHz FM Band Application Circuit



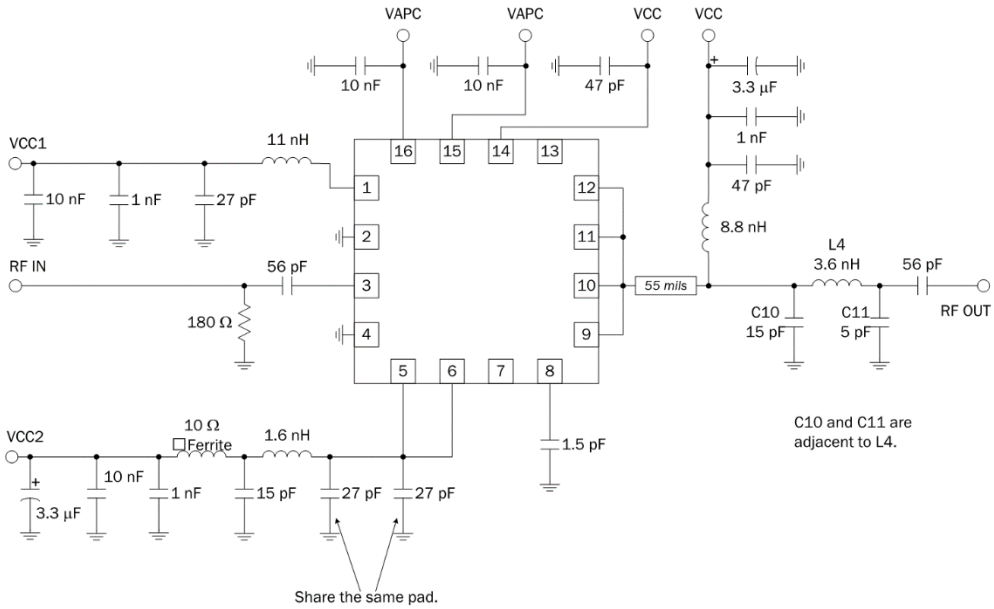
220 MHz FM Band Application Circuit



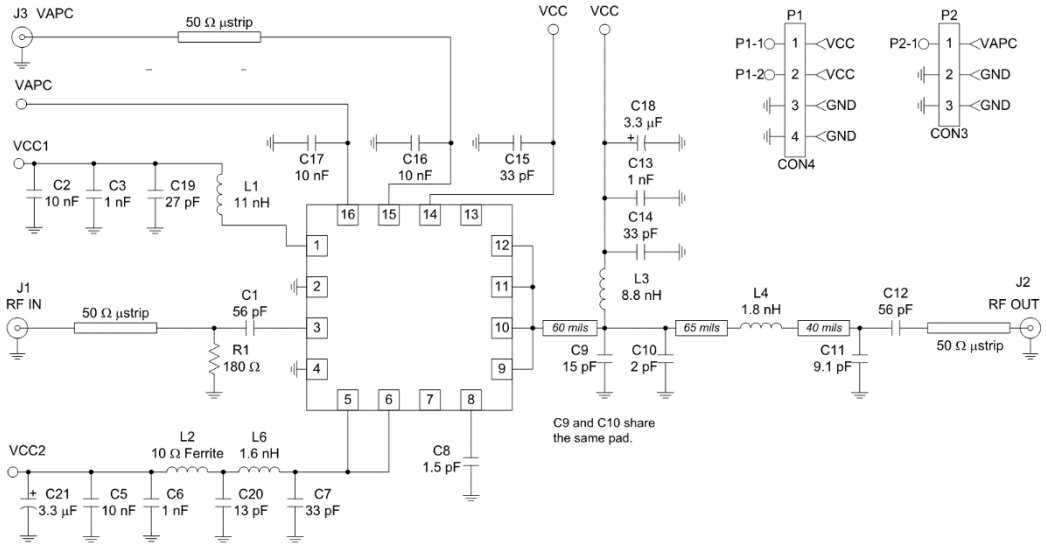
450 MHz FM Band Application Circuit



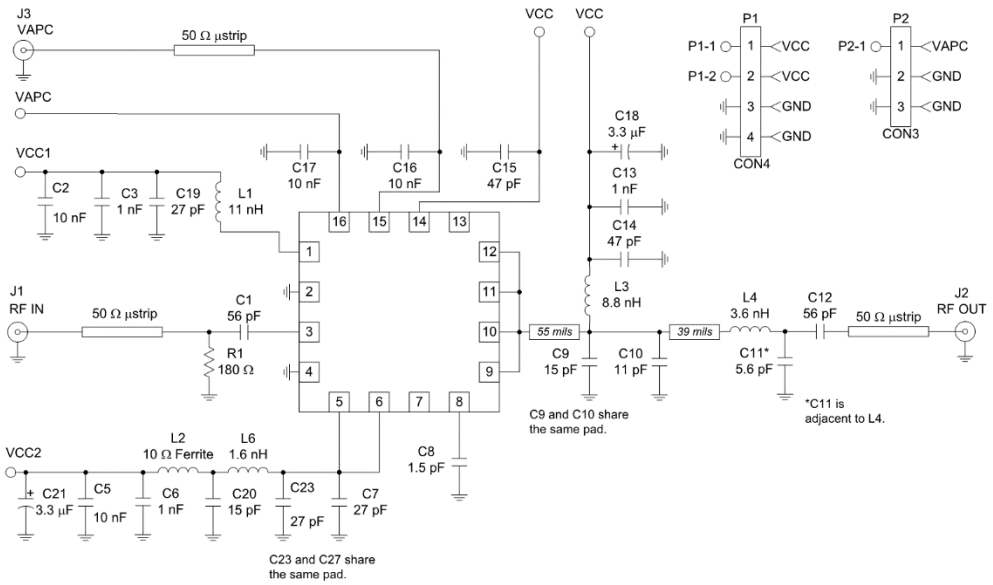
865 MHz and 902 MHz to 928 MHz ISM Band Application Circuit



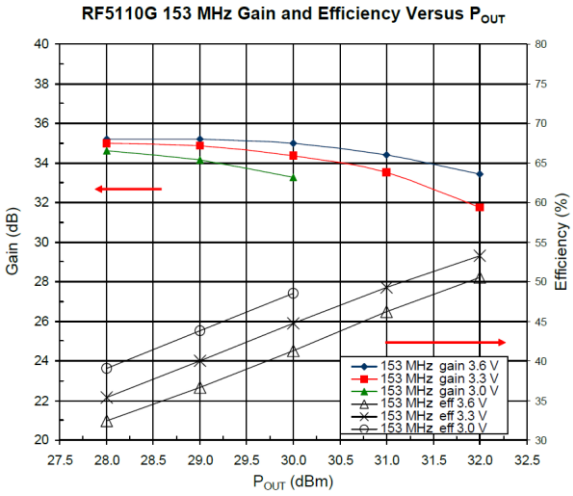
850 MHz GSM Band Application Circuit

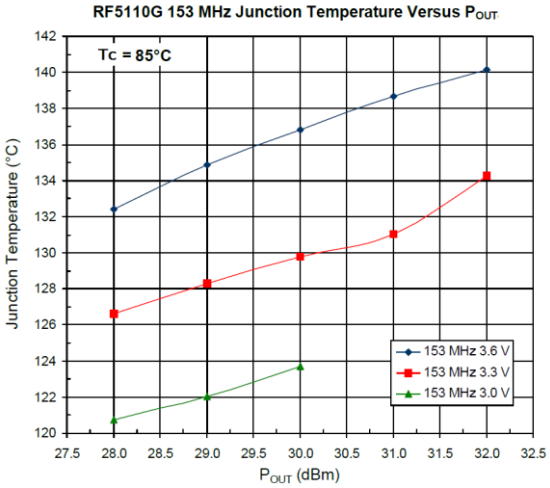


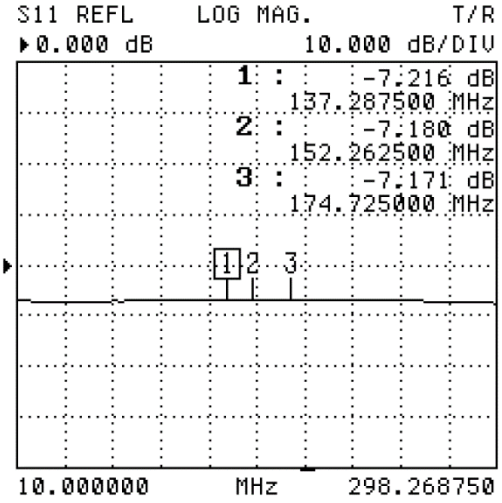
GSM900 Evaluation Board Circuit, RF5110GPCK-410

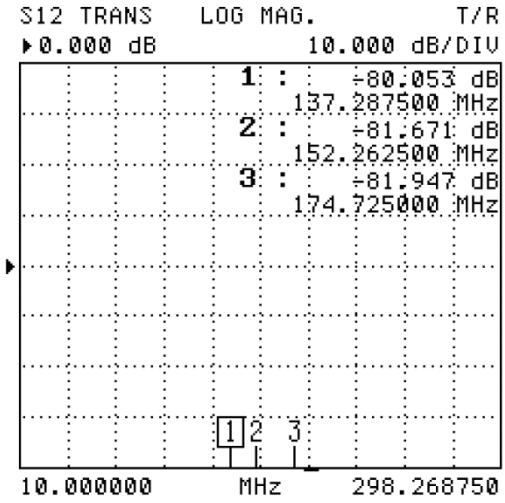


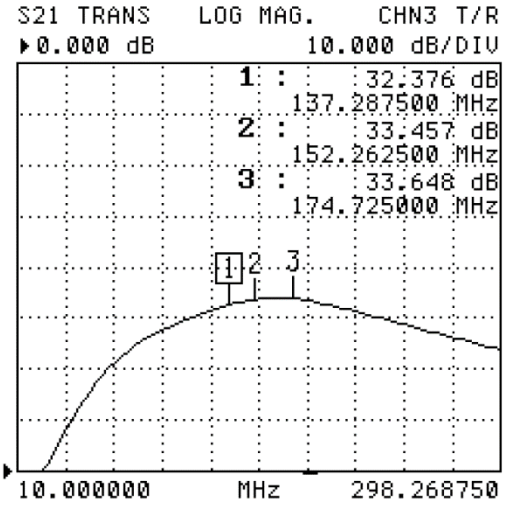
Performance Plots – 150 MHz

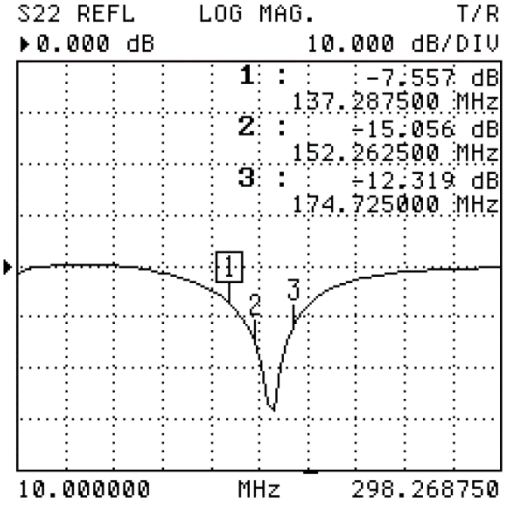




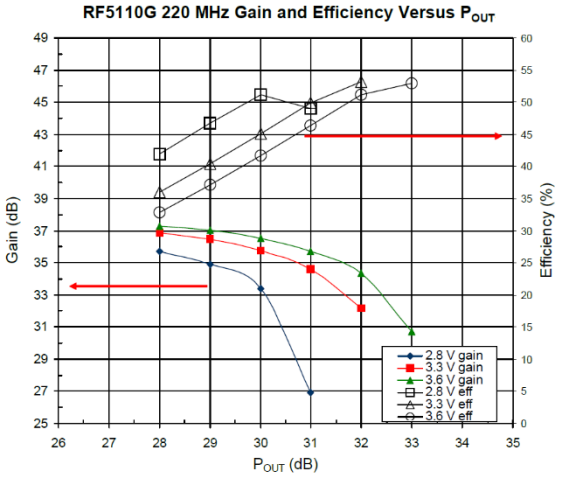


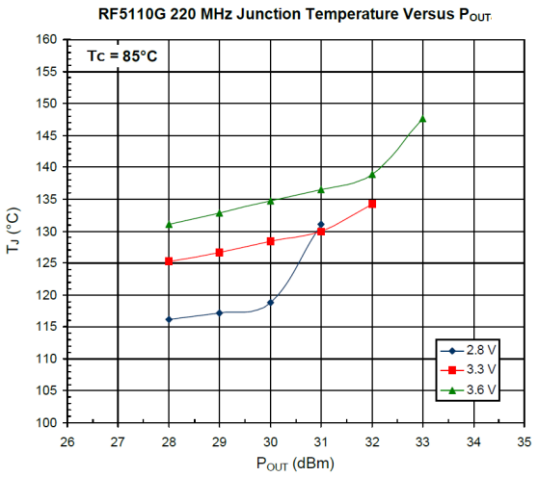


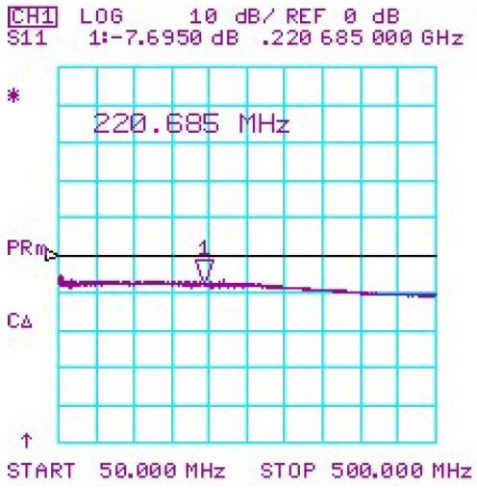


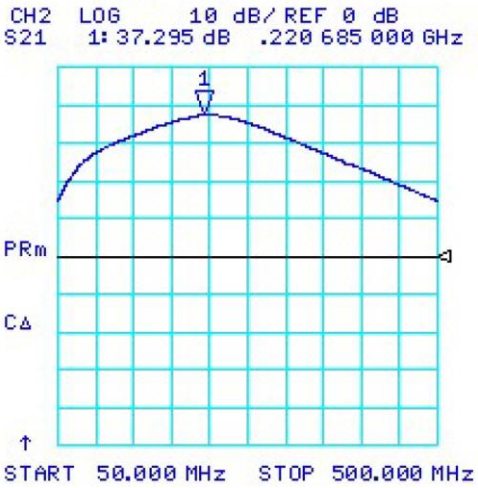


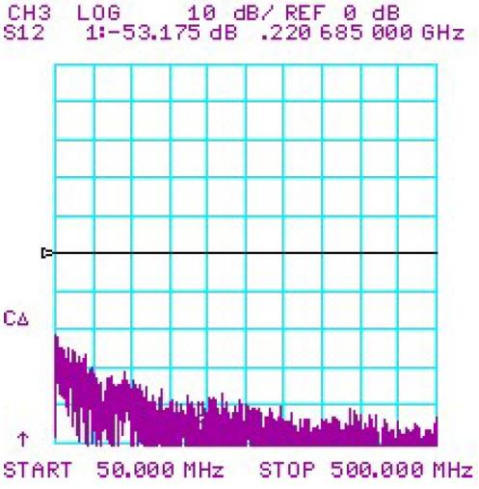
Performance Plots – 220 MHz

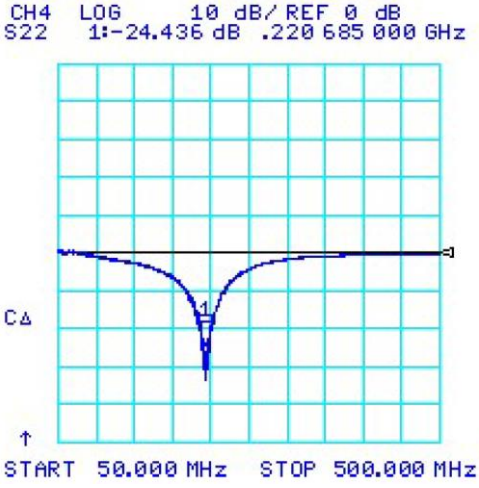




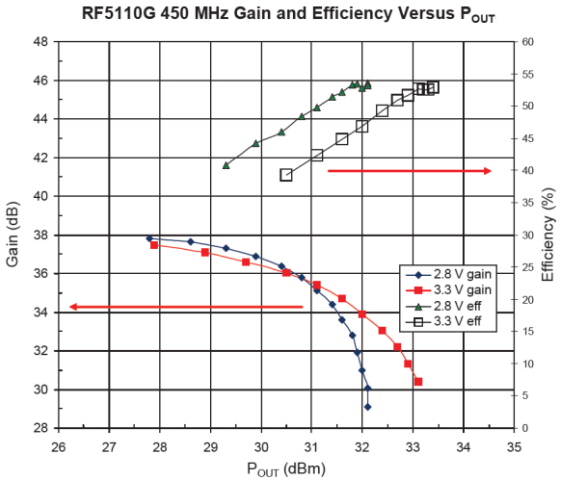


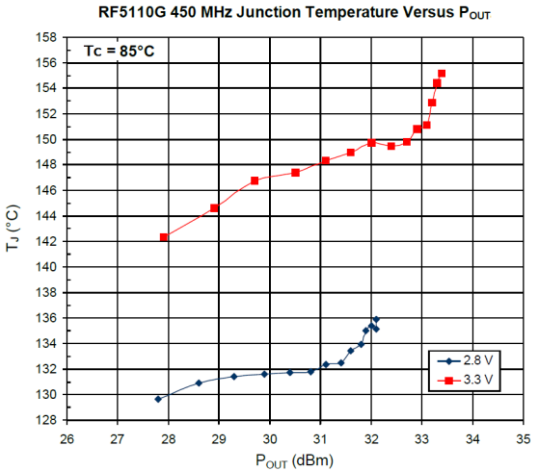


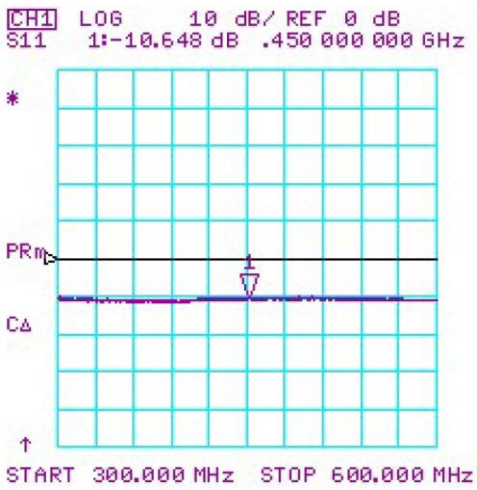


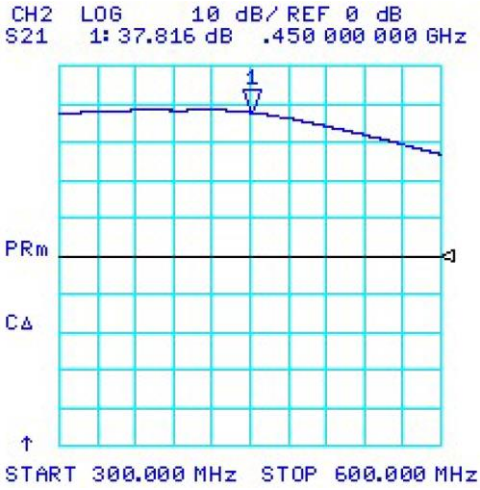


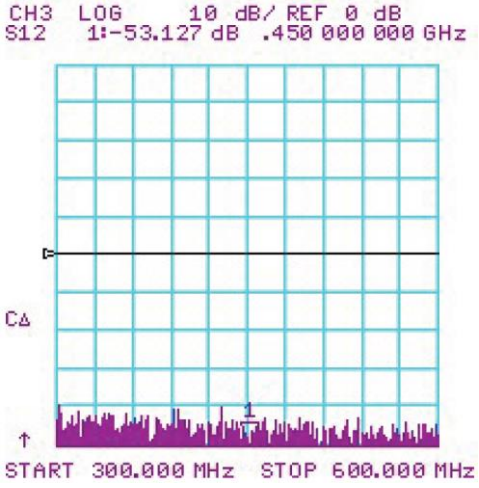
Performance Plots – 450 MHz

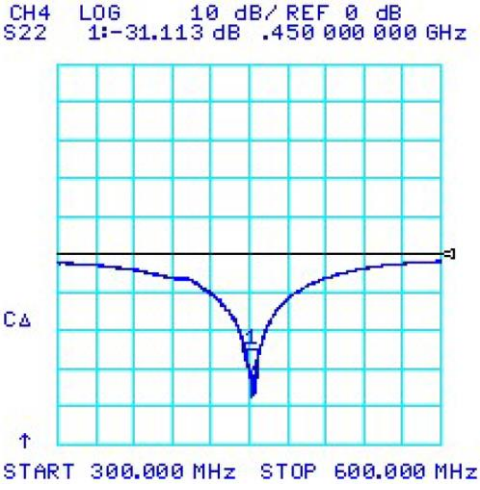






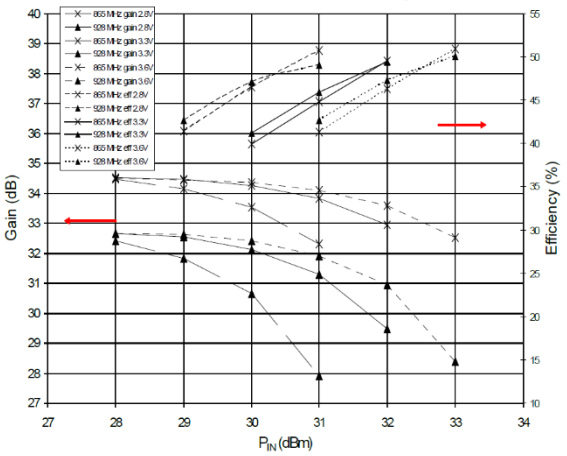




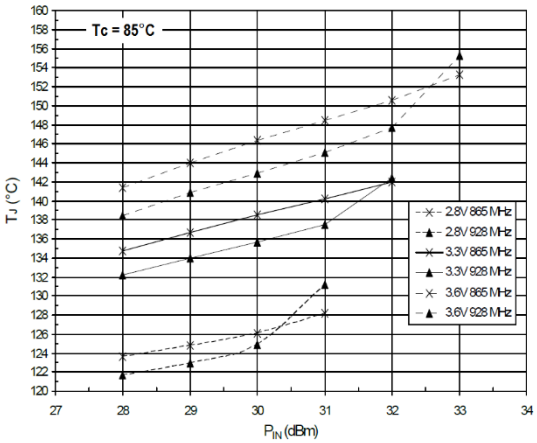


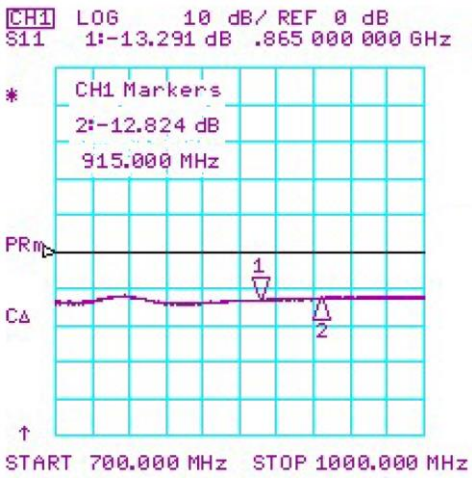
Performance Plots – 865 MHz to 925 MHz

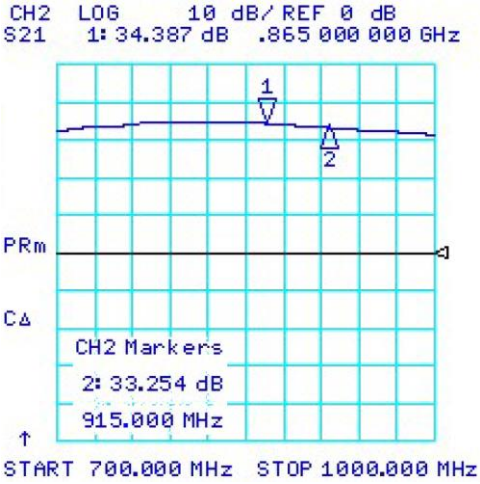
RF5110G 865 MHz to 928 MHz Gain and Efficiency Versus Pout

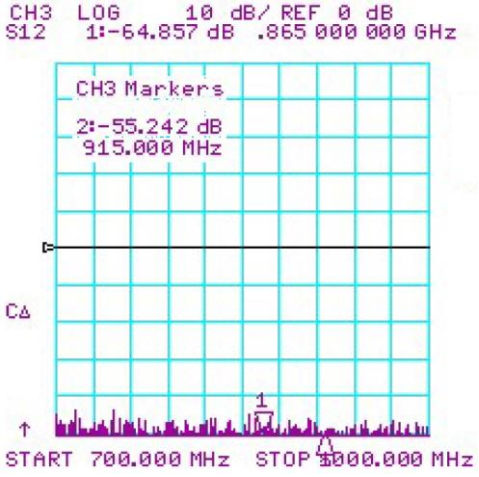


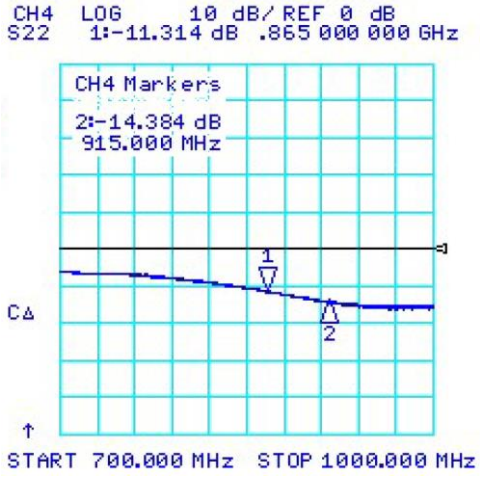
RF5110G 865 MHz to 928 MHz Junction Temperature Versus Pout



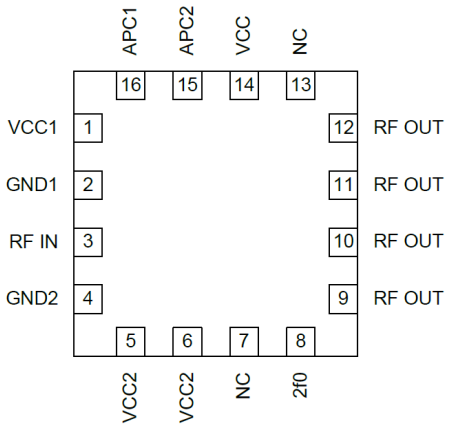




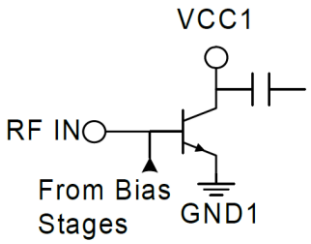
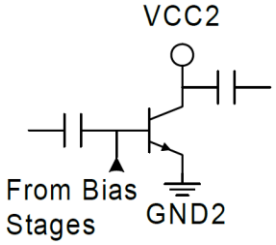
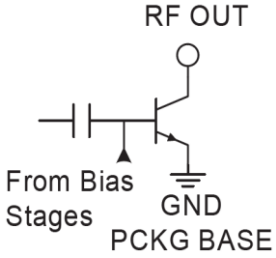




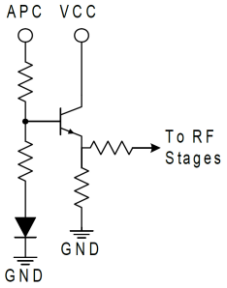
Pad Configuration and Description



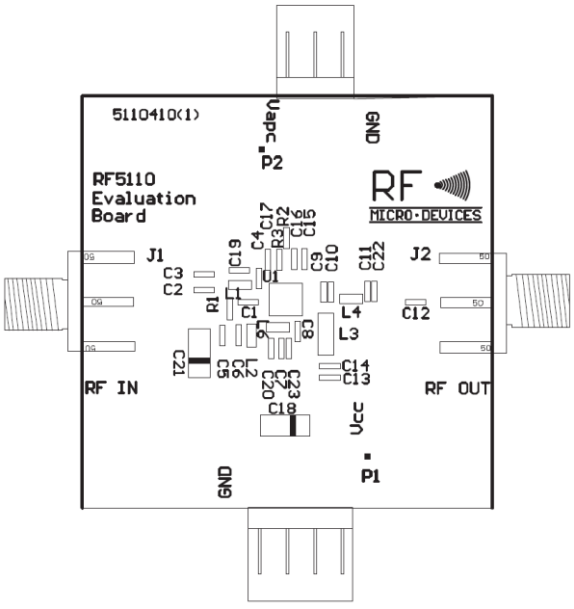
Top View

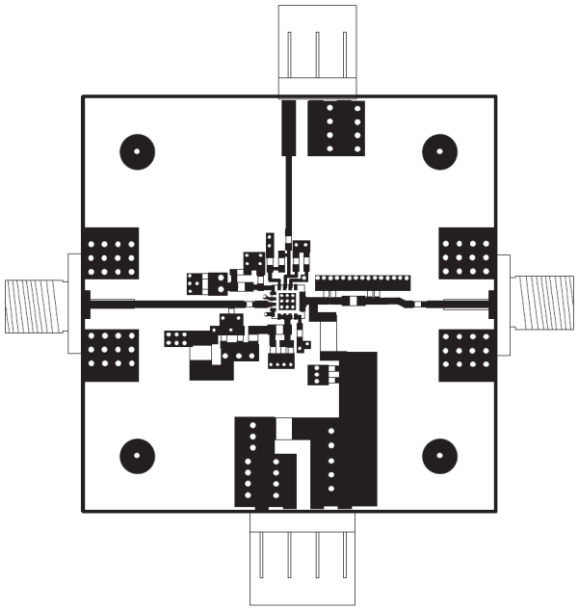
Pad No.	Label	Description	Interface Circuit
1	VCC1	Power supply for the pre-amplifier stage and interstage matching. This pin forms the shunt inductance needed for proper tuning of the interstage match. Refer to the application circuit for proper configuration. Note that position and value of the components are important.	
2	GND1	Ground connection for the pre-amplifier stage. Keep traces physically short and connect immediately to the ground plane for best performance. For stability concert, this pin requires dedicated ground via holes to the ground plane to minimize any common inductance.	
3	RF IN	RF Input. This is a 50Ω input, but the actual impedance could be affected by the interstage matching network connected on pin 1. An external DC blocking capacitor is required.	
4	GND2	Ground connection for the driver stage. To minimize the noise power at the output, it is recommended to connect this pin with a trace of about 40mil long to the ground plane. This will slightly reduce the small signal gain. For stability concert, this pin requires dedicated ground via holes to the ground plane to minimize any common inductance.	
5, 6	VCC2	Power supply for the driver stage and interstage matching. This pin requires a shunt inductance for proper interstage matching. Please refer to the application schematic for proper configuration.	
7, 13	NC	Not connected.	
8	2F0	Connection for the second harmonic trap. This pin is internally connected to the RF OUT pins. With the bonding wire together with an external capacitor form a series resonator. It should provide a second harmonic short termination to improve amplifier efficiency and reduce spurious outputs.	
9, 10, 11, 12	RF OUT	RF Output and power supply for the output stage. Bias voltage for the final stage is provided through this wide output pins. An external matching network is required to provide the optimum performance.	

Pad Configuration and Description (continue)

Pad No.	Label	Description	Interface Circuit
14	VCC	Power supply for the bias circuits.	
15	APC2	Power Control for the output stage. See pin 16 for more details.	
16	APC1	Power Control for the driver and pre-amplifier stages. When this pin is "low," all circuits shut off. A "low" is typically 0.5V or less at room temperature. A shunt bypass capacitor is required. For a typical power control operation, the V_{APC1} is about 1.0V for -10dBm to 2.6V for +35dBm RF output power. The maximum power that can be achieved depends on the actual output matching; see the application circuit for more details.	
Backside Paddle	GND	RF/DC ground. Ground connection for the output stage. This pad should be connected to the ground plane by ground via holes directly under the device. A short path is required to obtain optimum performance, as well as to provide a good thermal path to the PCB for maximum heat dissipation.	

Evaluation Board PCB Information

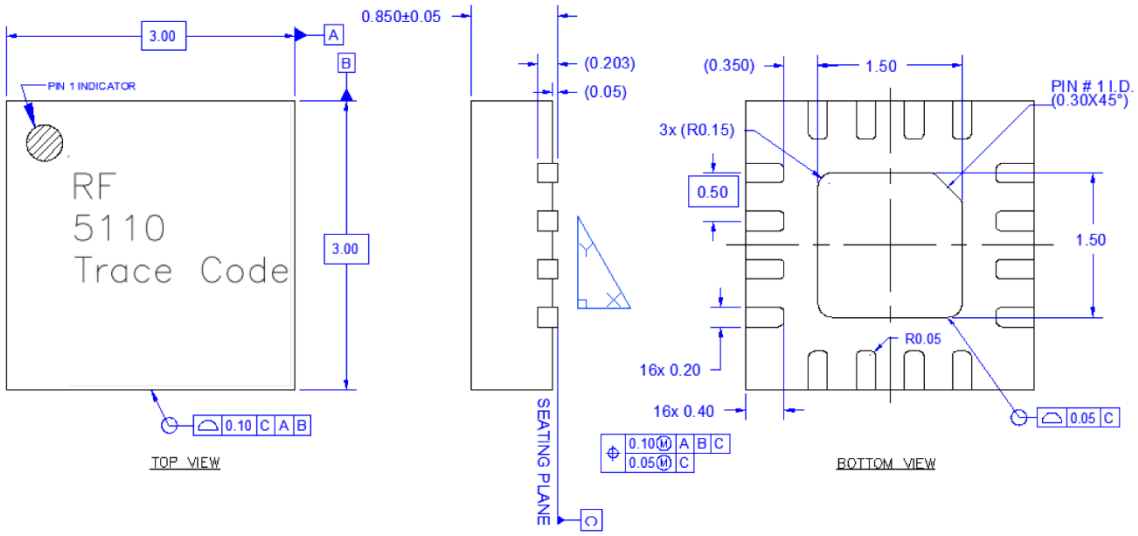




Evaluation Board: Size 2.0” x 2.0”; Material FR-4; Multi-Layer; Thickness 0.032”

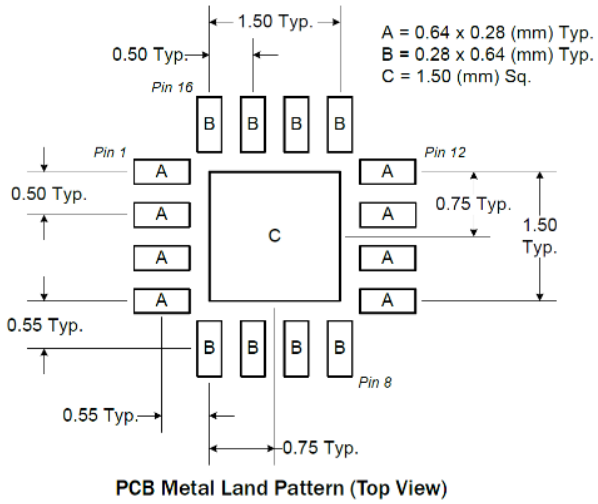
Package Marking and Dimensions

Marking: Part Number – RF5110
Trace Code – Assigned by sub-contractor

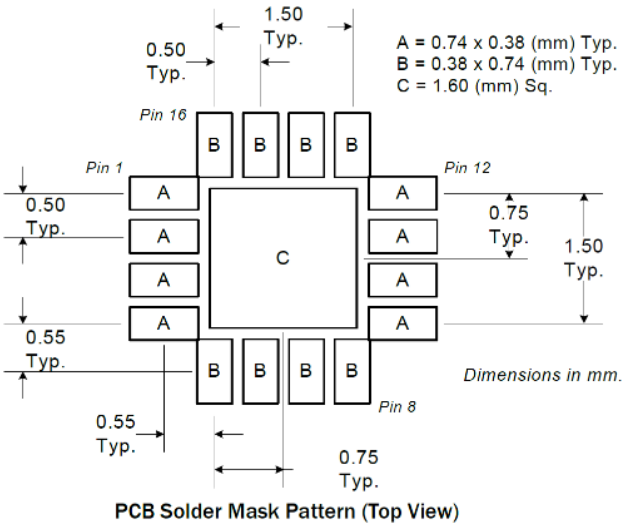


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: Matte Sn

PCB Mounting Pattern



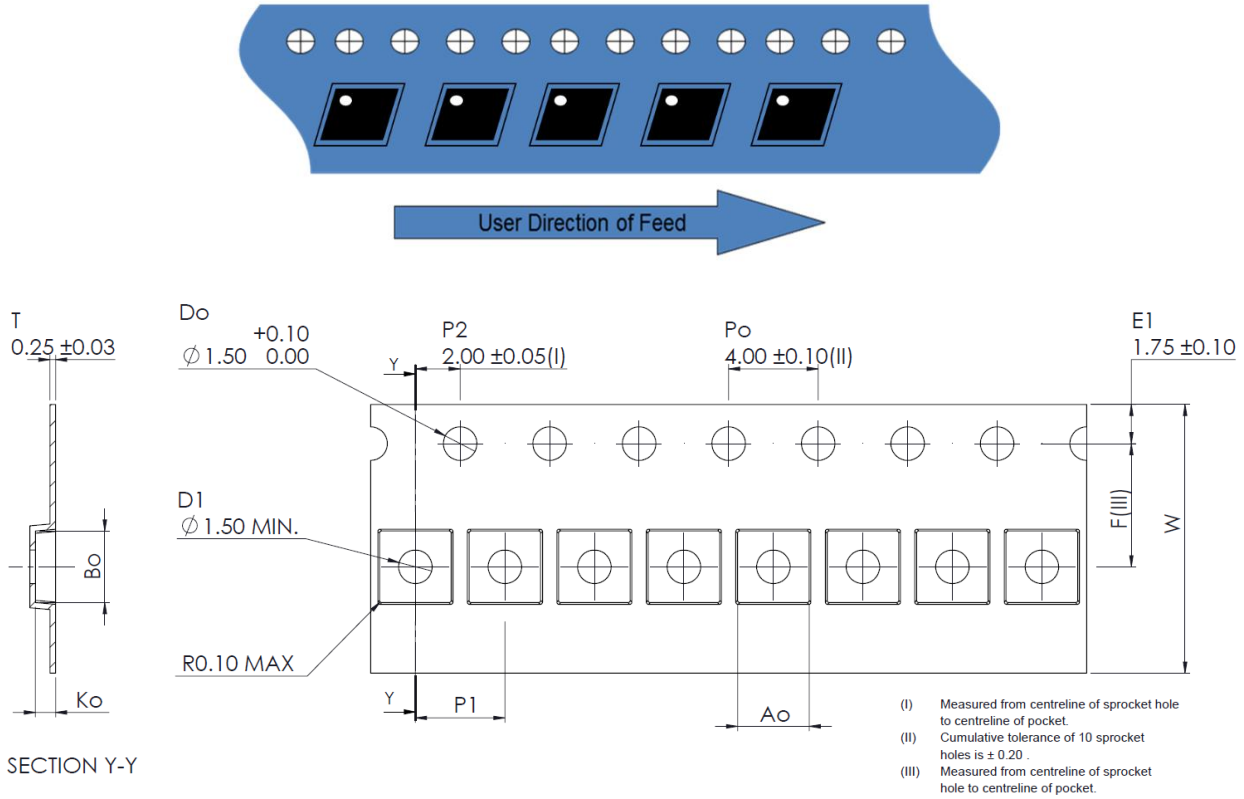
PCB Metal Land Pattern (Top View)



PCB Solder Mask Pattern (Top View)

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. ground via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. 0.203 mm to 0.330 mm finished hole size and 0.5 mm to 1.2 mm grid pattern recommended.
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

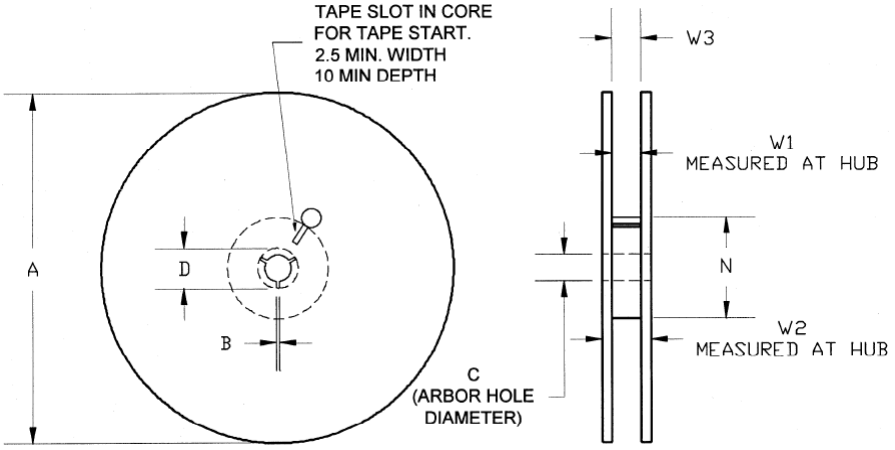
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.125	3.20
	Width	B0	0.125	3.20
	Depth	K0	0.040	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

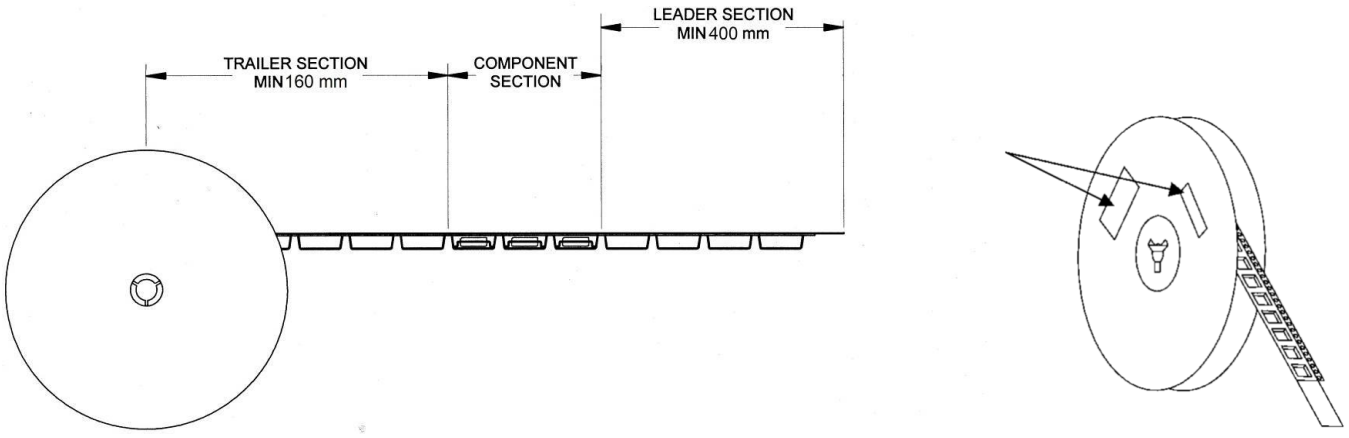
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.