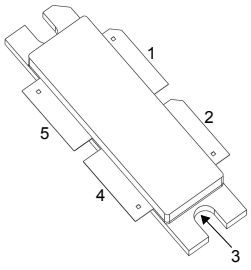
RF5L052K0CB4

Datasheet

2000 W, 50 V, HF to 500 MHz RF power LDMOS transistor



D4E

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Product status link
RF5L052K0CB4

Product summary	
Order code	RF5L052K0CB4
Marking	5L052K0
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L052K0CB4	108 MHz	50 V	2000 W	19.5 dB	77%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- High breakdown voltage enable class E operation
- On chip RC network enable high stability and ruggedness
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- 30-88 MHz/136-174 MHz ground communication
- 1.6-30 MHz HF transceiver
- Plasma generator
- Particle accelerator
- FM and VHF TV broadcast

Description

The RF5L052K0CB4 is a 2000 W, 50 V, high performance, unmatched LDMOS FET, designed for wideband commercial and industrial applications in the frequency range from HF to 500 MHz. It can be used for both CW and pulse application. It is featured for high power and high ruggedness, suitable for industrial, scientific and medical application, as well as FM radio, VHF TV and aerospace applications.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	110	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.09	°C/W

1. *T_C = 85 °C , P_{OUT} = 2000 W, CW, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	110			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 50 V			1	µA
		V_{GS} = 0 V, V_{DS} = 90 V			1	
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_D = 600 µA	2.3		2.9	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 50 V, I_D = 240 mA		3.25		V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 6 A			460	mV
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV			1	Ω
C_{iss}	Common source input capacitance	V_{GS} = 0 V, V_{DD} = 50 V, f = 1 MHz		640		pF
C_{rss}	Common source feedback capacitance			2.2		pF
C_{oss}	Common source output capacitance			218		pF

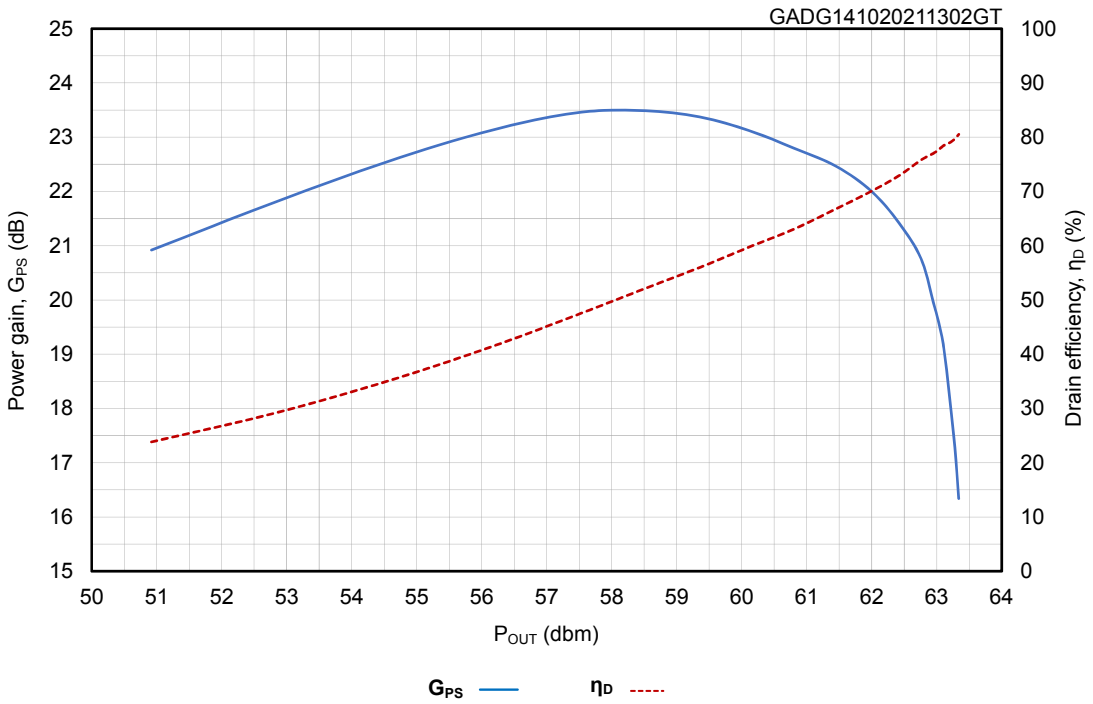
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				500	MHz
P_{OUT}	Output power	f = 108 MHz, 3 dB compression	-	2000		W
G_{PS}	Power gain		-	19.5		dB
η_D	Drain efficiency		-	77		%
VSWR	Load mismatch	P_{OUT} = 2000 W, all phases	-		10:1	

Note: V_{DD} = 50 V, I_{DQ} = 200 mA, pulsed CW, pulse width = 100 µs, duty cycle = 10%.

3 Typical performances

Figure 1. Power gain and drain efficiency vs output power (f = 108 MHz)



Note: V_{DD} = 50 V, I_{DQ} = 200 mA, pulsed CW, pulse width = 100 µs, duty cycle = 10%.

4 Test circuits

Figure 2. **Test circuit layout (f = 108 MHz)**

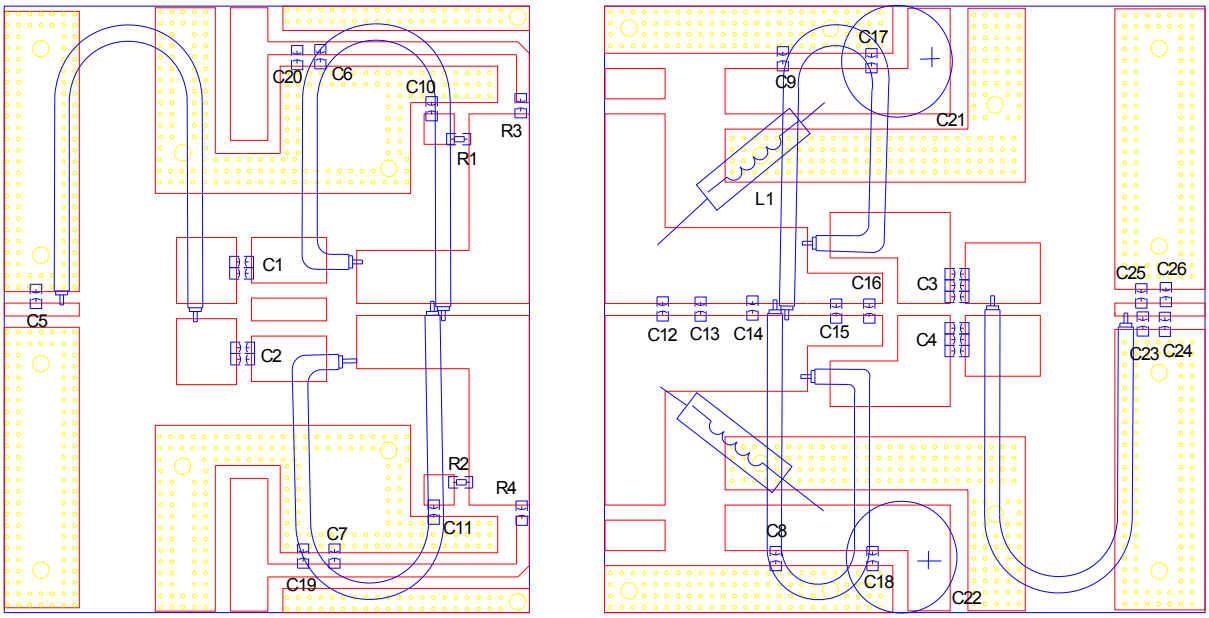


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Figure 3. **Test circuit photo**

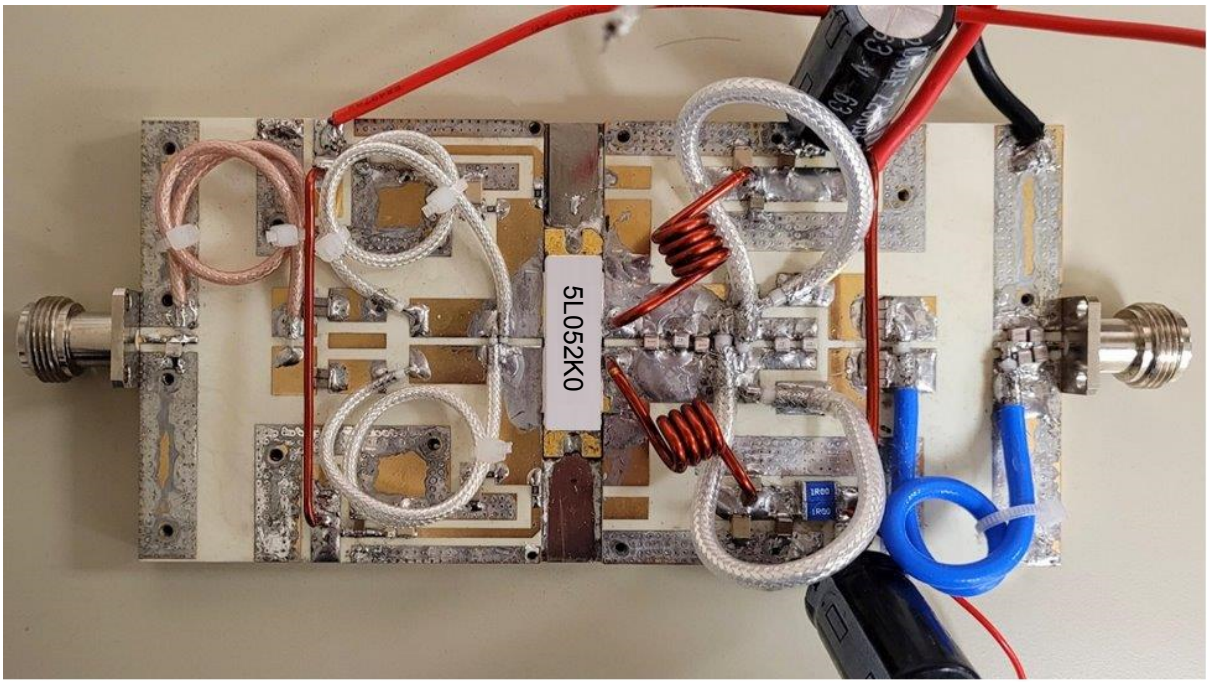

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Table 6. Components list

Component	Value	Reference
C1, C2	470 pF (2x)	ATC800B
C3, C4	470 pF (4x)	ATC800B
C5	33 pF	DLC70B
C6, C7, C8, C9, C10, C11	100 nF	C4532X7R3D103KT000N
C12, C13	20 pF	DLC70B
C14, C15, C16, C23	3.9 pF	DLC70B
C17, C18, C19, C20	10 µF	100 V ceramic capacitor
C21, C22	2200 µF	63 V electrolytic capacitor
R1, R2	16 Ω	0805 chip resistor
R3, R4	470 Ω	0805 chip resistor
T1	50 Ω, 150 mm	SFF-50-1.5
T2, T3	25 Ω, line length = 150 mm, 9:1	SFF-25-1.5
T4, T5	12.5 Ω, line length = 120 mm, 9:1	SFF-12.5-1.5
T6	25 Ω, 150 mm	RG402-3
L1, L2	4 turns, Φ 1 mm	
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B, 1 oz.	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 D4E package information

Figure 4. D4E package outline

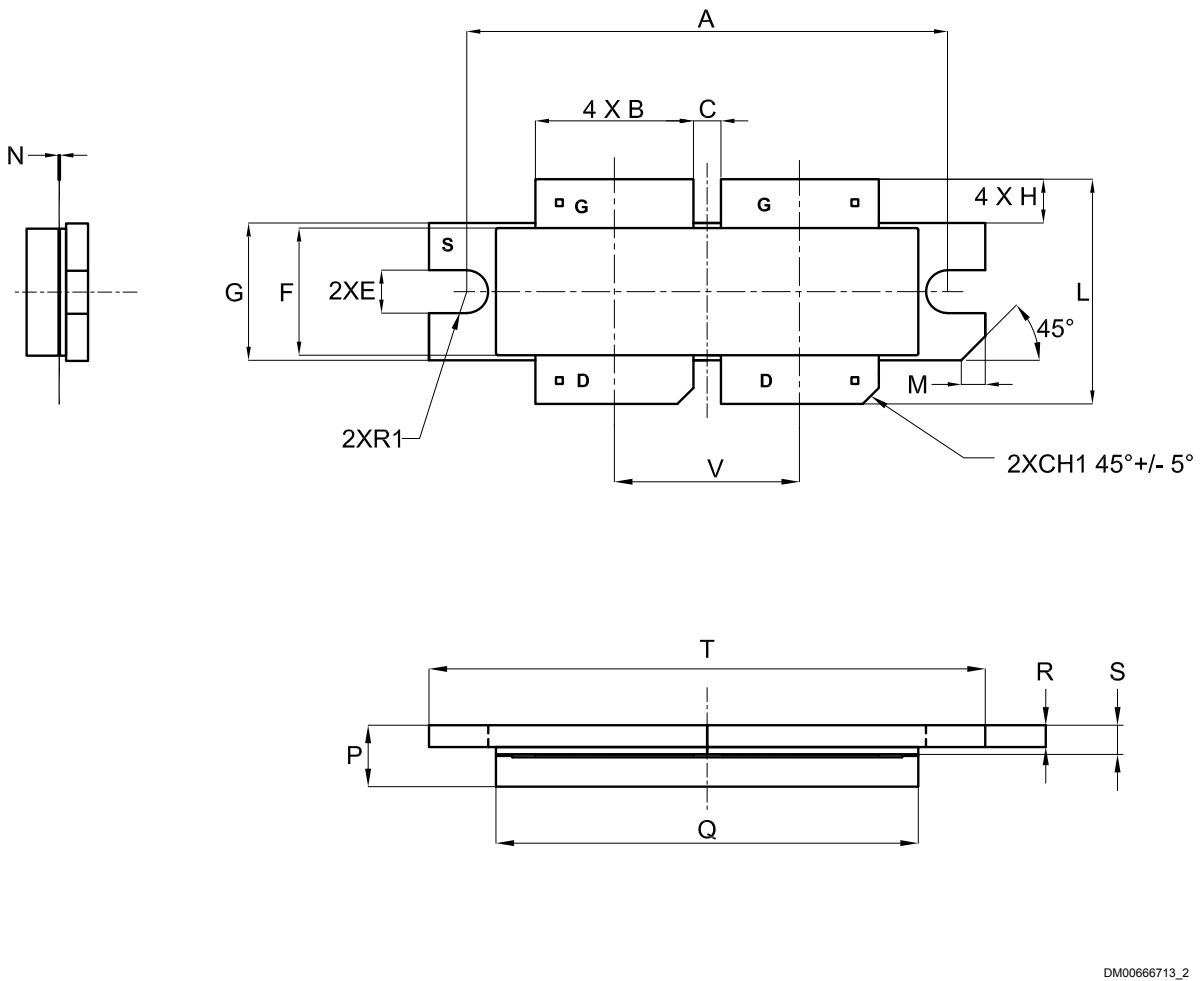
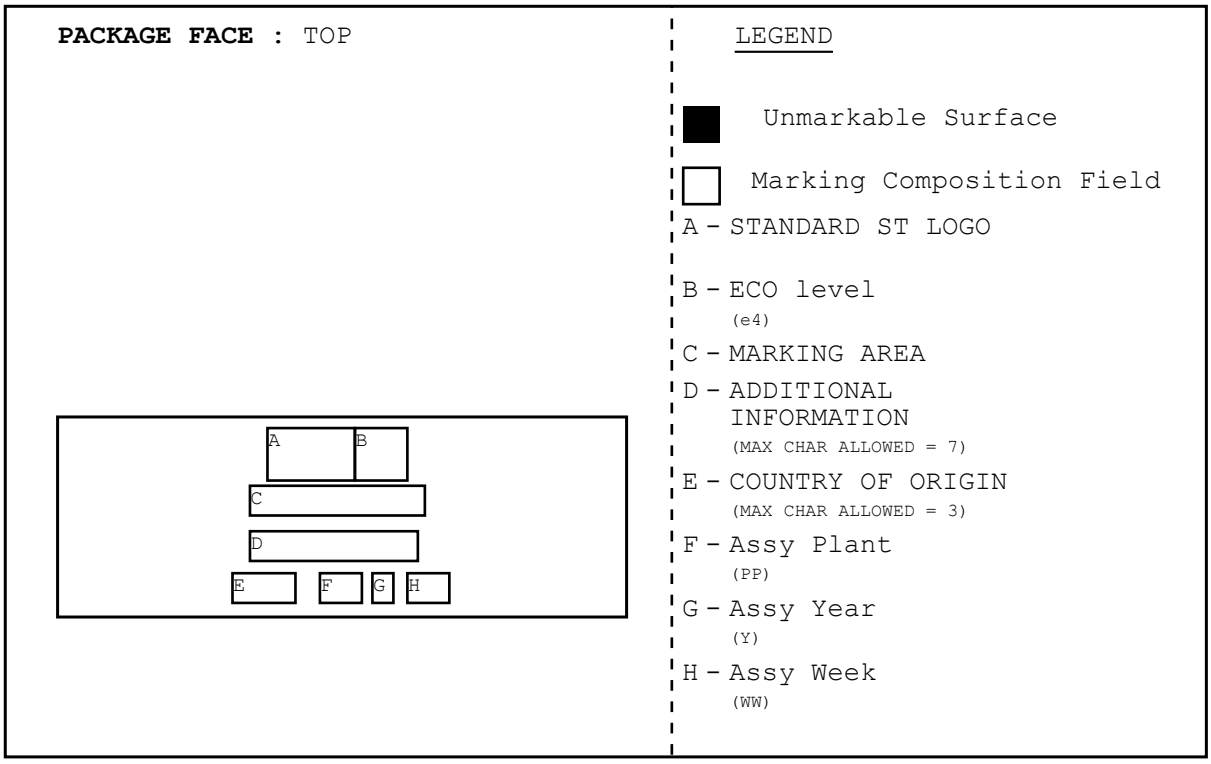


Table 7. **D4E package mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

5.2 Marking information

Figure 5. **Marking composition**



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Revision history

Table 8. **Document revision history**

Date	Version	Changes
24-May-2021	1	First release.
15-Oct-2021	2	Updated Description on cover page. Updated Table 1. Absolute maximum ratings (T_C = 25 °C). Updated Section 2 Electrical characteristics. Added Section 3 Typical performances. Updated Figure 3. Test circuit photo and Table 6. Components list.

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