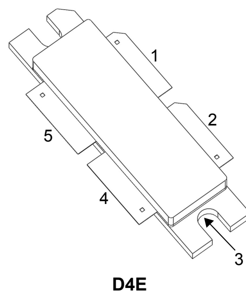
RF5L08600CB4

Datasheet

650 W, 50 V, 0.4 to 1 GHz RF power LDMOS transistor



D4E

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Product status link
RF5L08600CB4

Product summary	
Order code	RF5L08600CB4
Marking	5L08600
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L08600CB4	650 MHz	50 V	650 W	19.5 dB	67%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched pair transistors in push-pull configuration
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Wideband lab amplifier from 0.4 to 1 GHz
- Digital UHF TV 470-860 MHz
- 650 MHz particle accelerator
- 915 MHz RF energy applications

Description

The RF5L08600CB4 is a 650 W, 50 V, high performance, internally matched LDMOS FET, designed for multiple applications in the frequency range from 0.4 to 1 GHz.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	115	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC} [(1)]	Thermal resistance, junction-to-case	0.16	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	H3A
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	110	-		V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 50 V		-	1	µA
		V_{GS} = 0 V, V_{DS} = 90 V		-		
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_{DS} = 600 µA	2.0	-	2.8	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 1 V, I_{DS} = 100 mA	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 10 A		-	1.4	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV	0.1	-	2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV		-	1	Ω

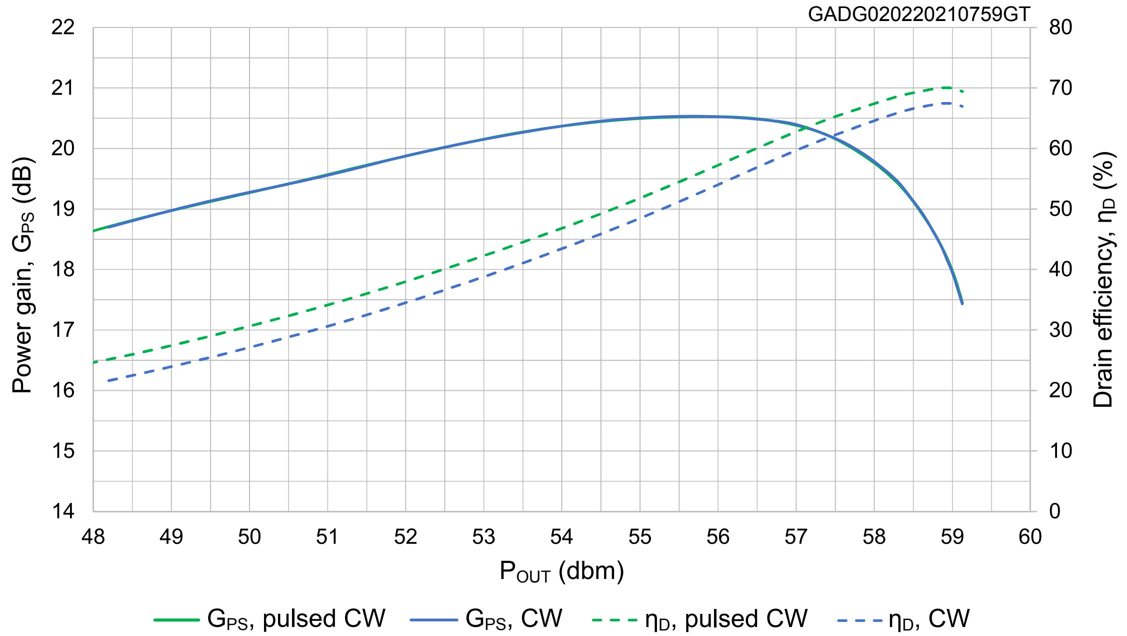
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	f = 650 MHz, 1 dB compression	-	650		W
G_{PS}	Power gain		-	19.5		dB
η_D	Drain efficiency		-	67		%
VSWR	Load mismatch	P_{OUT} = 650 W, all phases	-		10:1	

Note: *V_{DD} = 50 V, I_{DQ} = 110 mA, pulsed CW, pulse width = 100 µs, duty cycle = 10%.*

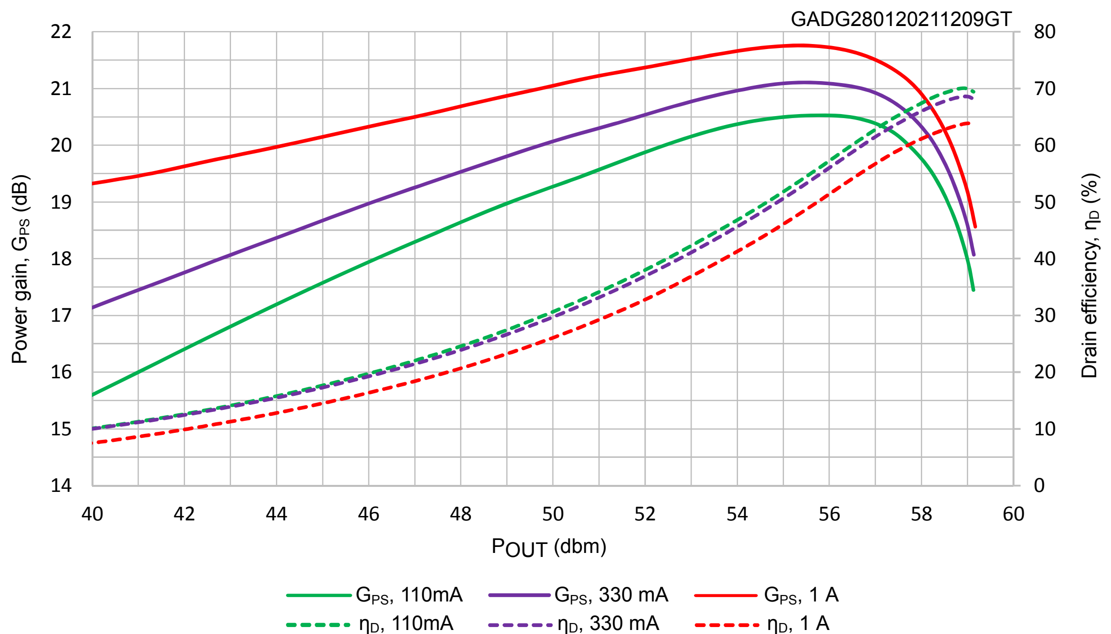
3 Typical performances

Figure 1. Power gain and drain efficiency versus output power (pulsed CW and CW)



Note: V_{DD} = 50 V, I_{DQ} = 110 mA, f = 650 MHz (pulse width = 100 µs, duty cycle = 10% in case of pulsed CW).

Figure 2. Power gain and drain efficiency versus output power at different I_{DQ} (110 mA, 330 mA, 1 A)



Note: V_{DD} = 50 V, f = 650 MHz, pulsed CW, pulse width = 100 µs, duty cycle = 10%.

4 Test circuits

Figure 3. Test circuit layout

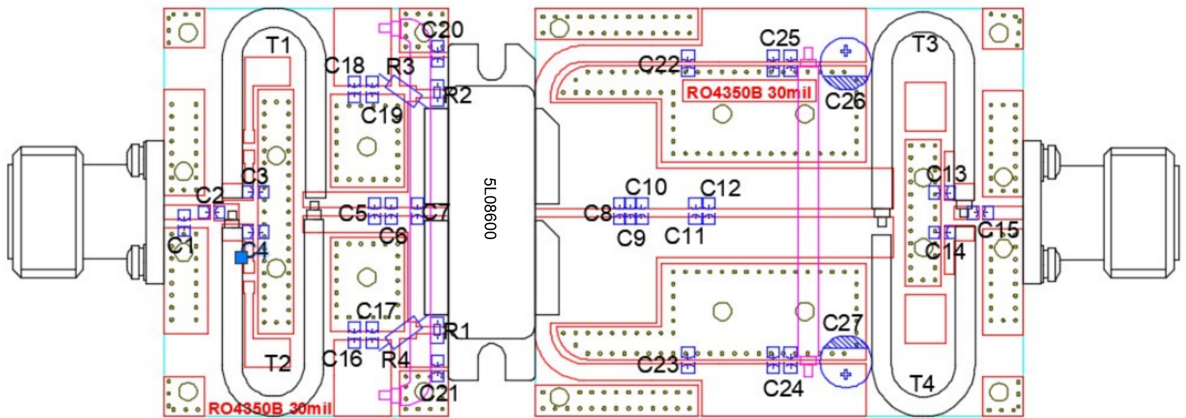
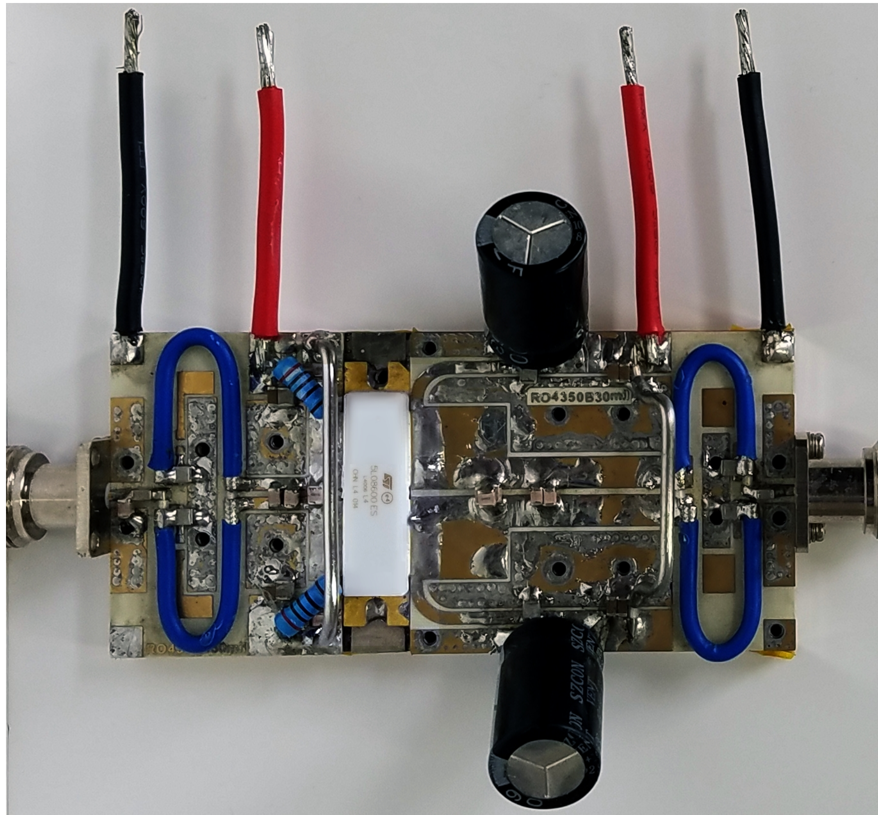


Table 6. Components list

Component	Description	Size	Reference
C1	8.2 pF	0.110" x 0.110"	DLC70B
C2, C17, C19	47 pF	0.110" x 0.110"	ATC800B
C3, C4, C13, C14	130 pF	0.110" x 0.110"	ATC800B
C5	2 pF	0.110" x 0.110"	DLC70B
C6, C7	18 pF	0.110" x 0.110"	DLC70B
C8, C9, C10	4.7 pF	0.110" x 0.110"	DLC70B
C11	15 pF	0.110" x 0.110"	DLC70B
C12	3.3 pF	0.110" x 0.110"	DLC70B
C15, C22, C23	110 pF	0.110" x 0.110"	ATC800B
C20, C21	220 pF	0.110" x 0.110"	DLC70B
C16, C18, C24, C25	10 µF, 50 V		Ceramic multilayer capacitor
C26, C27	1000 µF, 63 V		Electrolytic capacitor
R1, R2	16 Ω	1210	Chip resistor
R3, R4	200 Ω		Metal film resistor
T1, T2, T3, T4	25 Ω, line length = 50 mm		SF-086-25
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B, 1 oz. copper		

Figure 4. **Test circuit photo (f = 650 MHz)**



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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 D4E package information

Figure 5. D4E package outline

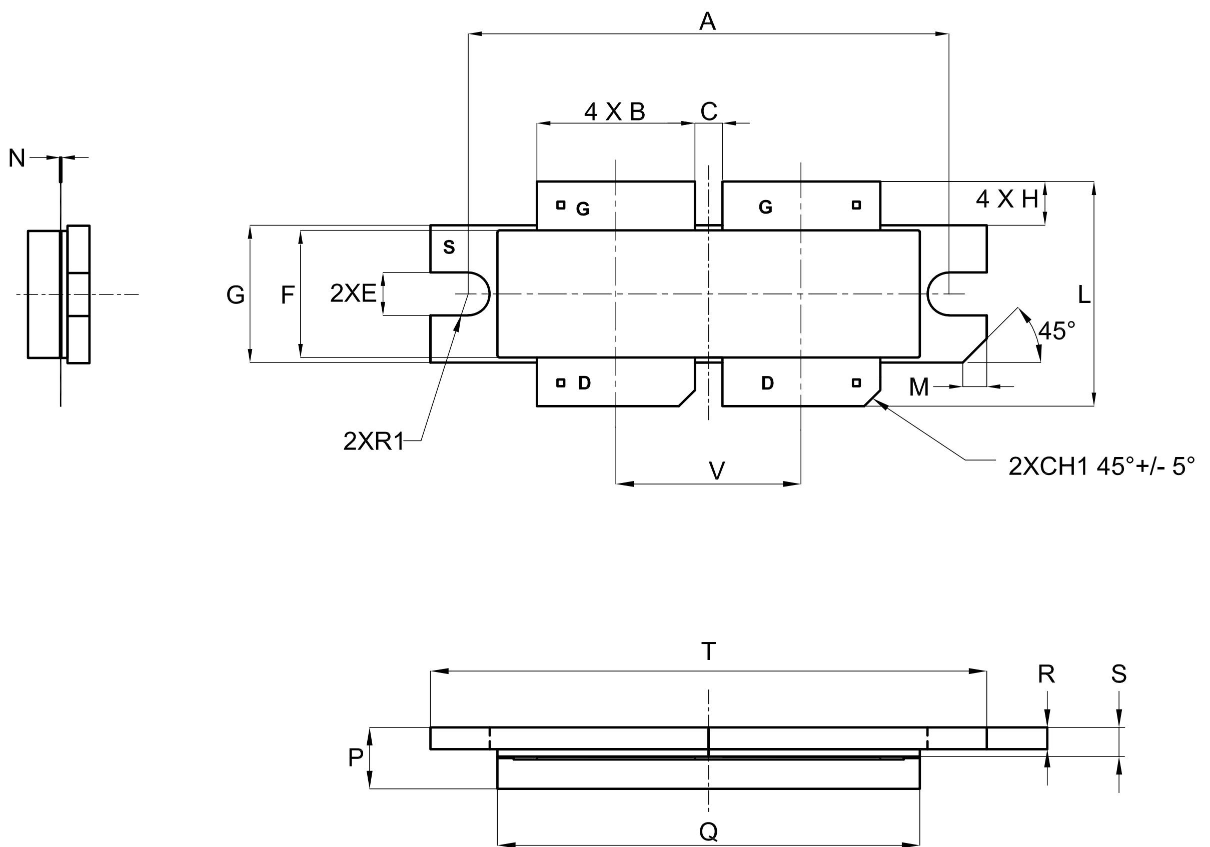
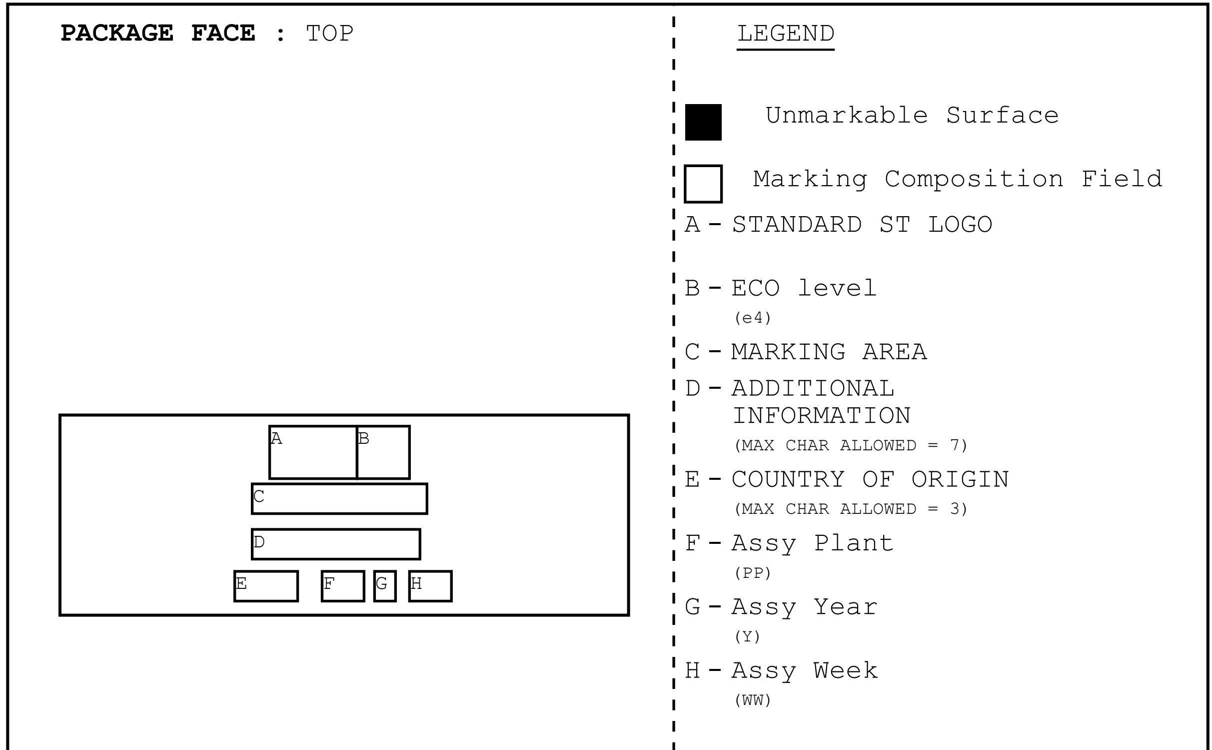


Table 7. D4E package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

5.2 Marking information

Figure 6. Marking composition



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Revision history

Table 8. Document revision history

Date	Version	Changes
02-Feb-2021	1	First release.
20-May-2021	2	Updated Features and Device summary in cover page. Updated Table 3. ESD protection. Updated Table 4. Static (per side). Updated Table 6. Components list. Added Section 5.2 Marking information.

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