



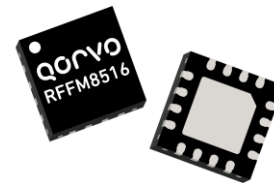
RFFM8516

5.0 GHz Wi-Fi Front-End Module

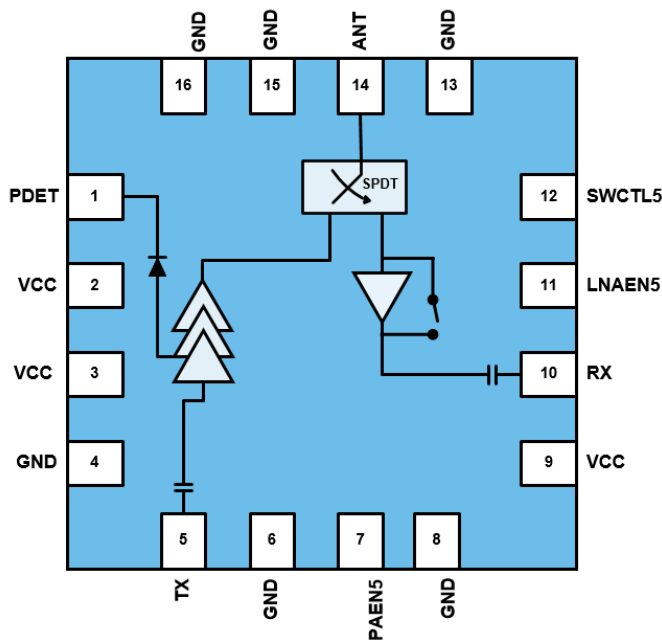
16 Pin 2.3 x 2.3 mm QFN Package

Product Overview

The RFFM8516 provides a complete integrated solution in a single front end module (FEM) for WiFi 802.11a/n/ac systems. Performance is focused on a balance of efficiency to enable long battery life and linear power that increases the range of connection. It is specifically designed to work with the RFFM8216 to greatly reduce BOM cost in dual band applications. The RFFM8516 integrates a 5 GHz power amplifier (PA), single pole double throw switch (SP2T), LNA with bypass, harmonic and 2.4 GHz Rx filtering and a power detector coupler for improved accuracy.



Functional Block Diagram



Top View

Key Features

- $P_{out} = 17$ dBm, 802.11ac, 80MHz MCS9 at 1.4% (-37 dB)
- High Efficiency
- Internally matched RF input/output to 50 ohms
- Integrated 5 GHz PA, SP2T, LNA with Bypass and PDET
- Integrated 2.4 GHz Rx Filter
- Integrated Power Detector
- High Impedance PA Enable

Applications

- IEEE 802.11a/n/ac WLAN Applications
- Single-Placement RF Front-End Module
- Single-band and Dual-band Wireless LAN Systems
- Portable Battery-Powered Equipment

Ordering Information

Part Number	Description
RFFM8516SB	5 piece sample bag
RFFM8516SQ	25 piece sample bag
RFFM8516SR	7" Reel with 100 pieces
RFFM8516TR7	7" Reel with 2500 pieces
RFFM8516TR7-5K	7" Reel with 5000 pieces
RFFM8516PCB-410	Fully Assembled Evaluation Board w/ 5-pieces bag

Absolute Maximum Ratings

PARAMETER	CONDITIONS	RATING
Storage Temperature		-40 to 150 °C
DC Supply Voltage	No RF Applied	-0.5 to +6.0 V
PA Enable Voltage		-0.5 to +5.0 V
DC Supply Current		800mA
RF Maximum Input Power (Tx Mode/RX Mode)	CW, 50Ω, VCC = 3.6 V, T = 25 °C	+10 dBm
RF Maximum Input Power (Rx Bypass Mode)	CW, 50Ω, VCC = 3.6 V, T = 25 °C	+25 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	CON	MIN.	TYP.	MAX.	UNITS
Operating Temperature		-20	25	60	°C
Extended Operating Temperature	Functional with reduced performance	-40	-	85	°C
Operating Voltage V _{CC}		3.0	3.6	4.2	V
Extended Operating Voltage V _{CC}	Functional with reduced performance	3.0	-	4.8	V
RF Impedance	All RF ports (single-ended)	-	50	-	Ω
Control Voltage (V-high)	PAEN5 / SWCTL5	2.75	2.9	3.6	V
Control Voltage (V-High)	LNAEN5	2.75	3.3	3.6	V
Control Voltage (V-Low)	PAEN5 / LNAEN5	0	0.1	0.4	V
Control Current (I-High)	PAEN5 / LNAEN5	-	5	135	uA
Control Current (I-Low)	PAEN5 / LNAEN5	-	0.5	1	uA
Leakage/Sleep/Bypass Mode Current	PAEN5 / LNAEN5/SWCTL5 = Low V _{CC} =4.2V	-	2	12	uA

Electrical specifications are measured at nominal operating conditions. Unless noted otherwise.

Logic Truth Table

MODE	PAEN5	LNAEN5	SWCTL5
802.11a/n/ac TX Mode	High	Low	High
802.11a/n/ac RX Gain	Low	High	Low
802.11a/n/ac RX Bypass	Low	Low	Low

Note: PAEN5 pin 7 and SWCTL5 pin 12 can be tied together for all operating modes.

Electrical Specifications – 5 GHz Transmit
($V_{CC}=3.6V$; Temp= $25^{\circ}C$; unless noted otherwise)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Frequency		5180	-	5825	MHz
Small Signal Gain		25	29	-	dB
Gain Flatness	For any 80 MHz bandwidth	-0.5	-	+0.5	dB
Gain Flatness	For entire frequency band	-1.5	-	+1.5	dB
Margin to Spectrum Emission Mask 11a, 6 Mbps	Pout = 21.0 dBm	-	3.0	-	dB
Margin to Spectrum Emission Mask 11n, MCS0 HT20	Pout = 21.0 dBm	-	3.0	-	dB
Margin to Spectrum Emission Mask 11ac, MCS0 VTH80	Pout = 20.0 dBm	-	3.0	-	dB
11n, MCS7 HT20	Output Power	+18.5	+19	-	dBm
	DEVM	-	-34	-29.6	dB
11ac, MCS9 VTH80	Output Power	+16.5	+17	-	dBm
	DEVM	-	-37	-35	dB
Current 11a, 6 Mbps	Pout = 21.0 dBm	-	300	350	mA
Current 11n, MCS7 HT20	Pout = 19.0 dBm	-	270	320	mA
Current 11ac, MCS9 VTH80	Pout = 17.0 dBm	-	250	300	mA
Harmonics (2f ₀)	Pout = 21.0 dBm; 6 Mbps	-	-	-30	dBm/MHz
Harmonics (3f ₀)	Pout = 21.0 dBm; 6 Mbps	-	-	-38	dBm/MHz
PA Switching Speed	TX Normal Mode	-	400	-	nS
ANT to RX Isolation	TX Normal Mode	24	28	-	dB
Return Loss – TX Port		10	15	-	dB
Return Loss – ANT Port		10	20	-	dB
Power Detector Voltage Low	Pout = 5 dBm	-	0.2	-	V
Power Detector Voltage High	Pout = 22 dBm	-	-	0.8	V

Operating condition is +25degC at 3.6V unless otherwise noted.

Electrical Specifications – 5.0 GHz Receive
($V_{CC}=3.6V$; Temp= $25^{\circ}C$; unless noted otherwise)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Frequency		5180	-	5825	MHz
Gain		10	12.5	-	dB
Gain Flatness	For any 80 MHz bandwidth	-1.5	-	+1.5	dB
Noise Figure		-	2.5	3.5	dB
Current		-	9	16	mA
P1dB		-8	-5	-	dBm
LNA Switching Speed		-	400	-	nS
Return Loss RX Port		10	20	-	dB
Return Loss ANT Port		5	8	-	dB

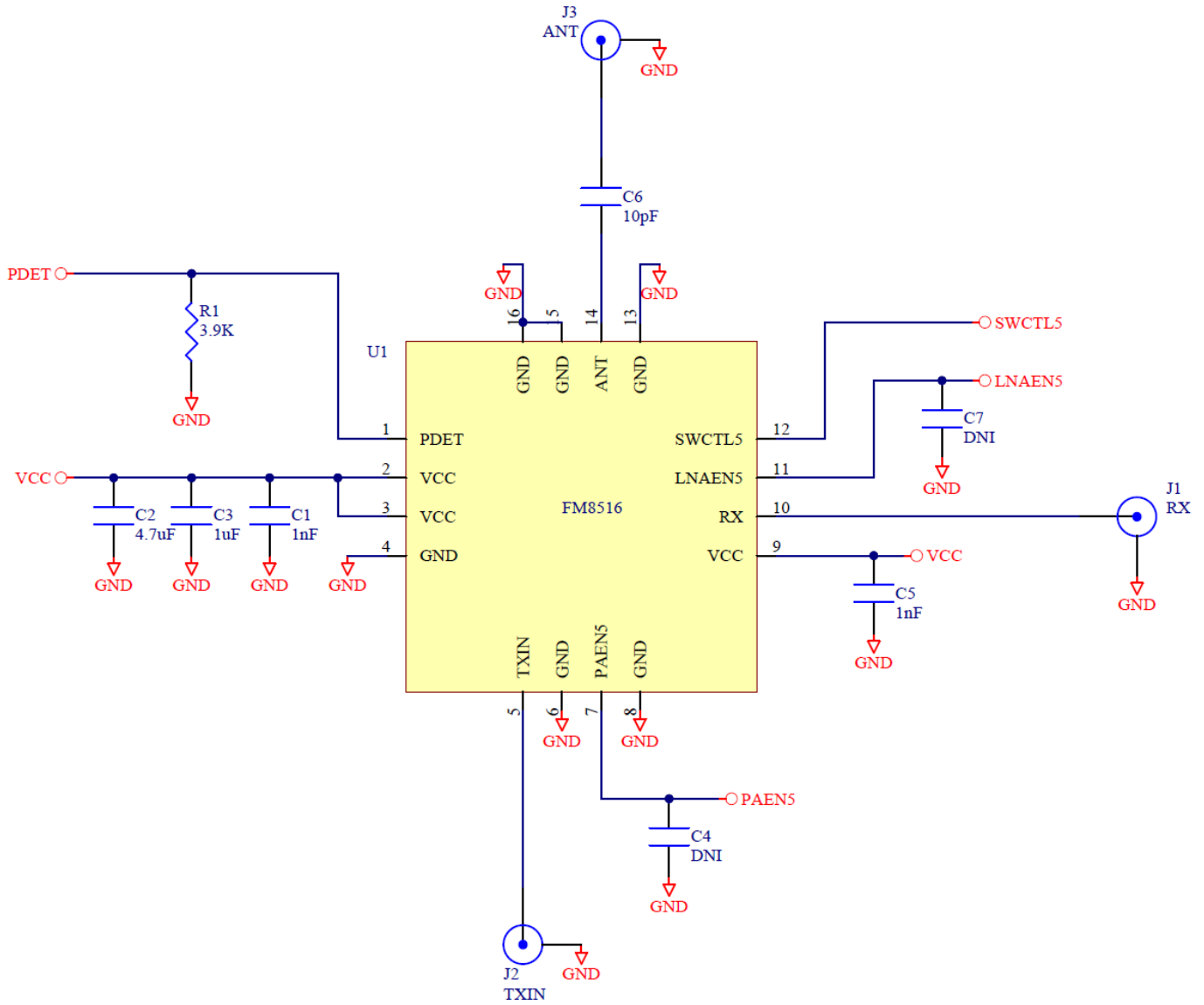
Operating condition is $+25^{\circ}C$ at $+3.6V$ unless otherwise noted.

Electrical Specifications – 5.0 GHz Rx Bypass
($V_{CC}=3.6V$; Temp= $25^{\circ}C$; unless noted otherwise)

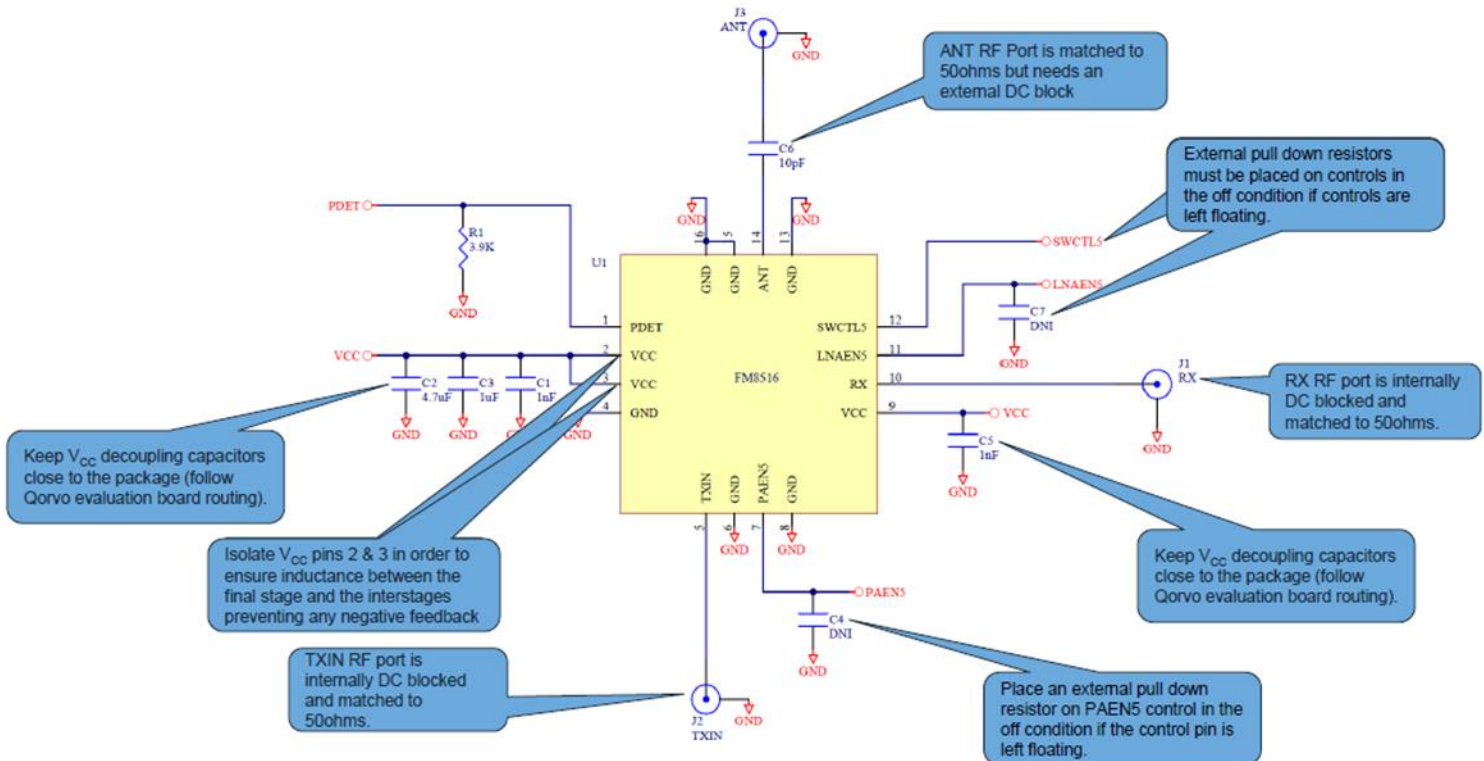
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Frequency		5180	-	5825	MHz
Gain		-3.5	- 4.5	-7	dB
Gain Flatness	For any 80 MHz bandwidth over the frequency range. LNA Disabled.	-1.0	-	+1.0	dB
Return Loss – RX Port		10	12	-	dB
Return Loss – ANT Port		14	20	-	dB

Test condition is $+25^{\circ}C$ at $+3.6V$ unless otherwise noted.

Application Circuit Schematic



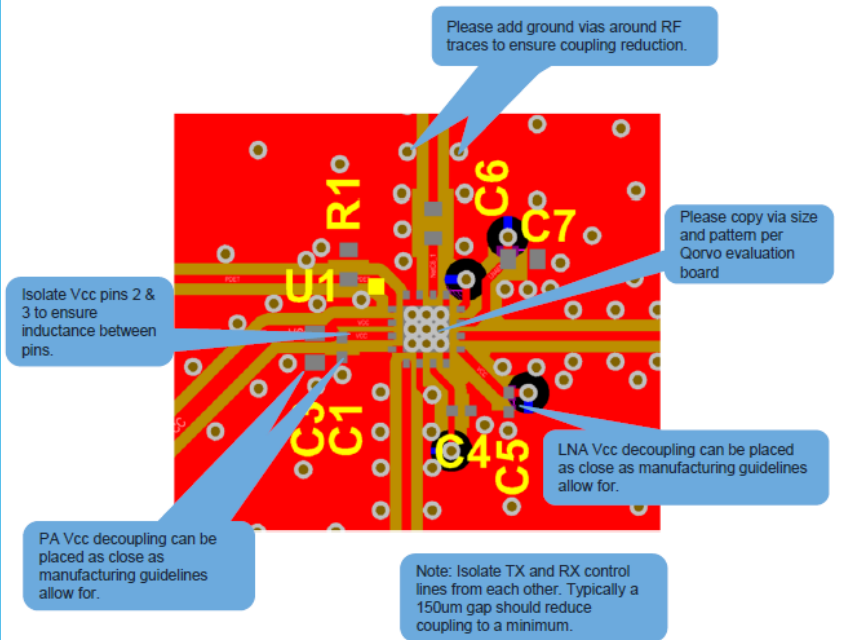
Application Circuit Schematic



Evaluation Board Layout

Key Notes:

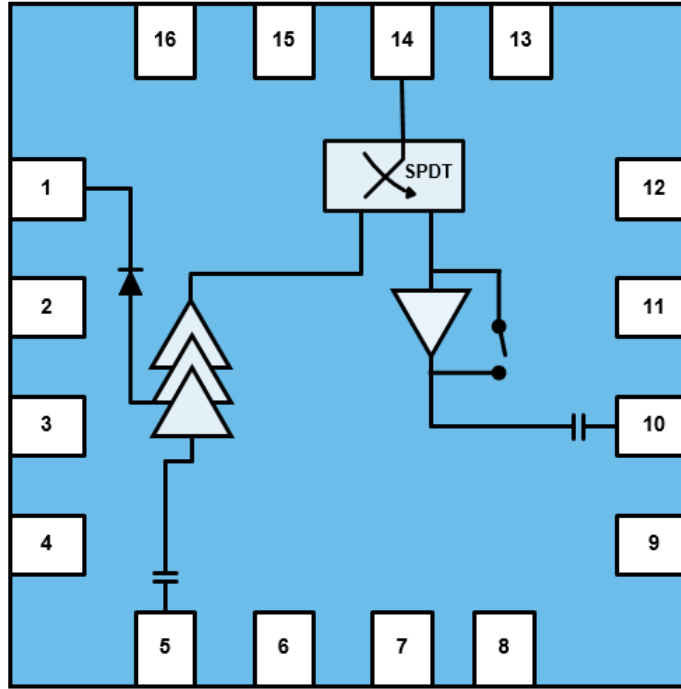
1. It is recommended to fully populate the ground slug with as many thermal vias as possible and to add ground vias around RF traces. The vias size used on the QORVO evaluation board is 12mil hole size and 22mil diameter.
2. Isolate Vcc pins 2 & 3 to ensure inductance between the final stage(pin2) and the interstages(pin3) to prevent negative feedbacks.
3. Route control lines on separate layer, other than the signal layer, whenever possible.
4. Keep a minimum distance of 150um between TX and RX control lines to minimize coupling.
5. In general, follow QORVO evaluation board layout as close as possible. Gerber files are available upon request.



Bill of Material

REF. DES.	QTY	DESCRIPTION	MANUF.	PART NUMBER
PCB	1	PCB, FM8516	Performance Micro	RFFM8516-410(A)
C3	1	CAP, 1uF, 10%, 6.3V, X5R, 0402	Murata	GRM155R60J105KE19D
C1, C5	2	CAP, 1000pF, 10%, 16V, X7R, 0201	Murata	GRM033R71C102KA01D
C2	1	CAP, 4.7uF, +80/-20%, 10V, Y5V, 0805	Taiyo Yuden	CE LMK212F475ZG-T
C6	1	CAP, 10pF, 5%, 50V, COG, 0402	Murata	GRM1555C1H100JZ01E
R1	1	RES, 3.9K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-392JTH
J1, J2, J3	3	CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	Molex	SD-73251-4000
P1	1	CONN, HDR, ST, PLRZD, 6-PIN, 0.100"	AMP	640454-6
C4, C7	N/A	Not Populated	N/A	N/A

Pin Configuration and Description

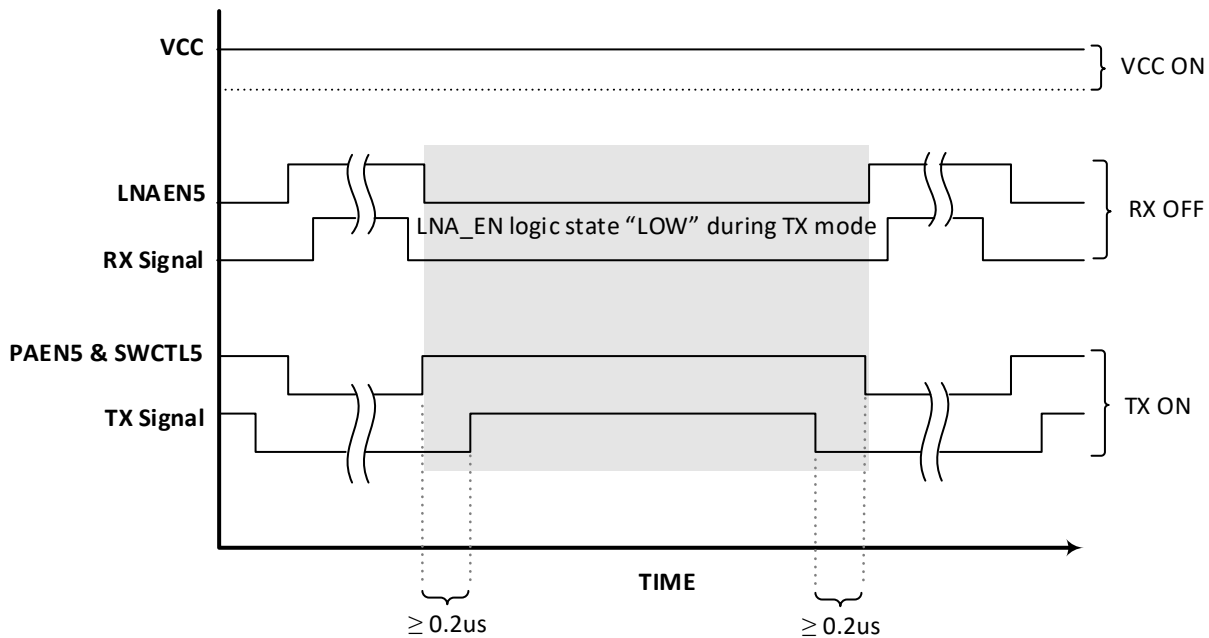


Top View

Pin Number	Label	Description
1	PDET	Power detector output
2,3,9	VCC	DC Power Supply voltage
4,6,8,13,15,16	GND	Ground connection
5	TX	RF input port for the 802.11a/n/ac PA. This port is matched to 50Ω and DC blocked internally
7	PAEN5	Logic control voltage 1. See truth table for proper voltage settings
10	RX	RF output port for the 802.11a/n/ac PA. This port is matched to 50Ω and DC blocked internally
11	LNAEN5	Logic control voltage 2. See truth table for proper voltage settings
12	SWCTL5	Logic control voltage 3. See truth table for proper voltage settings
14	ANT	RF bidirectional antenna port matched to 50Ω. An external DC block is required
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are required.

Timing Diagram

RFFM8516 Transmit Mode
RF/DC Power ON/OFF Sequence



Note:

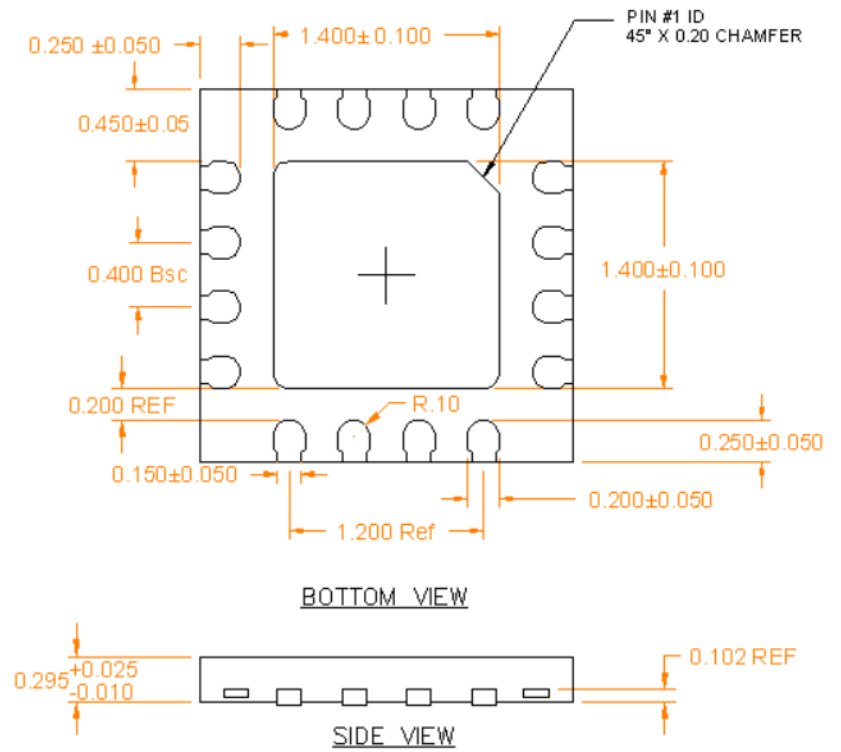
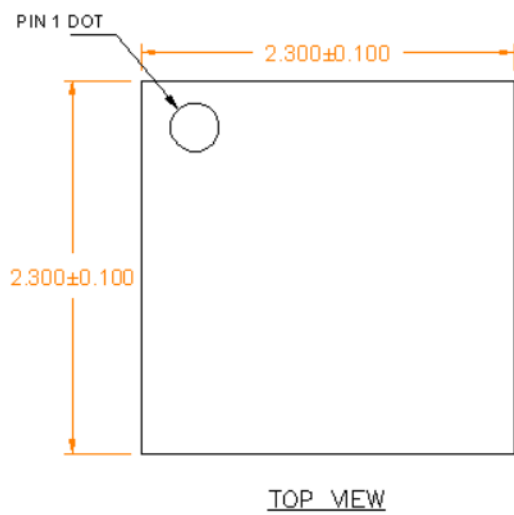
Observe the timing sequence shown in the diagram above and described below. DC, RF, and ON/OFF Time signal levels per datasheet specifications.

- Apply VCC prior to turning PA enable ON
- Turn PA enable ON prior to applying RF signal
- Turn RF signal OFF prior to turning PA enable OFF
- Turn PA enable OFF prior to turning VCC OFF
- TX/RX simultaneous transition is allowed

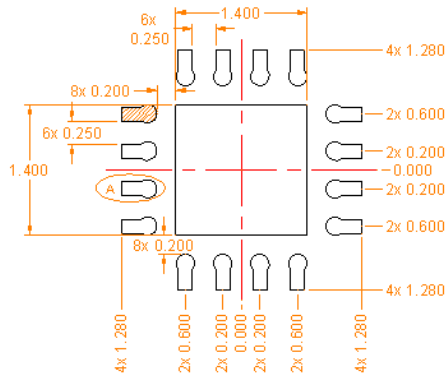
Package Outline Drawing

Marking: Part number – RFFM8516

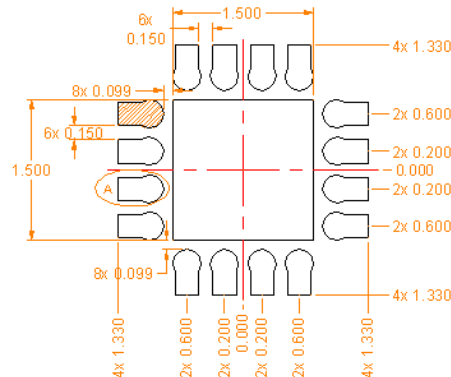
Trace code – XXXX



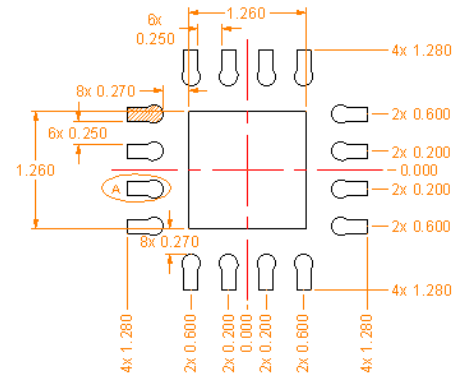
Recommended PCB Patterns



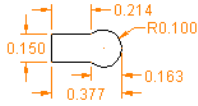
PCB METAL LAND PATTERN



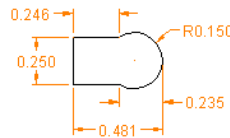
PCB SOLDER MASK PATTERN



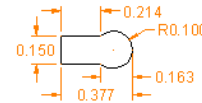
PCB STENCIL PATTERN



DETAIL A
PAD
SCALE: 2X
4X THIS ROTATION
4X ROTATED 180°
4X ROTATED 90° CW
4X ROTATED 90° CCW



DETAIL A
PAD
SCALE: 2X
4X THIS ROTATION
4X ROTATED 180°
4X ROTATED 90° CW
4X ROTATED 90° CCW



DETAIL A
PAD
SCALE: 2X
4X THIS ROTATION
4X ROTATED 180°
4X ROTATED 90° CW
4X ROTATED 90° CCW

Thermal vias for center slug should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout.

Notes:

1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.