# RFSA2023

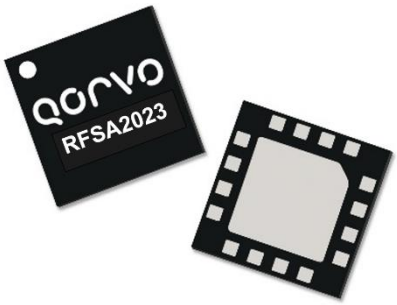
## Voltage Controlled Attenuator

## Product Overview

Qorvo's RFSA2023 is a fully monolithic analog voltage control attenuator (VCA) featuring exceptional linearity over 30dB adjustment range with on-chip temperature compensation.

RFSA2023 incorporates a revolutionary new circuit architecture. It solved the long-standing industry problems of IP3, attenuation range, DC current, bandwidth, and temperature compensation. RFSA2023 is also designed with linear in dB control characteristic. There is no external analog supporting circuitry required. This attenuator is controlled by a single positive variable voltage with DC conditioning circuitry also on-chip. The slope of the attenuation versus control voltage is selectable. The RFSA2023 draws only 1mA current. It is internally matched to 50 Ω and works quite well over its rated ranges of control voltage and frequency.

This game-changing product integrates the complete solution into a small 3mm x 3mm QFN package. That reduces the footprint by 20X in area and reduces the DC power by 10X over the PIN diode approaches.

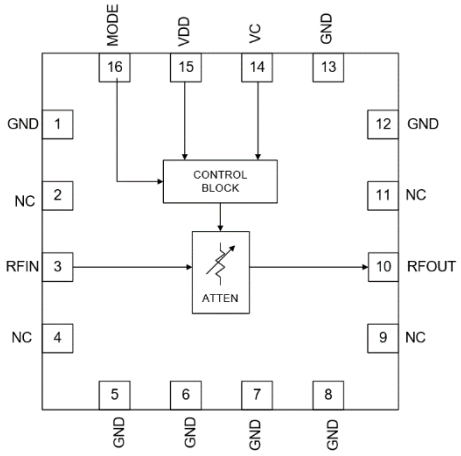



16 Pad 3 x 3 mm QFN Package

## Key Features

- Broadband 50MHz to 6000 MHz
- 30 dB Attenuation Range
- +50 dBm Input IP3
- +80 dBm Input IP2
- >+30 dBm High 1 dB Compression
- 1mA Low Current Consumption
- 3.3V Power Supply
- Linear in dB Control Characteristic
- Internal Temperature Compensation
- 5V Version Available - RFSA2013

## Functional Block Diagram




Top View

## Applications

- Cellular, 3G Infrastructure
- WiBro, WiMax, LTE
- Microwave Radio
- High Linearity Power Control

## Ordering Information

| Part No. | Description |
|---|---|
| RFSA2023TR7 | 2,500 pieces on a 7” reel (standard) |
| RFSA2023PCK-410 | 50 – 6000 MHz Evaluation Board with 5-piece sample bag |

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Storage Temperature | −65 to +150 °C |
| RF Input Power, CW, 50 Ω, T=25 °C | +30 dBm |
| Device Voltage (VDD)<br>Control Voltage (VC)<br>Mode Select Voltage (MODE) | -0.5 to +4 V |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Device Voltage (VDD) | +3.0 | +3.3 | +3.5 | V |
| Device Current (IDD) | | 1 | | mA |
| RF Input Power (RFIN) | | | 27 | dBm |
| $T_{CASE}$ | −40 | | +85 | °C |
| Tj | | | +125 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

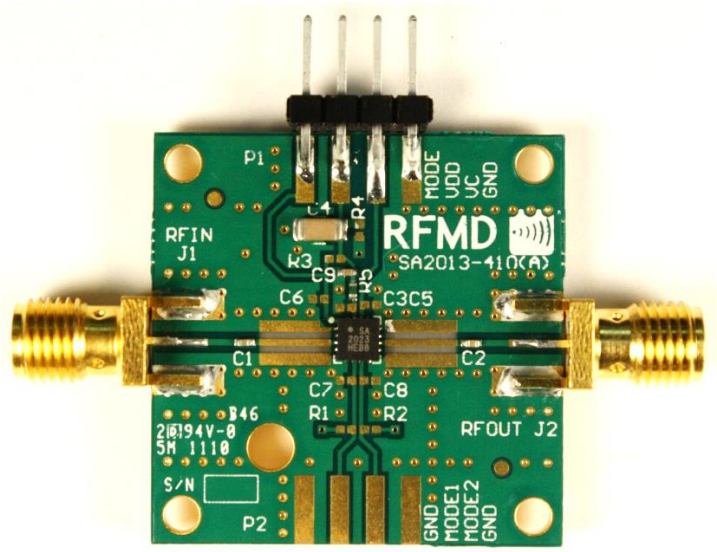
| Parameter | Conditions (1) | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 50 | | 6000 | MHz |
| Test Frequency | | | 2000 | | MHz |
| Minimum Attenuation | Insertion loss | | 2.6 | 3.5 | dB |
| Attenuation Adjustment Range | | 30 | 33.2 | | dB |
| Attenuation Variation | Over temperature with a fixed VC | | 1.7 | | dB |
| Relative Insertion Phase | At 15 dB attenuation relative to the phase at minimum attenuation | | 15.9 | | ° |
| Input / Output Return Loss | | | 15 | | dB |
| Input P1dB | | | 30 | | dBm |
| Input IP3 | Pin + ($IMD3_{dBc}$ / 2) | 45 | 50 | | dBm |
| Input IP2 | Pin + $IMD2_{dBc}$, IMD2 is F1 + F2 | | 80 | | dBm |
| Input IH2 | Pin + $H2_{dBc}$, H2 is second harmonic | | 85 | | dBm |
| Input IH3 | Pin + ($H3_{dBc}$ / 2), H3 is third harmonic | | 55 | | dBm |
| Control Voltage Range | VC | 0.0 | | 2.5 | V |
| VC Control Current | MODE Logic High, and VC 2.5V | | 1.1 | | µA |
| | MODE Logic Low, and VC 2.5V | | 1.7 | | µA |
| Mode Select Voltage | Logic Low | | | 0.4 | V |
| | Logic High | 1.0 | | | V |
| Setting Time | 1dB attenuation adjustment to steady state error ≤ 0.1 dB | | 15 | | µs |
| Thermal Resistance, $\theta_{jc}$ | Junction to case; RF input at RFIN pin | | 45 | | °C/W |

Notes:
1. Test conditions unless otherwise noted: VDD = +3.3 V, Temperature = +25 °C, RF Frequency 2 GHz, 50 Ω system.

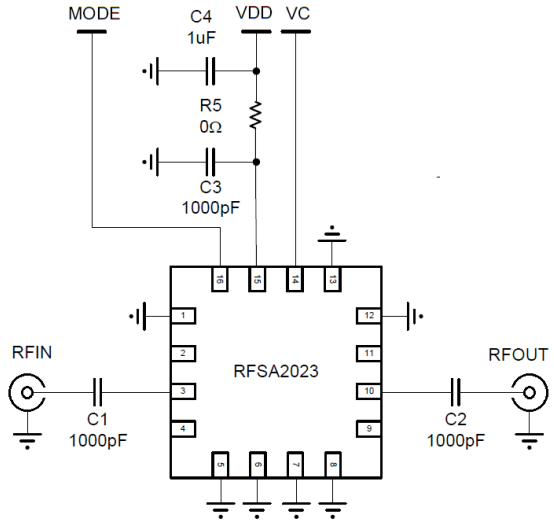
## Mode Select Table

| MODE Logic | MODE Voltage | Attenuator S21 Slope | VC, Minimum Attenuation |
|---|---|---|---|
| High | ≥ 1.0 V | Positive | 2.5 V |
| Low | ≤ 0.4 V | Negative | 0.0 V |

## 50 MHz to 6000 MHz Evaluation Board – RFSA2023PCK-410




Evaluation Board Assembly Top View




Evaluation Board Schematic

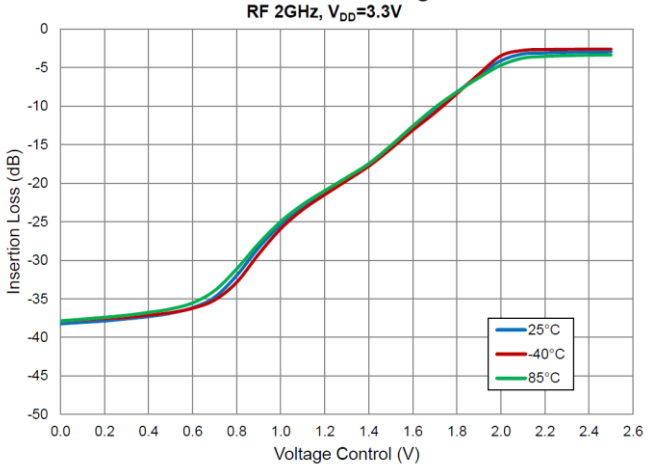
## Bill of Material – RFSA2023PCK-410

| Ref. Des. | Value | Description | Manuf. | Part Number |
|---|---|---|---|---|
| PCB | - | PCB, Printed Circuit Board, SA2013-410 | Qorvo | |
| U1 | - | VCA, Voltage Control Attenuator, 3.3 V | Qorvo | RFSA2023 |
| J1, J2 | - | CONN, SMA End LNCH MINI FLT, 0.068” | Emerson | 142-0741-851 |
| P1 | - | CONN, HDR, ST, 4-PIN, 0.100”, T/H | MOLEX | 22-28-4043 |
| C1, C2, C3 | 1000 pF | CAP, 1000pF, 10%, 25V, X7R, 0402 | Murata | GRM155R71H102KA01D |
| C4 | 1.0 µF | CAP, 1.0 µF, 10%, 25V, X7R, 1206 | Murata | GRM31MR71E105KA01L |
| R5 | 0 Ω | RES, 0 Ω, 5%, 0402 | Kamaya | RMC1/16SJPTH |

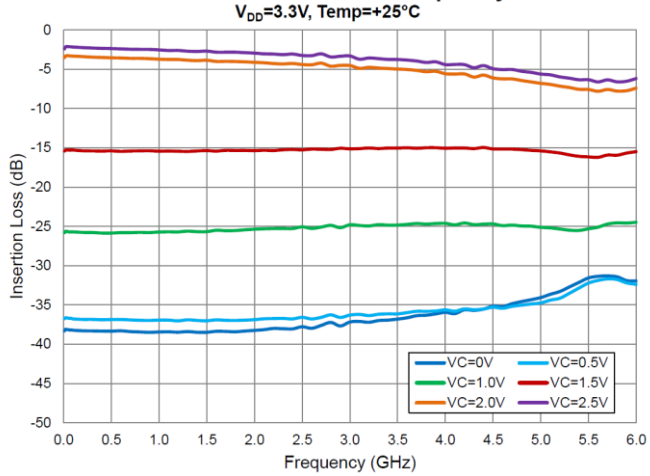
## Performance Plots – Positive S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

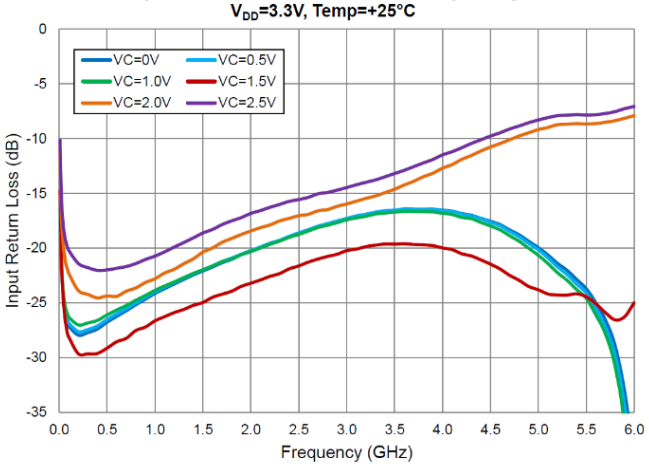
**Insertion Loss versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V



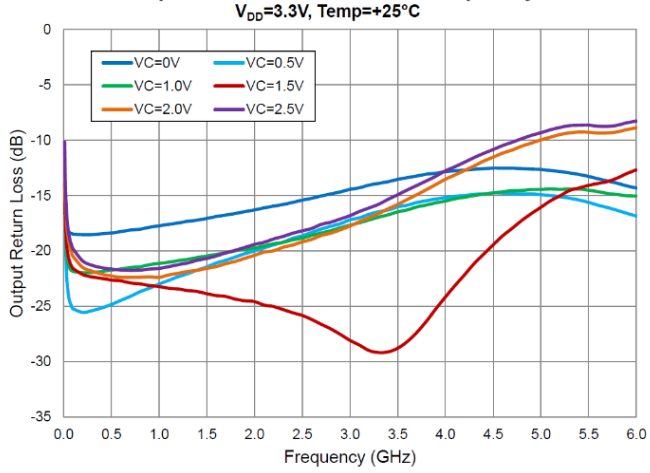

**Insertion Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C



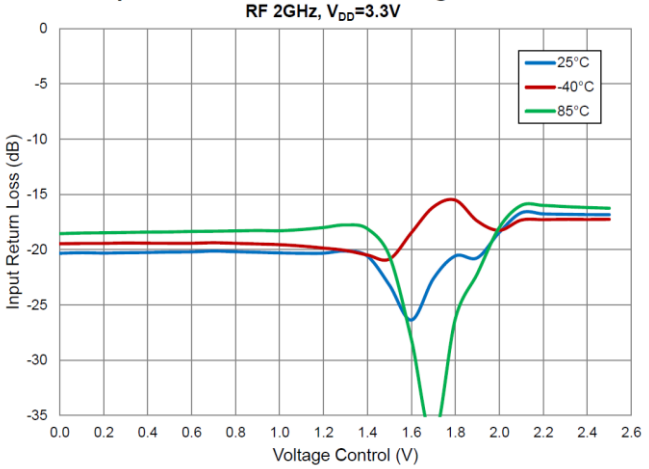

**Input Return Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C



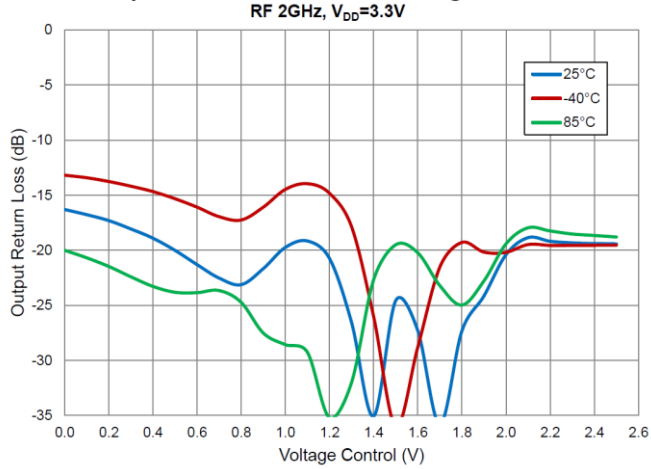

**Output Return Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C




**Input Return Loss versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V



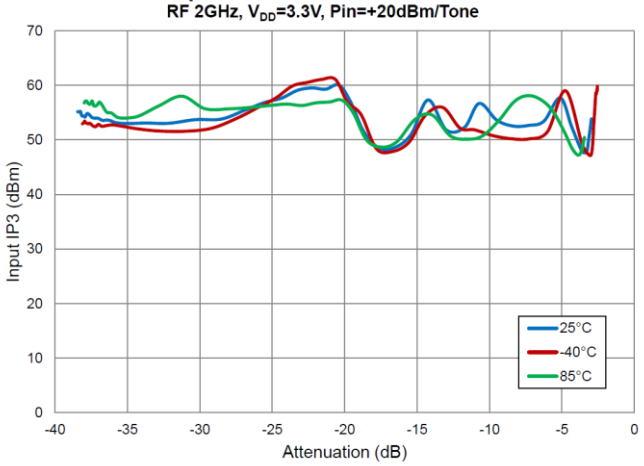

**Output Return Loss versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V



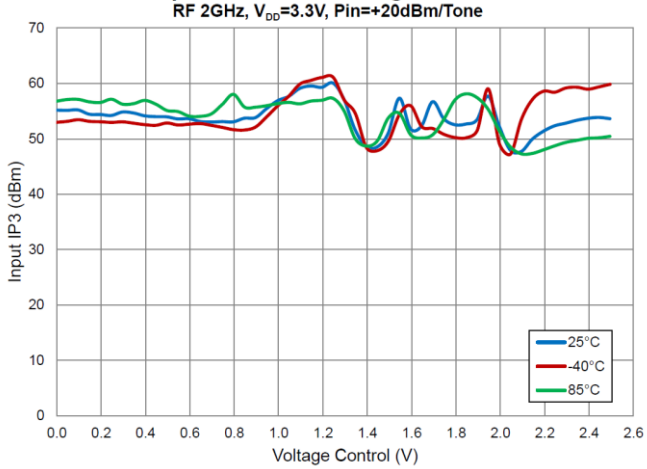
## Performance Plots – Positive S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

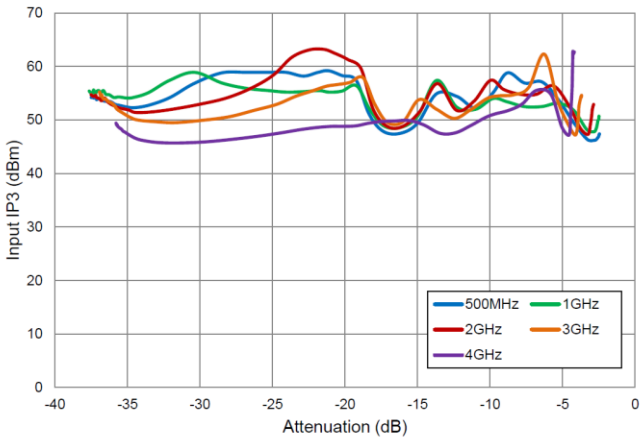
**Input IP3 versus Attenuation**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



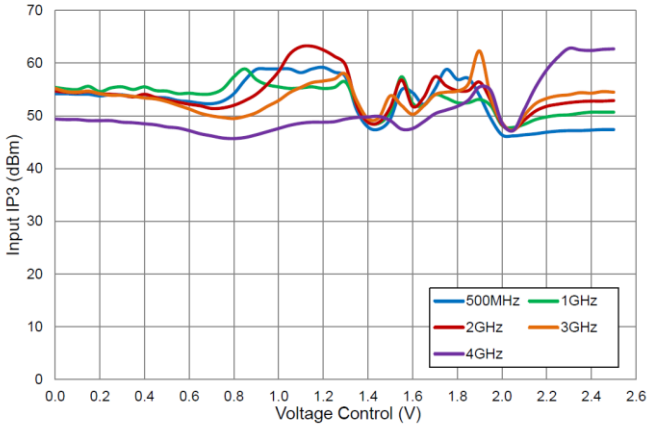

**Input IP3 versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



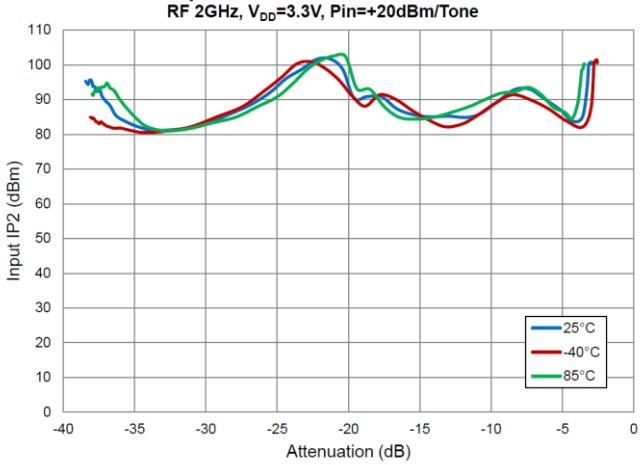

**Input IP3 versus Attenuation**
$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C



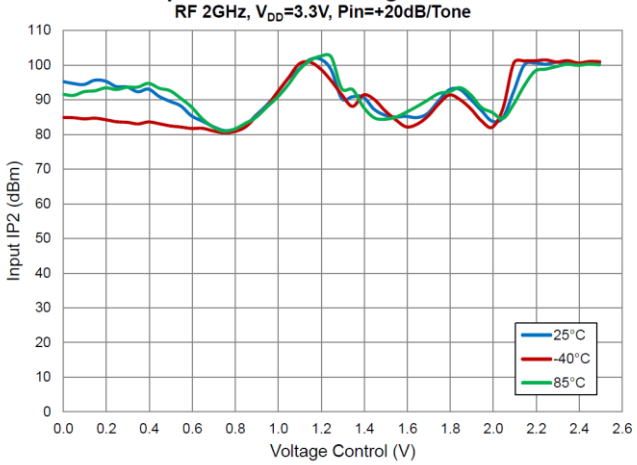

**Input IP3 versus Voltage Control**
$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C




**Input IP2 versus Attenuation**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



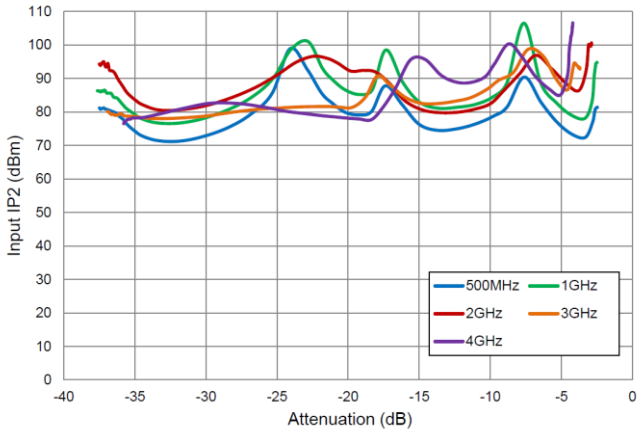

**Input IP2 versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dB/Tone



## Performance Plots – Positive S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

**Input IP2 versus Attenuation**
**$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C**

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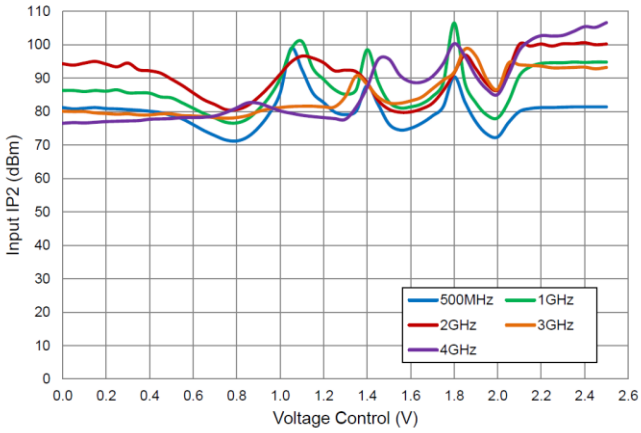
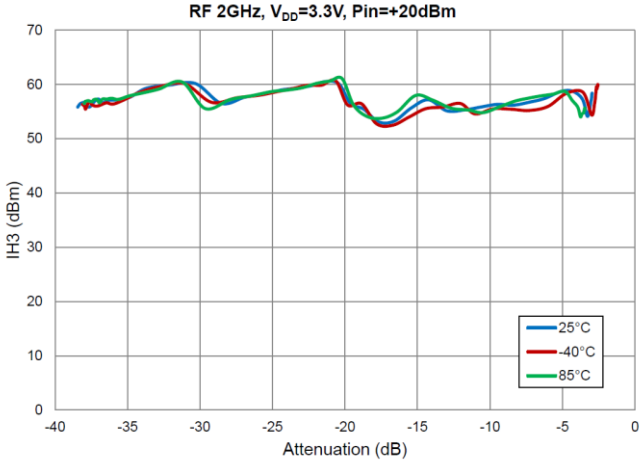
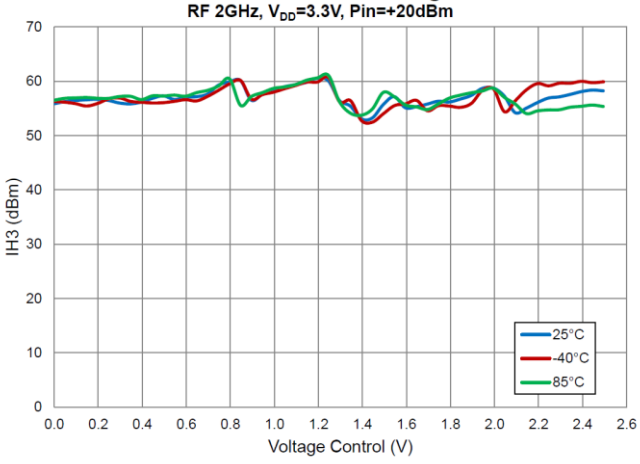
**$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C**



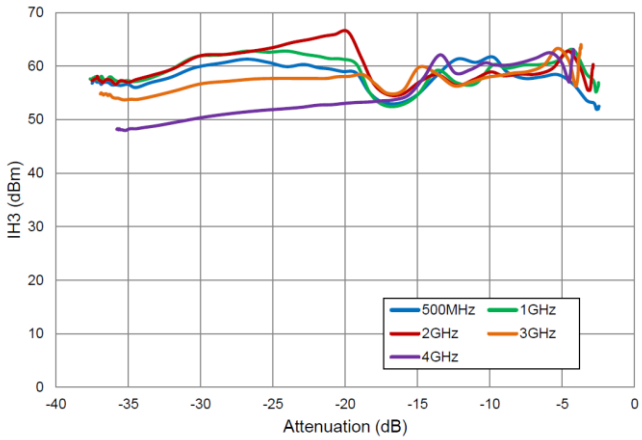

**3rd Harmonic IH3 versus Attenuation**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**



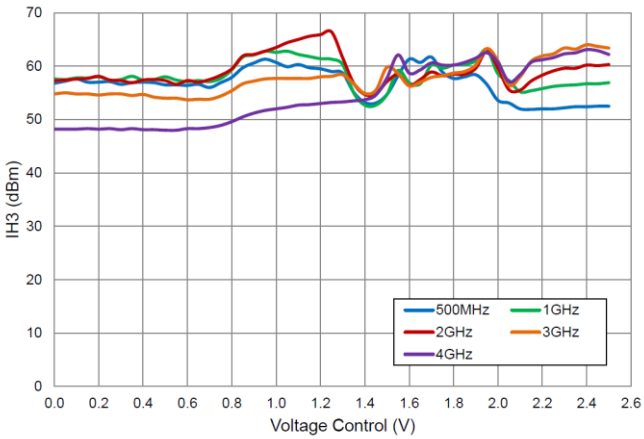

**3rd Harmonic IH3 versus Voltage Control**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**




**3rd Harmonic IH3 versus Attenuation**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**



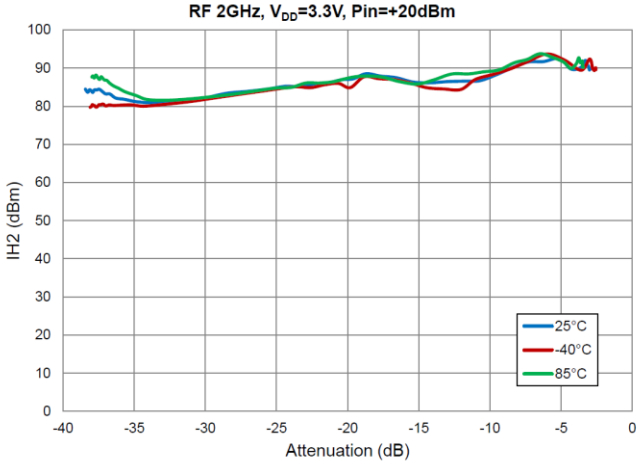

**3rd Harmonic IH3 versus Voltage Control**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**



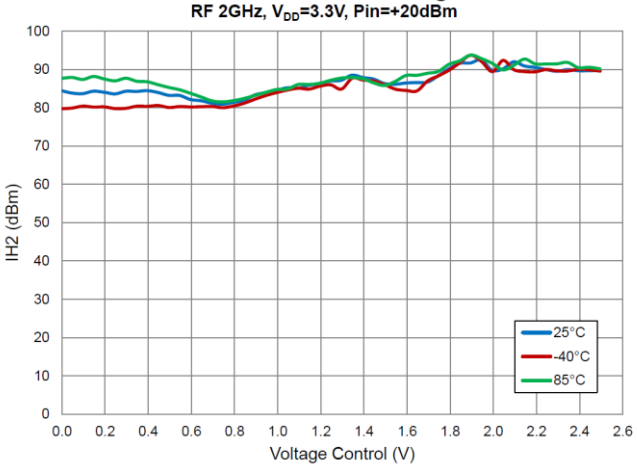
## Performance Plots – Positive S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

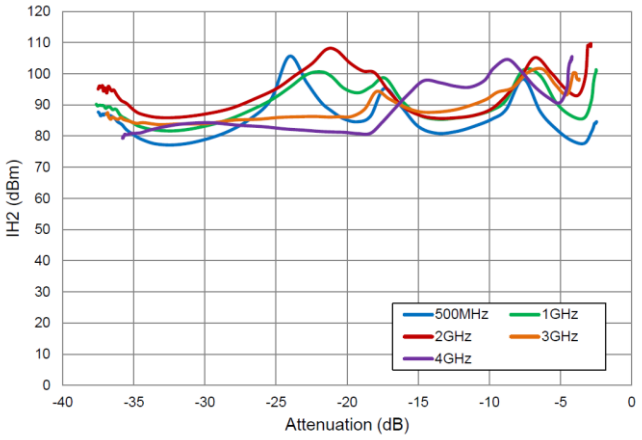
**2nd Harmonic IH2 versus Attenuation**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**



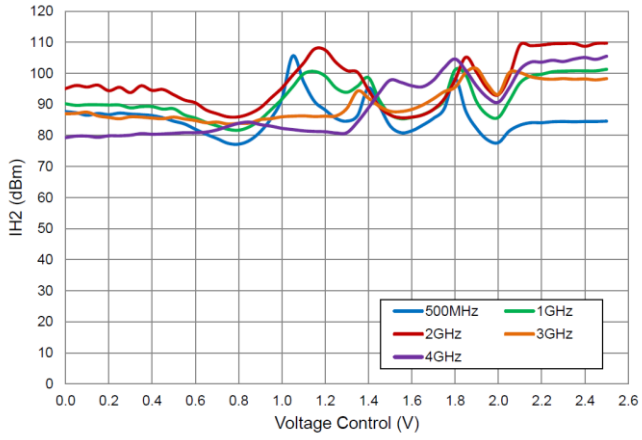

**2nd Harmonic IH2 versus Voltage Control**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**




**2nd Harmonic IH2 versus Attenuation**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**



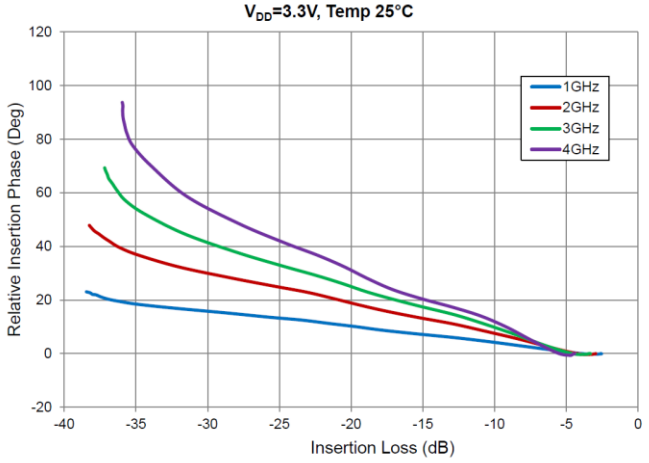

**2nd Harmonic IH2 versus Voltage Control**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**



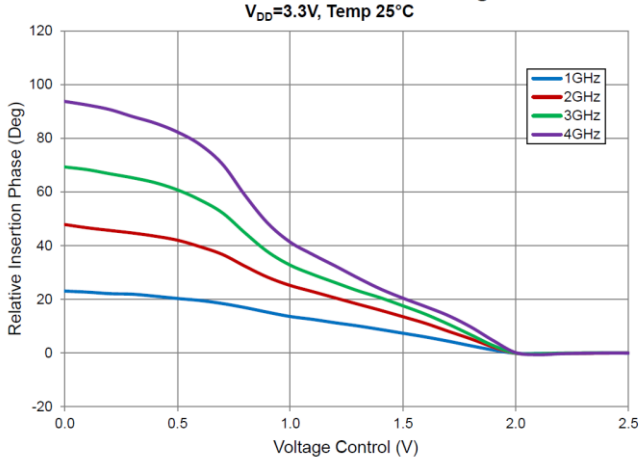
## Performance Plots – Positive S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

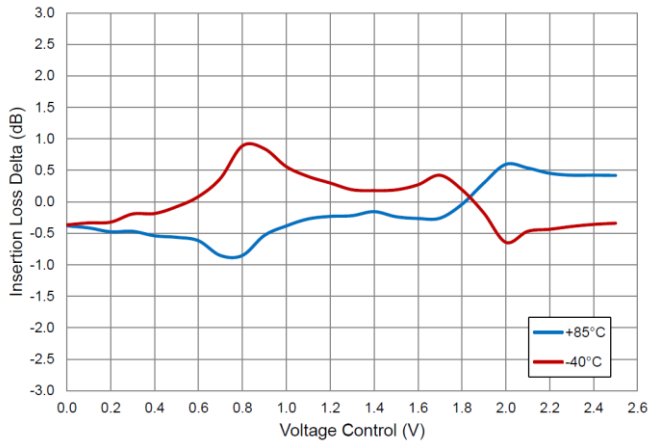
**Relative Insertion Phase versus Insertion Loss**
$V_{DD}$=3.3V, Temp 25°C



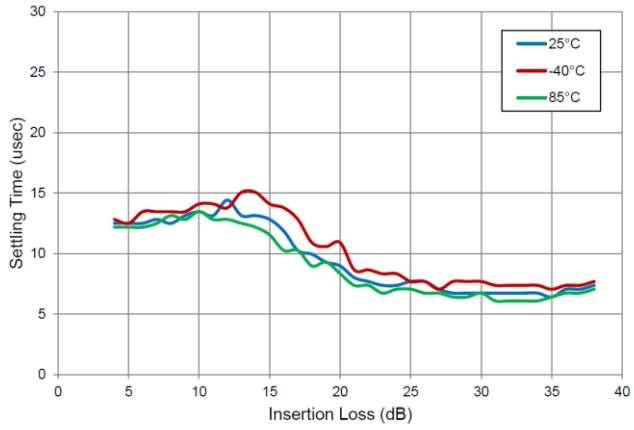

**Relative Insertion Phase versus Voltage Control**
$V_{DD}$=3.3V, Temp 25°C




**Insertion Loss Relative to +25°C**
RF 2GHz, $V_{DD}$=3.3V



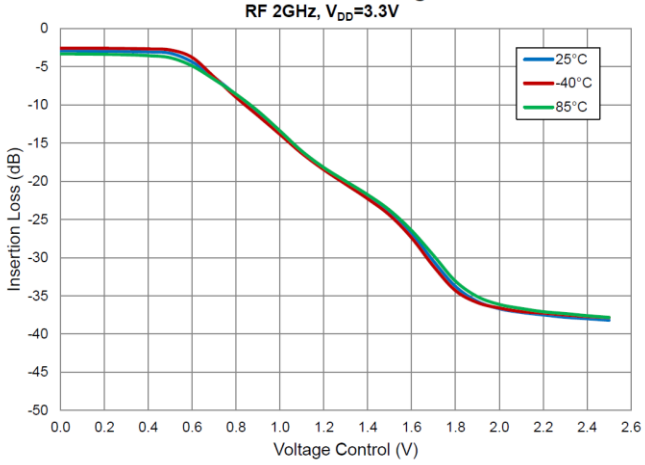

**Insertion Loss Settling Time - 1dB Steps**
RF 2GHz, $V_{DD}$=3.3V



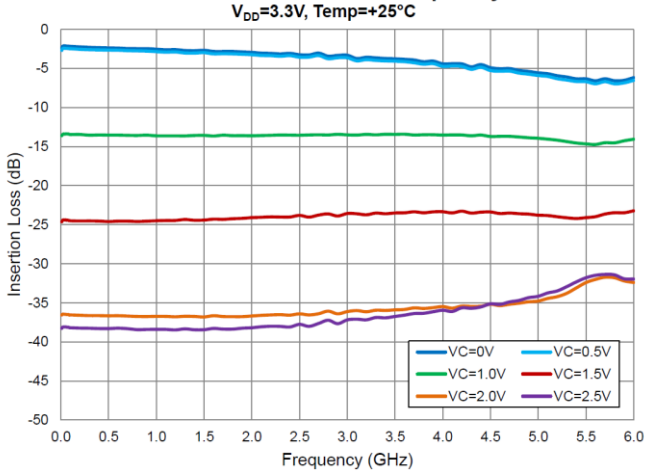
## Performance Plots – Negative S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

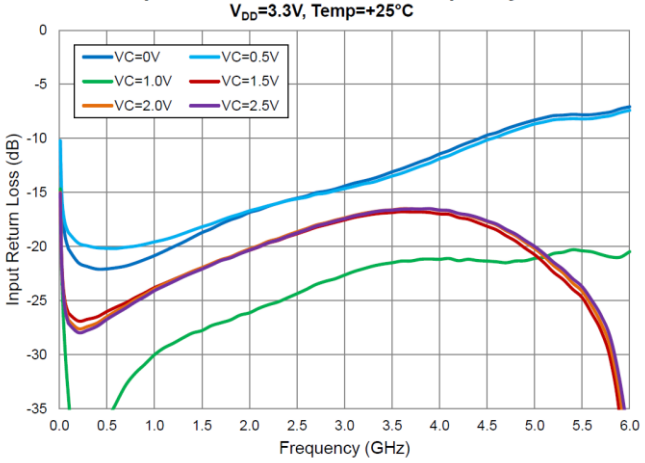
**Insertion Loss versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V



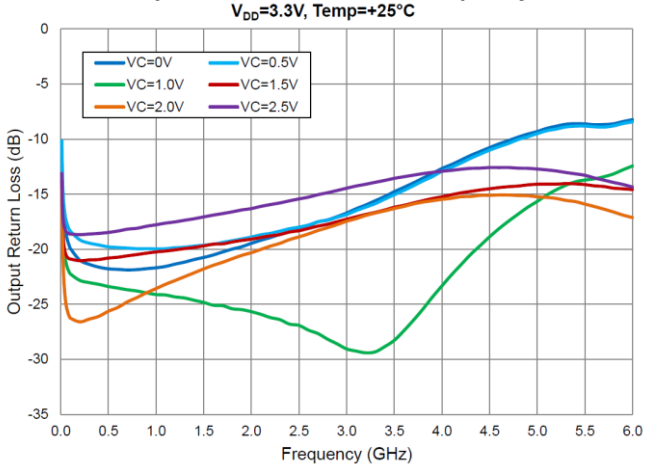

**Insertion Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C



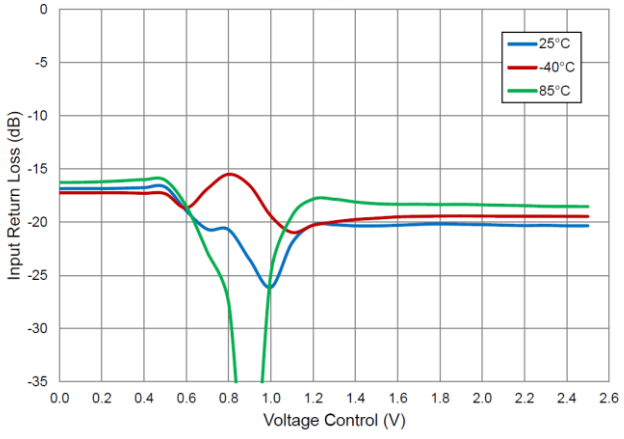

**Input Return Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C



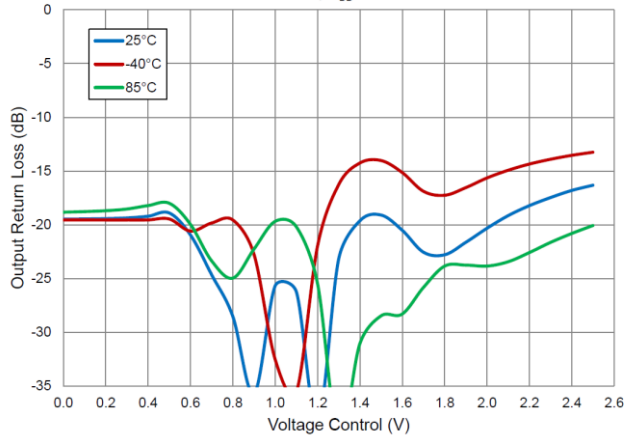

**Output Return Loss versus Frequency**
$V_{DD}$=3.3V, Temp=+25°C




**Input Return Loss versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V



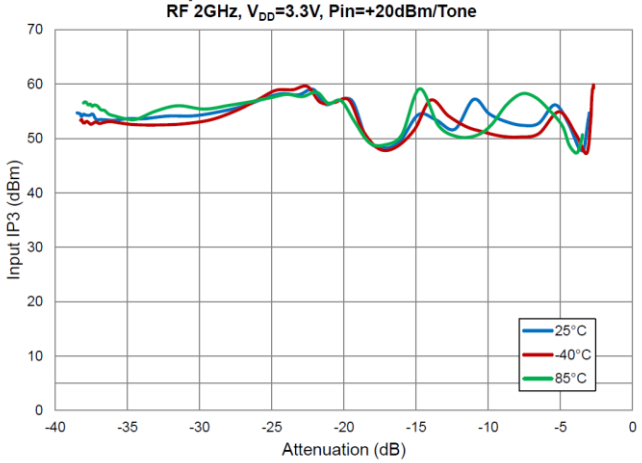

**Output Return Loss versus Voltrage Control**
RF 2GHz, $V_{DD}$=3.3V



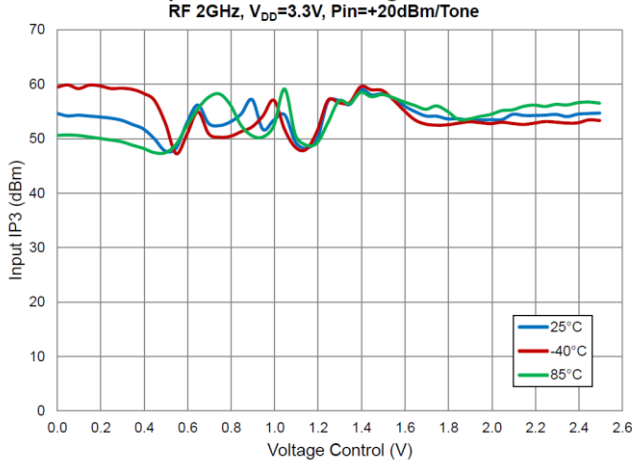
## Performance Plots – Negative S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

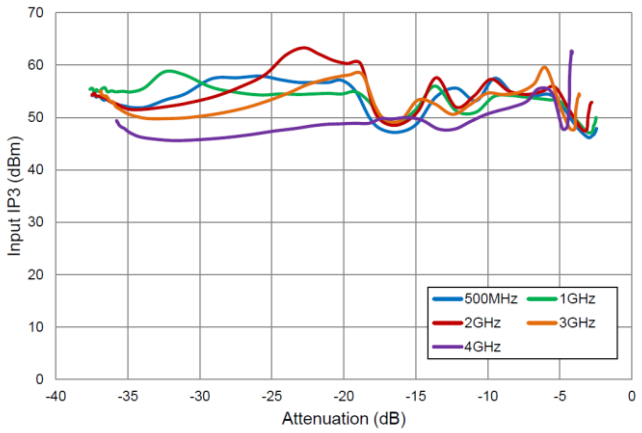
**Input IP3 versus Attenuation**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



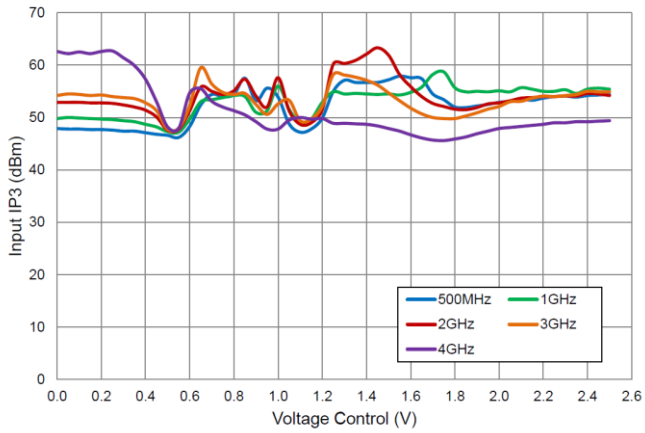

**Input IP3 versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



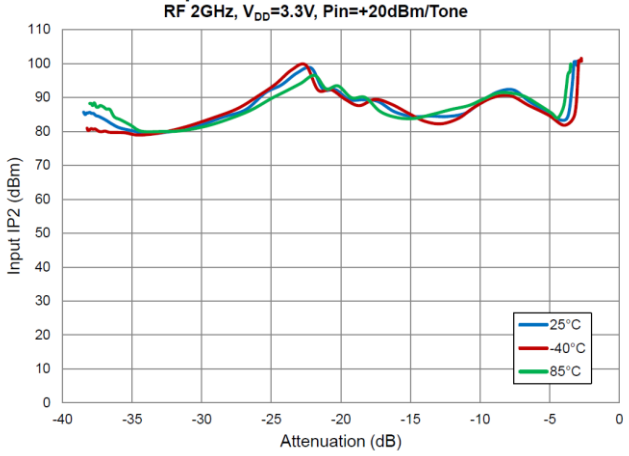

**Input IP3 versus Attenuation**
$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C



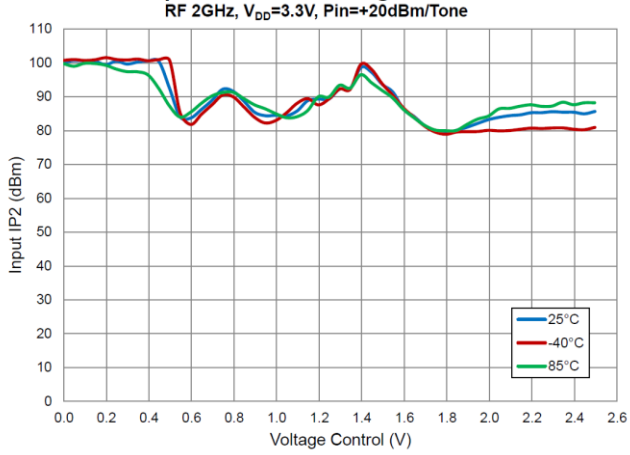

**Input IP3 versus Voltage Control**
$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C




**Input IP2 versus Attenuation**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



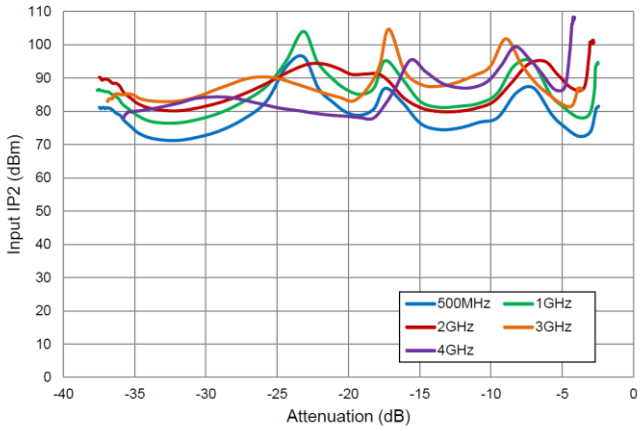

**Input IP2 versus Voltage Control**
RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm/Tone



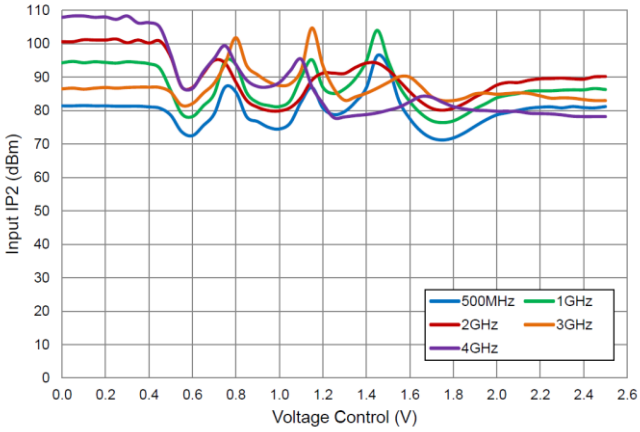
## Performance Plots – Negative S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

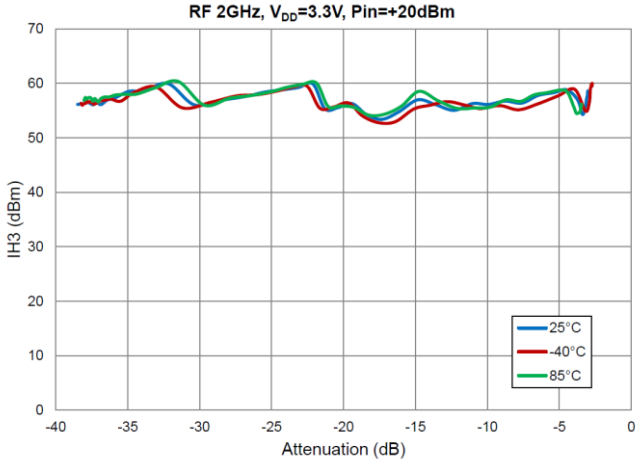
**Input IP2 versus Attenuation**
**$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C**



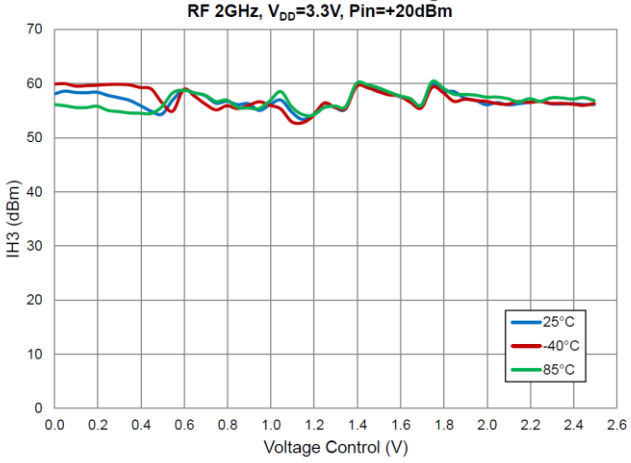

**Input IP2 versus Voltage Control**
**$V_{DD}$=3.3V, Pin=+20dBm/Tone, Temp=+25°C**



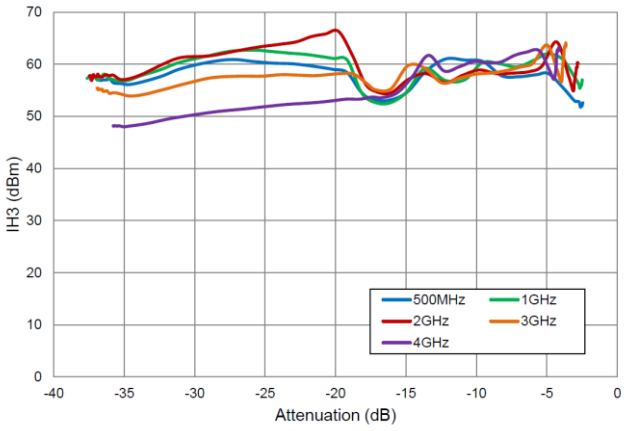

**3rd Harmonic IH3 versus Attenuation**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**



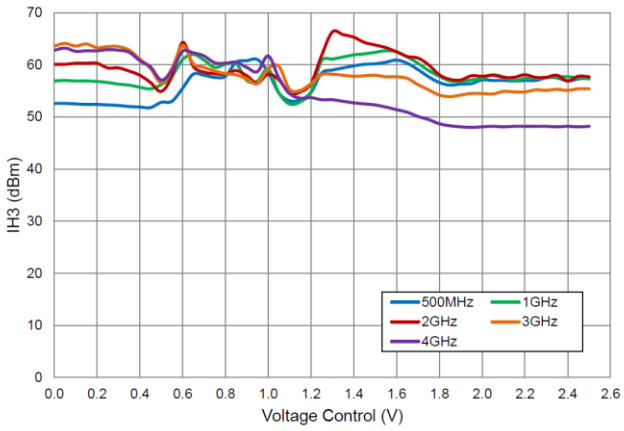

**3rd Harmonic IH3 versus Voltage Control**
**RF 2GHz, $V_{DD}$=3.3V, Pin=+20dBm**




**3rd Harmonic IH3 versus Attenuation**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**

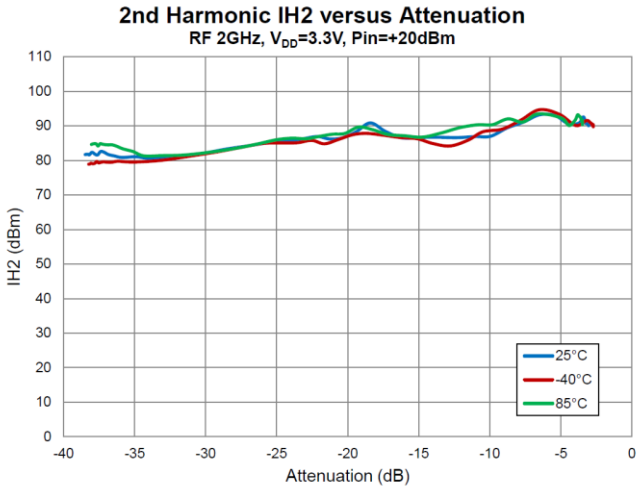


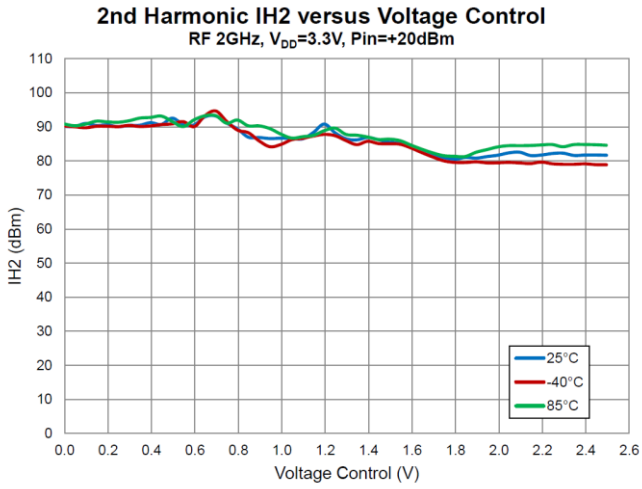

**3rd Harmonic IH3 versus Voltage Control**
**$V_{DD}$=3.3V, Pin=+20dBm, Temp=+25°C**

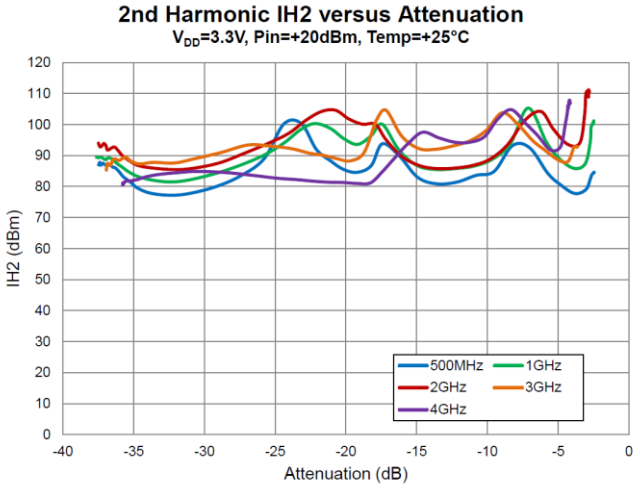


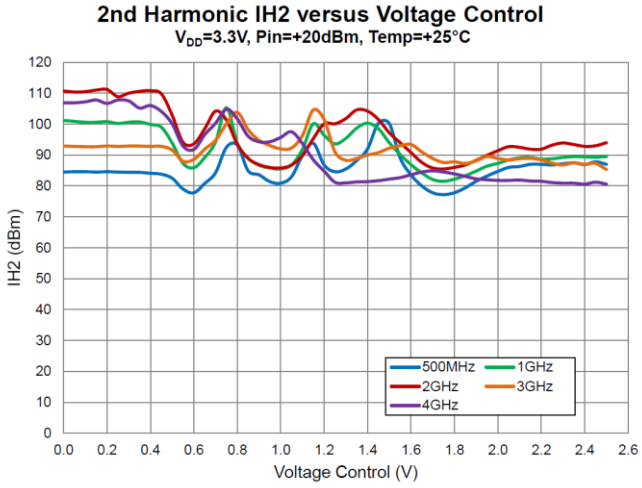
## Performance Plots – Negative S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included



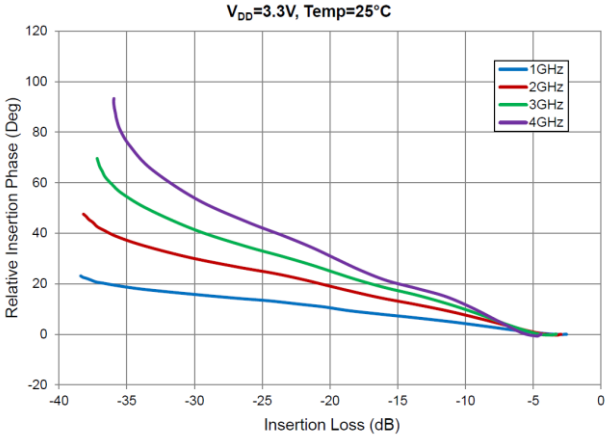



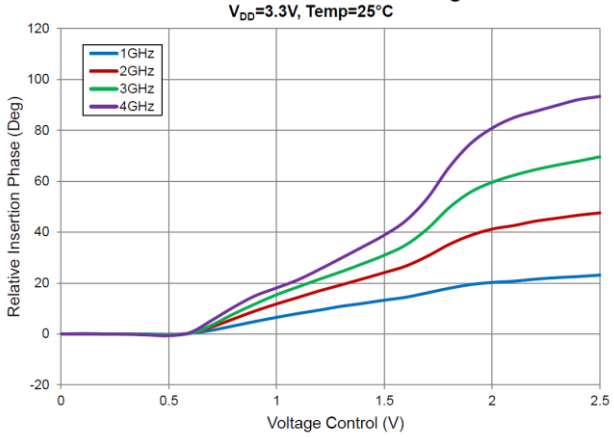
## Performance Plots – Negative S21 Slope

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

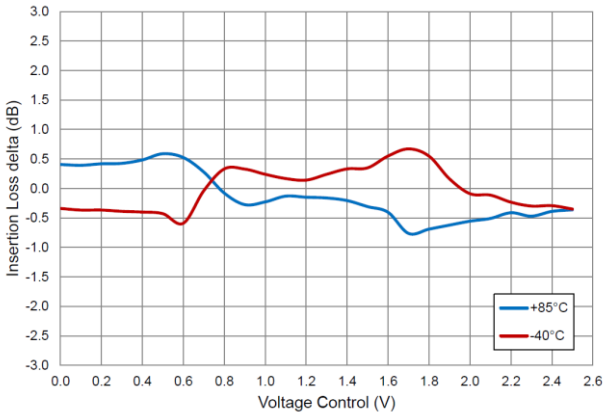
**Relative Insertion Phase versus Insertion Loss**
**$V_{DD}$=3.3V, Temp=25°C**




**Relative Insertion Phase versus Voltage Control**
**$V_{DD}$=3.3V, Temp=25°C**



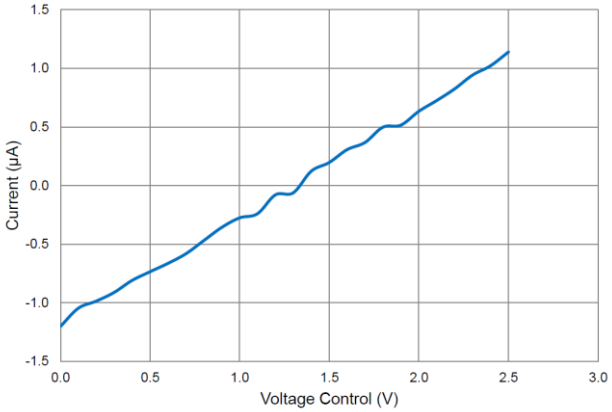

**Insertion Loss Relative to +25°C**
**RF 2GHz, $V_{DD}$=3.3V**



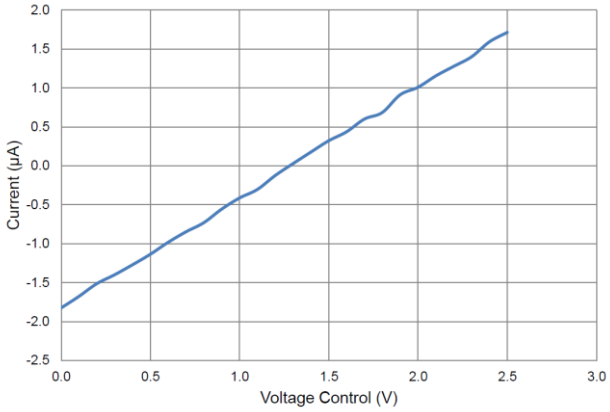

## Performance Plots – Voltage Control Pin Current

Test conditions unless otherwise noted: $V_{DD}$ = +3.3 V, Temp.=+25 °C, EVB trace and connector losses included

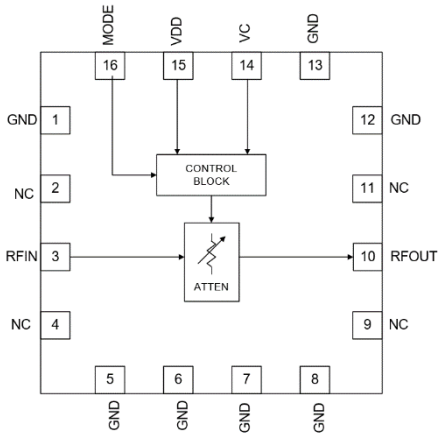
**VC Pin Current versus Voltage Control**
**Postive Slope, MODE=High, $V_{DD}$=3.3V**




**VC Pin Current versus Voltage Control**
**Negative Slope, MODE=Low, $V_{DD}$=3.3V**



## Pad Configuration and Description

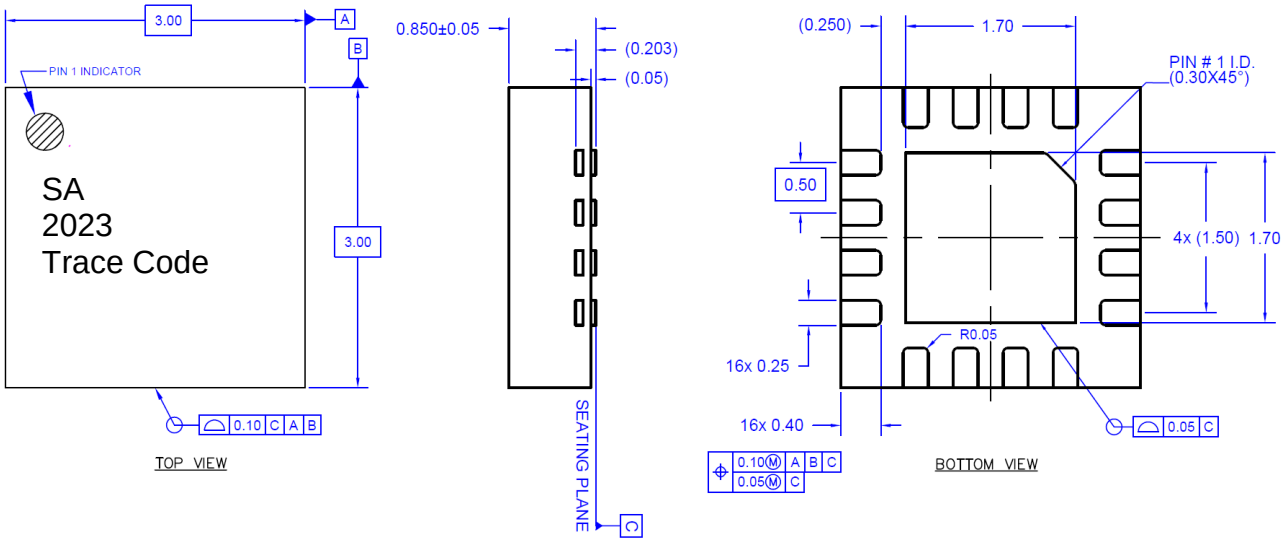



Top View

| Pad No. | Label | Description |
|---|---|---|
| 2, 4, 9, 11 | NC | No Connection. Do not connect to PC board ground plane |
| 3 | RFIN | RF Input. External DC Block required. RF must input to this pin to ensure linearity and thermal performance |
| 10 | RFOUT | RF Output. External DC Block required. RF must output from this pin to ensure linearity and thermal performance |
| 14 | VC | Control Voltage Input for Attenuation adjustment |
| 15 | VDD | Device DC Voltage Supply Input |
| 16 | MODE | Attenuation Slope Selection: Logic Low Negative S21 slope; Logic High Positive S21 slope |
| 1, 5, 6, 7, 8, 12, 13, Backside Paddle | GND | RF/DC ground. Use via holes to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint. |

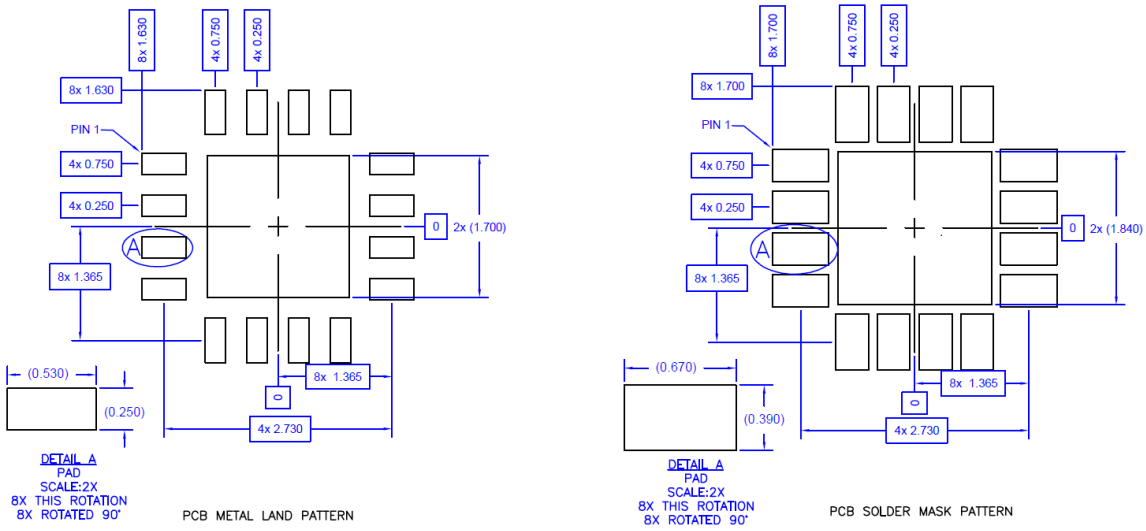
## Package Marking and Dimensions

Marking: Part Number – SA
2023
Trace Code – Assigned by Sub-Contractor




Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: Matte Tin

## PCB Mounting Pattern




Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.