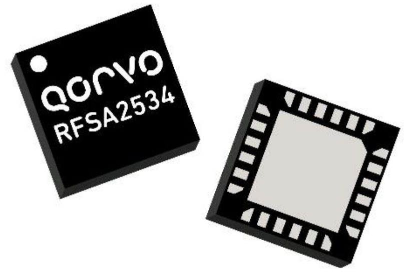
RFSA2534

50 MHz to 4000 MHz Digial Step Attenuator

Product Overview

The RFSA2534 is a 5-bit digital step attenuator (DSA) that features high linearity over the entire 15.5dB gain control range with 0.5dB steps and uses a serial control interface. It has a low insertion loss of 1.3dB at 2GHz. Patented circuit architecture provides Overshoot-free transient switching performance The RFSA2534 is available in a 4.2mm x 4.2mm laminate package that is footprint compatible with a 4mm x 4mm QFN 24 lead package.

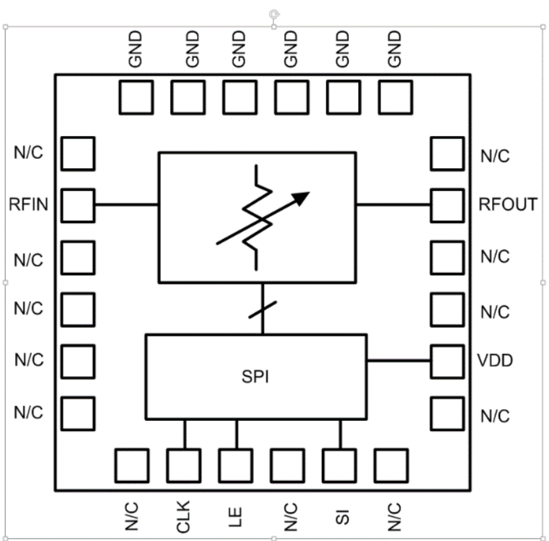


24 Pad 4.2 x 4.2 x 0.975 mm MCM Package

Key Features

- 5-Bit, 15.5 dB, 0.5 dB Step
- Patented Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 50 MHz to 4000 MHz
- High Linearity, IIP3 = +52 dBm
- Serial Control Interface
- Fast Switching Speed, 200 ns Typical
- Single Supply 3 V to 5 V Operation

Functional Block Diagram



Top View

Applications

- 2G through 4G Base Stations
- Point-to-Point
- Wi-Fi
- Test Equipment

Ordering Information

Part No.	Description
RFSA2534SQ	Sample bag with 25 pieces
RFSA2534SR	7" Reel with 100 pieces
RFSA2534TR13	13" Reel with 2500 pieces
RFSA2534PCK-410	50 MHz to 4000 MHz PCBA w/ 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
RF Input Power at RFIN	+30 dBm
RF Input Power at RFOUT	+27 dBm
Device Supply Voltage (V_{DD})	-0.5 to +6 V
All Other DC and Logic Pins, V_{DD} Appplied Prior to Any Other	-0.5 to +6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Supply Voltage (1)	+2.7		+5.5	V
Digital Logic High	+2.0			V
Digital Logic Low			+0.08	
Operating Temperature (2)	−40		+105	°C
Operating Junction Temperature			+125	°C

(1) Device performance is constant over this range; LDO on chip
(2) Derate RF Input Handing about 85°C

Electrical Specifications

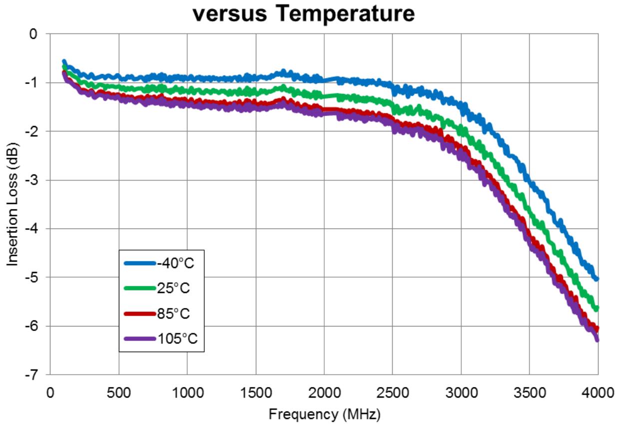
Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		50		4000	MHz
Insertion Loss	2000MHz, 0 dB attenuation		1.3	2.8	dB
Attenuation Range	0.5dB step size		15.5		dB
Absolute Attenuation Error			0.2 ±4%		dB
Input IP3			+52		dBm
Input P0.1dB			+30		dBm
Input/Output Return Loss	50MHz to 4000MHz, all attenuation states		15		dB
Input/Output Return Loss	700MHz to 2300MHz, all attenuation states		18		dB
Input/Output Return Loss	2300MHz to 2700MHz, all attenuation states		22		dB
Input and Output Impedance			50		Ω
Attenuation Step Time	50% control signal level to 10% / 90% RF		200		nsec
Successive Step Phase Delta	2000MHz		3		Deg
Supply Current, I_{CQ}	Steady state, transient between states higher		230	500	µA
RF Input Power at RFIN	Continuous operation st +85°C case temperature			+27	dBm
Thermal Resistance, θ_{jc}	At maximum attenuation state with RF power			78	°C/W

Notes:
1. Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp = +25 °C, 50 Ω system.

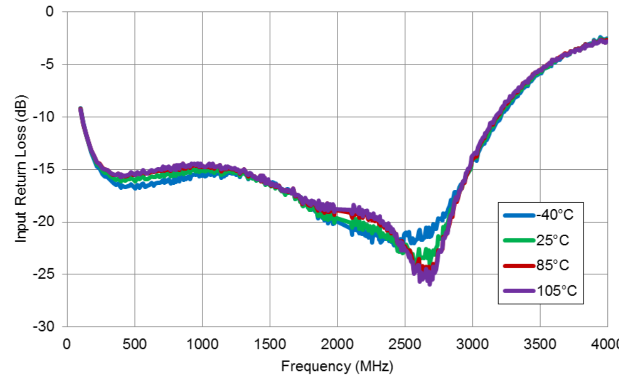
RF Performance Plots

T = 25°C, V_{DD} = 5V unless otherwise noted

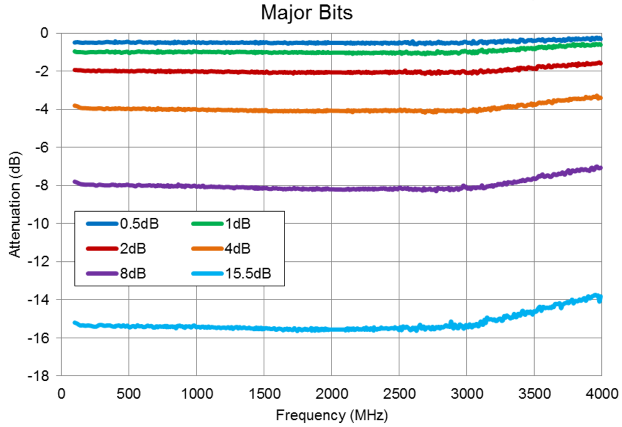
Insertion Loss versus Frequency versus Temperature



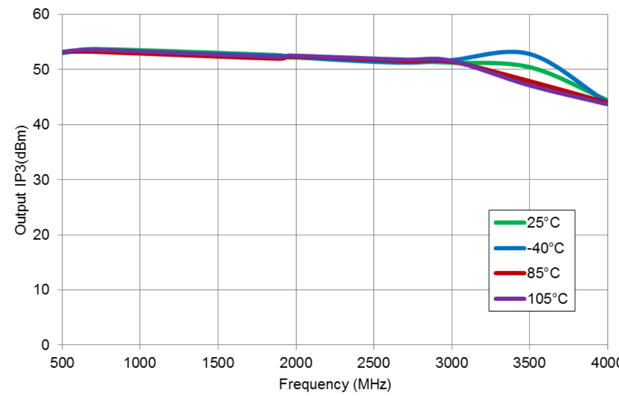
Input Return Loss versus Frequency versus Temperature
0dB Attenuation



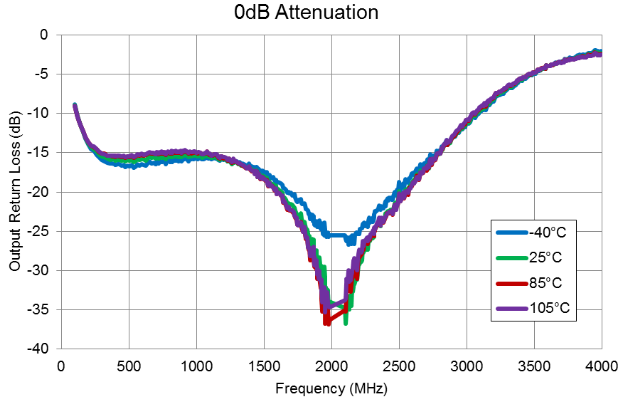
Normalized Attenuation versus Frequency
Major Bits



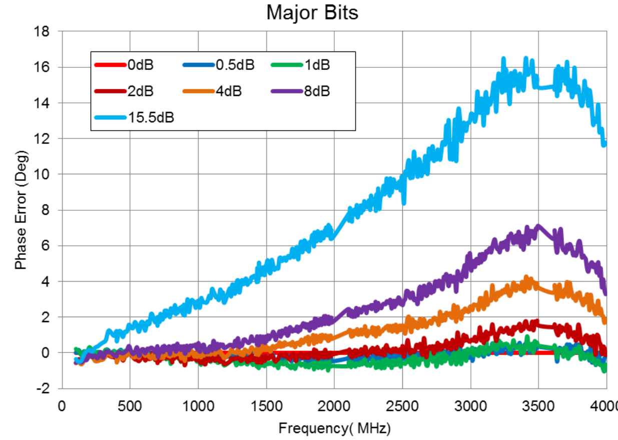
Output IP3 versus Frequency versus Temperature



Output Return Loss versus Frequency versus Temperature
0dB Attenuation

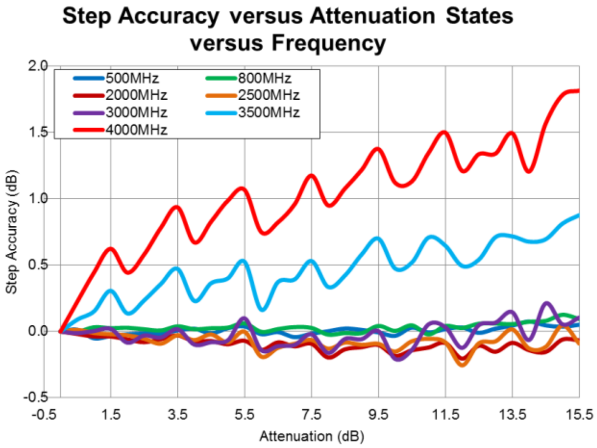


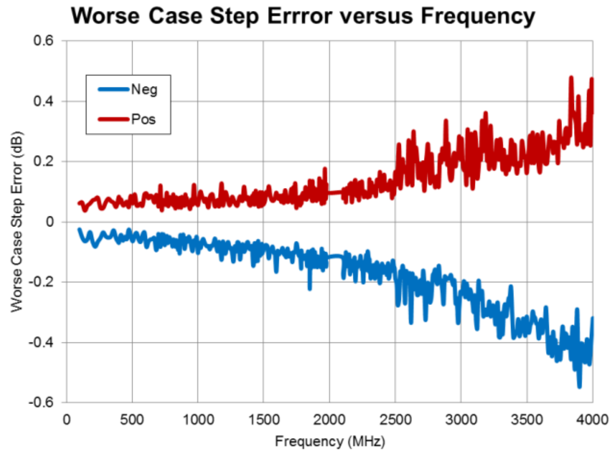
Relative Phase Error versus Frequency
Major Bits



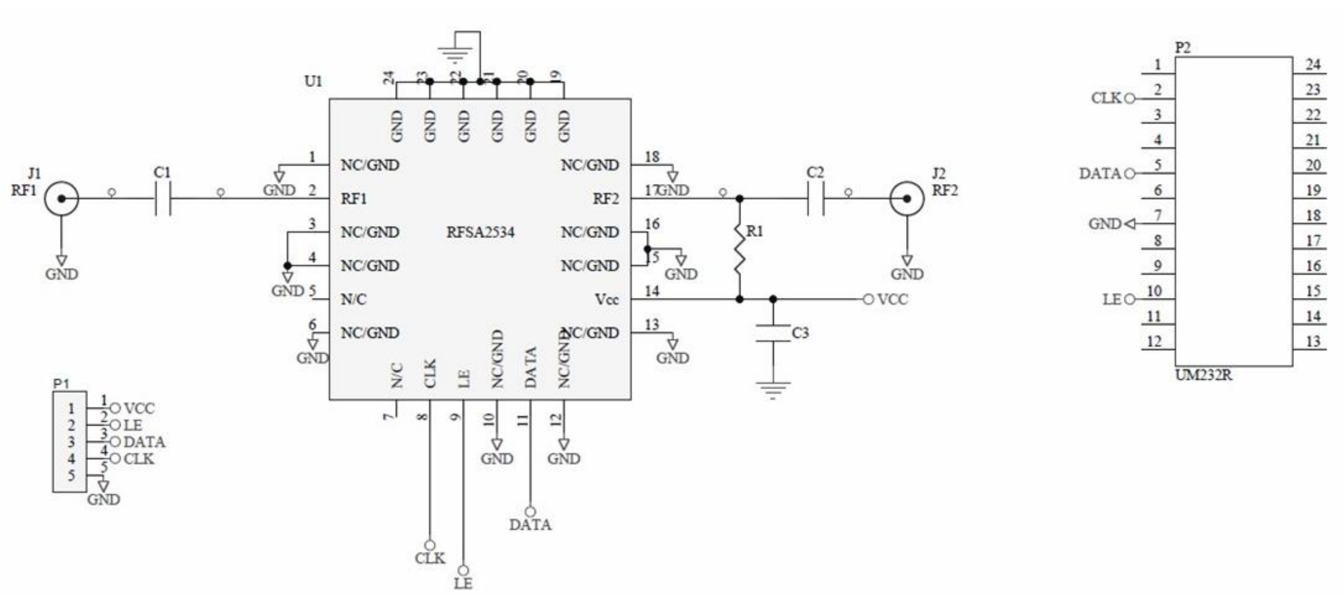
RF Performance Plots (continune)

T = 25°C, V_{DD} = 5V unless otherwise noted





Evaluation Board Schematic, RFSA2534PCK-410 50MHz to 4000MHz



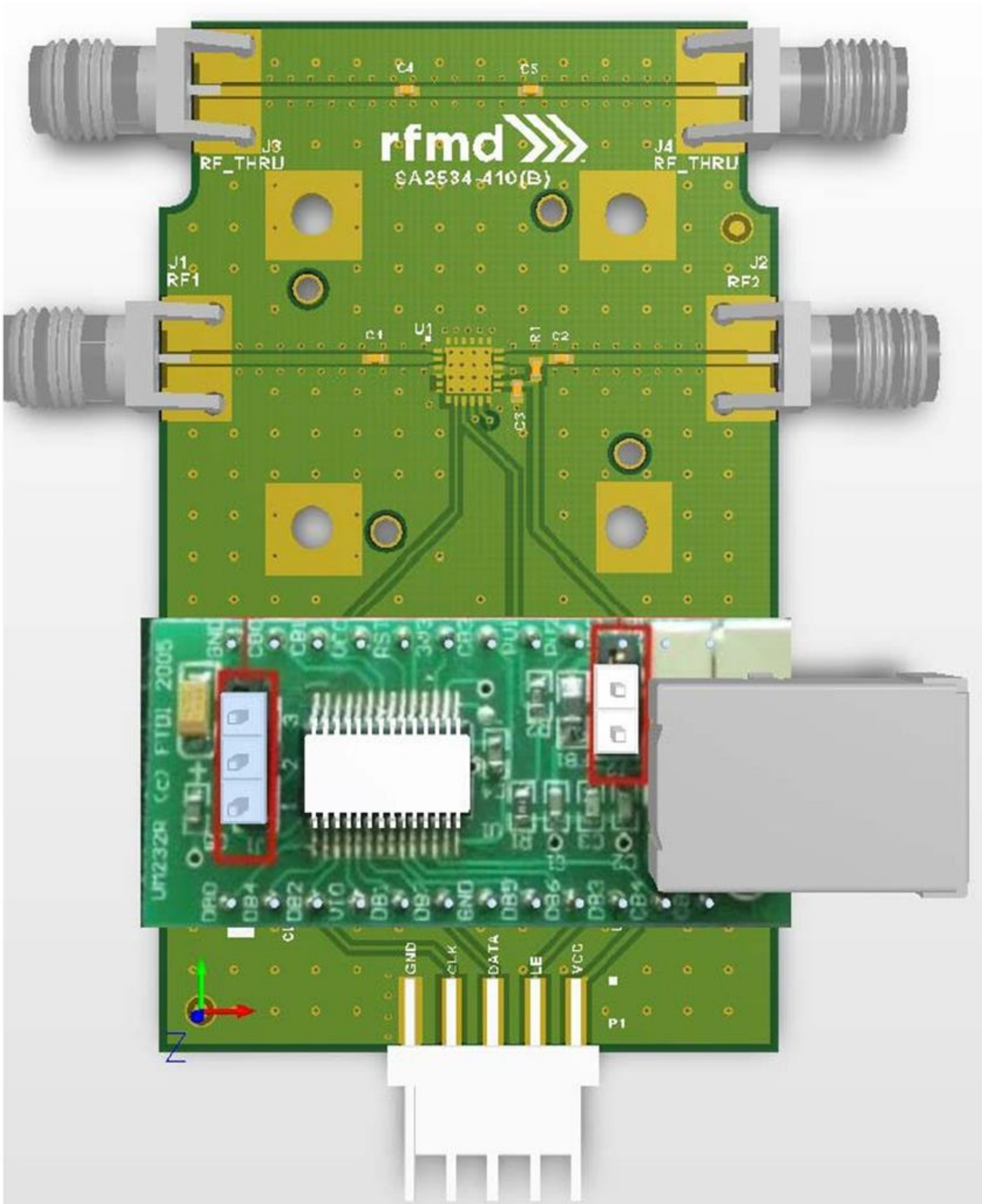
Bill of Material – RFSA2534PCK-410

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	RFSA2534-410(B)
U1	n/a	Module, Digital Step Attenuator, 50-4000MHz	Qorvo	RFSA2534
C1, C2	100 pF	CAP, 100pF, 5%, 50V, C0G, 0402	Taiyo Yuden (USA), Inc.	RM UMK105 CG101JV-F
C3	10000pF	CAP, 10000pF, 10%, 16V, X7R, 0402	Taiyo Yuden (USA), Inc.	RM EMK105 BJ103KV-F
J1, J2	n/a	CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	Heilind Electronics	142-0751-841
P1	n/a	CONN, HDR, ST, PLRZD, 5-PIN, 0.100”	AMP	640454-5
P2	n/a	CONN, SKT, 24-PIN DIP, 0.600”, T/H	Aries Electronics Inc.	24-6518-10
M1	n/a	Module, USB to Serial Uart, SSOP-28	Future Technology Devices	UM232R

Notes:

1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.

Evaluation Board Assembly, RFSA2534PCK-410 50MHz to 4000MHz



RFSA2534 Programming by Using USB Interface

Refer to Qorvo Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the software for use. Apply the supply voltage to P1. Select RFSA2534 from the Qorvo Parts List of the CBG user interface. Set the attenuation value using the CBG Graphic User Interface (GUI). The attenuator is set to the desired state and measurements can be taken.

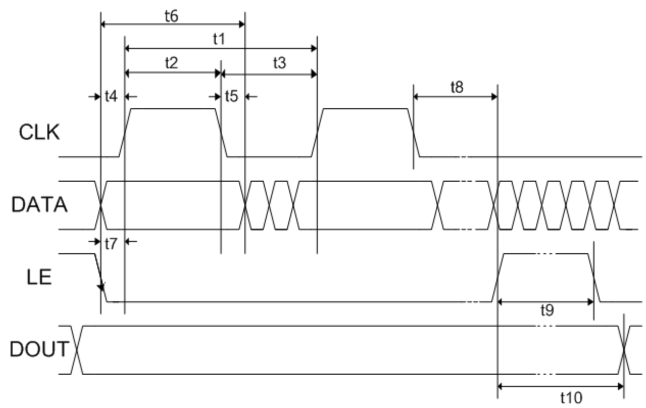
RFSA2534 Programming by Using Its Serial Bus

This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. Send the appropriate signals onto the serial bus lines in accordance with the Serial Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken.

Serial Bus Timing

Parameter	Limit	Units	Comment
t1	25	MHz max.	CLK Frequency
t2	20	ns min.	CLK High
t3	20	ns min.	CLK Low
t4	5	ns min.	DATA to CLK Setup Time
t5	5	ns min.	DATA to CLK Hold Time
t6	30	ns min.	DATA Valid
t7	5	ns min.	LE to CLK Setup Time
t8	5	ns min.	CLK to LE Setup Time
t9	10	ns min.	LE Pulse Width
t10	20	ns max.	Output Set

Serial Bus Timing Diagram

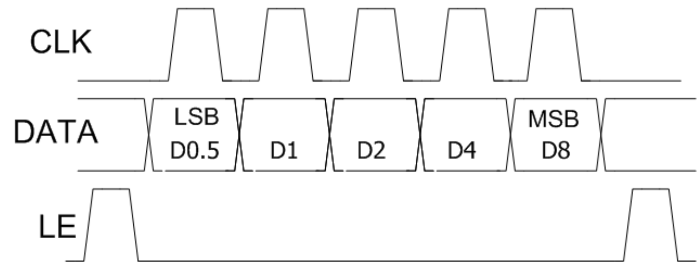


Control Bit Truth Table (Major States)

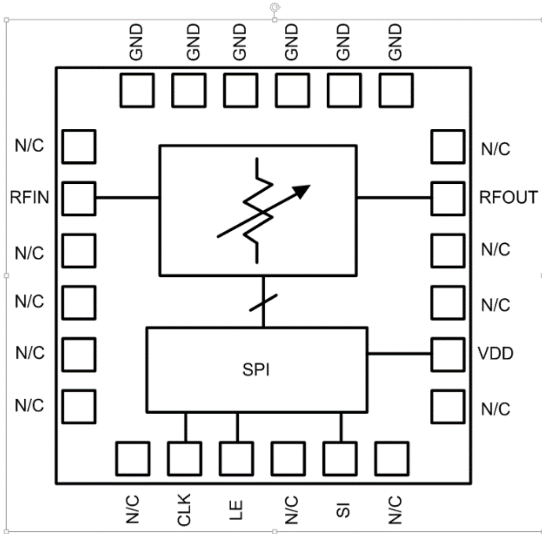
D0.5	D1	D2	D4	D8	Attenuation State
H	H	H	H	H	0 dB *
L	H	H	H	H	0.5 dB
H	L	H	H	H	1 dB
H	H	L	H	H	2 dB
H	H	H	L	H	4 dB
H	H	H	H	L	8 dB
L	L	L	L	L	15.5 dB

*0 dB Reference State with the Insertion Loss as specified

Serial Bus Timing Diagram



Pad Configuration and Description

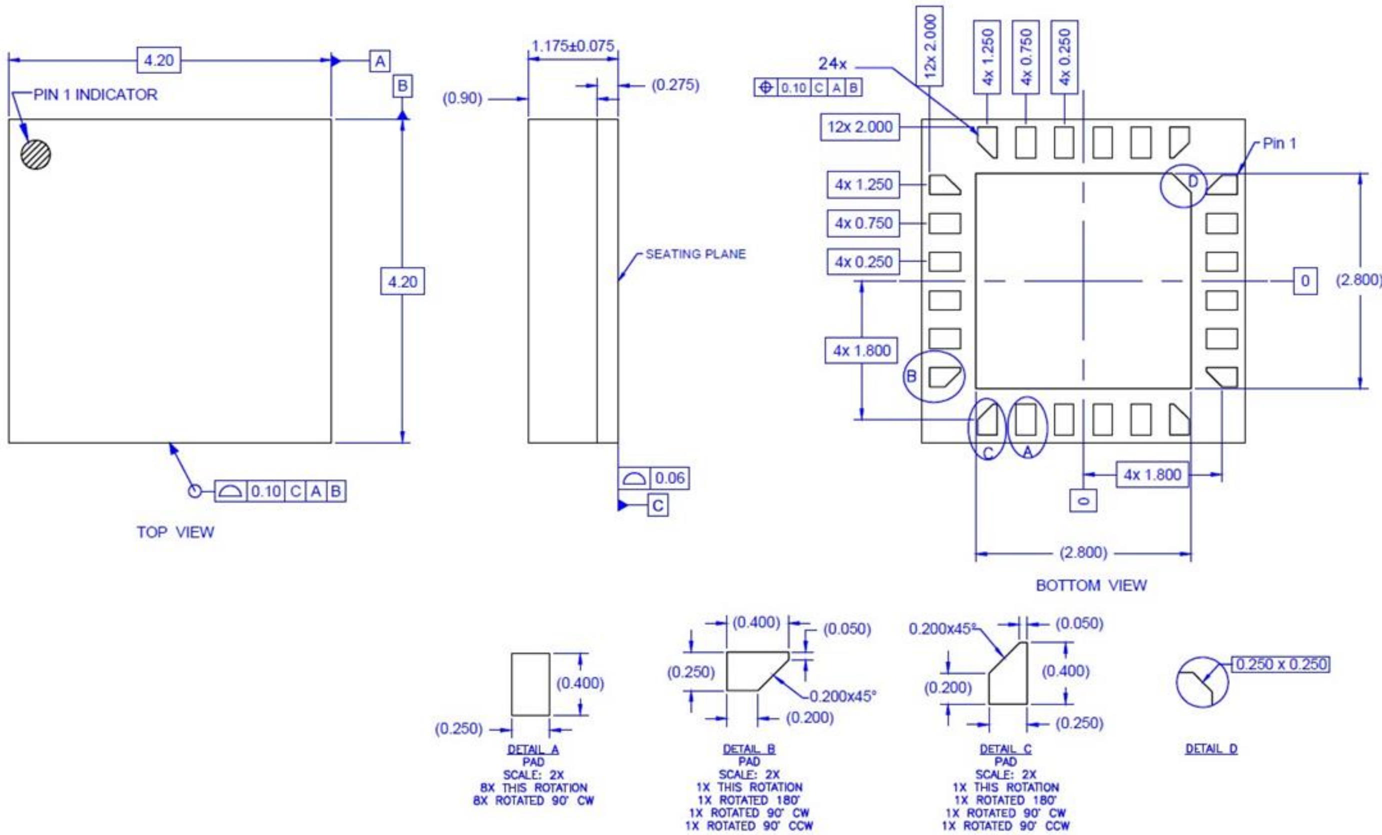


Top View

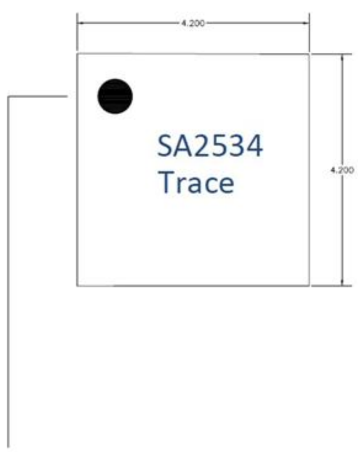
Pad No.	Label	Description
1, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15, 16, 18	NC	No Internal Connection. Land pads should be provided on PCB for mounting integrity.
2	RFIN	RF Input: Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
8	CLK	Serial Clock Input
9	LE	Latch Enable: The leading edge of signal on LE causes the attenuator to change state
11	SI	Serial Data Input
14	VDD	Supply Voltage for DSA and Logic Circuitry
17	RF OUT	RF Output: Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
19, 20, 21, 22, 23	GND	RF/DC/Digital ground connection. Ground these pins on the PCB
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Package Outline

(Dimensions in Millimeters)



Package Marking



Pin 1 Indicator
Trace Code to be assigned by SubCon