



## N-Channel Enhancement Mode Power MOSFET

### Description

The RMD50N40DF uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### **General Feature**

V<sub>DS</sub> =40V,I<sub>D</sub> =65A

$$\begin{split} R_{DS(ON)} &< 7.5 m \Omega @ V_{GS} = 10V \quad (Typ:6.8m\Omega) \\ R_{DS(ON)} &< 10m\Omega @ V_{GS} = 4.5V \quad (Typ:8.5m\Omega) \end{split}$$

- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E<sub>AS</sub>
- Excellent package for good heat dissipation

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Halogen-free

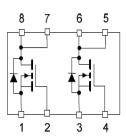
#### 100% UIS TESTED! 100% ∆Vds TESTED!

#### **Package Marking and Ordering Information**

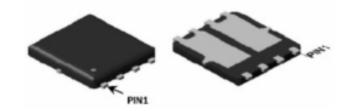
U	0	0			
Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
D50N40	RMD50N40DF	DFN5X6-8L	-	-	-

### Absolute Maximum Ratings (T<sub>c</sub>=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	40	V
Gate-Source Voltage	Vgs	±20	V
Continuous Drain Current (T <sub>a</sub> =25℃)	lD	65	A
Continuous Drain Current (T <sub>a</sub> =100℃)	lD	41	A
Pulsed Drain Currenr <sup>(1)</sup>	Ідм	260	A
Singel Pulsed Avalanche Energy <sup>(2)</sup>	Eas	96	mJ
Power Dissipation	PD	48	W
Thermal Resistance from Junction to Case <sup>(4)</sup>	Rejc	2.6	°C/W
Thermal Resistance from Junction to Ambient <sup>(4)</sup>	R <sub>0JA</sub>	62	°C/W
Junction Temperature	TJ	150	°C
Storage Temperature	T <sub>STG</sub>	-55~ +150	°C



Schematic diagram



**Top View** 

**Bottom View** 

## Electrical Characteristics (T<sub>c</sub>=25 $^{\circ}$ C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Туре	Max	Unit	
Static Characteristics	·		•	•			
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250µA	40	-	-	V	
Zero gate voltage drain current	DSS	V <sub>DS</sub> =40V, V <sub>GS</sub> = 0V	-	-	1	μA	
Gate-body leakage current	GSS	V <sub>GS</sub> =±20V,V <sub>DS</sub> = 0V	-	-	±100	nA	
Gate threshold voltage <sup>(3)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	1	1.5	2.5	V	
		V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	6.8	7.5		
Drain-source on-resistance <sup>(3)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	8.5	10	mΩ	
Dynamic characteristics							
Input Capacitance	Ciss	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f =1MHz	-	2956	-	pF	
Output Capacitance	Coss		-	225	-		
Reverse Transfer Capacitance	Crss		-	197	-		
Switching characteristics	·						
Turn-on delay time	t <sub>d(on)</sub>		-	8	-	ns	
Turn-on rise time	tr		-	16	-		
Turn-off delay time	t <sub>d(off)</sub>	V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	21	-		
Turn-off fall time	tr		-	10	-		
Total Gate Charge	Qg	VDS=20V, ID=30A,	-	46	-	nC	
Gate-Source Charge	Qgs		-	7.2	-		
Gate-Drain Charge	Qgd	VGS=10V	-	8.8	-		
Source-Drain Diode characteristics	•	•	·				
Diode Forward voltage <sup>(3)</sup>	VDS	V <sub>GS</sub> =0V, I <sub>S</sub> =1A	-	-	1.2	V	
Diode Forward current <sup>(4)</sup>	ls		-	-	65	А	

#### Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature

- 2. EAS Condition:TJ=25 $^\circ C$ ,V\_DD=20V,R\_G=25 $^\Omega$ ,L=0.5mH
- 3. Pulse Test: pulse width≤300µs, duty cycle≤2%
- 4. Surface Mounted on FR4 Board,t≤10 sec



## **Test Circuit**

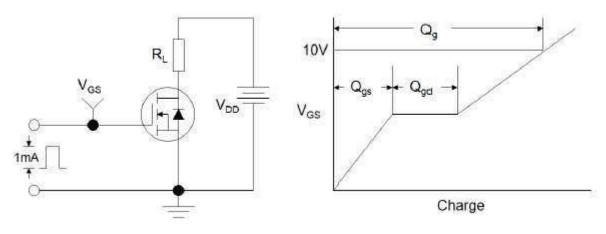


Figure1:Gate Charge Test Circuit & Waveform

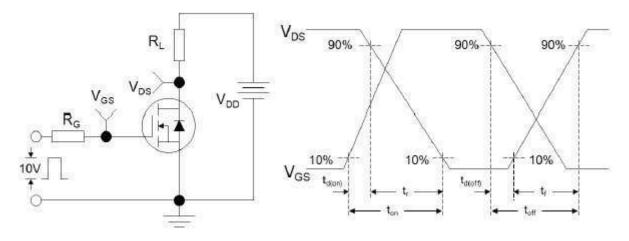


Figure 2: Resistive Switching Test Circuit & Waveforms

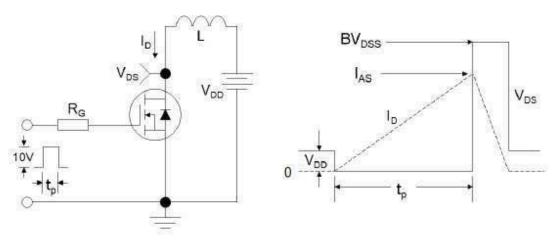
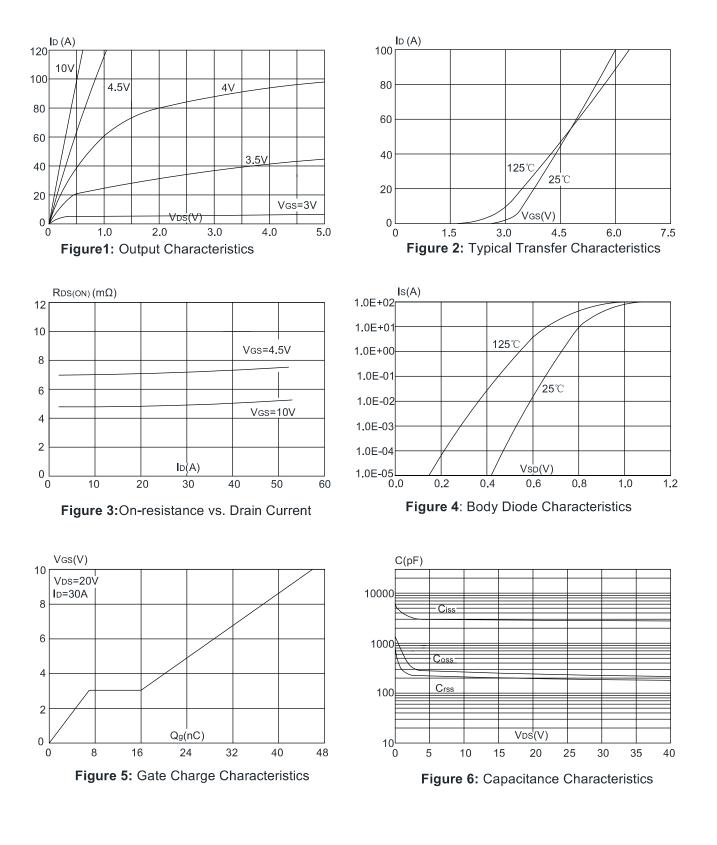


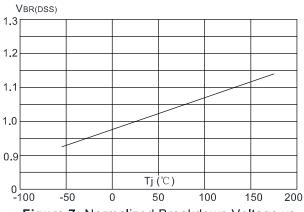
Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms





## **RATING AND CHARACTERISTICS CURVES (RMD50N40DF)**





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**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

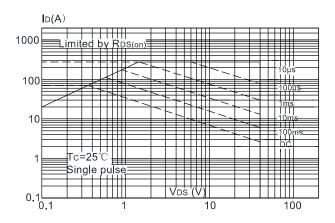


Figure 9: Maximum Safe Operating Area

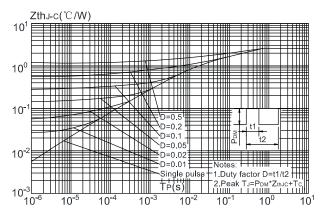
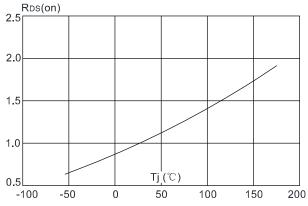
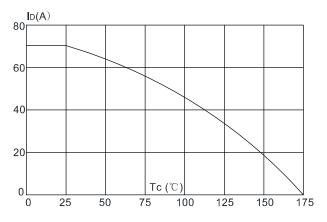


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



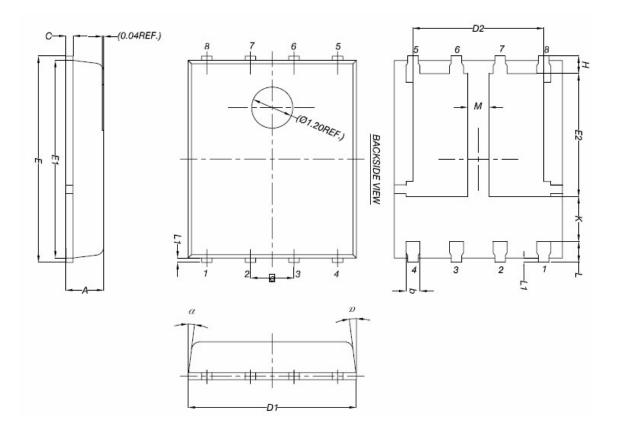
**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs Case Temperature



# DFN5X6-8L Package Information



DUA	MILLIMETERS			
DIM.	MIN.	NOM.	MAX	
Α	0.90	1.00	1.10	
b	0.33	0.41	0.51	
С	0.20	0.25	0.30	
D1	4.80	4.90	5.00	
D2	3.61	3.81	3.96	
Е	5.90	6.00	6.10	
E1	5.70	5.75	5.80	
E2	3.38	3.58	3.78	
е	1.27 BSC			
Н	0.41	0.51	0.61	
κ	1.10		-	
L	0.51	0.61	0.71	
L1	0.06	0.13	0.20	
М	0.50	-	-	
α	0°	-	12°	

