RECTRON SEMICONDUCTOR
TECHNICAL SPECIFICATION

RMD50N40DFV

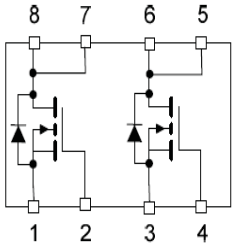
N-Channel Enhancement Mode Power MOSFET

Description

The RMD50N40DFV uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Feature

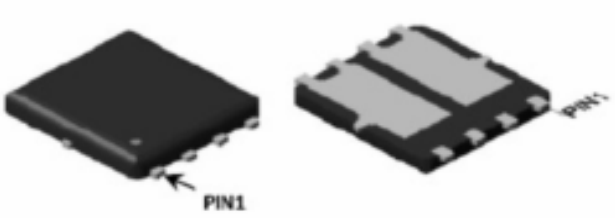
- V_{DS} =40V,I_D =65A
  $R_{DS(ON)}$ < 7.5mΩ @ V_{GS}=10V (Typ:6.8mΩ)
  $R_{DS(ON)}$ < 10mΩ @ V_{GS}=4.5V (Typ:8.5mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Schematic diagram

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Halogen-free
- P/N suffix V means AEC-Q101 qualified, e.g:RMD50N40DFV



Top View **Bottom View**

100% UIS TESTED!
100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
D50N40	RMD50N40DFV	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	65	A
Continuous Drain Current (T_a =100℃)	I_D	41	A
Pulsed Drain Currenr (1)	I_{DM}	260	A
Singel Pulsed Avalanche Energy (2)	E_{AS}	96	mJ
Power Dissipation	P_D	48	W
Thermal Resistance from Junction to Case (4)	$R_{\theta JC}$	2.6	℃/W
Thermal Resistance from Junction to Ambient (4)	$R_{\theta JA}$	62	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V,V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.5	2.5	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =30A	-	6.8	7.5	mΩ
		V_{GS} =4.5V, I_D =20A	-	8.5	10	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =20V, V_{GS} =0V, f =1MHz	-	2956	-	pF
Output Capacitance	C_{oss}		-	225	-	
Reverse Transfer Capacitance	C_{rss}		-	197	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, I_D=30A, R_L=1Ω V_{GS}=10V, R_G=3Ω	-	8	-	ns
Turn-on rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	21	-	
Turn-off fall time	t_f		-	10	-	
Total Gate Charge	Qg	VDS=20V, ID=30A, VGS=10V	-	46	-	nC
Gate-Source Charge	Qgs		-	7.2	-	
Gate-Drain Charge	Qgd		-	8.8	-	
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	V_{GS} =0V, I_S=1A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	65	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=20V,R_G=25Ω,L=0.5mH
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

Test Circuit

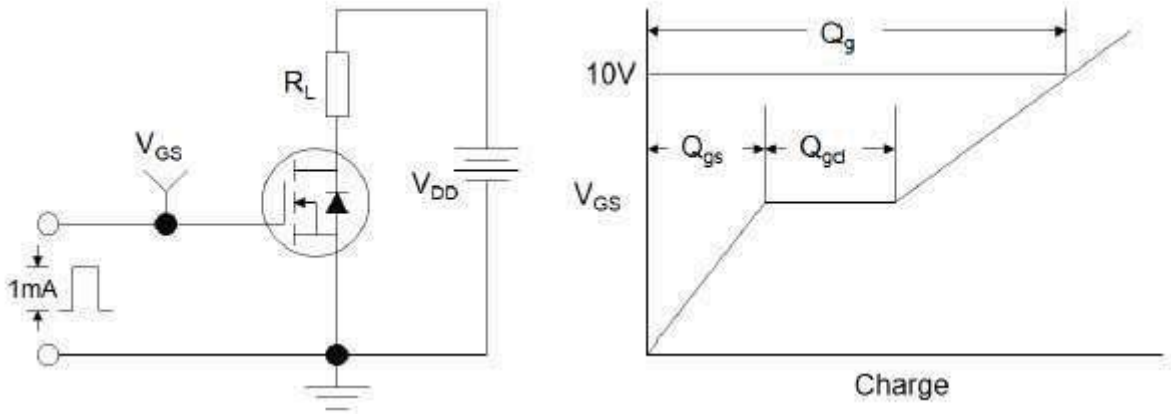


Figure1:Gate Charge Test Circuit & Waveform

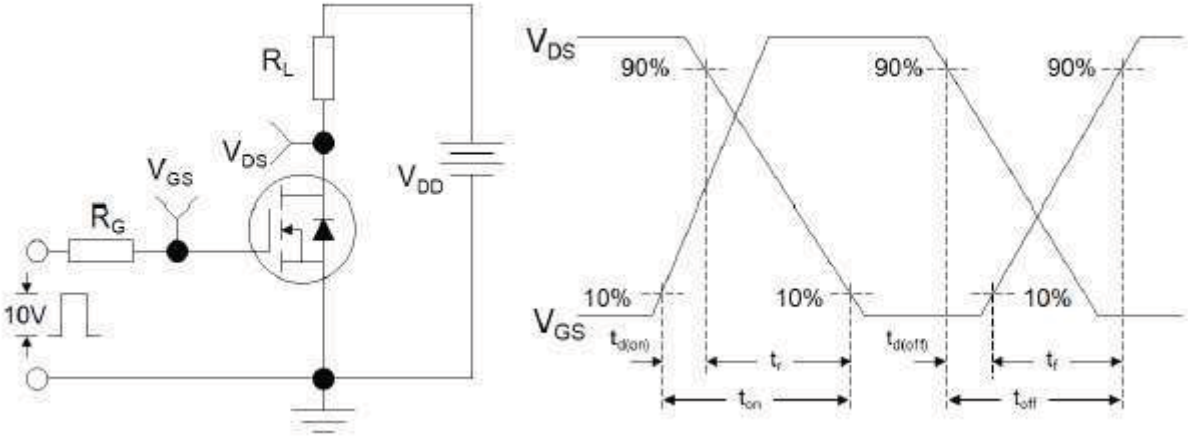


Figure 2: Resistive Switching Test Circuit & Waveforms

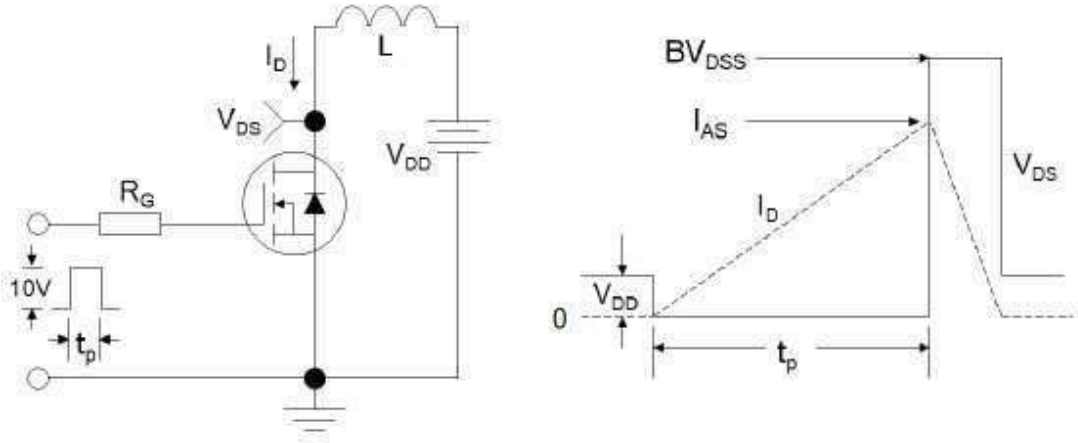


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

RATING AND CHARACTERISTICS CURVES (RMD50N40DFV)

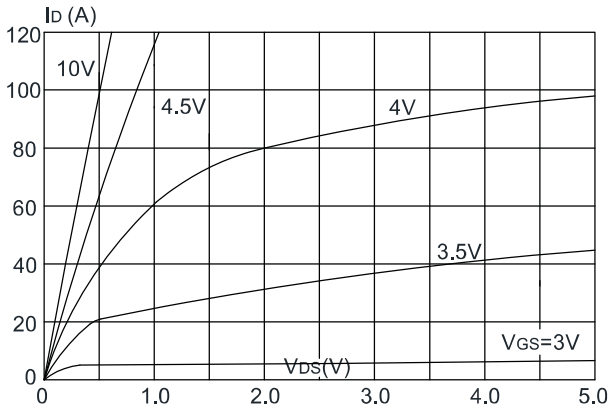


Figure1: Output Characteristics

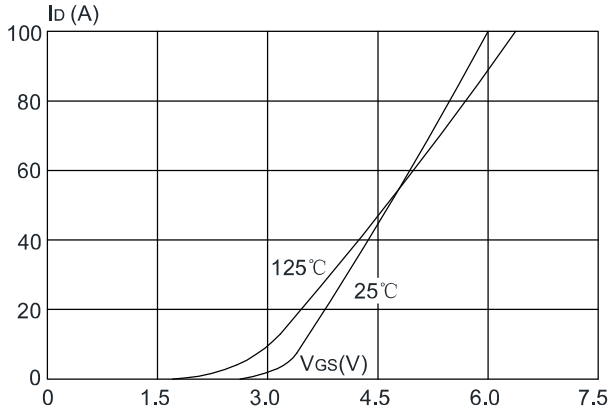


Figure 2: Typical Transfer Characteristics

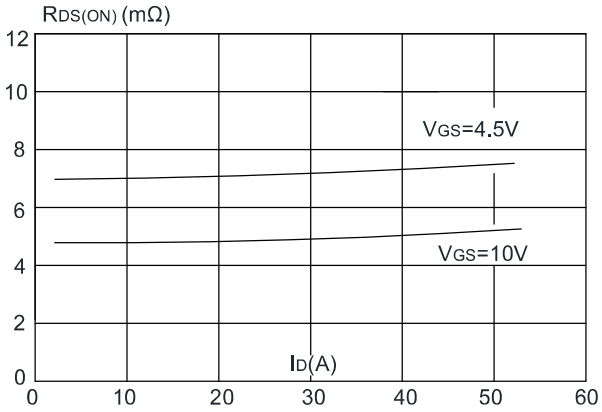


Figure 3: On-resistance vs. Drain Current

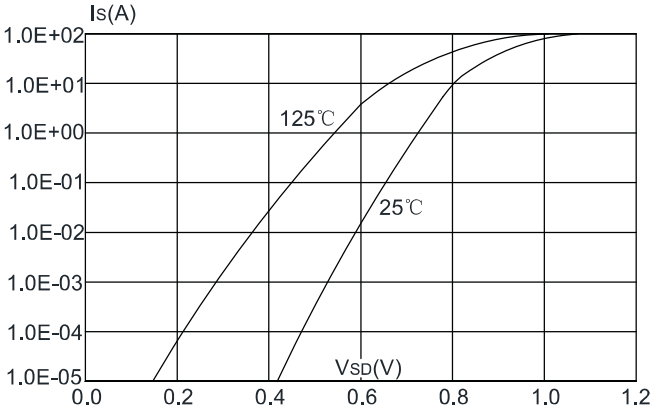


Figure 4: Body Diode Characteristics

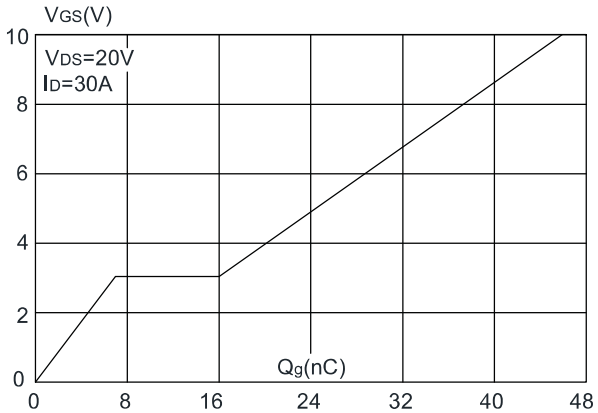


Figure 5: Gate Charge Characteristics

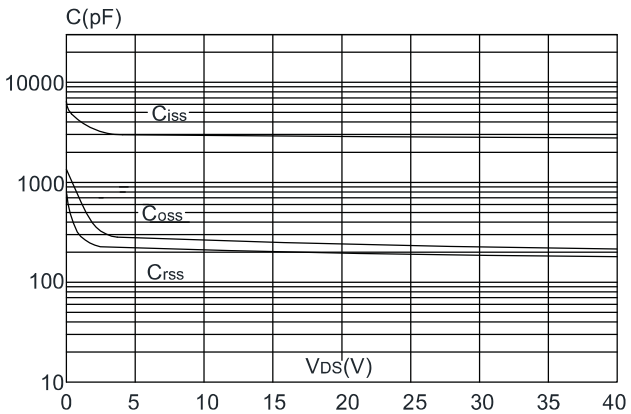


Figure 6: Capacitance Characteristics

RATING AND CHARACTERISTICS CURVES (RMD50N40DFV)

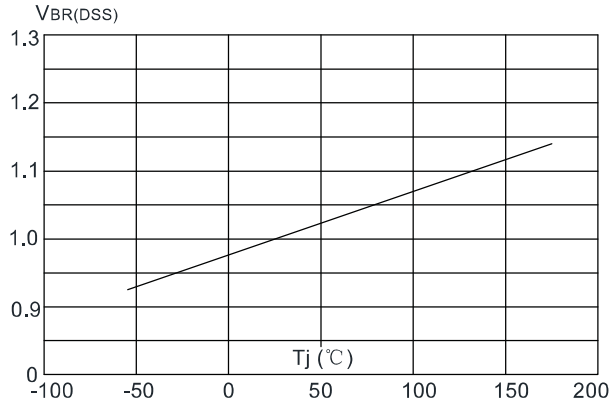


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

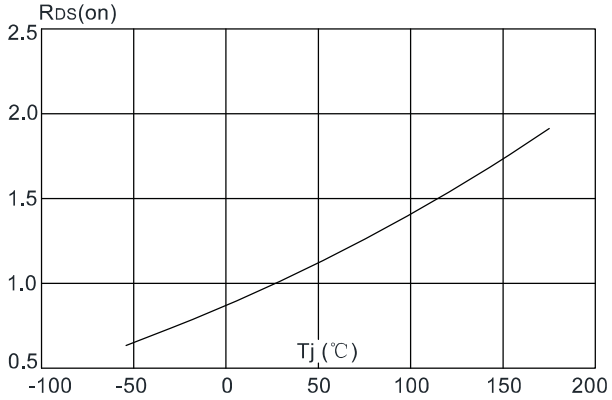


Figure 8: Normalized on Resistance vs. Junction Temperature

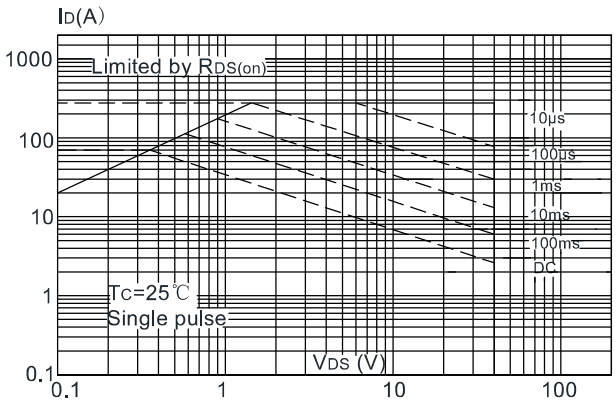


Figure 9: Maximum Safe Operating Area

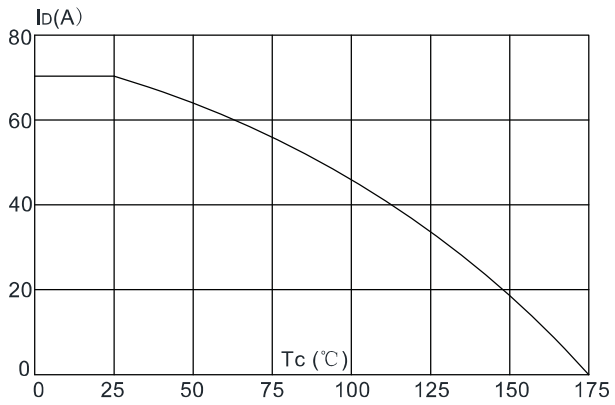


Figure 10: Maximum Continuous Drain Current vs Case Temperature

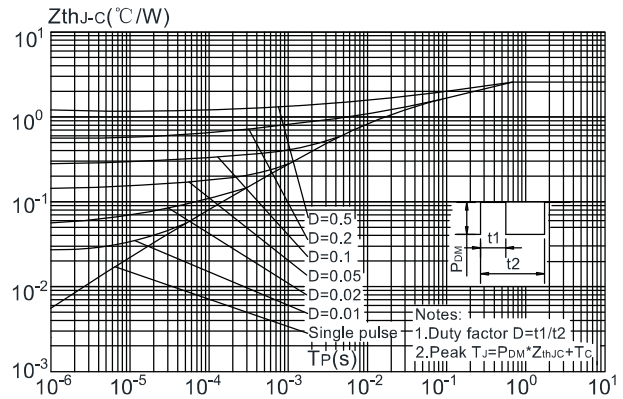
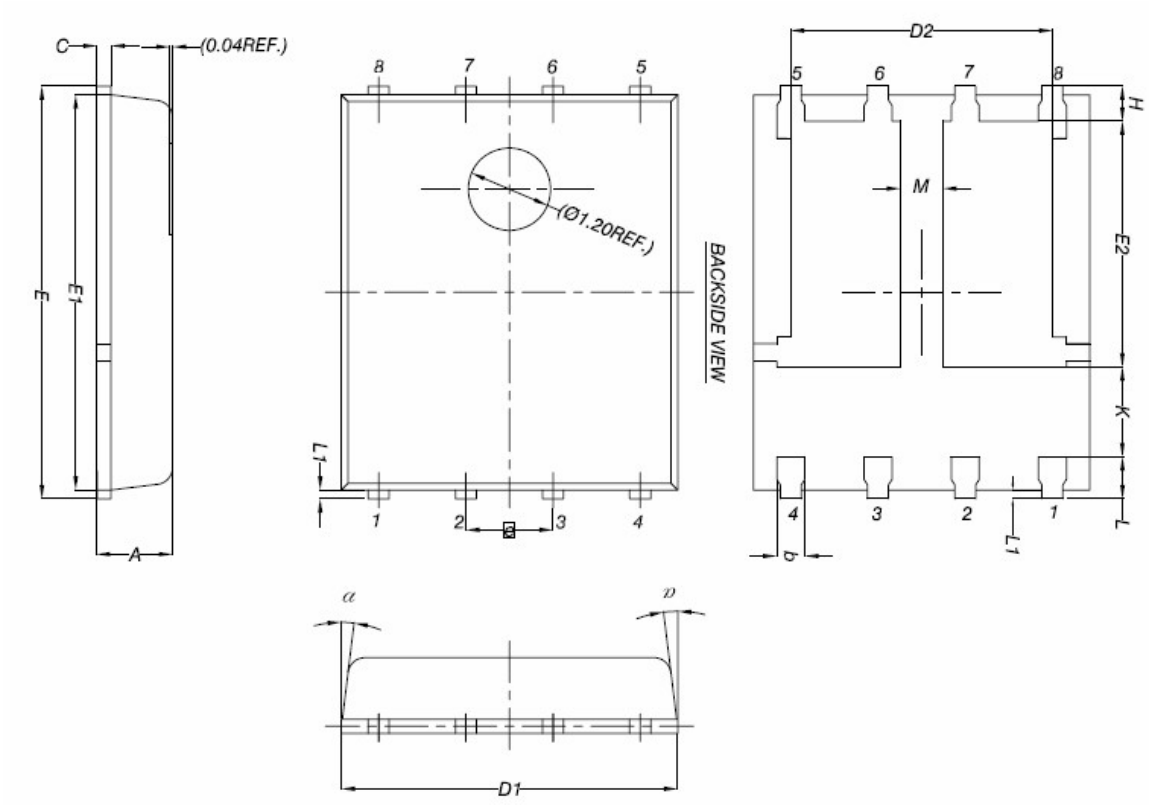


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°