Dual Output LCD Bias for Smartphones and Tablets

General Description

The RT4801T is a highly integrated Boost and LDO and inverting charge pump to generate positive and negative output voltage. The output voltages can be adjusted from ±4V to ±6V with 100mV steps by I^2C interface protocols. With its input voltage range of 2.5V to 5.5V, the RT4801T is optimized for products powered by single-cell batteries and symmetrical output currents up to 150mA. The RT4801T is available in the WL-CSP-15B 1.31x2.07 (BSC) package.

Ordering Information

RT4801T□

Package Type
WSC : WL-CSP-15B 1.31x2.07 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

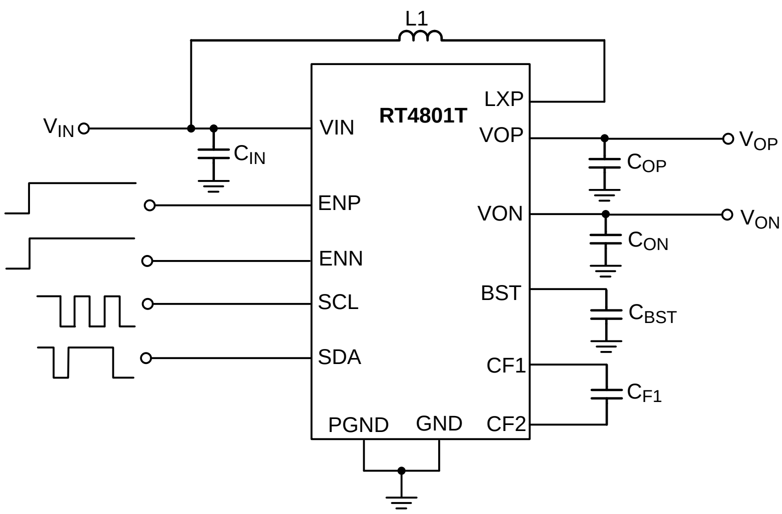
Features

- **2.5V to 5.5V Supply Voltage Range**
- **Up to 90% Efficiency with Small Magnetics**
- **Support Up to 150mA Output Current**
- **Low 1μA Shut Down Current**
- **Internal Soft-start Function**
- **Short Circuit Protection Function**
- **Over-Voltage Protection Function**
- **Over-Current Protection Function**
- **Over-Temperature Protection Function**
- **Elastic Positive and Negative Voltage On/Off Control by ENP/ENN**
- **Voltage Output from 4V to 6V per 0.1V**
- **Low Input Noise and EMI**
- **Output with Programmable Fast Discharge when IC Shut Down**
- **Adjustable Output Voltage by I^2C Compatible Interface**
- **Available in the 15-Ball WL-CSP Package**

Applications

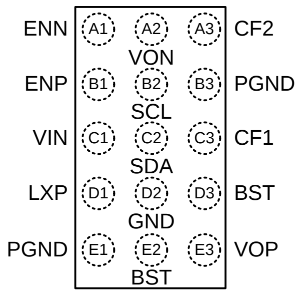
- TFT-LCD Smartphones
- TFT-LCD Tablets
- General Dual Power Supply Applications

Simplified Application Circuit



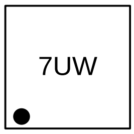
Pin Configuration

(TOP VIEW)



WL-CSP-15B 1.31x2.07 (BSC)

Marking Information

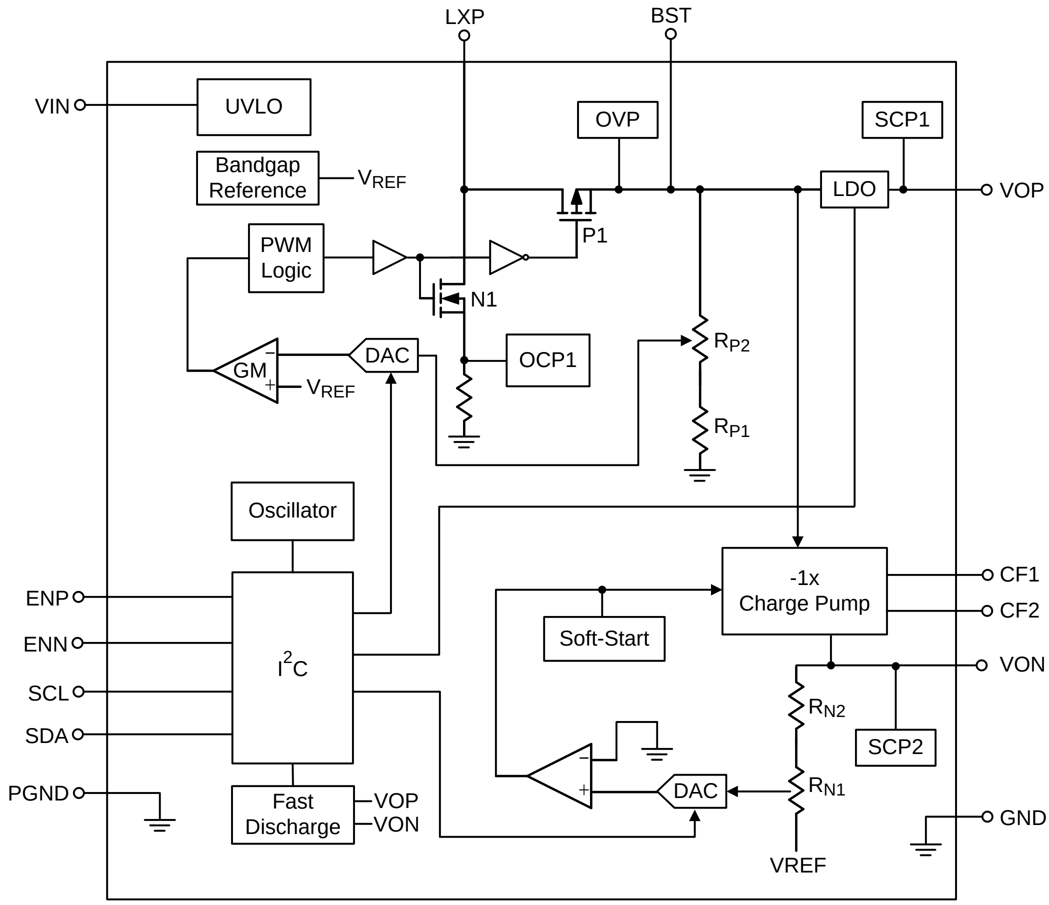


7U : Product Code
W : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	ENN	Enable control input for VON.
A2	VON	Negative terminal output.
A3	CF2	Negative charge pump flying capacitor pin.
B1	ENP	Enable control input for VOP.
B2	SCL	Clock of I^2C.
B3, E1	PGND	Power ground.
C1	VIN	Power input.
C2	SDA	Data of I^2C.
C3	CF1	Negative charge pump flying capacitor pin.
D1	LXP	Switching node of boost converter.
D2	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
D3, E2	BST	Output voltage of boost converter.
E3	VOP	Positive terminal output.

Functional Block Diagram



Operation

The RT4801T is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltages for LCD panel bias or consumer products. It can support input voltage range from 2.5V to 5.5V and the output current up to 150mA. Both positive and negative voltages can be programmed by a MCU through the dedicated I^2C interface. The RT4801T provides Over-Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from damage with abnormal operations. When the EN voltage is logic low for more than 375μs, the IC will be shut down with low input supply current less than 1μA.

Absolute Maximum Ratings (Note 1)

- VIN, BST, VOP, ENP, ENN, CF1, LXP, SCL and SDA ---------- –0.3V to 7V
- LXP (< 100ns) ---------- –2.4V to 10.7V
- VON and CF2 ---------- –7V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-15B 1.31x2.07 (BSC) ---------- 2.00W
- Package Thermal Resistance (Note 2)
  WL-CSP-15B 1.31x2.07 (BSC), θ_{JA} ---------- 49.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.7V, C_{IN} = C_{OP} = C_{F1} = 4.7μF, C_{BST} = C_{ON1}= C_{ON2} = 10μF, L1 = 2.2μH, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V_{IN}		2.5	--	5.5	V
Under Voltage Lockout Threshold Voltage	V_{UVLO_H}	V_{IN} Rising	--	--	2.5	V
	V_{UVLO_L}	V_{IN} Falling	--	--	2.3	
Over-Temperature Protection	T_{OTP}	(Note 5)	--	140	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYST}	(Note 5)	--	15	--	°C
Shut Down Current	I_{SHDN}	ENP = ENN = 0V	--	--	1	μA
Boost Converter						
Boost Voltage Range	V_{BST}		4.15	--	6.2	V
Peak Current Limit	I_{OCP}		--	1.3	--	A
Boost Switching Frequency	f_{OSC_P}		0.8	1	1.2	MHz
LDO						
Positive Output Voltage Range	V_{OP}		4		6	V
Positive Output Voltage Setting Range	V_{OP_SET}	Per step	--	100	--	mV
Positive Output Voltage Accuracy	V_{OP_ACC}		–1	--	1	%

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Output Current Capability		I_{OP_MAX}		--	--	150	mA
Dropout Voltage		V_{OP_DROP}	V_{BST} = 5.4V, V_{OP} = 5.4V, I_{OP} = 100mA	--	--	150	mV
Line Regulation		ΔV_{LINE_OP}	V_{IN} = 2.5 to 5.5V, I_{OP} = 40mA	--	2	--	mV
Load Regulation		ΔV_{LOAD_OP}	ΔI_{OP} = 80mA	--	3	--	%/A
Short Circuit Protection Current		I_{OP_SC}		--	250	--	mA
Fast Discharge Resistance		R_{DISP}		--	70	--	Ω
Negative Charge Pump							
Negative Output Voltage Range		V_{ON}		–4	--	–6	V
Negative Output Voltage Setting Range		V_{ON_SET}	Per step	--	100	--	mV
Negative Output Voltage Accuracy		V_{ON_ACC}		–1	--	1	%
Negative Output Current Capability		I_{ON_MAX}		--	--	150	mA
Negative Charge Pump Switching Frequency		f_{OSC_N}		0.8	1	1.2	MHz
Line Regulation		ΔV_{LINE_ON}	V_{IN} = 2.5 to 5.5V, I_{ON} = 40mA	--	10	--	mV
Load Regulation		ΔV_{LOAD_ON}	ΔI_{ON} = 80mA	--	6	--	%/A
Short Circuit Protection Level		V_{ON_SC}	Percentage of target value	--	75	--	%
Fast Discharge Resistance		R_{DISN}		--	20	--	Ω
Logic Input (ENP, ENN, SCL, SDA)							
Input Threshold Voltage	Logic-High	V_{IH}	V_{IN} =2.5V to 5.5V	1.2	--	--	V
	Logic-Low	V_{IL}	V_{IN} =2.5V to 5.5V	--	--	0.4	
ENP, ENN Pull-down Resistance		R_{EN}		--	200	--	kΩ
SDA, SCL Sink Current		I_{IH}	V_{SDA} , V_{SCL} = 3V	--	0.5	--	μA
SDA, SCL Logic Input Voltage	Low-Level	V_{SCL_L}		--	--	0.4	V
	High-Level	V_{SCL_H}		1.2	--	--	
SCL Clock Frequency		f_{CLK}		--	--	400	kHz
Output Fall Time		$t_{FL2COUT}$		--	--	250	ns
Bus Free Time Between Stop/Start		t_{BUF}		1.3	--	--	μs
Hold Time Start Condition		$t_{HD,STA}$		0.6	--	--	μs
Setup Time for Start Condition		$t_{SU,STA}$		0.6	--	--	μs
SCL Low Time		t_{LOW}		1.3	--	--	μs
SCL High Time		t_{HIGH}		0.6	--	--	μs
Data Setup Time		$t_{SU,DAT}$		100	--	--	ns
Data Hold Time		$t_{HD,DAT}$		0	--	900	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time for Stop Condition	$t_{SU,STO}$		0.6	--	--	μs

Note 1. Stresses beyond those under listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

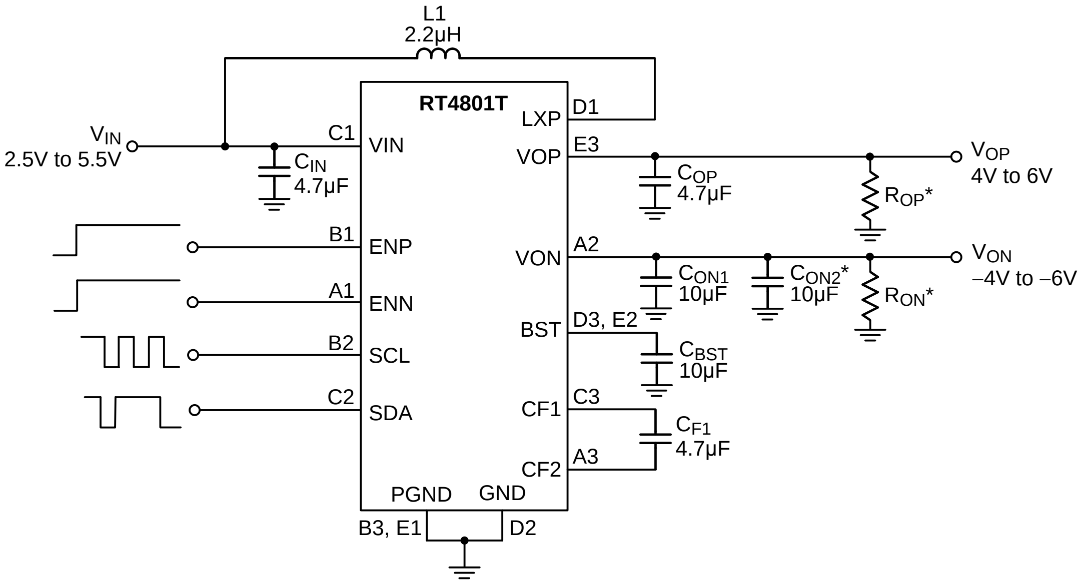
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. T_{OTP}, T_{OTP_HYST} are guaranteed by design.

Typical Application Circuit



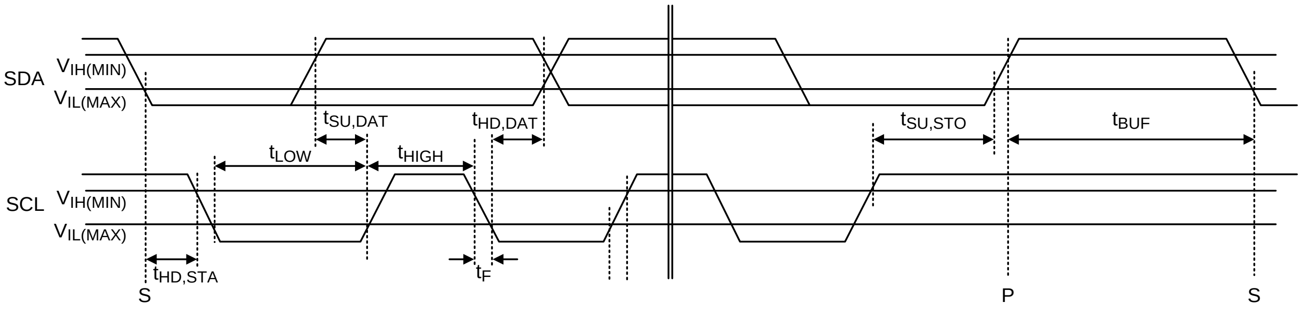
* : (1) R_{OP} and R_{ON} should be paralleled with V_{OP} and V_{ON} if output continuous discharge is required when channel is powered off.

(2) C_{ON2} is suggest to be paralleled with C_{ON1} to get better performance when output 150mA application.

Table 1. Component List of Evaluation Board

Reference	Qty	Part Number	Description	Package	Supplier
C_{IN}, C_{OP}, C_{F1}	1	GRM188R61C475KAAJ	4.7μF/16V/X5R	0603	Murata
C_{BST}, C_{ON1}, C_{ON2}	1	GRM188R61C106KAAL	10μF/16V/X5R	0603	Murata
L1	1	1269AS-H-2R2N=P2	2.2μH/130mΩ	2.5 x 2.0 x 1.0mm	Toko

I²C Interface



I²C Command

Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
1	1	1	0	0	1	1	R/$\overline{W}$

Write Command

(a) Write single byte of data to Register

Slave Address / Register Address / Data From Master

Start	1	1	1	0	0	1	1	0	Slave ACK	R7	R6	R5	R4	R3	R2	R1	R0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK	Stop

(b) Write multiple bytes of data to Registers

Slave Address / Register Address n_{th} / n_{th} Data From Master

Start	1	1	1	0	0	1	1	0	Slave ACK	R7	R6	R5	R4	R3	R2	R1	R0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK

$(n + 1)_{th}$ Data From Master / Last Data From Master

D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK	....	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK	Stop

Read Command

(a) Read single byte of data from Register

Slave Address / Register Address

Start	1	1	1	0	0	1	1	0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK

Slave Address / Data From Master

Re-start	1	1	1	0	0	1	1	1	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Master NACK	Stop

(b) Read multiple bytes of data from Registers

Slave Address / Register Address

Start	1	1	1	0	0	1	1	0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK

Slave Address / n_{th} Data From Master / Last Data From Master

Re-start	1	1	1	0	0	1	1	1	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Master ACK	....	D7	D6	D5	D4	D3	D2	D1	D0	Master NACK	Stop

Start : Start command

R7 to R0 : Register Address.

VOP : Register address = 0X00h

VON : Register address = 0X01h

DISP : Register address = 0x03h

DISN : Register address = 0x03h

APPS : Register address = 0x03h

R/W : Read active (R/W = H) or Write active (R/W = L)

ACK : Acknowledge = L active

D7 to D0 : Write data when WRITE command or read data when READ command

Stop : Stop command

Registers Map

Table 2. VOP Voltage Selection

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VOP(V)
VOP	00h	00h	Reserved	Reserved	Reserved	0	0	0	0	0	4
VOP	00h	01h	Reserved	Reserved	Reserved	0	0	0	0	1	4.1
VOP	00h	02h	Reserved	Reserved	Reserved	0	0	0	1	0	4.2
VOP	00h	03h	Reserved	Reserved	Reserved	0	0	0	1	1	4.3
VOP	00h	04h	Reserved	Reserved	Reserved	0	0	1	0	0	4.4
VOP	00h	05h	Reserved	Reserved	Reserved	0	0	1	0	1	4.5
VOP	00h	06h	Reserved	Reserved	Reserved	0	0	1	1	0	4.6
VOP	00h	07h	Reserved	Reserved	Reserved	0	0	1	1	1	4.7
VOP	00h	08h	Reserved	Reserved	Reserved	0	1	0	0	0	4.8
VOP	00h	09h	Reserved	Reserved	Reserved	0	1	0	0	1	4.9
VOP	00h	0Ah	Reserved	Reserved	Reserved	0	1	0	1	0	5
VOP	00h	0Bh	Reserved	Reserved	Reserved	0	1	0	1	1	5.1
VOP	00h	0Ch	Reserved	Reserved	Reserved	0	1	1	0	0	5.2
VOP	00h	0Dh	Reserved	Reserved	Reserved	0	1	1	0	1	5.3
VOP	00h	0Eh	Reserved	Reserved	Reserved	0	1	1	1	0	5.4
VOP	00h	0Fh	Reserved	Reserved	Reserved	0	1	1	1	1	5.5
VOP	00h	10h	Reserved	Reserved	Reserved	1	0	0	0	0	5.6
VOP	00h	11h	Reserved	Reserved	Reserved	1	0	0	0	1	5.7
VOP	00h	12h	Reserved	Reserved	Reserved	1	0	0	1	0	5.8
VOP	00h	13h	Reserved	Reserved	Reserved	1	0	0	1	1	5.9
VOP	00h	14h	Reserved	Reserved	Reserved	1	0	1	0	0	6

Table 3. VON Voltage Selection

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON(V)
VON	01h	00h	Reserved	Reserved	Reserved	0	0	0	0	0	-4
VON	01h	01h	Reserved	Reserved	Reserved	0	0	0	0	1	-4.1
VON	01h	02h	Reserved	Reserved	Reserved	0	0	0	1	0	-4.2
VON	01h	03h	Reserved	Reserved	Reserved	0	0	0	1	1	-4.3
VON	01h	04h	Reserved	Reserved	Reserved	0	0	1	0	0	-4.4
VON	01h	05h	Reserved	Reserved	Reserved	0	0	1	0	1	-4.5
VON	01h	06h	Reserved	Reserved	Reserved	0	0	1	1	0	-4.6
VON	01h	07h	Reserved	Reserved	Reserved	0	0	1	1	1	-4.7
VON	01h	08h	Reserved	Reserved	Reserved	0	1	0	0	0	-4.8
VON	01h	09h	Reserved	Reserved	Reserved	0	1	0	0	1	-4.9
VON	01h	0Ah	Reserved	Reserved	Reserved	0	1	0	1	0	-5
VON	01h	0Bh	Reserved	Reserved	Reserved	0	1	0	1	1	-5.1
VON	01h	0Ch	Reserved	Reserved	Reserved	0	1	1	0	0	-5.2

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON(V)
VON	01h	0Dh	Reserved	Reserved	Reserved	0	1	1	0	1	-5.3
VON	01h	0Eh	Reserved	Reserved	Reserved	0	1	1	1	0	-5.4
VON	01h	0Fh	Reserved	Reserved	Reserved	0	1	1	1	1	-5.5
VON	01h	10h	Reserved	Reserved	Reserved	1	0	0	0	0	-5.6
VON	01h	11h	Reserved	Reserved	Reserved	1	0	0	0	1	-5.7
VON	01h	12h	Reserved	Reserved	Reserved	1	0	0	1	0	-5.8
VON	01h	13h	Reserved	Reserved	Reserved	1	0	0	1	1	-5.9
VON	01h	14h	Reserved	Reserved	Reserved	1	0	1	0	0	-6

Table 4. VOP Active Discharge

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VOP Discharge
DISP	03h	00h	Reserved	APPS	Reserved	Reserved	Reserved	Reserved	0	DISN	W/O
DISP	03h	02h	Reserved	APPS	Reserved	Reserved	Reserved	Reserved	1	DISN	W

Table 5. VON Active Discharge

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON Discharge
DISN	03h	00h	Reserved	APPS	Reserved	Reserved	Reserved	Reserved	DISP	0	W/O
DISN	03h	01h	Reserved	APPS	Reserved	Reserved	Reserved	Reserved	DISP	1	W

Table 6. Application

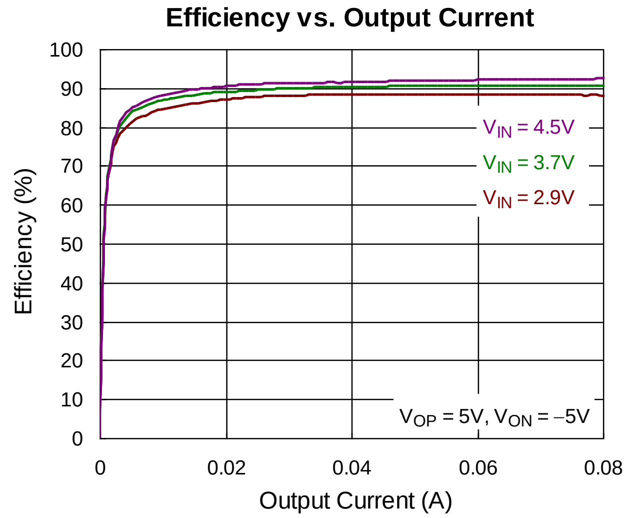
Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Application
APPS	03h	00h	Reserved	0	Reserved	Reserved	Reserved	Reserved	DISP	DISN	Tablet
APPS	03h	40h	Reserved	1	Reserved	Reserved	Reserved	Reserved	DISP	DISN	Smartphone

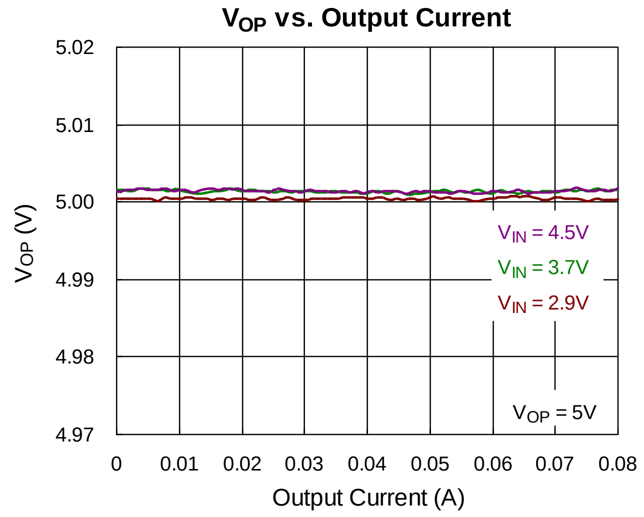
The Reserved bits are ignored when written and return either 0 or 1 when read.

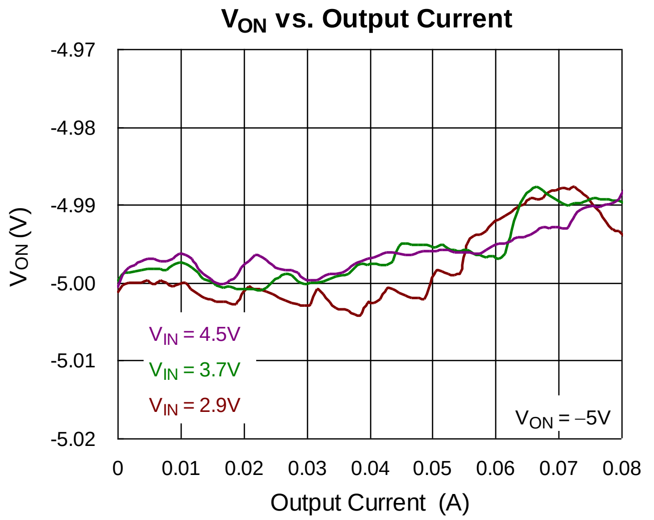
Factory Default Register Value

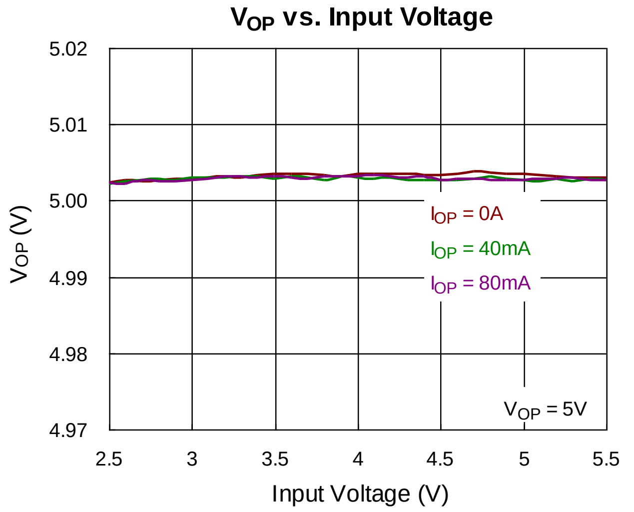
Name	Register Address	DATA
VOP	00h	0Ah
VON	01h	0Ah
DISP	03h	43h
DISN	03h	43h
APPS	03h	43h

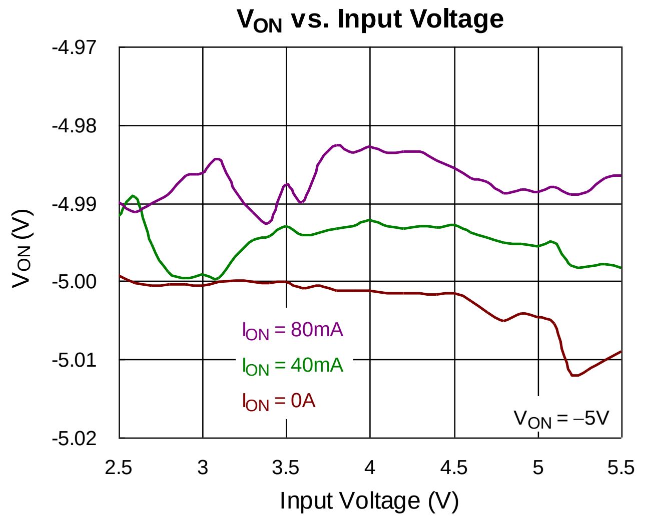
Typical Operating Characteristics

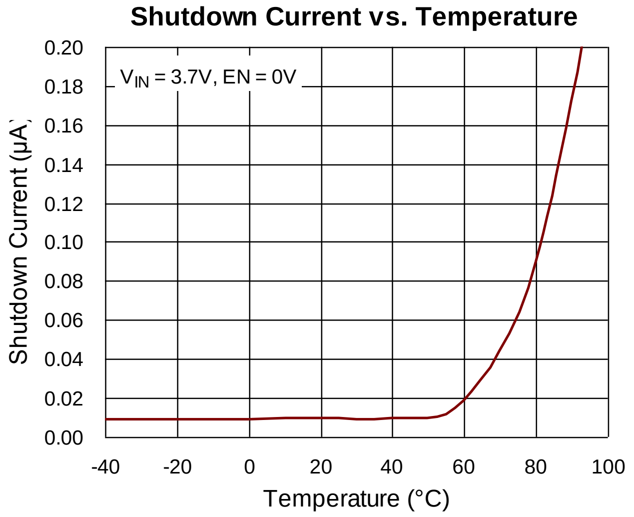




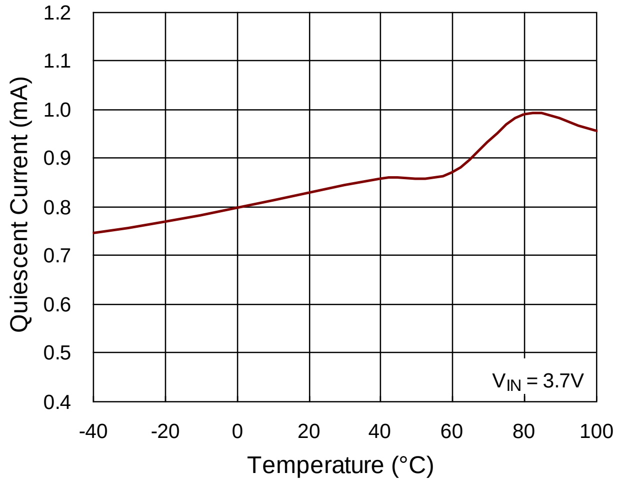




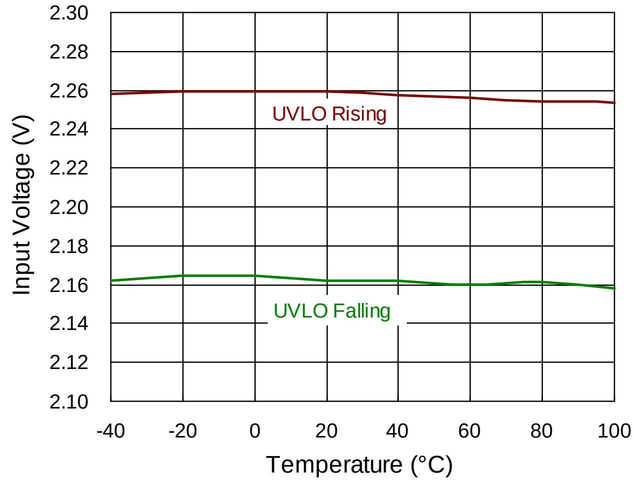




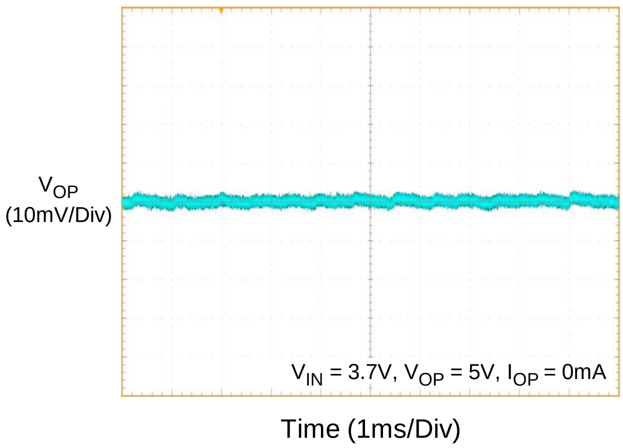
Quiescent Current vs. Temperature



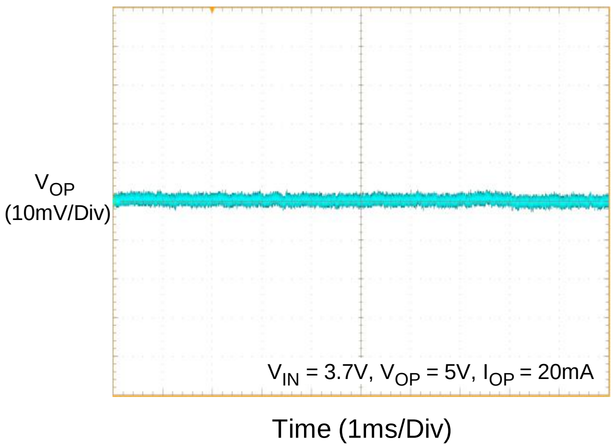
Input Voltage vs. Temperature



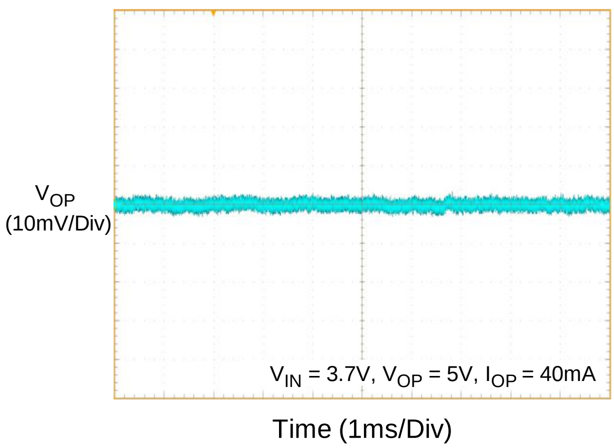
V_{OP} Ripple Voltage



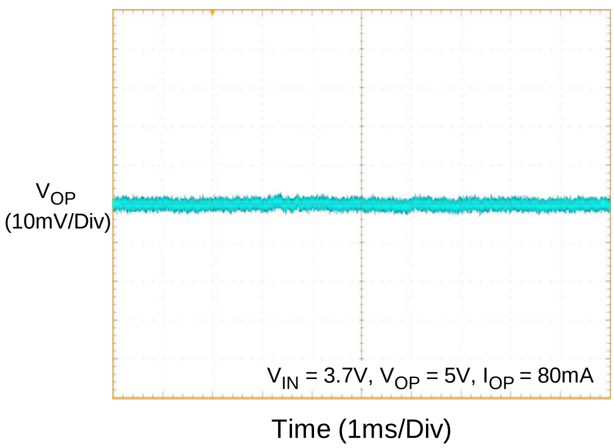
V_{OP} Ripple Voltage



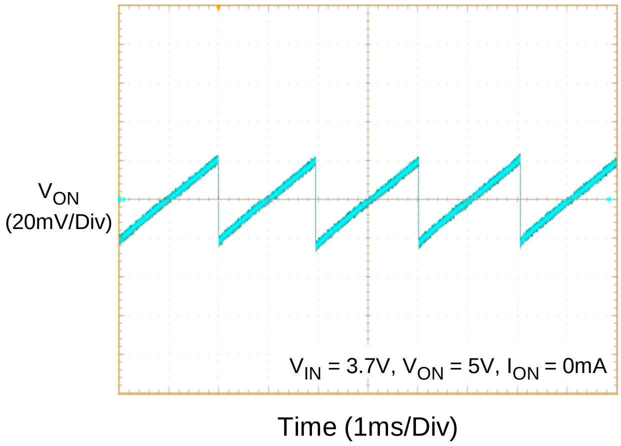
V_{OP} Ripple Voltage



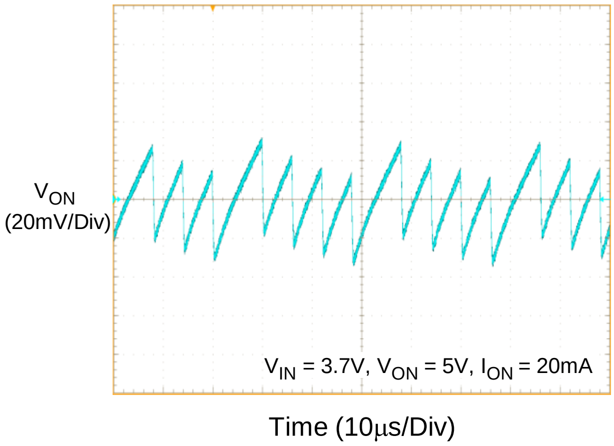
V_{OP} Ripple Voltage



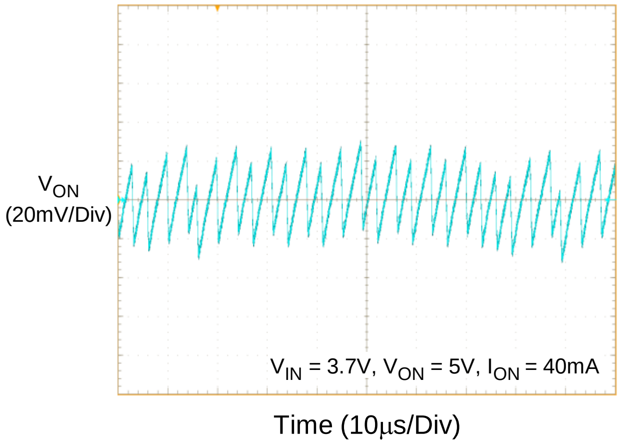
V_{ON} Ripple Voltage



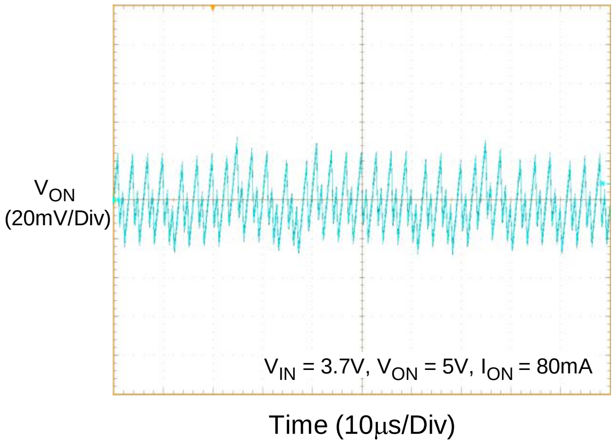
V_{ON} Ripple Voltage



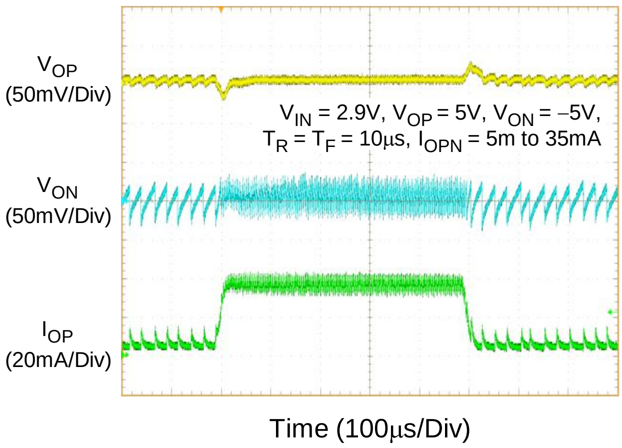
V_{ON} Ripple Voltage



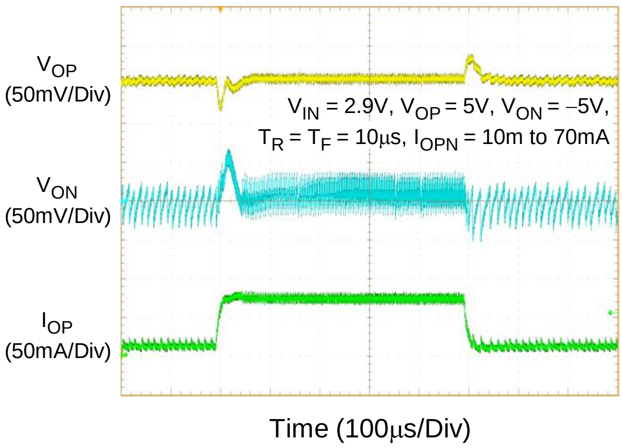
V_{ON} Ripple Voltage



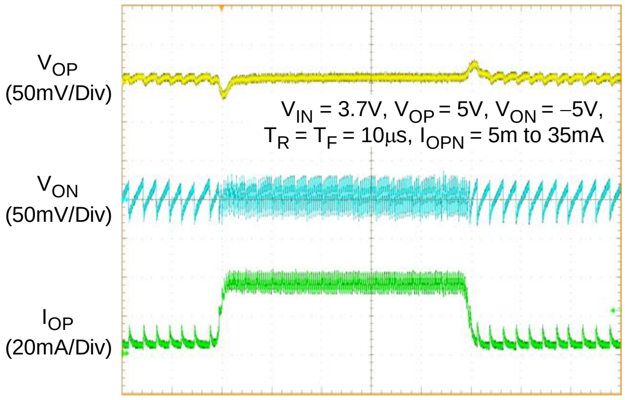
Load Transient



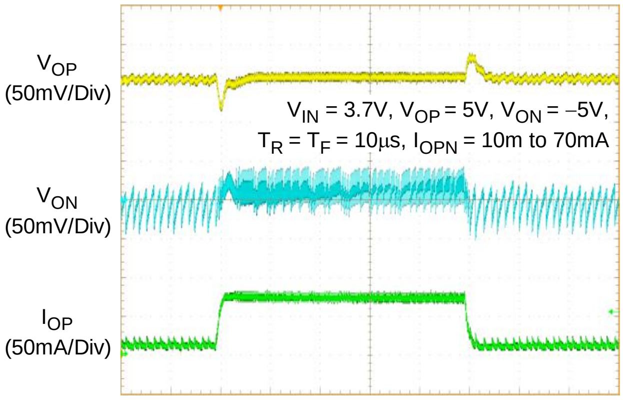
Load Transient



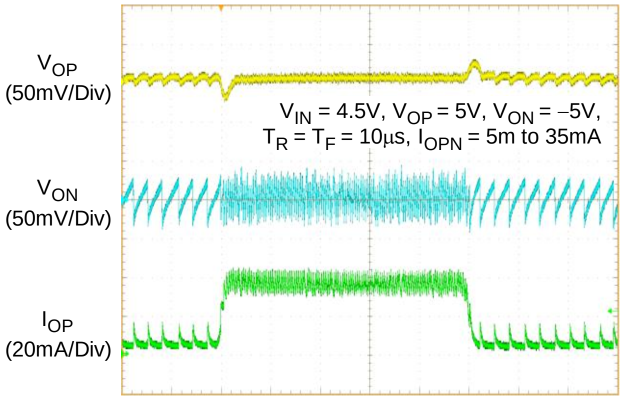
Load Transient



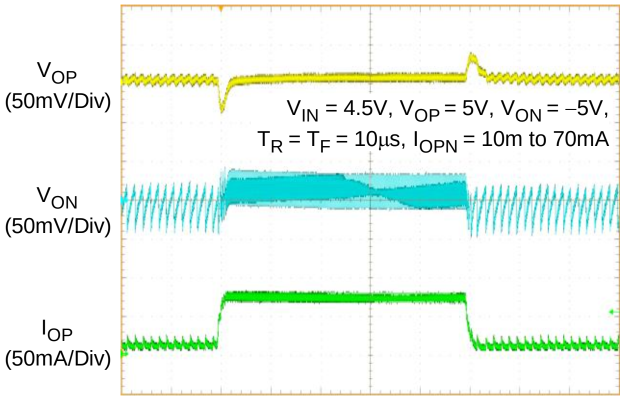
Load Transient



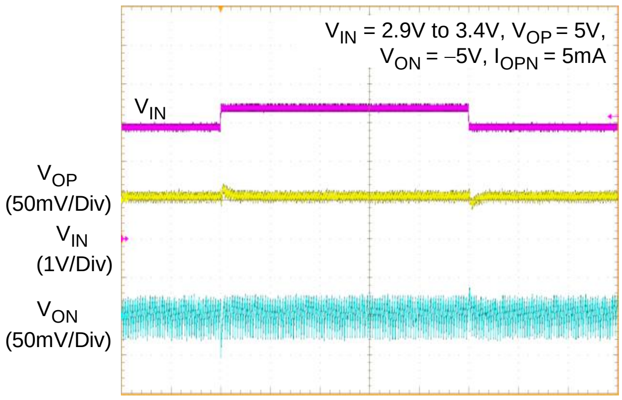
Load Transient



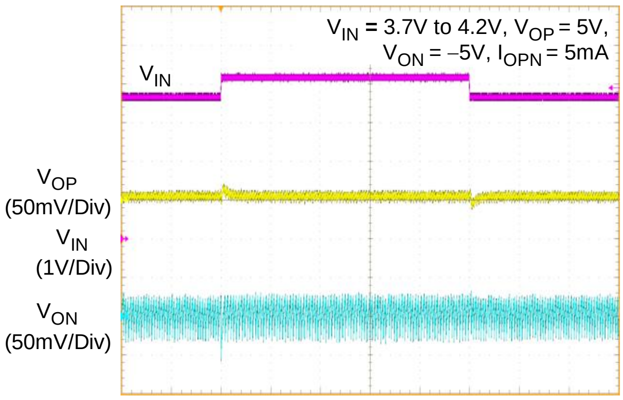
Load Transient



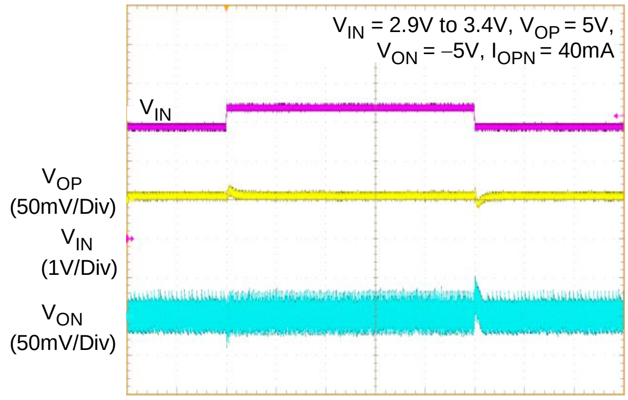
Line Transient



Line Transient

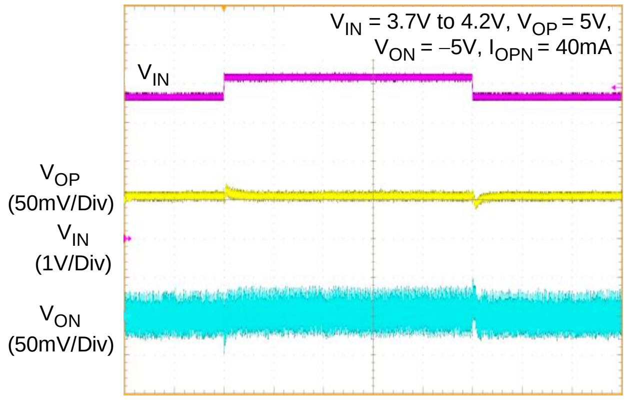


Line Transient



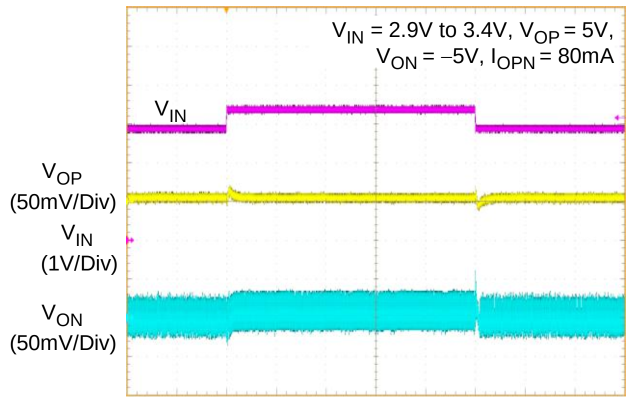
Time (500μs/Div)

Line Transient



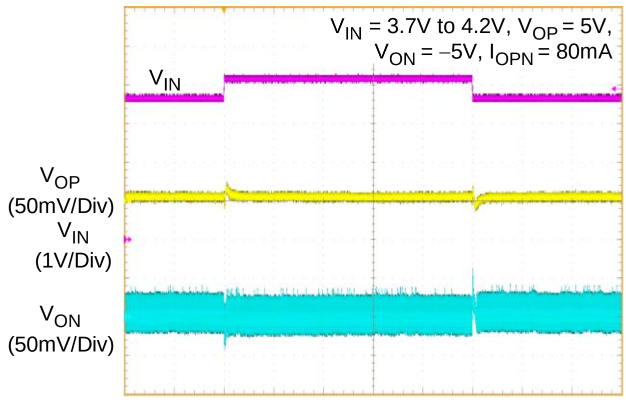
Time (500μs/Div)

Line Transient



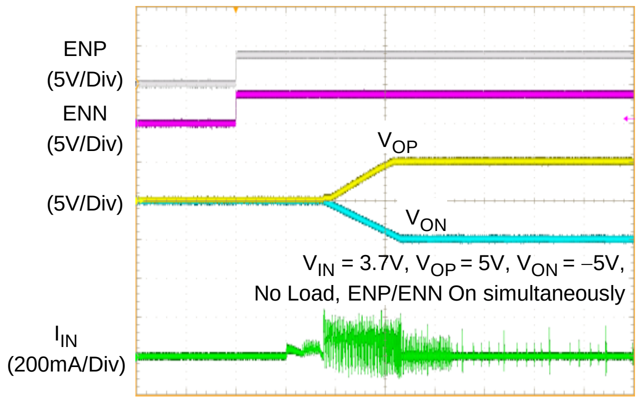
Time (500μs/Div)

Line Transient



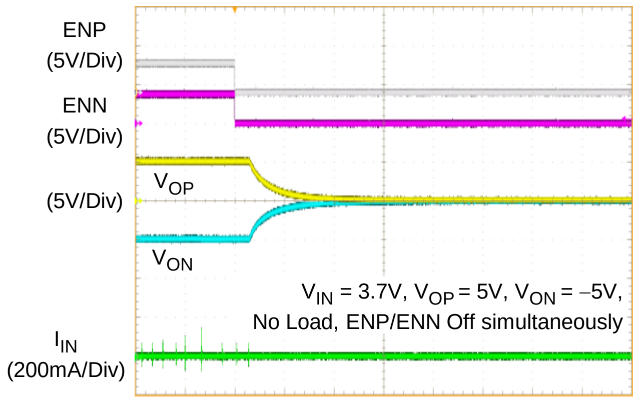
Time (500μs/Div)

Power On



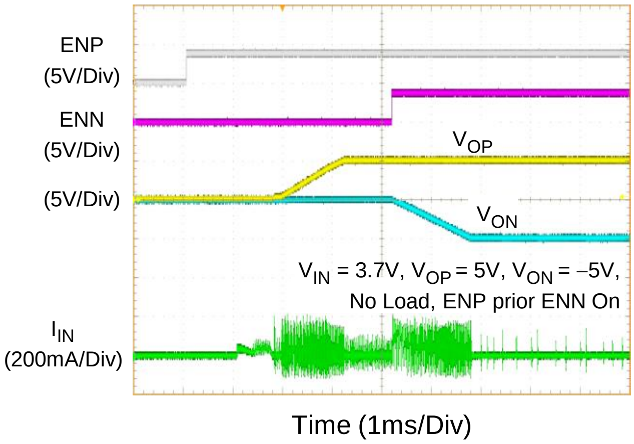
Time (1ms/Div)

Power Off

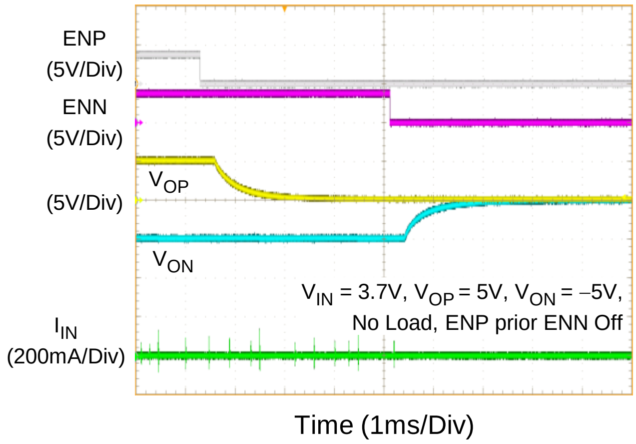


Time (1ms/Div)

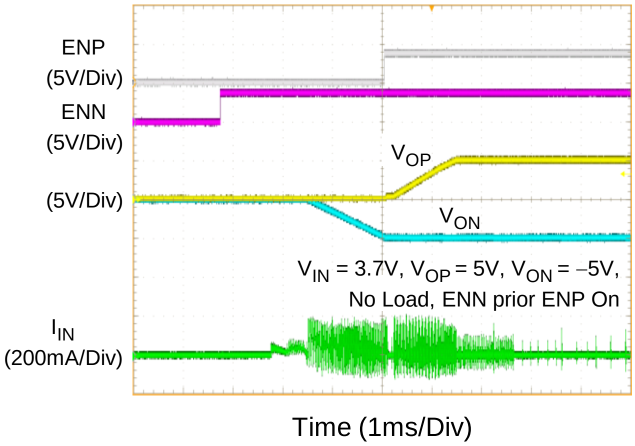
Power On



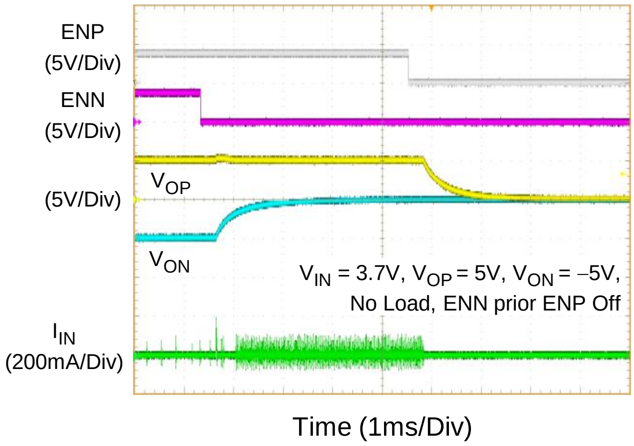
Power Off



Power On



Power Off



Application Information

The RT4801T is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltages for LCD panel bias or consumer products. It can support input voltage range from 2.5V to 5.5V and the output current up to 150mA. The V_{OP} positive output voltage is generated from the LDO supplied from a synchronous Boost converter, and V_{OP} is set at a typical value of 5V. The Boost converter output also drives an inverting charge pump controller to generate V_{ON} negative output voltage which is set at a typical value of −5V. Both positive and negative voltages can be programmed by a MCU through the dedicated I^2C interface and the available voltage range is from ±4V to ±6V with 100mV per step.

Input Capacitor Selection

Input ceramic capacitor with 4.7μF capacitance is suggested for applications. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the VOP Boost converter, $I_{IN(MAX)}$ is the maximum input current, and ΔI_L is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$I_{PEAK} = 1.2 \times I_{IN(MAX)}$

Note that the saturated current of the inductor must be greater than I_{PEAK}.

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating IC performance. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the ΔV_{OUT1} value can be calculated as the following equation :

$$Q = I_{OUT} \times D \times \frac{1}{f_{SOC}} = C_{OUT} \times \Delta V_{OUT1}$$

$$\Delta V_{OUT1} = \frac{I_{OUT} \times D}{f_{SOC} \times C_{OUT}}$$

where f_{OSC} is the switching frequency and D is the duty cycle.

Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{SER} + \frac{I_{OUT} \times D}{f_{OSC} \times C_{OUT}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

The output capacitor, C_{OUT}, should be selected accordingly.

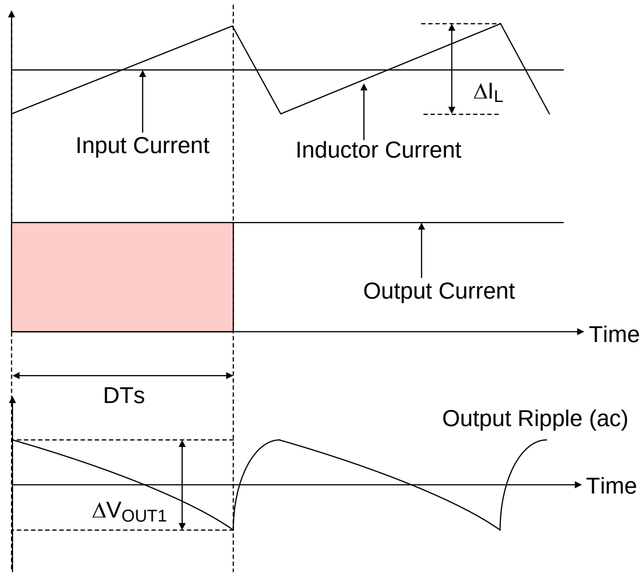


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Under Voltage Lockout

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down IC operation when input voltage is lower than the specified threshold voltage.

Soft-Start

The RT4801T employs an internal soft-start feature to avoid high inrush current during start-up. The soft-start function is achieved by clamping the output voltage of the internal error amplifier with another voltage source that is increased slowly from zero to near VIN during the soft-start period.

Output Voltage Setting

The output voltage of WL-CSP package can be programmed by a MCU through the dedicated I^2C interface according to the V_{OP}/V_{ON} Voltage Selection Table.

Shut Down Delay and Discharge

When the EN signal is logic low for more than 375μs, the output will be powered off. When the output discharge function is selected, the RT4801T starts to discharge the output voltage to ground with 20ms duration and then the output goes back to floating state. If the output continuous discharge function is required for application, the external resistor is recommended to be paralleled with the output. In shut down mode, the input supply current for the IC is less than 1μA.

Over-Current Protection

The RT4801T includes a cycle-by-cycle current limit function which monitors the inductor current during each ON period. The power switch will be forced off to avoid large current damage once the current is over the limit level.

Output Short Circuit Protection

The RT4801T has an advanced output short-circuit protection mechanism which prevents the IC from damage by unexpected applications.

- **VOP short to ground**

  When the output current is higher than the current limit level 250mA (typ.) for 1ms (typ.), both VPOS and VON outputs shut down and only can re-start to normal operation after re-toggling the ENP/ENN pin.

- **VON short to ground**

  The RT4801T activates short-circuit protection once the VON voltage drops below 75% (typ.) of target voltage due to excessive loading. The protection stops after the VON voltage backs to higher than the protection level for 1ms (typ.). There is not any influence on VOP.

Over-Temperature Protection

The RT4801T equips an over-temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down LCD bias operation when ambient temperature exceeds 140°C. Once the ambient temperature cools down by approximately 15°C, IC will automatically resume normal operation. To maintain continuous operation, the maximum junction temperature should be prevented from rising above 125°C.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-15B 1.31x2.07 (BSC) package, the thermal resistance, θ_{JA}, is 49.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (49.8°C/W) = 2W for a WL-CSP-15B 1.31x2.07 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

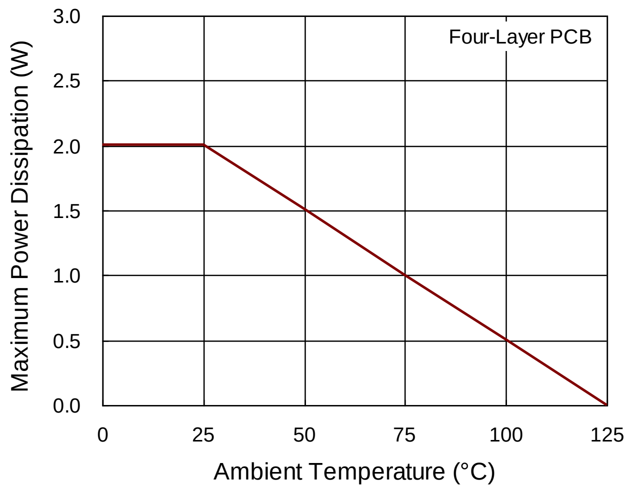


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT4801T, the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power components as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- The flying capacitor should be placed as close to the CF1/CF2 pin as possible to avoid noise injection.
- Minimize the size of the LXP node and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LXP or high-current traces.
- Separate power ground (PGND) and analog ground (GND). Connect the GND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.

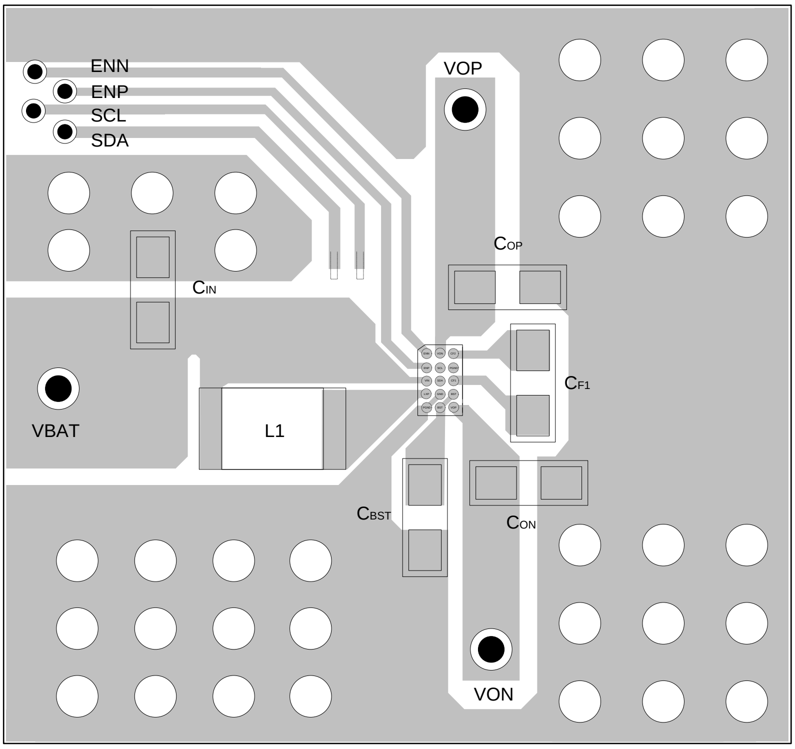
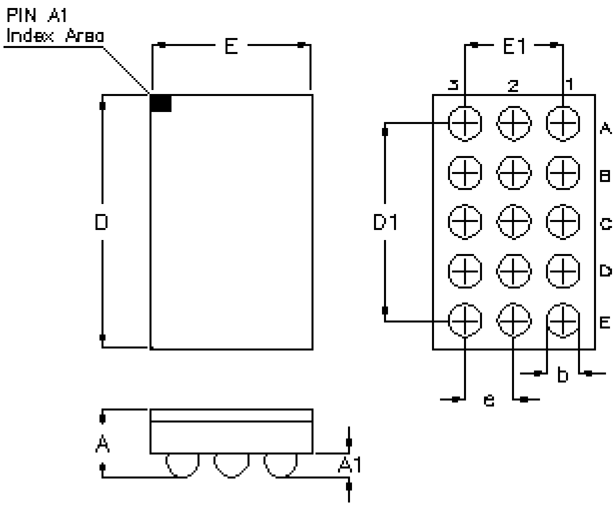


Figure 3. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.020	2.120	0.080	0.083
D1	1.600		0.063	
E	1.260	1.360	0.050	0.054
E1	0.800		0.031	
e	0.400		0.016	

WL-CSP-15B 1.31x2.07 (BSC)