4A, 18V, 500kHz, ACOT™ Step-Down Converter

General Description

The RT6254A/B is a high-performance, synchronous step-down DC-DC converter that can deliver up to 4A output current from a 4.5V to 18V input supply. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode of bootstrap circuit to offer a very compact solution.

The RT6254A/B adopts Advanced Constant On-Time (ACOT™) control architecture that provides ultrafast transient response and further reduces the external-component count. In steady states, the ACOT™ operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers Independent enable control input pin and power good indicator (TSOT-23-8 only) for easily sequence control. To control the inrush current during the startup, the device provides a fixed 1.5ms soft-start up. Fully protection features are also integrated in the device including the cycle-by-cycle current limit control, UVP, input UVLO and OTP.

The RT6254A/B is available in the TSOT-23-6 (FC) and TSOT-23-8 (FC) package.

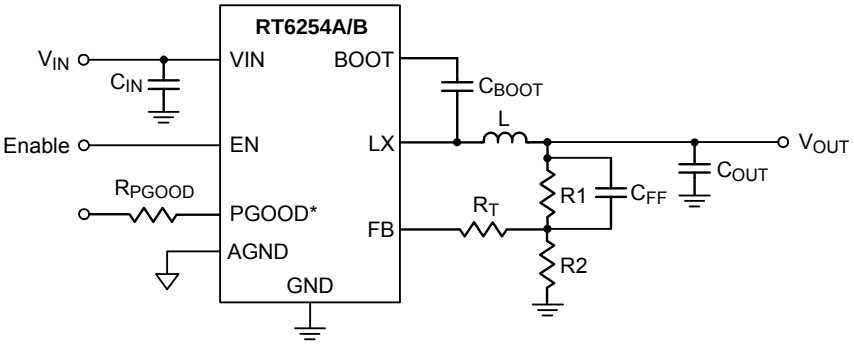
Features

- **4.5V to 18V Input Voltage Range**
- **4A Output Current**
- **Constant-on-Time Mode to Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **500kHz Switching Frequency**
- **High Efficient Internal Power MOSFET Switch Optimized for Lower Duty Cycle Applications**
- **Integrated 48mΩ/25mΩ MOSFETs**
- **Adjustable Output Voltage from 0.6V to 5V**
- **Internal Soft-Start (1.5ms typ.)**
- **Built-In UVP/OTP**
- **Power Good Indicator (90%)**
- **Input Under Voltage Lockout**
- **TSOT-23-6 (FC) and TSOT-23-8 (FC) Packages**

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Simplified Application Circuit



* : PGOOD pin is for TSOT23-8 (FC) package.

Ordering Information

RT6254A/B □□□

- Package Type
  - J6F : TSOT-23-6 (FC)
  - J8F : TSOT-23-8 (FC)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- UVP Option
  - H : Hiccup
- PSM/PWM
  - A : PSM/PWM
  - B : Force-PWM

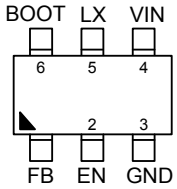
Note :

Richtek products are :

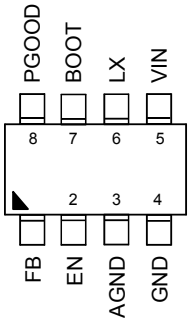
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



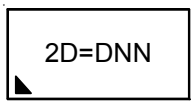
TSOT-23-6 (FC)



TSOT-23-8 (FC)

Marking Information

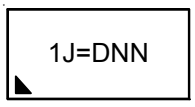
RT6254AHGJ6F



2D= : Product Code

DNN : Date Code

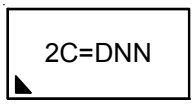
RT6254AHGJ8F



1J= : Product Code

DNN : Date Code

RT6254BHGJ6F



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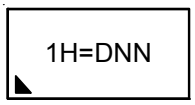

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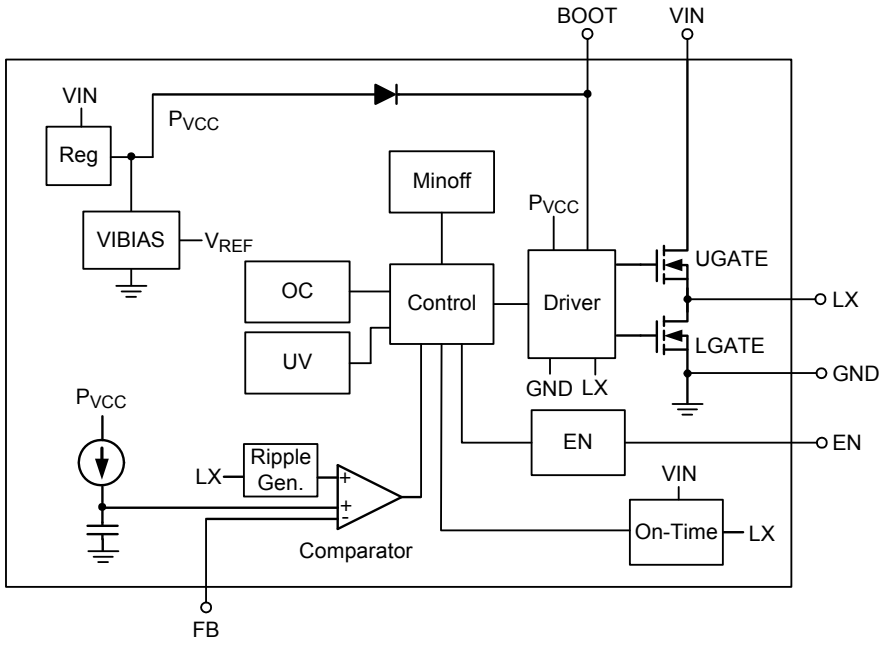
Functional Pin Description

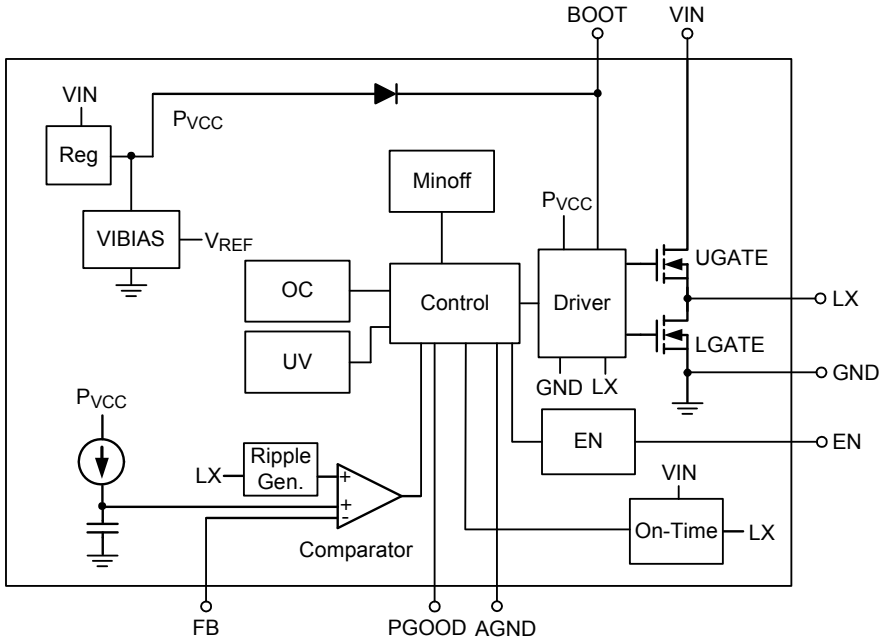
Pin No.		Pin Name	Pin Function
TSOT-23-6 (FC)	TSOT-23-8 (FC)		
1	1	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider.
--	3	AGND	Analog ground. This is the signal ground reference for the IC.
2	2	EN	Enable control input. Connecting this pin to logic high can enable the device and connecting this pin to GND can disable the device.
3	4	GND	System ground. This is the power return for the IC.
4	5	VIN	Power input. Supplies the power switches of the device.
5	6	LX	Switch node. LX is the switching node that supplies power to the output and connect the output LC filter from LX to the output load.
6	7	BOOT	Bootstrap supply for high-side gate driver. Connect a 0.1μF ceramic capacitor from LX to BOOT to power the high-side switch.
--	8	PGOOD	Power good indicator. Open-drain output when the output voltage is within 90% to 120% of regulation point.

Functional Block Diagram

TSOT-23-6 (FC)



TSOT-23-8 (FC)



Operation

The RT6254A/B is a high-efficiency, monolithic synchronous step-down DC-DC converter that can deliver up to 4A output current from a 4.5V to 18V input supply. Using the ACOT™ control mode can reduce the output capacitance and perform fast transient response. It can minimize the component size without additional external compensation network.

Current Limit

The RT6254A/B current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until it drops below the current limit level. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section) the IC will stop switching to avoid excessive heat.

Hiccup Mode

The RT6254A/B use hiccup mode for UVP. When the protection function is triggered, the IC will shut down for a period of time and then attempt to recover automatically. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short circuit is removed.

Input Under-Voltage Lockout

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be lockout.

Shut-Down, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level. When V_{EN} is below this level the IC enters shutdown mode. When V_{EN} exceeds its logic-high level the IC is fully operational.

The power up sequence is shown in Figure 1.

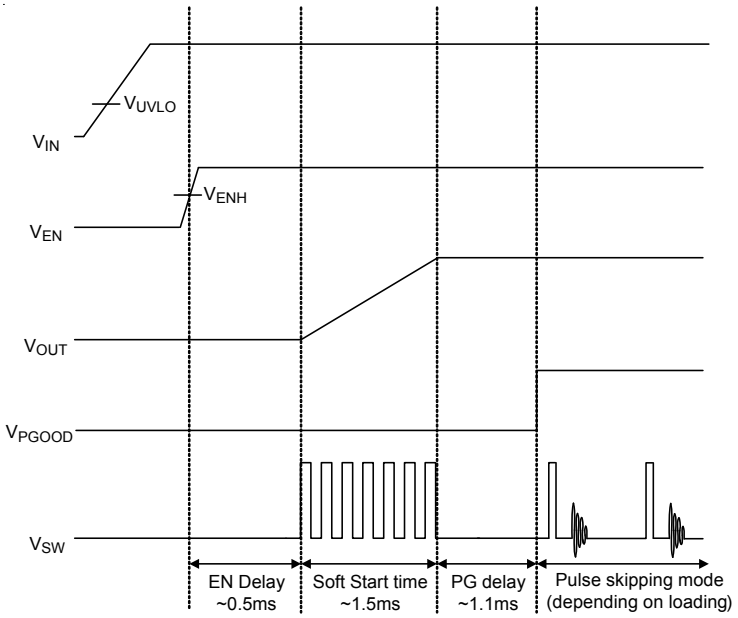


Figure 1. Power Up Sequence

External Bootstrap Capacitor

Connect a 0.1µF low ESR ceramic capacitor between BOOT and LX. This bootstrap capacitor provides the gate driver supply voltage for the high side N-MOSFET switch.

Over-Temperature Protection

The RT6254A/B includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the IC will resume normal operation. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

UVP Protection

The RT6254A/B detects under-voltage conditions by monitoring the feedback voltage on FB pin. When the feedback voltage is lower than 60% of the target voltage, the UVP comparator will go high to turn off both internal high-side and low-side MOSFETs.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Enable Pin Voltage, EN ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –0.3V to 20V
  <100ns ---------- –9V to 27V
- BOOT to LX, V_{BOOT} – V_{LX}, <100ns ---------- –3V to 9V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-6 (FC) ---------- 1.923W
  TSOT-23-8 (FC) ---------- 1.923W
- Package Thermal Resistance (Note 2)
  TSOT-23-6 (FC), θ_{JA} ---------- 52°C/W
  TSOT-23-8 (FC), θ_{JA} ---------- 52°C/W
  TSOT-23-6 (FC), θ_{JC} ---------- 5°C/W
  TSOT-23-8 (FC), θ_{JC} ---------- 5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	18	V
Vin Under-Voltage Lockout Threshold-Rising	V_{UVLO}	VIN rising	3.9	4.1	4.3	V
VIN Under-Voltage Lockout Threshold-Hysteresis	ΔV_{UVLO}		--	0.3	--	V
Supply Current						
Shutdown Current	I_{SHDN}	V_{EN} = 0	--	3	--	μA
Quiescent Current	I_Q	I_{OUT} = 0 V_{FB} = V_{REF} x 105% (no switching)	--	115	--	μA
Soft-Start						
Soft-Start Time	t_{SS}		--	1.5	--	ms

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Voltage							
EN Input Voltage	Logic-High	V_{EN_H}		1.5	--	--	V
	Logic= Low	V_{EN_L}		--	--	0.4	V
Feedback Voltage							
Feedback Voltage		V_{REF}		0.594	0.6	0.606	V
Feedback Current		I_{FB}	V_{FB} = 4V	–50	--	50	nA
Internal MOSFET							
High-Side Switch-On Resistance		$R_{DS(ON)\_H}$	$V_{BOOT} - V_{LX}$ = 4.8V	--	48	--	mΩ
Low-Side Switch-On Resistance		$R_{DS(ON)\_L}$		--	25	--	mΩ
Discharge FET R_{ON}		R_{DISCHG}		--	50	--	Ω
Current Limit							
Hide-Side Switch Current Limit		I_{LIM_H}		--	10	--	A
Low-Side Switch Valley Current Limit		I_{LIM_L}		4.2	6.2	8.2	A
Switching Frequency							
Oscillator Frequency		f_{SW}		400	500	600	kHz
On-Time Timer Control							
Minimum On-Time		t_{ON_MIN}	$V_{IN} = V_{IN(MAX)}$	--	60	--	ns
Minimum Off-Time		t_{OFF_MIN}		--	200	--	ns
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	15	--	°C
Output Under Voltage							
UVP Trip Threshold			UVP detect	--	60	--	%
			Hysteresis	--	10	--	%
Power Good for TSOT 23-8 (FC) Package							
Power Good Threshold		V_{PGOOD}	FB rising	85	90	95	%
			FB falling	80	85	90	%

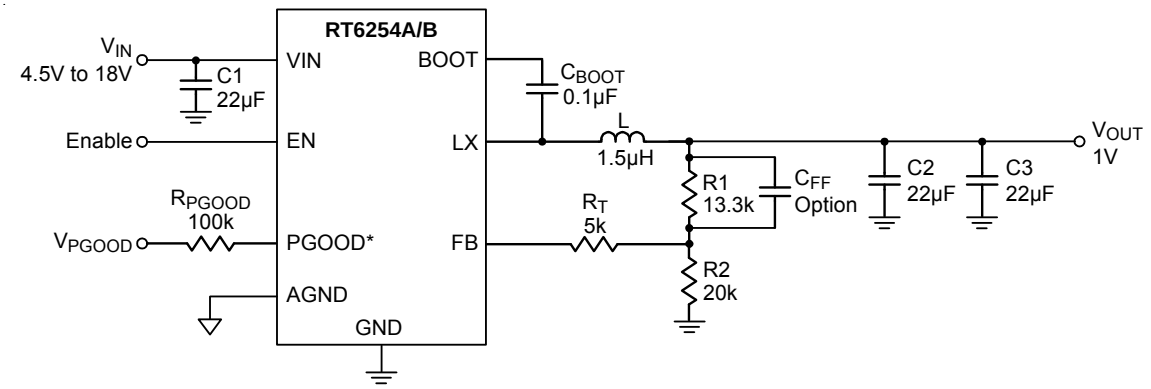
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a Four-layer Richtek Evaluation Board. θ_{JC} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



* : PGOOD pin is for TSOT23-8 (FC) package.

Table 1. Suggested Component Values

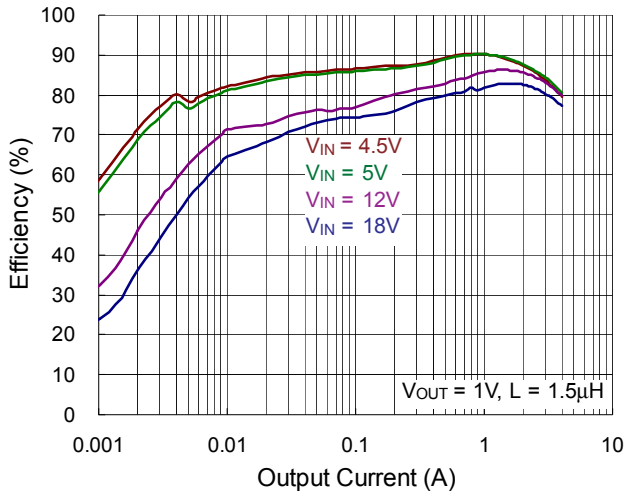
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)
1	13.3	20	1.5	44	--
1.2	20	20	1.5	44	--
1.8	40.2	20	2	44	--
2.5	63.4	20	2.8	44	47 to 82
3.3	90.9	20	3.3	44	47 to 82
5	147	20	4.7	44	47 to 82

Note 1 : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

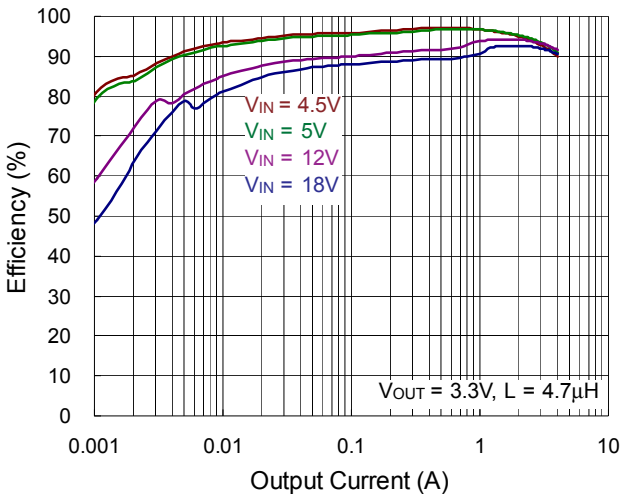
Note 2 : Considering the noise immunity, it is necessary to add RT = 4.99k between feedback network and chip FB pin.

Typical Operating Characteristics

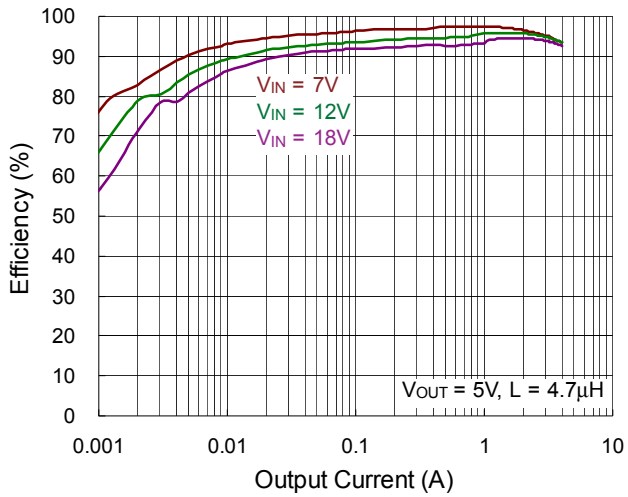
Efficiency vs. Output Current



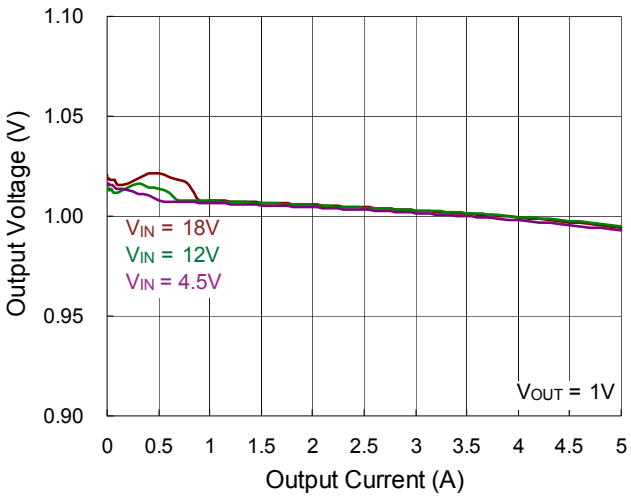
Efficiency vs. Output Current



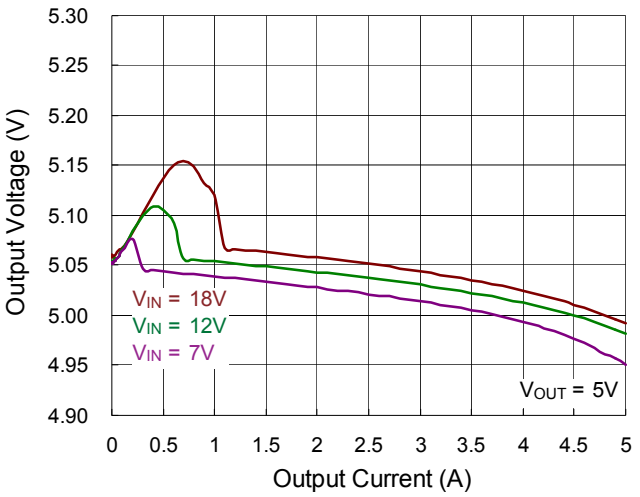
Efficiency vs. Output Current



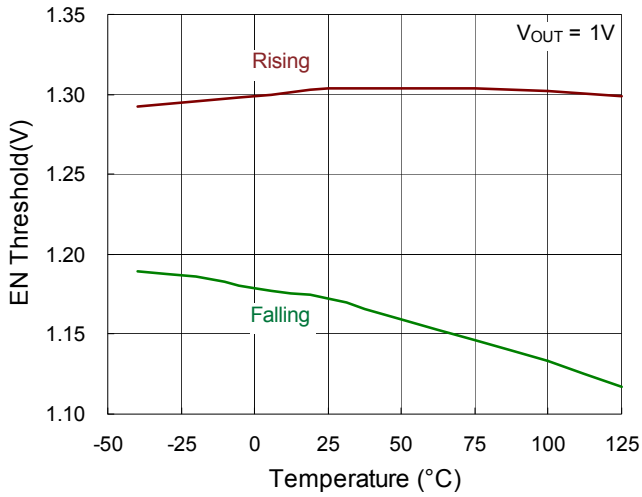
Output Voltage vs. Output Current



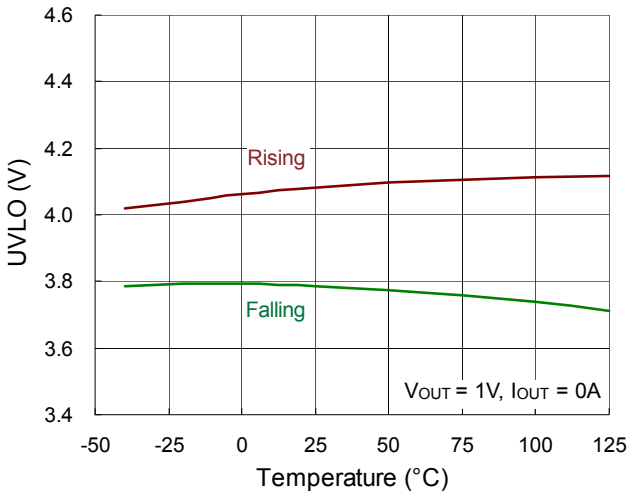
Output Current vs. Output Current



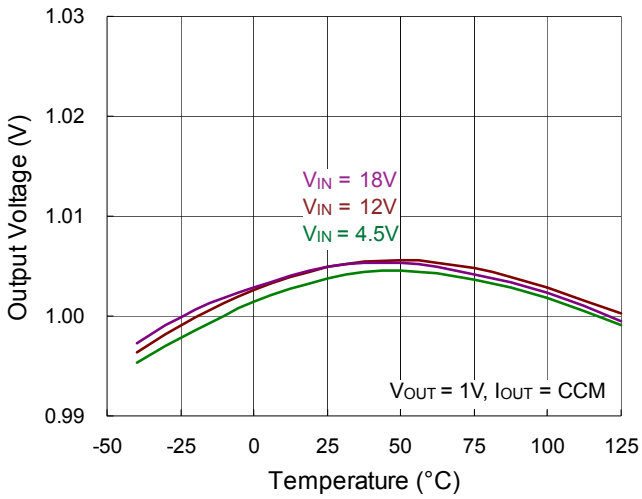
EN Threshold vs. Temperature



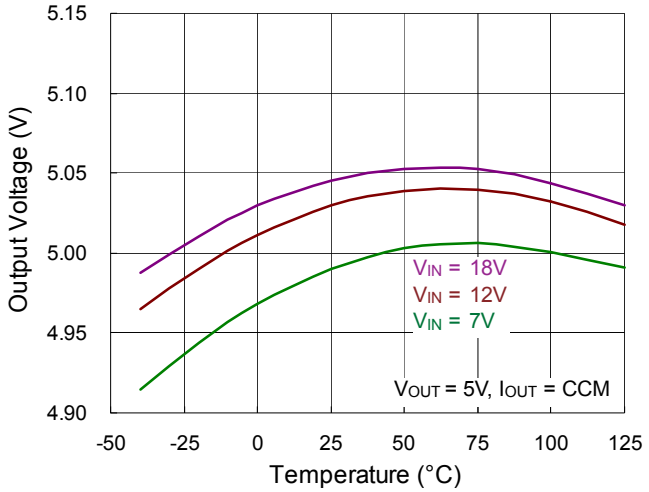
UVLO vs. Temperature



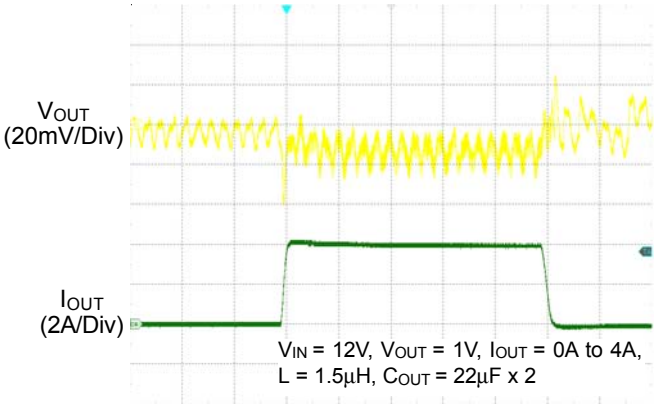
Output Voltage vs. Temperature



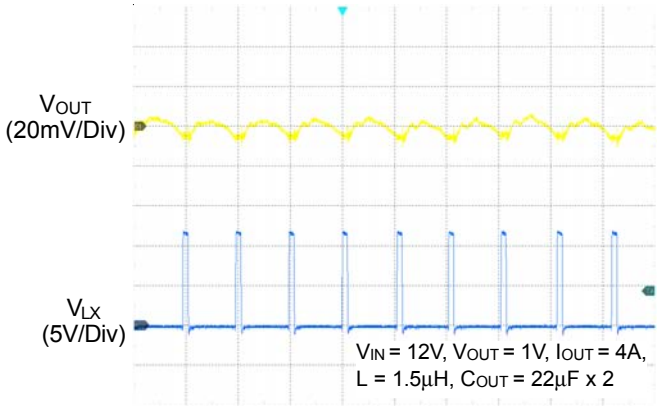
Output Voltage vs. Temperature



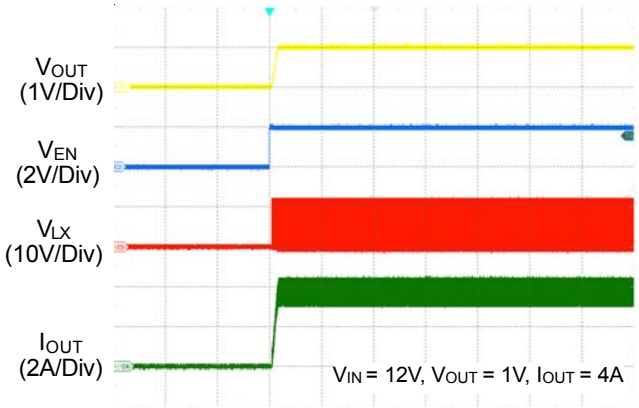
Load Transient Response



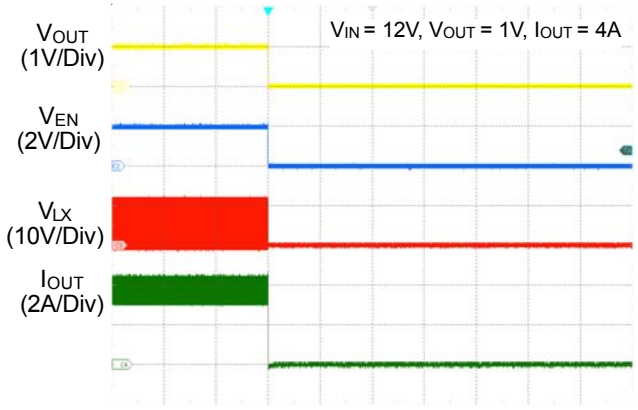
Output Ripple Voltage



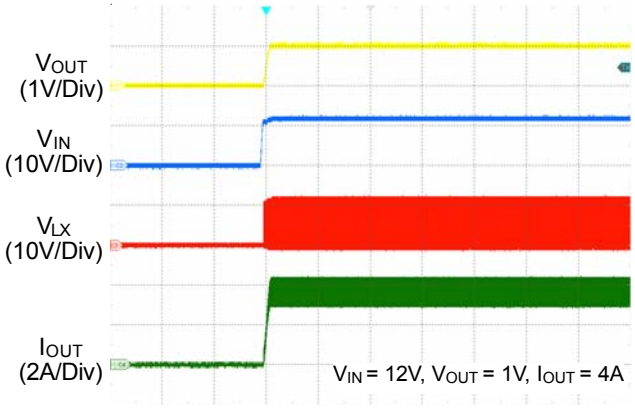
Power On from EN



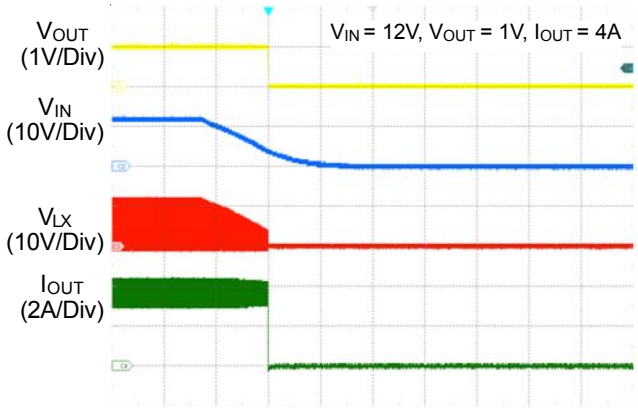
Power Off from EN



Power On from VIN



Power Off from VIN



Application Information

Inductor Selection

The consideration of inductor selection includes inductance, RMS current rating and, saturation current rating. The inductance selection is generally flexible and is optimized for the low cost, low physical size, and high system performance.

Choosing lower inductance to reduce physical size and cost, and it is useful to improve the transient response. However, it causes the higher inductor peak current and output ripple voltage to decrease system efficiency. Conversely, higher inductance increase system efficiency, but the physical size of inductor will become larger and transient response will be slow because more transient time is required to change current (up or down) by inductor. A good compromise between size, efficiency, and transient response is to set a inductor ripple current (ΔI_L) about 20% to 50% of the desired full output load current.

Calculate the approximate inductance by the input voltage, output voltage, switching frequency (f_{SW}), maximum rated output current ($I_{OUT(MAX)}$) and inductor ripple current (ΔI_L).

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current can be calculated.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2}\Delta I_L$$

$$I_{L(VALLY)} = I_{OUT(MAX)} - \frac{1}{2}\Delta I_L$$

The typical operating circuit design for the RT6254A/B, the output voltage is 1V, maximum rated output current is 4A, input voltage is 12V, and inductor ripple current is 1.2A which is 30% of the maximum rated output current, the calculated inductance value is :

$$L = \frac{1 \times (12-1)}{12 \times 500 \times 10^3 \times 1.2} = 1.527\mu H$$

The inductor ripple current set at 1.2A and so we select 1.5μH inductance. The actual inductor ripple current and required peak current is shown as below :

$$\Delta I_L = \frac{1 \times (12-1)}{12 \times 500 \times 10^3 \times 1.5 \times 10^{-6}} = 1.23A$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2}\Delta I_L = 4 + \frac{1.23}{2} = 4.615A$$

Inductor saturation current should be chosen over IC's valley current limit.

Input Capacitor Selection

The effective input capacitance is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), rated output current (I_{OUT}), switching frequency (f_{SW}), and input ripple voltage of the regulator (ΔV_{INP}) :

$$C_{IN(MIN)} = \frac{I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times \Delta V_{INP}}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. It should pay attention that value of capacitors change as temperature, bias voltage, and operating frequency change. For example the capacitance value of a capacitor decreases as the dc bias across the capacitor increases. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. Considering the DC bias effects for the input capacitor, the typical operating circuit used two 10μF low ESR ceramic capacitors on the VIN pin and an additional 0.1μF is recommended to place as close as possible to the IC input side for high frequency filtering.

Output Capacitor Selection

The RT6254A/B is optimized for output terminal with ceramic capacitors application and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output ripple voltage level and transient response requirements for sag which is undershoot on positive load steps and soar which is overshoot on negative load steps.

Output Ripple Voltage

Output ripple voltage at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple.

Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The typical operating circuit design for the RT6254A/B, the output voltage is 1V, inductor ripple current is 1.23A, and using 2 pieces of 22μF output capacitor with about 5mΩ ESR, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR} = 1.23A \times 5m\Omega = 6.15mV$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} = \frac{1.23A}{8 \times 44\mu F \times 500kHz} = 6.99mV$$

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} = 13.13mV$$

Output Transient Undershoot and Overshoot

In addition to output ripple voltage at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT™ transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 500kHz switching frequency.

But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Feed-Forward Capacitor (C_{FF})

The RT6254A/B is optimized for ceramic output capacitors and for low duty cycle applications. However for high-output voltages, with high feedback attenuation, the circuit's transient response can be slowed. In high-output voltage circuits transient response is improved by adding a small "feedforward" capacitor (C_{FF}) across the upper FB divider resistor (Figure 2), to speed up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value that following suggested component BOM.

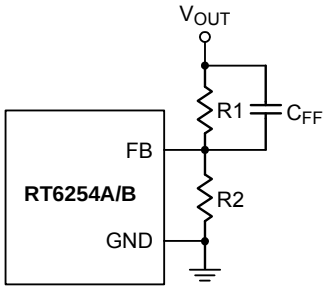


Figure 2. C_{FF} Capacitor Setting

Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to VIN, through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to VIN by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 3). Calculate the delay time using EN's internal threshold where switching operation begins.

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 4). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 5).

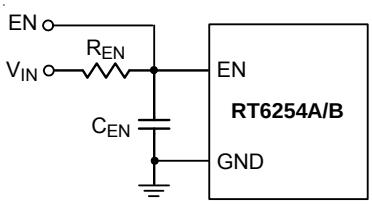


Figure 3. External Timing Control

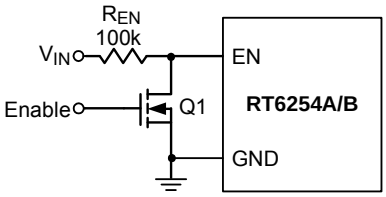


Figure 4. Digital Enable Control Circuit

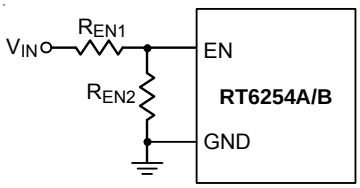


Figure 5. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT} = 0.6V \times (1 + \frac{R1}{R2})$$

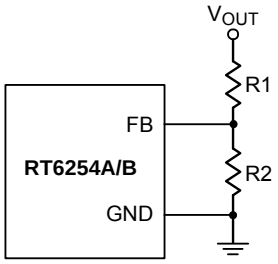


Figure 6. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{LX} rises rapidly. During switch turn-off, LX is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{LX}'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in Figure 7 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

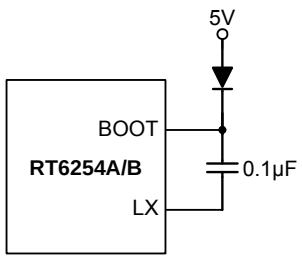


Figure 7. External Bootstrap Diode

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSOT-23-6 (FC) package, the thermal resistance, θ_{JA}, is 52°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 52°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for a TSOT-23-6 (FC) package.

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for a TSOT-23-8 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

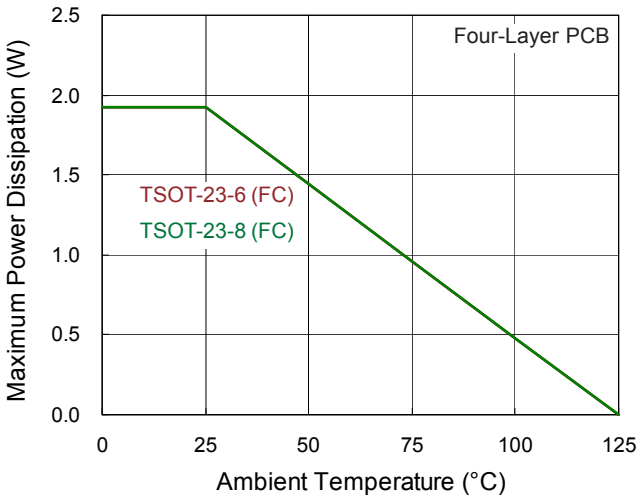


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to VIN pin.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the device.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.
- An example of the RT6254A/B PCB layout guide is shown in Figure 9 and Figure 10 for references.

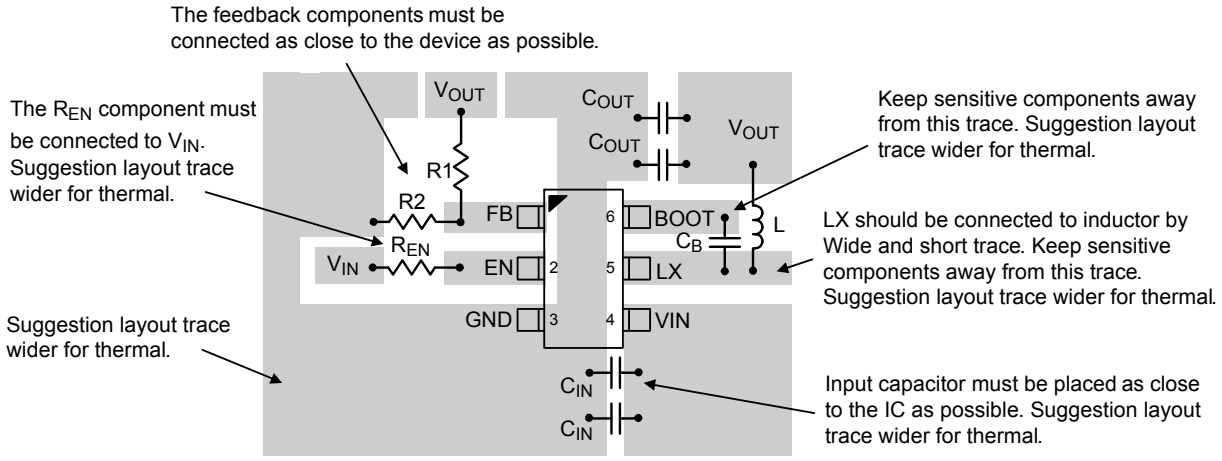


Figure 9. PCB Layout Guide for TSOT-23-6 package

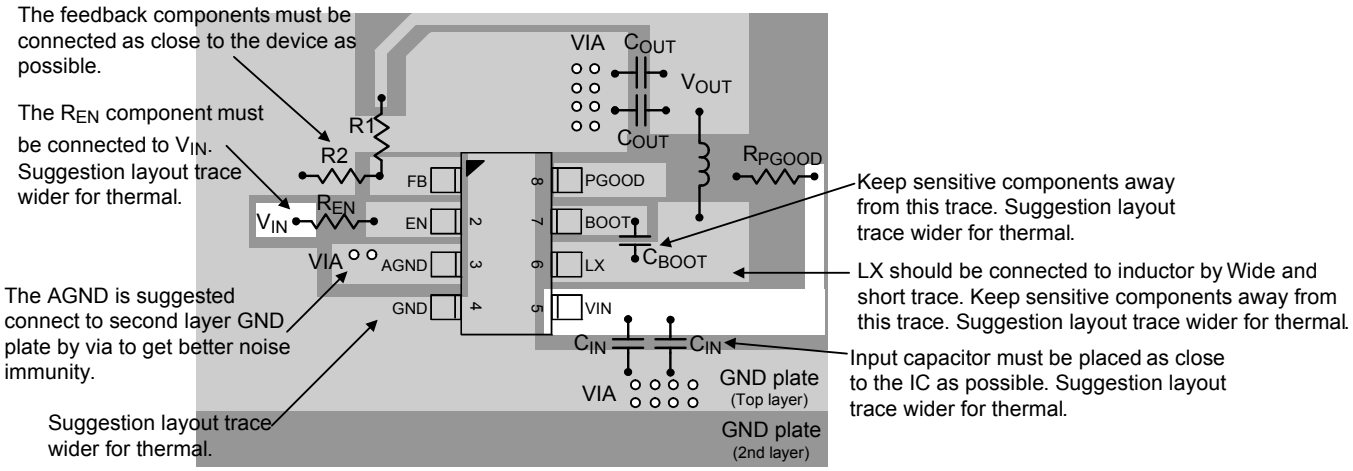
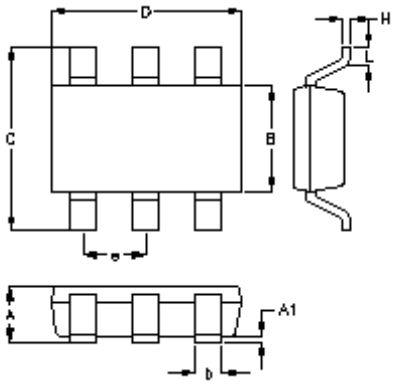


Figure 10. PCB Layout Guide for TOST-23-8 package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.950		0.037	
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-6 (FC) Surface Mount Package