17V Input, 3A, ACOT® Buck Converter with Both FETs OC Protection

General Description

The RT6263A/B is a simple, easy-to-use, 3A synchronous step-down DC-DC converter with an input supply voltage range of 4.5V to 17V. The device possesses an accurate reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency.

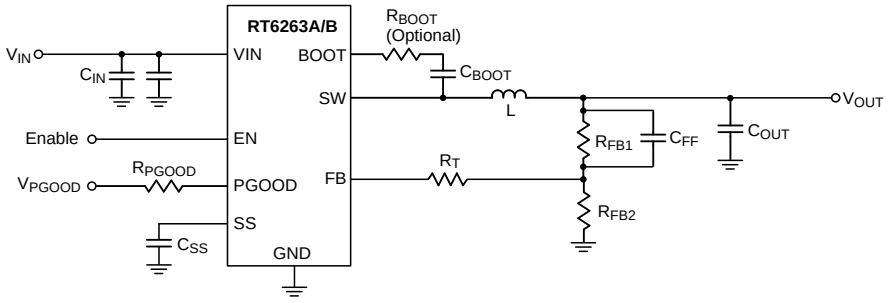
The RT6263A/B adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT6263A operates in automatic PSM that maintains high efficiency during light load operation. The RT6263B operates in Forced PWM that helps meet tight voltage regulation accuracy requirements.

The RT6263A/B senses both FETs current for a robust over-current protection (OCP). The device features cycle-by-cycle current limit protection to prevent the device from the catastrophic damage in output short circuit, over-current or inductor saturation conditions. The RT6263A/B offers programmable start-up by connecting a capacitor at external SS pin. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (OTP) to provide safe and smooth operation in all operating conditions.

Features

- **3A Converter Integrated 66mΩ and 36mΩ FETs**
- **Input Supply Voltage Range : 4.5V to 17V**
- **Output Voltage Range : 0.765V to 7V**
- **Advanced Constant On-Time (ACOT®) Control**
  - **Ultrafast Transient Response**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **High Accuracy Feedback Reference Voltage : Typ. ± 1%**
- **Optional for Operation Modes :**
  - **RT6263A : Power Saving Mode (PSM)**
  - **RT6263B : Forced PWM Mode**
- **Fixed Switching Frequency : 650kHz**
- **Enable Control and Externally Adjustable Soft-Start**
- **Input Under-Voltage Lockout (UVLO)**
- **Protection Function**
  - **Output Under-Voltage Protection (UVP) with Hiccup Mode**
  - **High- / Low-side MOSFET OCP and OTP Function**
- **Power Good Indication**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



Ordering Information

RT6263A/B □□□

- Package Type
  J8F : TSOT-23-8 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup
- PWM Operation Mode
  A : Automatic PSM
  B : Forced PWM

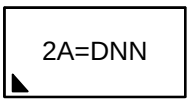
Note :

Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ Suitable for use in SnPb or Pb-free soldering processes.

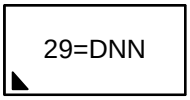
Marking Information

RT6263AHGJ8F



2A= : Product Code
DNN : Date Code

RT6263BHGJ8F



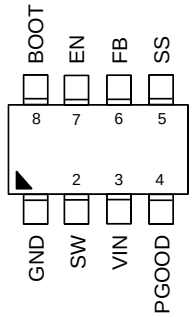
29= : Product Code
DNN : Date Code

Applications

- Set-Top Boxes
- LCD TVs
- Home Networking Devices
- Surveillance
- General Purpose

Pin Configuration

(TOP VIEW)

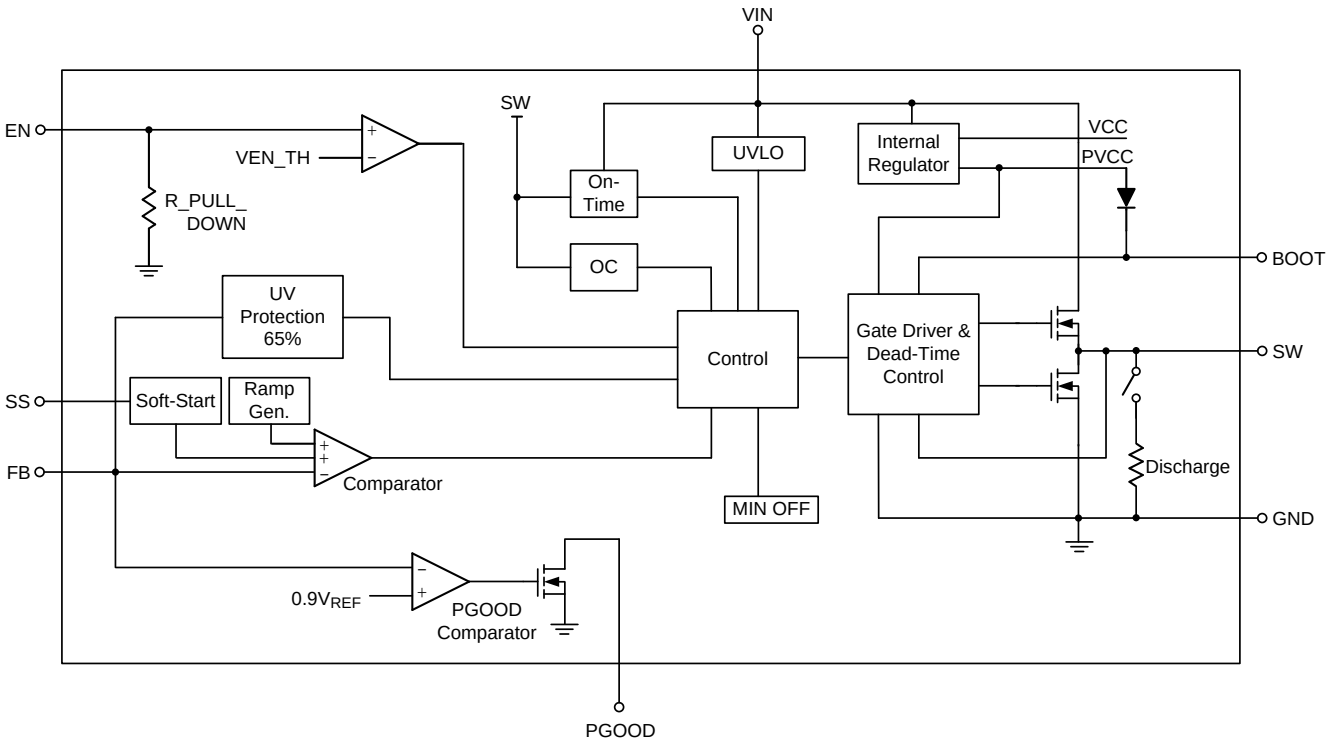


TSOT-23-8 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Power ground.
2	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor and bootstrap capacitor.
3	VIN	Power input. The input voltage range is from 4.5V to 17V. Connect input bypass capacitors directly to this pin and GND pins. The MLCC with capacitance higher than 20μF is recommended.
4	PGOOD	Open-drain output for power-good indication. This pin will be pulled low to GND if any internal protection is triggered during start-up interval.
5	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time. Do not leave this pin unconnected. A capacitor of 8.2nF is suggested.
6	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at feedback reference voltage.
7	EN	Enable control input. Connect this pin to logic high enables the device and connect this pin to GND disables the device.
8	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the SW pin.

Functional Block Diagram



Operation

The RT6263A/B is a high-efficiency, synchronous step-down DC-DC converter that can deliver up to 3A output current from a 4.5V to 17V input supply.

Advanced Constant On-Time Control and PWM Operation

The RT6263A/B adopts ACOT® control for its ultrafast transient response, low external component counts and stable with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (200ns, typ.) has timed out and the inductor current is below the current limit threshold, then the internal on-time one-shot circuitry is triggered and the high-side switch is turn-on. Since the minimum off-time is short, the device exhibits ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to input voltage and directly proportional to output voltage to achieve pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer expired, the high-side switch is turned off and the low-side switch is turned on until the on-time one-shot is triggered again. To achieve stable operation with low-ESR ceramic output capacitors, an internal ramp signal is added to the feedback reference voltage to simulate the output voltage ripple.

Power Saving Mode (RT6263A Only)

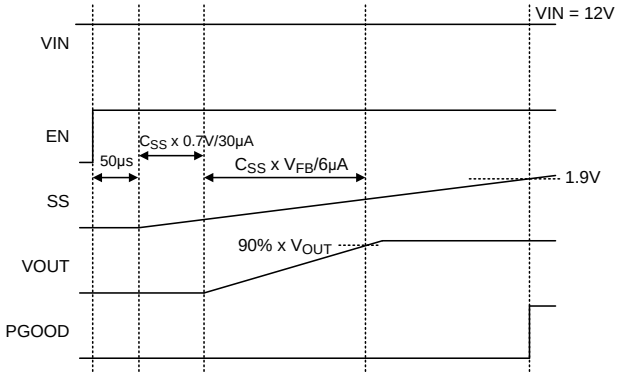
The RT6263A automatically enters power saving mode (PSM) at light load to maintain high efficiency. As the load current decreases, the inductor current ripple valley eventually touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. In this case, the output capacitor is only discharged by load current so that the switching frequency decreases. As the result, the light-load efficiency can be enhanced due to lower switching loss.

Enable Control

The RT6263A/B provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{EN_L}) of the enable input (EN), the converter will disable output voltage, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (10μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_H}) while the VIN voltage is higher than UVLO threshold, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. An internal resistor R_{EN_DN} from EN to GND allows EN float to shutdown the chip.

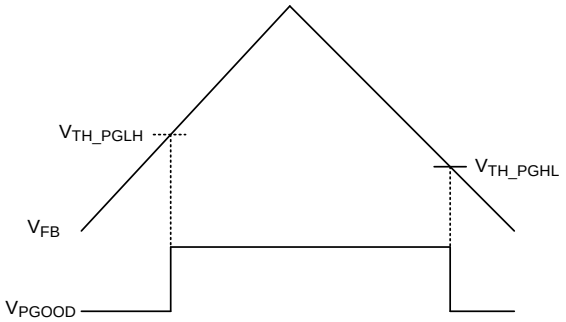
Soft-Start (SS)

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RT6263A/B provides an SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to GND. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 6μA) to generate a soft-start ramp voltage, and the internal reference voltage follows this slew rate. The out voltage can be built smoothly due to the method described above, so the SS pin should not be left unconnected to prevent overshoot voltage in soft-start interval. After the SS pin voltage rises above 1.9V (typically) and V_{FB} reaches 90% of reference voltage, the open-drain output of PGOOD will be high impedance to indicate power-good status. The typical start-up waveform shown below indicates the sequence and timing between the output voltage and related voltage.



Power Good Indication

The RT6263A/B features an open-drain output as power-good indication to monitor the output voltage status. The logic delay of comparator prevents false flag as a short excursion occurs, such as line and load transients. Tie PGOOD to VOUT or an external voltage which is below 5.5V. The power-good function is activated after soft-start is finished and controlled by a comparator connected to the feedback signal V_{FB}. After a certain delay time that V_{FB} reaches the power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PGOOD pin becomes high impedance to hold V_{PGOOD} logic high. On the contrary, the PGOOD pin is forced to logic-low while V_{FB} falls to the power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage). Furthermore, this pin is also forced to logic-low as any internal protection is triggered. The power good indication profile is shown below.



Input Under-Voltage Lockout

In addition to the EN pin, the RT6263A/B also provides enable control through the VIN pin. It features an under-voltage lockout (UVLO) function that monitors the internal linear regulator (VCC). If V_{EN} rises above V_{EN_H} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

Output Under-Voltage Protection and Hiccup Mode

The RT6263A/B possesses output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 65% of the internal feedback reference voltage), the UV comparator will go high to turn off both internal high-side and low-side MOSFET switches. If the output under-voltage condition continues for a period of time, the RT6263A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF},

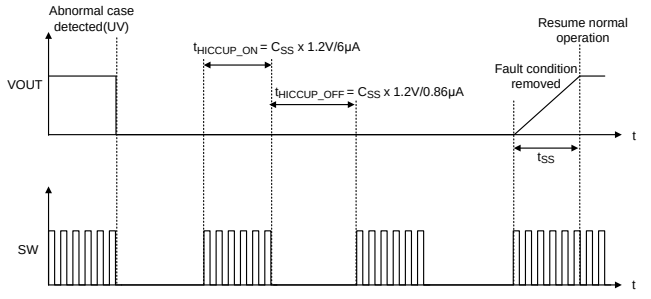
$t_{HICCUP\_OFF} = C_{SS}$ x 1.2V/0.86µA

, and then attempt to recover automatically for t_{HICCUP_ON},

$t_{HICCUP\_ON} = C_{SS}$ x 1.2V/6µA.

Upon completion of the soft-start sequence, the converter will resume normal operation if the fault condition is removed; otherwise, the RT6263A/B stays in auto-recovery until the fault condition is cleared.

The hiccup mode allows the circuit to operate safely while over-load or short-circuit condition occurs, and it makes converter resume normal operation rapidly once the fault condition is gone.



The Over-Current Protection

The RT6263A/B features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and prevents the device from the catastrophic damage in output short-circuit, over-current or inductor saturation conditions.

The high-side MOSFET over-current protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain amount of delay when the high-side switch being turned on each cycle. If an over-current condition occurs, the converter will immediately turns off the high-side switch and turns on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET over-current protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Negative Over-Current Limit

The RT6263B is the part which is forced to PWM and allows negative current operation.

In case of PWM operation, high negative current may be generated as an external power source which is tied to output terminal unexpectedly.

As the risk described above, the internal circuit monitors negative current in each on-time interval of low-side MOSFET and compares it with NOC threshold.

Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect low-side MOSFET. However, the negative current can't be limited at NOC threshold anymore since minimum off-time is reached.

Thermal Shutdown

The RT6263A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold (T_{SD}). Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair the reliability of the device or permanently damage the device.

Discharge

The RT6263A/B features the discharge function to release the output power the condition that EN pin goes low, UVP and OTP.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Enable Voltage, EN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to 20.3V
  <100ns ---------- –5V to 25V
- BOOT Voltage, BOOT ---------- –0.3V to 26V
- BOOT to SW, V_{BOOT} – V_{SW} ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 (FC) ---------- 1.6W

ESD Ratings

- ESD Susceptibility (Note 2)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 4.5V to 17V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		TSOT-23-8 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	86	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	108.2	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	62.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	11.21	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.64	°C/W

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	17	V
Under-Voltage Lockout Threshold	V_{UVLO}		3.7	4	4.3	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	400	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	3	10	µA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.8V	--	180	280	µA
Soft-Start						
Soft-Start Internal Charging Current	I_{SS}		--	6	--	µA
Enable Voltage						
Enable Voltage Threshold	V_{EN_H}	EN high-level input voltage	1.16	1.25	1.34	V
	V_{EN_L}	EN low-level input voltage	1.01	1.1	1.19	
EN Pin Pull-Down Resistance	R_{EN_DN}	EN pin resistance to GND, V_{EN} = 12V	225	450	900	kΩ
Feedback Voltage and Discharge Resistance						
Feedback Threshold Voltage	V_{FB}	V_{OUT} = 1.05V	758	765	772	mV
Feedback Input Current	I_{FB}	V_{FB} = 0.8V, T_A = 25°C	–0.1	0	0.1	µA
Discharge Resistance	R_{DISCHG}	V_{EN} = 0V, V_{SW} = 1V	--	100	200	Ω
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$	V_{BOOT} – V_{SW} = 4.8V	--	66	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	36	--	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}		--	5.6	--	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		3.3	4.2	--	
Low-Side Switch Negative Current Limit	I_{NOC}	Forced PWM mode only	--	2.5	--	A
Switching Frequency						
Switching Frequency	f_{SW}	V_{OUT} = 1.05V, PWM mode	--	650	--	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	60	--	ns
Minimum Off-Time	t_{OFF_MIN}	V_{FB} = 0.5V	--	200	260	ns
Output Under-Voltage Protections						
UVP Trip Threshold	V_{UVP}	Hiccup detect	--	65	--	%
Hiccup Power On-Time	t_{HICCUP_ON}	Relative to SS time	--	1	--	cycle

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hiccup Power Off-Time	t_{HICCUP_OFF}	Relative to SS time	--	7	--	cycles
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	155	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	35	--	
Power Good						
Power Good Threshold	V_{TH_PGLH}	V_{FB} rising, PGOOD from low to high	85	90	95	%
	V_{TH_PGHL}	V_{FB} rising, PGOOD from high to low	--	85	--	
Power Good Sink Current	I_{PGOOD}	V_{PGOOD} = 0.5V	0.5	1	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Typical Application Circuit

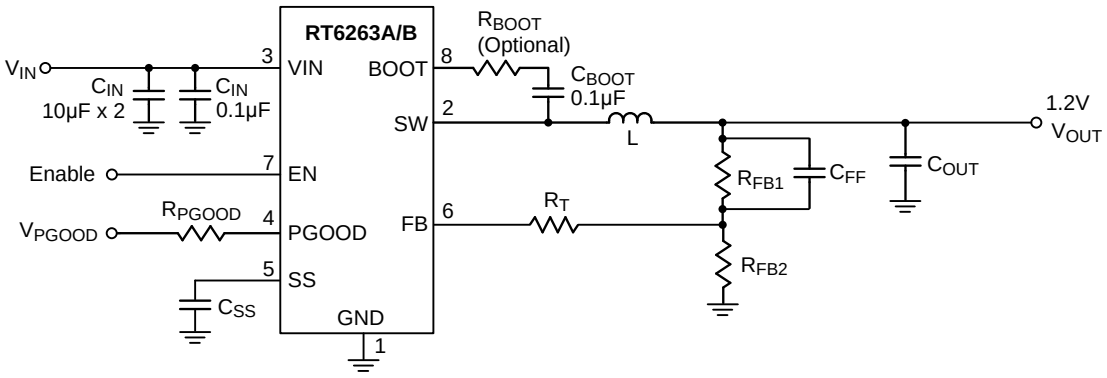


Table 1. Recommended Components Selection

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FF} (pF)	R_T (kΩ)	L (µH)	C_{OUT} (µF)
5.0	54.9	10	10 to 100	10	2.2 to 4.7	20 to 68
3.3	33.2	10	10 to 100	10	1.5 to 4.7	20 to 68
2.5	22.6	10	10 to 100	10	1.5 to 4.7	20 to 68
1.8	13.7	10	10 to 100	10	1.5 to 4.7	20 to 68
1.5	9.53	10	--	--	1.0 to 4.7	20 to 68
1.2	5.76	10	--	--	1.0 to 4.7	20 to 68
1.0	3.09	10	--	--	1.0 to 4.7	20 to 68

Table 2. Recommended External Components

Component	Description	Vendor P/N
C_{IN}	10µF, 25V, X5R, 0805	GRM21BR61E106MA73 (MURATA) 0805X106M250 (WALSIN)
C_{OUT}	22µF, 6.3V, X5R, 0603	GRM187R60J226ME15 (MURATA) 0603X226M6R3 (WALSIN)
L	2.2µH	74404054022 (WE) LQH5BPN2R2N38 (MURATA)
	4.7µH	74404054047 (WE) LQH5BPN4R7N38 (MURATA)

Note :

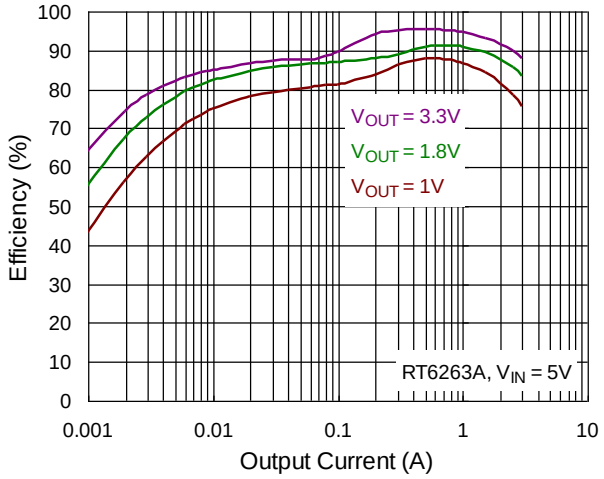
Considering effective capacitance de-rating which is related to biased voltage level and size, the effective capacitance of C_{OUT} should meet 18µF as 3.3V ≤ V_{OUT} ≤ 5V and 16µF as V_{OUT} < 3.3V.

The effect of higher C_{FF} value (>100pF) may not be obvious. Furthermore, it probably results in worse load regulation. Checking the load regulation is suggested if higher C_{FF} is applied.

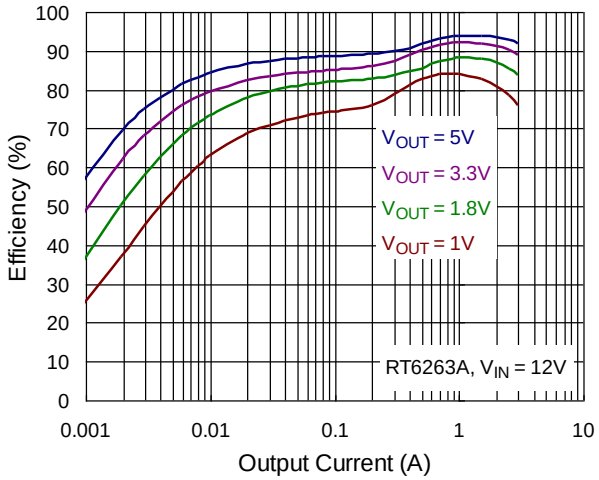
Typical Operating Characteristics

L: WE-74404054022 (DCR = 19mΩ) for VOUT = 1V and 1.8V.
L: WE-74404054047 (DCR = 30mΩ) for VOUT = 3.3V and 5V.

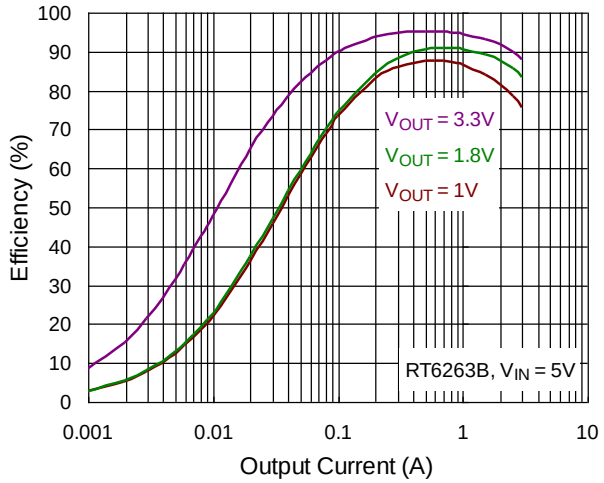
Efficiency vs. Output Current



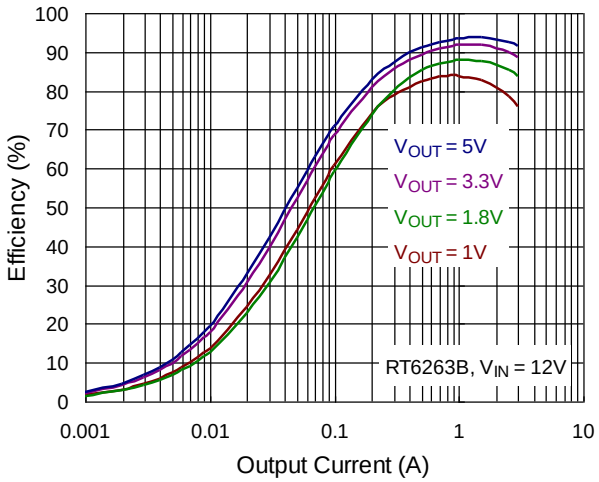
Efficiency vs. Output Current



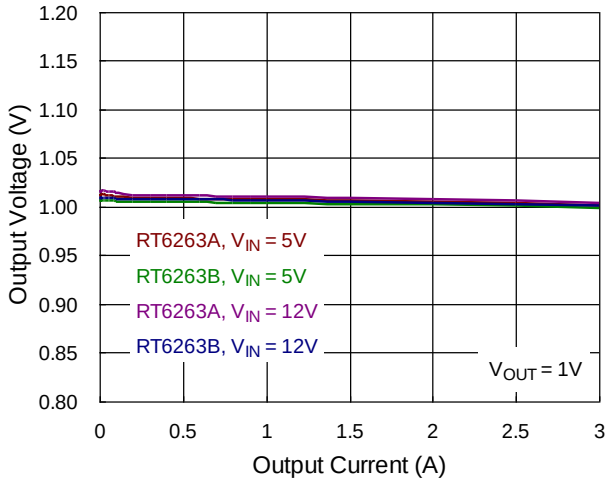
Efficiency vs. Output Current



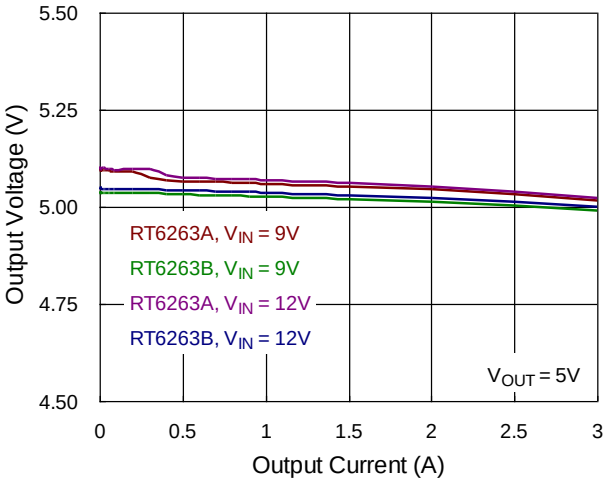
Efficiency vs. Output Current



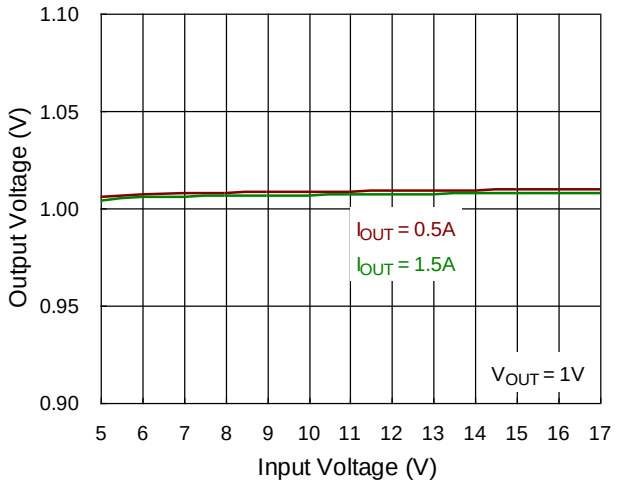
Output Voltage vs. Output Current



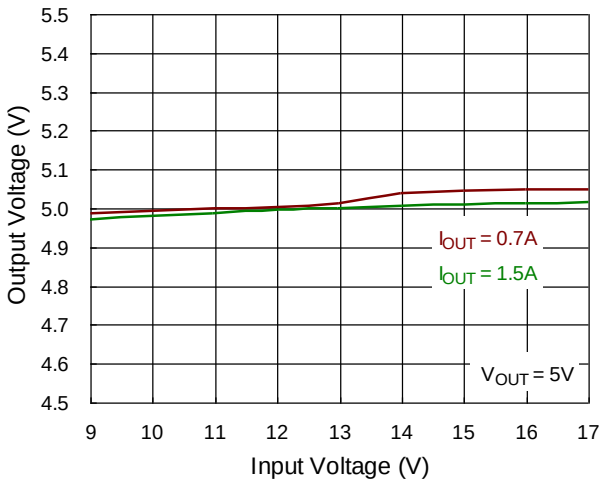
Output Voltage vs. Output Current



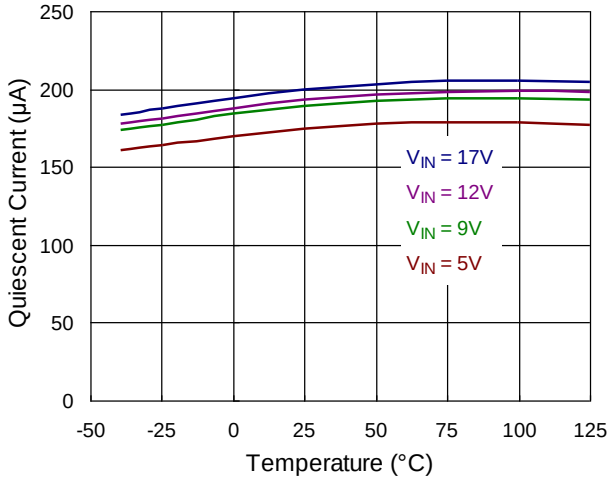
Output Voltage vs. Input Voltage



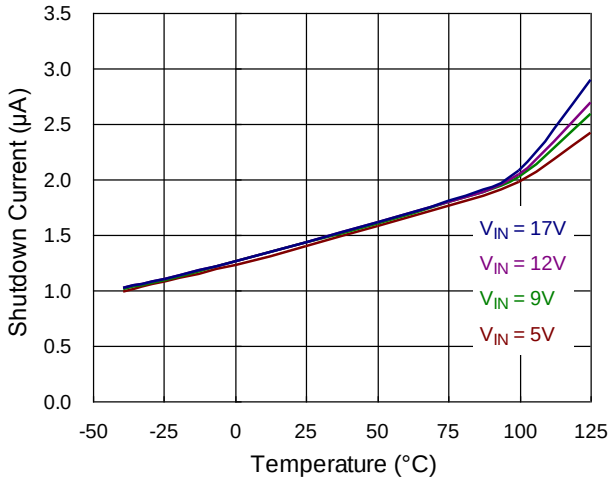
Output Voltage vs. Input Voltage



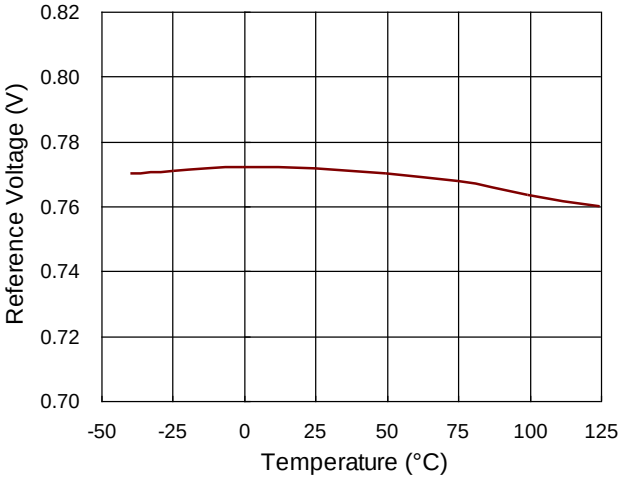
Quiescent Current vs. Temperature



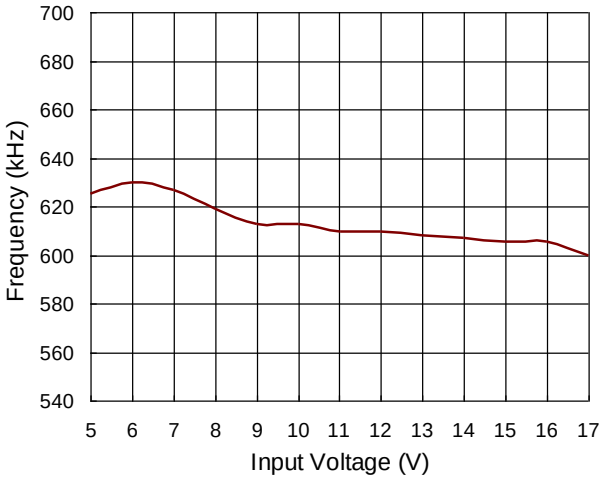
Shutdown Current vs.Temperature



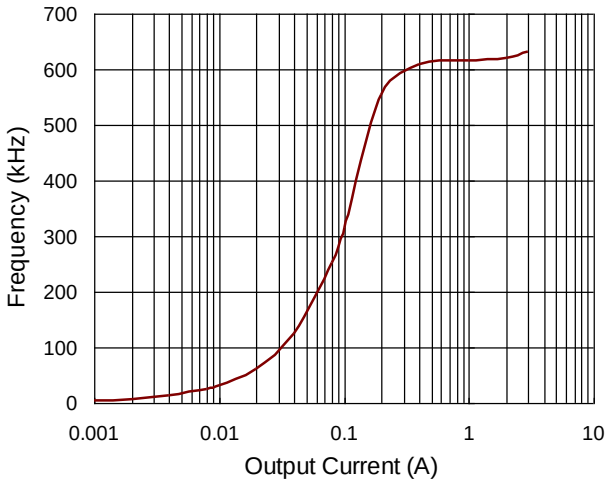
Reference Voltage vs.Temperature



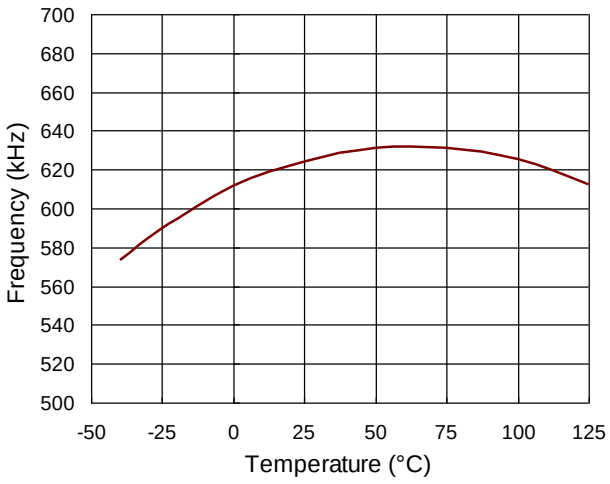
Frequency vs. Input Voltage



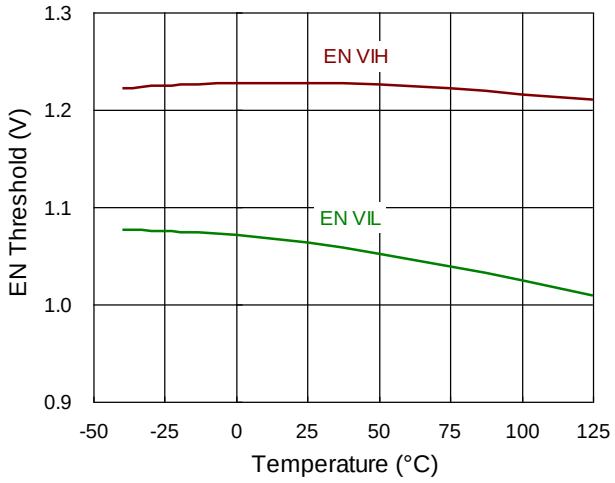
Frequency vs. Output Current



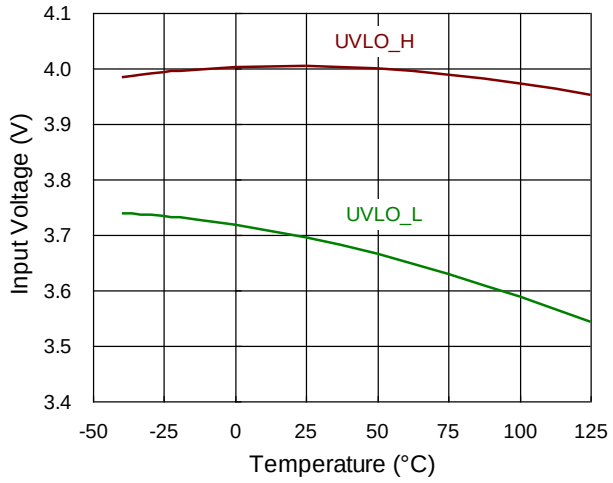
Frequency vs. Temperature



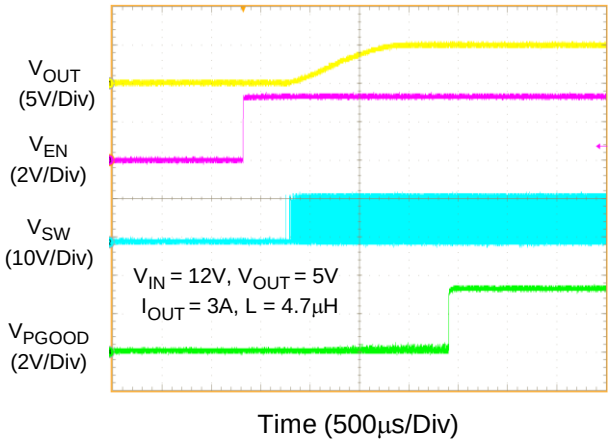
EN Threshold vs. Temperature



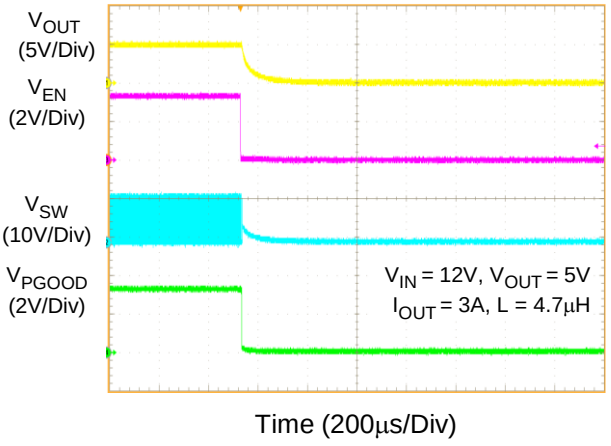
UVLO vs. Temperature



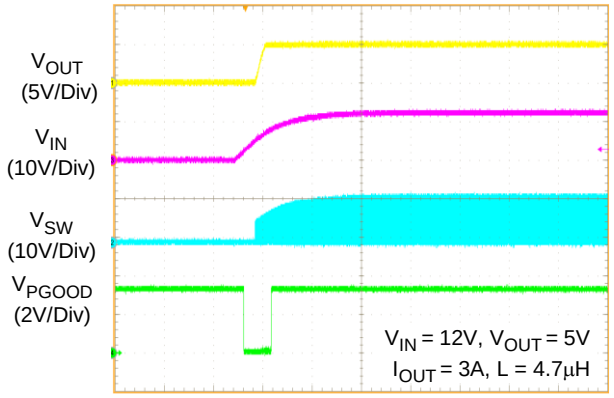
Power On from EN



Power Off from EN

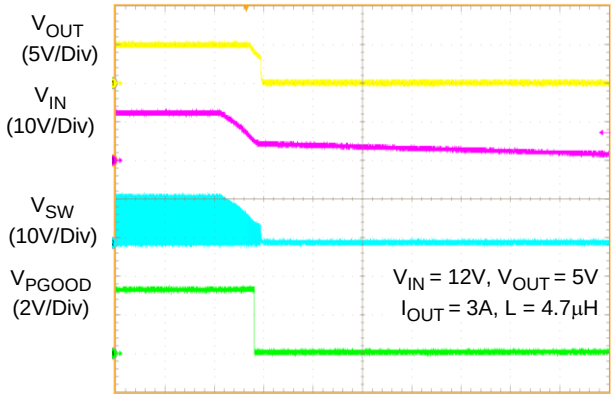


Power On from VIN



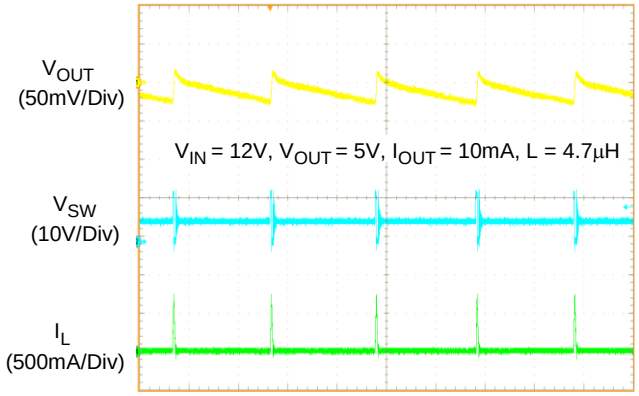
Time (5ms/Div)

Power Off from VIN



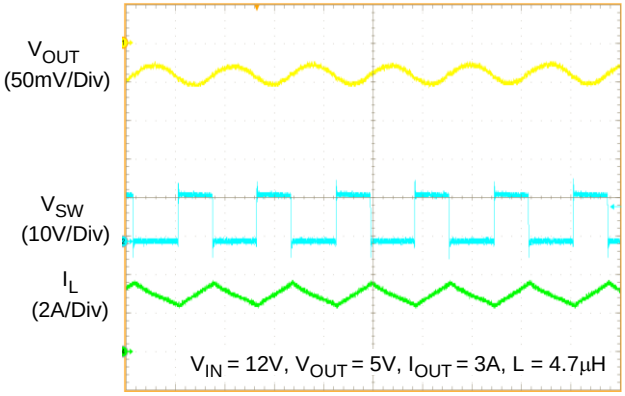
Time (5ms/Div)

Output Ripple as I_{OUT} = 10mA



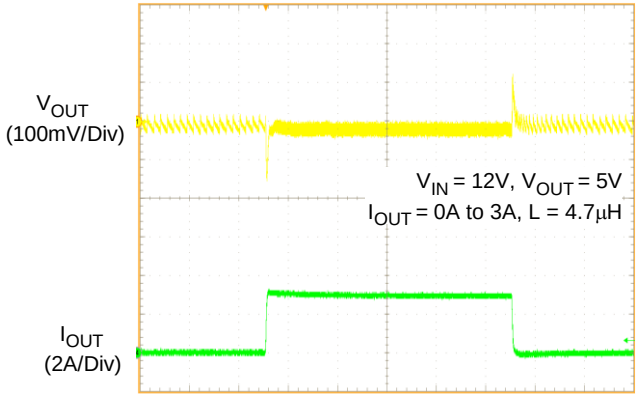
Time (20µs/Div)

Output Ripple as I_{OUT} = 3A



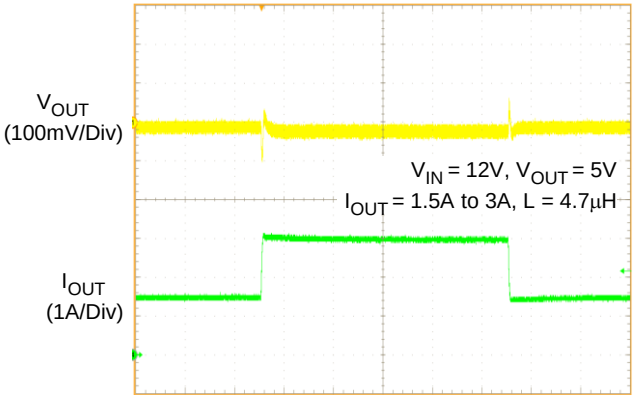
Time (1µs/Div)

Load Transient (No Load to Full Load)



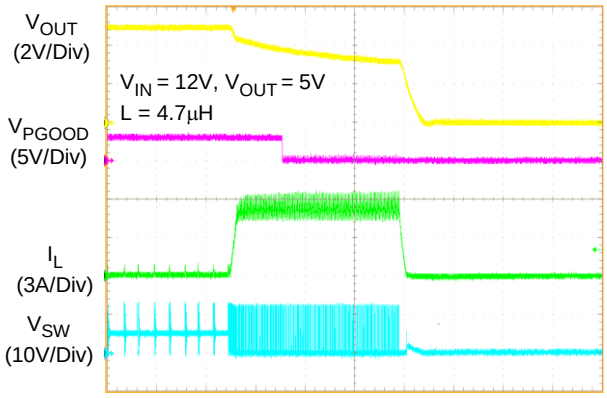
Time (200µs/Div)

Load Transient (Half Load to Full Load)



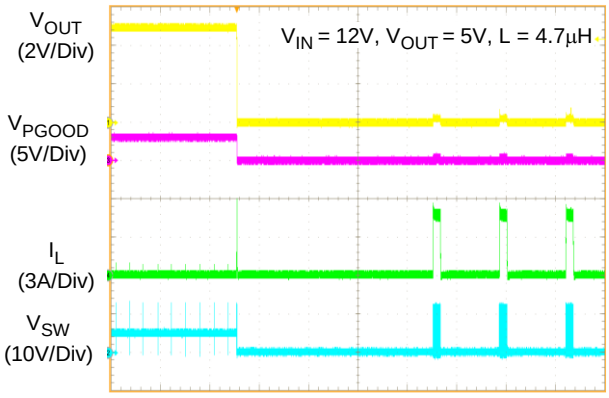
Time (200µs/Div)

Over-Current Protection and UVP



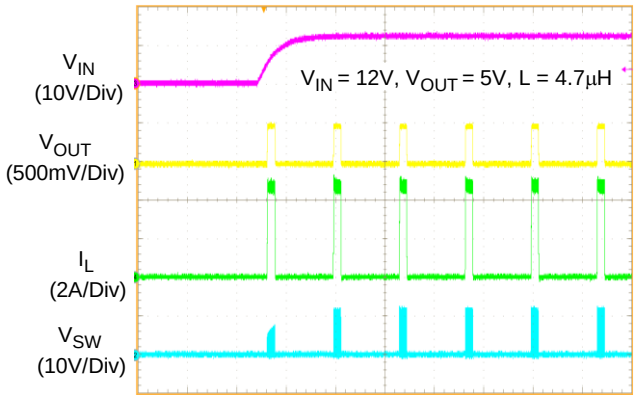
Time (50µs/Div)

Short Circuit Protection



Time (10ms/Div)

Short Circuit before Power On



Time (10ms/Div)

Application Information

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20%~50% of the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating which is equal to or greater than the switch current limit rather than the peak inductor current.

Considering the Typical Application Circuit for 1.2V output at 3A and an input voltage of 12V, using an inductor ripple of 1A (33% of the IC rated current), the calculated inductance value is :

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1A} = 1.66\mu H$$

For the typical application, a standard inductance value of 1.5μH can be selected.

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 650kHz \times 1.5\mu H} = 1.1A \text{ (37\% of the IC rated current)}$$

$$\text{and } I_{L(PEAK)} = 3A + \frac{1.1A}{2} = 3.55A$$

For the 1.5μH value, the inductor's saturation and thermal rating should exceed at least 3.55A. For more conservative, the rating for inductor saturation current must be equal to or greater than switch current limit of the device rather than the inductor peak current.

For EMI sensitive application, choosing shielding type inductor is preferred.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The waveform of C_{IN} ripple voltage and ripple current are shown in Figure 1. The peak-to-peak voltage ripple on input capacitor can be estimated as the equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \left(\frac{1 - D}{C_{IN} \times f_{SW}} \right) + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as the equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1 - D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where $\Delta V_{CIN\_MAX} \leq 200mV$

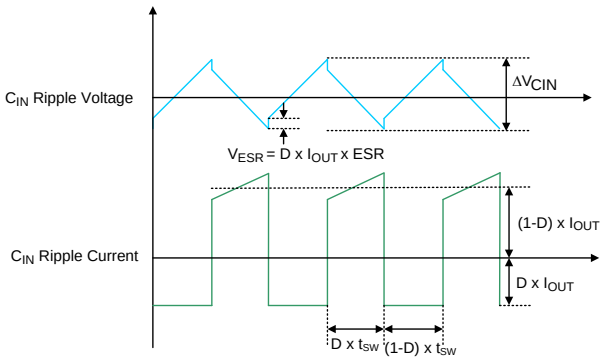


Figure 1. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is commonly to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of its small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT6263A/B circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1μF should be placed close to the VIN and GND pin. This capacitor should be 0402 or 0603 in size.

Output Capacitor Selection

The RT6263A/B are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance (C_{OUT}) and its equivalent series resistance (R_{ESR}) must be taken into consideration. The output peak-to-peak ripple voltage (V_{RIPPLE}) caused by the inductor current ripple (ΔI_L) is characterized by two components, which are ESR ripple ($V_{RIPPLE(ESR)}$) and capacitive ripple ($V_{RIPPLE(C)}$), and can be expressed as below :

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$
$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$
$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

As ceramic capacitors are used, both parameters should be estimated due to the extremely low ESR and relatively small capacitance. Refer to the RT6263A/B's typical application circuit of 1.2V application, the actual inductor current ripple (ΔI_L) is 1.1A, and the output capacitor is 22μF (Murata ceramic capacitor: GRM219R60J226ME47), V_{RIPPLE} can be obtained as below.

The ripple caused by ESR (2mΩ) can be calculated as :

$$V_{RIPPLE(ESR)} = 1.1A \times 2m\Omega = 2.2mV$$

Considering the capacitance derating, the effective capacitance is approximately 18μF as the output voltage is 1.2V, and another parameter is :

$$V_{RIPPLE(C)} = \frac{1.1A}{8 \times 2 \times 18\mu F \times 650kHz} = 5.9mV$$
$$V_{RIPPLE} = 2.2mV + 5.9mV = 8.1mV$$

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

Both undershoot voltage and overshoot voltage consist of two factors : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The real on-time will slightly extend due to the voltage drop which is related to output current; however, this on-time compensation can be neglected. Besides, the minimum on-time is 60ns, typ. If the calculated on-time is smaller than minimum on-time, it and V_{OUT} will both be clamped. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Because some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR should be taken into consideration while calculating the V_{SAG} & V_{SOAR}.

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$V_{OUT} = 0.765V \times (1 + R_{FB1} / R_{FB2})$

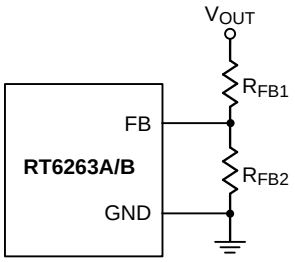


Figure 2. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R_{FB2} between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R_{FB1} as follows :

$$R_{FB1} = \frac{R_{FB2} \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

Feed-forward Capacitor Selection (C_{FF})

The RT6263A/B is optimized for low duty-cycle applications and the control loop is stable with low ESR ceramic output capacitors. In higher duty-cycle applications (higher output voltages or lower input voltages), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become slower and under-damped. This situation will result in ringing

waveform at output terminal. In case of high output voltage application, the phenomenon described above is more visible because of large attenuation in feedback network. As shown in Figure 3, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

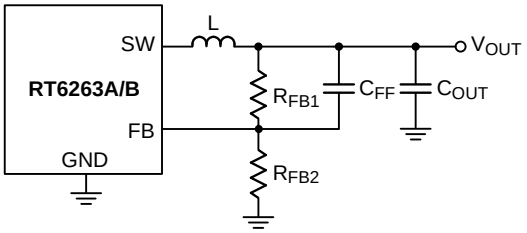


Figure 3. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For ACOT®, loop bandwidth can be in the order of 100 ~ 200kHz, so a load step with 500ns maximum rising time (dI/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current limit threshold. A load transient from 30% to 60% of maximum load is reasonable which is shown in Figure 4.

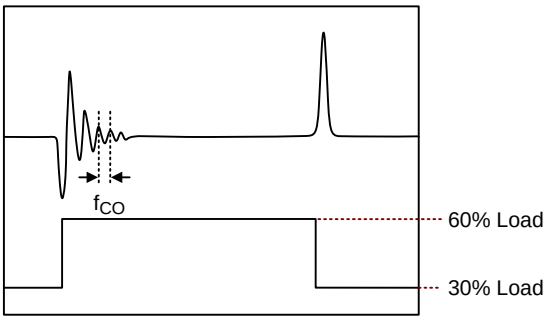


Figure 4. Example of Measuring the Converter BW by Fast Load Transient

C_{FF} can be calculated basing on below equation :

$$C_{FF} = \frac{1}{2\pi \times BW} \sqrt{\frac{1}{R_{FB1}} \times \left(\frac{1}{R_{FB1}} + \frac{1}{R_{FB2}} \right)}$$

Figure 5. shows the transient performance with and without feedfoward capacitor.

Note that, after defining the C_{FF} please also check the load regulation, because feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over spec caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF} or place a series resistor of R_T to FB pin.

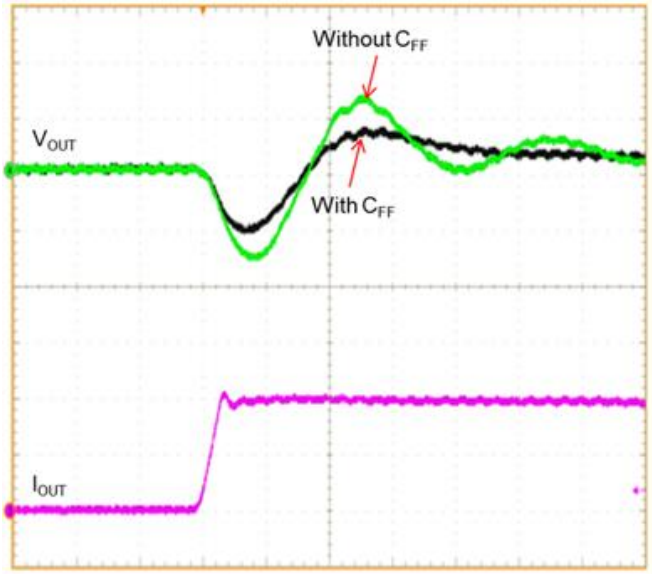


Figure 5. Load Transient Response with and without Feedforward Capacitor

Enable Operation

The RT6263A/B is enabled when the VIN pin voltage rises above V_{UVLO} while the EN pin voltage exceeds V_{EN_H}. The RT6263A/B is disabled when the VIN pin voltage falls below $V_{UVLO} - \Delta V_{UVLO}$ or when the EN pin voltage is below V_{EN_L}. An internal pull-down resistor R_{EN_DN}, which is connected form EN to GND, ensures that the chip still stays in shutdown even if EN pin is floated.

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN} directly as shown in Figure 6.

The built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor REN and a capacitor C_{EN}, as shown in Figure 7, to have an additional delay. The time delay can be calculated by the equation below with the EN's internal threshold, at which switching operation begins.

$$C_{EN} = \frac{t}{R_{th} \times \ln \frac{V_{th}}{V_{th} - V_{EN\_H}}}$$

, where

$R_{th} = R_{EN} // R_{EN\_DN}$

$$V_{th} = V_{IN} \times \frac{R_{EN\_DN}}{R_{EN\_DN} + R_{EN}}$$

An external MOSFET can be used for logic control which is shown in Figure 8. In this case, R_{EN} is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin.

If the device is desired to be shut down by EN pin before V_{IN} falls below the UVLO threshold, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold as shown in Figure 9. For a given R_{EN1}, R_{EN2} can be found by the equation below for the desired V_{IN} stop voltage.

$$V_{IN\_STOP} \times \frac{R_{EN2} // R_{EN\_DN}}{R_{EN1} + R_{EN2} // R_{EN\_DN}} < V_{EN\_L}$$

After R_{EN1} and R_{EN2} are defined, the input voltage V_{IN_START} is obtained from

$$V_{EN\_H} \times \frac{R_{EN1} + R_{EN2} // R_{EN\_DN}}{R_{EN2} // R_{EN\_DN}} = V_{IN\_START}$$

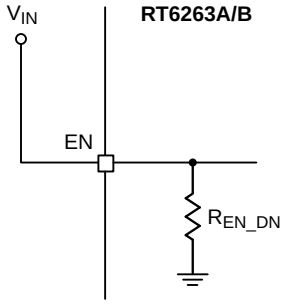


Figure 6. Automatic Start-Up Setting

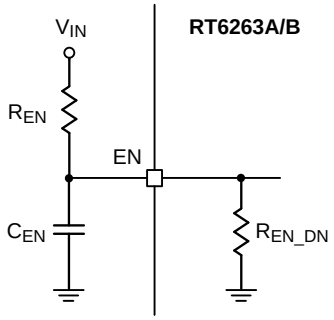


Figure 7. External Timing Control

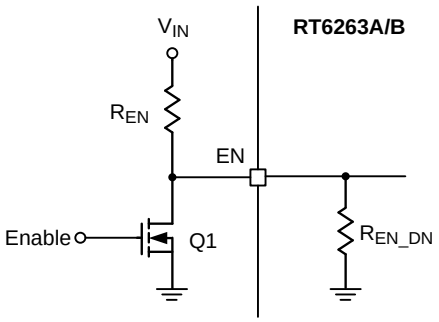


Figure 8. Digital Enable Control Circuit

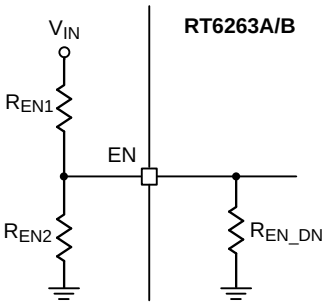


Figure 9. Resistor Divider for Lockout Threshold Setting

If V_{IN} shuts down faster than V_{OUT} and V_{OUT} is larger than 3.7V, buck converter becomes boost converter and generates negative current. To prevent these condition, EN should be shut down before V_{IN} falls below V_{OUT}. Therefore, the resistor divider for lockout threshold is recommended.

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately PVCC each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1μF, 0603 or 0402 ceramic capacitor is recommended and the capacitor should have a 6.3 V or higher voltage rating.

External Bootstrap Diode (Optional)

A bootstrap capacitor of 0.1μF low-ESR ceramic capacitor is connected between the BOOT and SW pins to supply the high-side gate driver. It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT

pin as shown in Figure 10 to improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6263A/B. Note that the BOOT voltage V_{BOOT} must be lower than 5.5V.

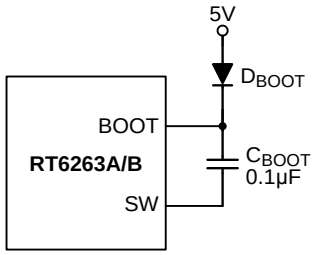


Figure 10. External Bootstrap Diode

External Bootstrap Resistor (Optional)

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch. The gate driver is not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to the induced high di/dt noises. When the high-side switch is turned off, the discharging time on SW node is relatively slow because there's the presence of dead time, both high-side and low-side MOSFETs are turned off in this interval. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor as shown in Figure 11. The recommended range for the R_{BOOT} is several ohms to 47 ohms, and it could be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal MOSFET switch, the recommended application circuit is shown in Figure 12, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection.

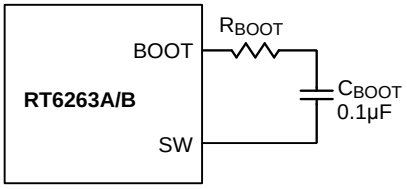


Figure 11. External Bootstrap Resistor at the BOOT Pin

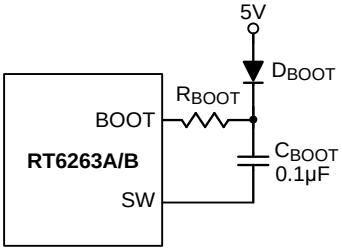


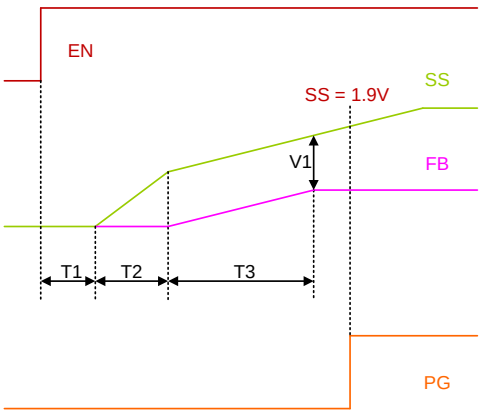
Figure 12. External Bootstrap Diode and Resistor at the BOOT Pin

Soft-Start

The RT6263A/B provides adjustable soft-start function. When the EN pin becomes logic-high, the SS charge current (I_{SS}) begins to charge the capacitor which is connected from the SS pin to GND (C_{SS}).The soft-start function is used to prevent large inrush current while the converter is in power-up stage The soft-start time can be programmed by the external capacitor C_{SS} between SS and GND. An internal current source I_{SS} (6µA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is calculated as below :

$$t_{SS} = C_{SS} \times 0.7V/30\mu A + C_{SS} \times V_{FB}/I_{SS}$$

, where t_{SS} = SS rises to FB settled point (T2 + T3)



T1 : EN delay, from EN go high to SS start rising, T1 = 50μs;
T2 : speed up SS, from SS rising to FB start rising, T2 = C_{SS} x 0.7/30μA;
T3 : normal SS, from FB rising to settled, T3 = C_{SS} x V_{FB}/I_{SS};
V1 : offset voltage between SS and FB, V1 = 700mV;
PG go high after SSOK (SS = 1.9V)

Figure 13. Operation of SS Pin when Starting

Power Good

The PGOOD pin is an open-drain output for power-good indication and should be connected to an external voltage source through a pull-up resistor. The voltage source can be an external voltage supply or the output of the RT6263A/B, and it must be lower than 5.5V to avoid the damage risk on this pin. It is recommended to connect a 100kΩ between the external voltage source and PGOOD pin.

The power-good function is activated after soft-start is completed and controlled by the feedback signal V_{FB}. During soft-start, this pin stays in logic-low, and it's only allowed to transfer to logic-high as soft-start cycle is done. After a certain delay time that V_{FB} reaches the power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PGOOD pin becomes high impedance to hold V_{PGOOD} logic high. On the contrary, the PGOOD pin is forced to logic-low while V_{FB} falls to the power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage). Furthermore, this pin is also forced to logic-low as any internal protection is triggered.

Thermal Consideration

In many applications, the RT6263A/B does not generate much heat due to its high efficiency and low thermal resistance of its TSOT-23-8(FC) package. However, in applications in which the RT6263A/B runs at a high ambient temperature and high input voltage, the generated heat may exceed the maximum junction temperature of the part.

The 6263A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. If the junction temperature reaches approximately 155°C, the RT6263A/B stops switching the power MOSFETs until the temperature is cooled down by 35°C.

Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

, where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 125°C. TA is the ambient operating temperature, and $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

As an example, considering the case when the RT6263A is used in application where V_{IN} = 12V, I_{OUT} = 3A, f_{SW} = 650kHz, V_{OUT} = 3.3V. The efficiency at 3.3V, 3A is 85.9% by using WE-74404054047 (4.7μH, 30mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website and it's 102mW. In this case, the power dissipation of the RT6263A is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.25W$$

Considering the system-level $\theta_{JA(EFFECTIVE)}$ is 68.7°C/W (other heat sources are also considered), the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 1.25W \times 68.7°C/W + 25°C = 110.9°C$$

Figure 14 shows the RT6263A/B $R_{DS(ON)}$ versus different junction temperatures. If the application requires a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature of the device need to recalculated based on a higher $R_{DS(ON)}$ since it increases with temperature.

Using 35°C ambient temperature as an example. Due to the variation of junction temperature is dominated by the ambient temperature, the T'_J at 35°C ambient temperature can be pre-estimated as

$$T'_J = 110.9°C + (35°C - 25°C) = 120.9°C$$

According to Figure 14, the increasing $R_{DS(ON)}$ can be found as

$$\Delta R_{DS(ON)\_H} = 90.5m\Omega \text{ (at } 120.9°C) - 88m\Omega \text{ } (110.9°C) = 2.5m\Omega$$

$$\Delta R_{DS(ON)\_L} = 44.7m\Omega \text{ } (\text{at } 120.9°C) - 43.7m\Omega \text{ } (110.9°C) = 1m\Omega$$

The external power dissipation caused by the increasing $R_{DS(ON)}$ at higher temperature can be calculated as

$$\Delta P_{D,RDS(ON)} = (3A)^2 \times \frac{3.3}{12} \times 2.5m\Omega + (3A)^2 \times \left(1 - \frac{3.3}{12}\right) \times 1m\Omega = 0.013W$$

As a result, the new power dissipation is 1.263W due to the variation of $R_{DS(ON)}$. Therefore, the estimated new junction temperature is

$$T'_J = 1.263W \times 68.7°C/W + 35°C = 121.77°C$$

If the application requires a higher ambient temperature and may exceed the recommended maximum junction temperature of 125°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

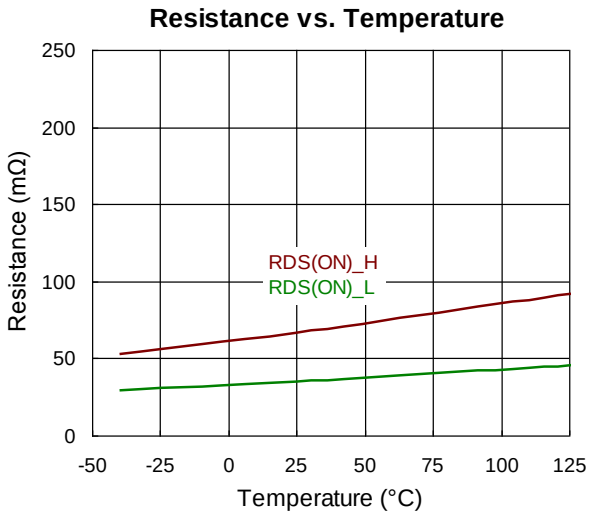


Figure 14. RT6263A/B $R_{DS(ON)}$ vs. Temperature

Layout Considerations

Follow the PCB layout guidelines below for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable and jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT6263A/B.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

An example of PCB layout guide is shown in Figure 15.

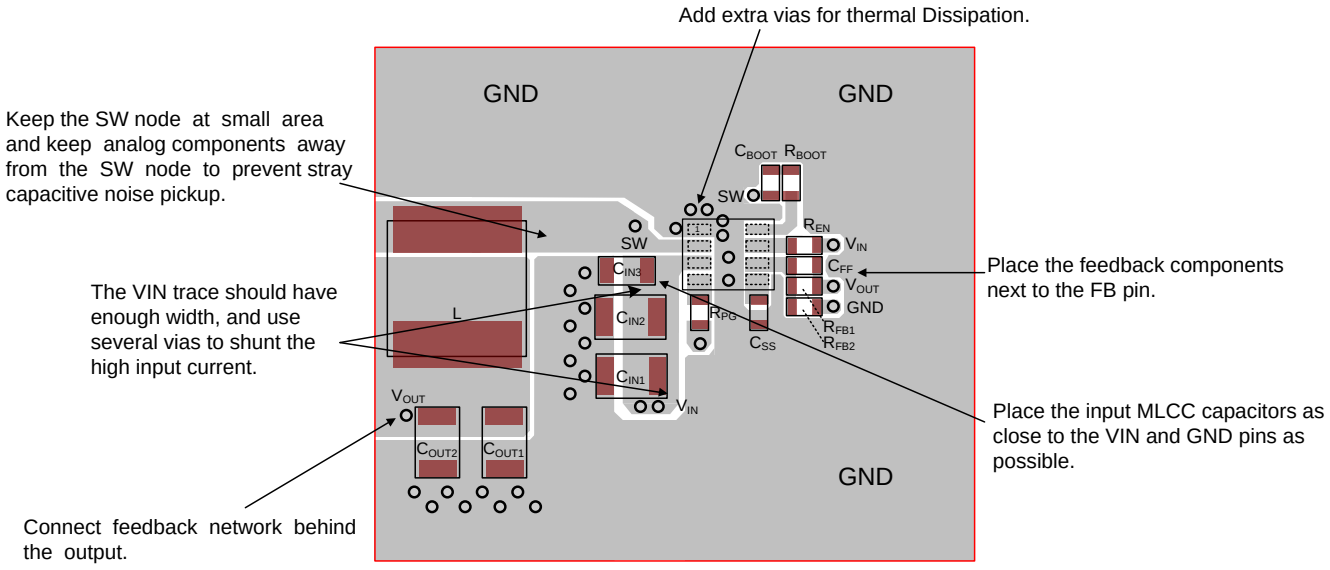
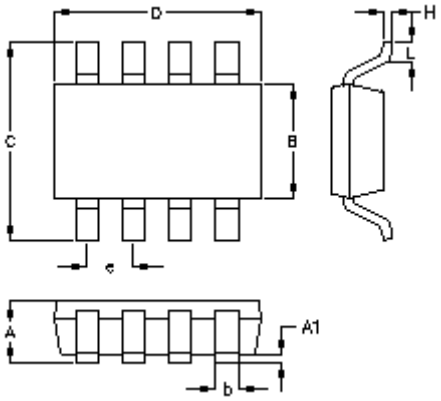


Figure 15. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package