3A, 17V Current Mode Synchronous Step-Down Converter

General Description

The RT7296F is a high-efficiency, 3A current mode synchronous step-down DC-DC converter with a wide input voltage range from 4.5V to 17V. The device integrates 80mΩ high-side and 30mΩ low-side MOSFETs to achieve high efficiency conversion. The current mode control architecture supports fast transient response and internal compensation. The RT7296F provides power good pin to be an output voltage ready indicator. A cycle-by-cycle current limit function provides protection against shorted output. The RT7296F provides complete protection functions such as input under-voltage lockout, output under-voltage protection, over-current protection, and thermal shutdown. The PWM frequency is adjustable by the EN/SYNC pin. The RT7296F is available in the TSOT-23-8 (FC) package.

Ordering Information

RT7296F □□

- Package Type
  J8F : TSOT-23-8 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **4.5V to 17V Input Voltage Range**
- **3A Output Current**
- **Internal N-Channel MOSFETs**
- **Current Mode Control**
- **Fixed Switching Frequency : 500kHz**
- **Synchronous to External Clock : 200kHz to 2MHz**
- **Cycle-by-Cycle Current Limit**
- **Internal Soft-Start Function**
- **Power Saving Mode at Light Load**
- **Power Good Indicator**
- **Input Under-Voltage Lockout**
- **Output Under-Voltage Protection**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

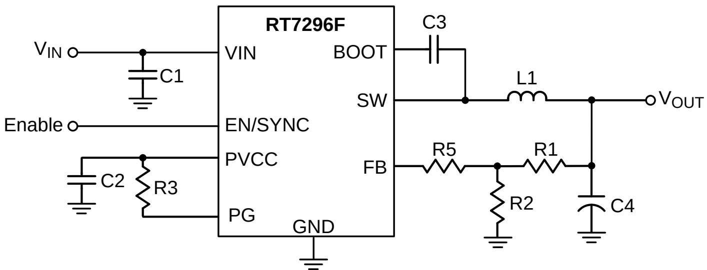
- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Set-top Boxes

Marking Information

08=DNN

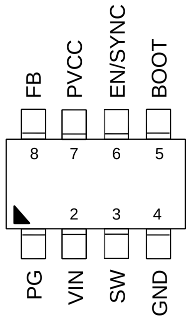
08= : Product Code
DNN : Date Code

Simplified Application Circuit



Pin Configuration

(TOP VIEW)

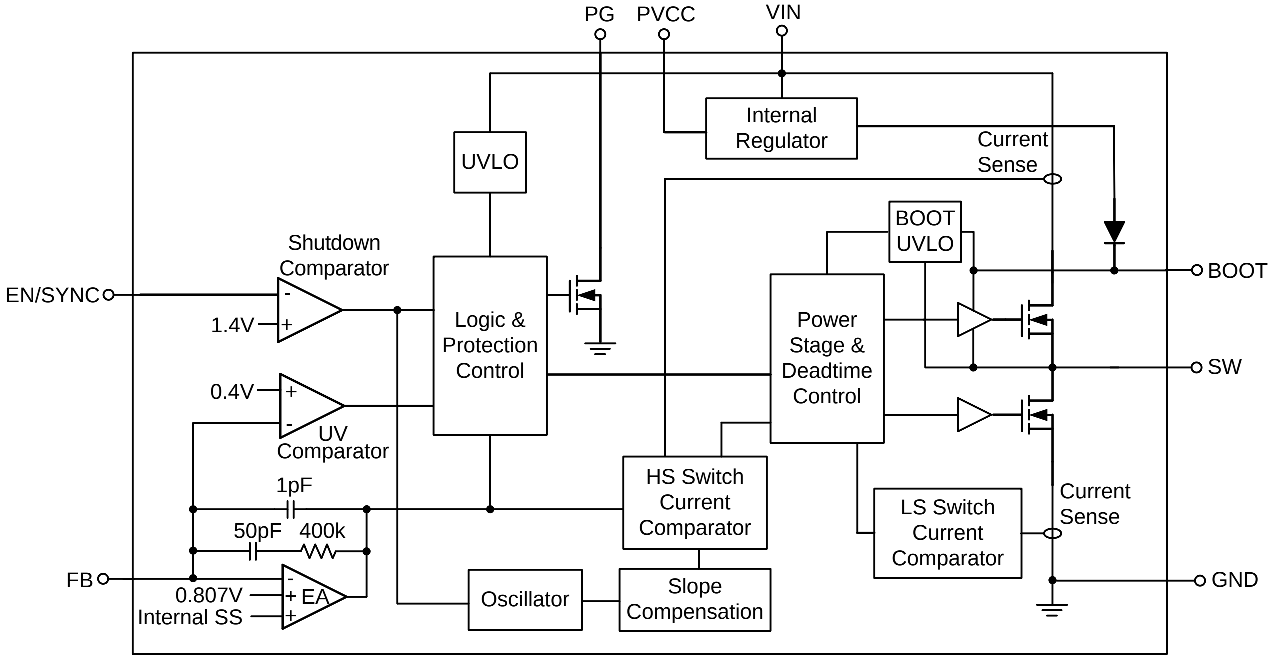


TSOT-23-8 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PG	Power good output. This pin is an open drain which can be connected to PVCC by a resistor. If output voltage achieve 90% of the normal voltage, the PG pin will go high after 400μs delay.
2	VIN	Power input. Support 4.5V to17V Input Voltage. Must bypass with a ceramic capacitor at this pin.
3	SW	Switch node. Connect to external L-C filter.
4	GND	System ground.
5	BOOT	Bootstrap supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between the BOOT and SW pins.
6	EN/SYNC	Enable control input. High = Enable. Apply an external clock to adjust the switching frequency. If using pull high resistor connected to VIN, the recommended value range is 60kΩ to 300kΩ.
7	PVCC	5V Bias supply output. Connect a minimum of 0.1μF capacitor to ground.
8	FB	Feedback voltage input. The pin is used to set the output voltage of the converter to regulate to the desired voltage via a resistive divider. Feedback reference = 0.807V.

Functional Block Diagram



Operation

Power Saving Mode

The RT7296F automatically enters into power saving mode (PSM) at light load to improve efficiency. In PSM, the RT7296F disable the internal CLK when V_{FB} is above the V_{REF} x 1.005 (typ.). In other words, the device automatically skip the PWM pulse at light load. While V_{FB} falls below the V_{REF} x 1.005, the RT7296F enables the internal CLK again and hence the new switching cycle is activated. When the internal switches are activated, for each cycle the device detects the peak inductor current (I_{L_PEAK}) and keeps high-side switch on until the I_L reaches its minimum peak current level (as shown in Figure 1). When low-side switch is turn-on, the zero-current detection is also activated to prevent that I_L becomes negative and enables the higher efficiency at light load. During the period that both switches are off, the device turns off the most of the internal circuit to reduce the quiescent power consumption further.

With lower output loading, the non-switching period is longer, so the effective switching frequency becomes lower to reduce the switching loss and switch driving loss.

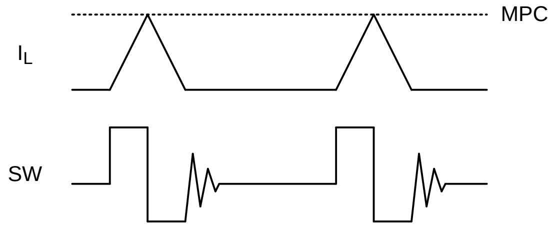


Figure 1. Minimum Peak Current at PSM

Power Good Indication

The RT7296F features an open-drain power-good output (PG) to monitor the output voltage status. Connect PG to PVCC or an external voltage below 5.5V with a resistor. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (PG_{vth_Hi}, typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high after a certain delay elapsed (typically, 400μs). When V_{FB} fall short of power good low threshold (PG_{vth_Lo}, typically 85% of the reference voltage), the PG pin will be pulled low.

Under-Voltage Lockout Threshold

The IC includes an input Under Voltage Lockout Protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (3.9V), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage (3.25V) during normal operation, the device stops switching. The UVLO rising and falling threshold voltage includes a hysteresis to prevent noise caused reset.

Chip Enable

The EN pin is the chip enable input. Pulling the EN pin low (<1.1V) will shutdown the output voltage. During shutdown mode (<0.4V), the RT7296F's quiescent current drops to lower than 1μA. Driving the EN pin high (>1.6V) will turn on the device.

Operating Frequency and Synchronization

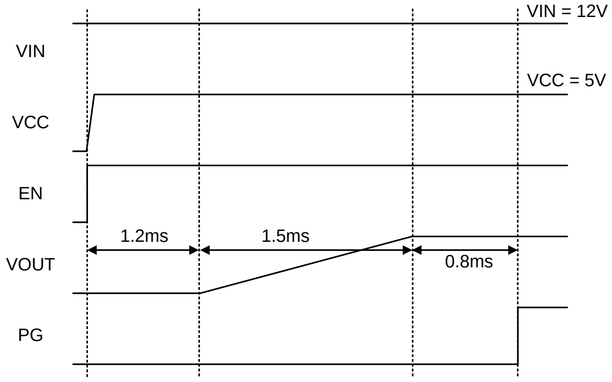
The internal oscillator runs at 500kHz (typ.) when the EN/SYNC pin is at logic-high level (>1.6V). If the EN pin is pulled to low-level over 8μs, the IC will shut down. The RT7296F can be synchronized with an external clock ranging from 200kHz to 2MHz applied to the EN/SYNC pin. The external clock duty cycle must be from 20% to 80% with logic-high level = 2V and logic-low level = 0.8V.

Internal Regulator

The internal regulator generates 5V power and drive internal circuit. When VIN is below 5V, PVCC will drop with VIN. A capacitor (>0.1μF) between PVCC and GND is required.

Internal Soft-Start Function

The RT7296F provides internal soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. Output voltage starts to rise 1.2ms after EN rising, and the soft-start time (V_{FB} from 0V to 0.8V) is 1.5ms. PG signal goes high 0.8ms after completing soft-start.



High-Side MOSFET Over-Current Limit

The RT7296F features cycle-by-cycle current-limit protection and prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation. During the on-time of the high side switch, the device monitors the switch current. If the switch current overs the current limit threshold, the device turns off the high side switch to prevent the device from damage.

Output Under-Voltage Protection

The RT7296F includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold, 50% (typ.) of the internal reference voltage, the UV comparator will go high to turn off the internal high-side MOSFET switches. If the output under-voltage condition continues for a period of time, the RT7296F will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. The UVP profile is shown in Figure 2.

Over-Temperature Protection

Over-temperature protection is implemented to prevent the chip from operating at excessively high temperatures. When the junction temperature is higher than 150°C, the OTP will shut down switching operation. The chip will automatically resume normal operation with a complete soft-start sequence once the junction temperature cools down by approximately 20°C.

BOOT UVLO

The RT7296F implements BOOT UVLO function to ensure the $V_{BOOT-SW}$ is sufficient to correctly activate the high side switch at any condition. BOOT UVLO usually actives at higher V_{OUT}, very light load and small TTH threshold. With such conditions, the low side switch may not have sufficient turn-on time to charge the BOOT capacitor. The BOOT UVLO actives when $V_{BOOT-SW}$ is lower than 2.65V (typ.), the device will be forced to turn on the low side switch for 200ns (typ.) to charge the BOOT capacitor. The BOOT UVLO behavior continues for each PWM cycle until the $V_{BOOT-SW}$ is higher than 2.9V (typ.)

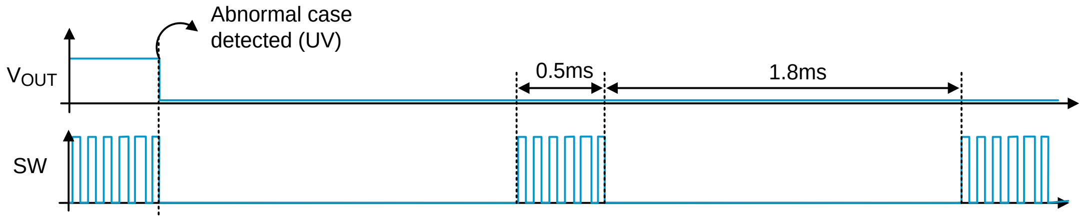


Figure 2. Output Under-Voltage Protection with Hiccup Mode

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to 20.3V
  <20ns ---------- –5V to 23V
- BOOT to SW, $V_{BOOT-SW}$ ---------- –0.3V to 6V (7V for < 10μs)
- Bias Supply Output, PVCC ---------- –0.3V to 6V (7V for < 10μs)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 (FC) ---------- 1.428W
- Package Thermal Resistance (Note 2)
  TSOT-23-8 (FC), θ_{JA} ---------- 70°C/W
  TSOT-23-8 (FC), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 17V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current			V_{EN} = 0V	--	7	--	μA
Quiescent Current with no Load at DCDC Output			V_{EN} = 2V, V_{FB} = 1V	--	0.8	1	mA
Feedback Voltage		V_{FB}		0.799	0.807	0.815	V
Feedback Current		I_{FB}	V_{FB} = 820mV	--	10	50	nA
Switch On-Resistance	High-Side	$R_{DS(ON)H}$		--	80	--	mΩ
	Low-Side	$R_{DS(ON)L}$		--	30	--	
Switch Leakage			V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Current Limit		I_{LIM}	Under 40% duty-cycle	4.2	5	5.8	A
Low-Side Switch Current Limit			From drain to source	--	2	--	A
Oscillation Frequency		f_{OSC}	V_{FB} = 0.75V	440	500	570	kHz
SYNC Frequency Range		f_{SYNC}		200	--	2000	kHz
Fold-Back Frequency			V_{FB} < 400mV	--	125	--	kHz

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty-Cycle		D_{MAX}	V_{FB} = 0.7V	90	95	--	%
Minimum On-Time		t_{ON}		--	60	--	ns
EN Input Voltage	Logic-High	V_{IH}		1.2	1.4	1.6	V
	Logic-Low	V_{IL}		1.1	1.25	1.4	
EN Input Current		I_{EN}	V_{EN} = 2V	--	2	--	μA
			V_{EN} = 0V	--	0	--	
EN Turn-off Delay		ENtd-off		--	8	--	μs
Power-Good Rising Threshol		PG_{vth-Hi}		--	0.9	--	V_{FB}
Power-Good Falling Threshol		PG_{vth-Lo}		--	0.85	--	V_{FB}
Power-Good Delay		PG_{Td}		--	0.4	--	ms
Power-Good Sink Current Capability		V_{PG}	Sink 4mA	--	--	0.4	V
Power-Good Leakage Current		$I_{PG-LEAK}$		--	--	1	μA
Input Under-Voltage Lockout Threshold	V_{IN} Rising	V_{UVLO}	V_{IN} rising	3.7	3.9	4.1	V
	Hysteresis	ΔV_{UVLO}		--	650	--	mV
PVCC Regulator		V_{CC}		--	5	--	V
PVCC Load Regulation		ΔV_{LOAD}	I_{VCC} = 5mA	--	3	--	%
Soft-Start Time		t_{SS}	FB from 0V to 0.8V	--	1.5	--	ms
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Richtek Evaluation Board. θ_{JC} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

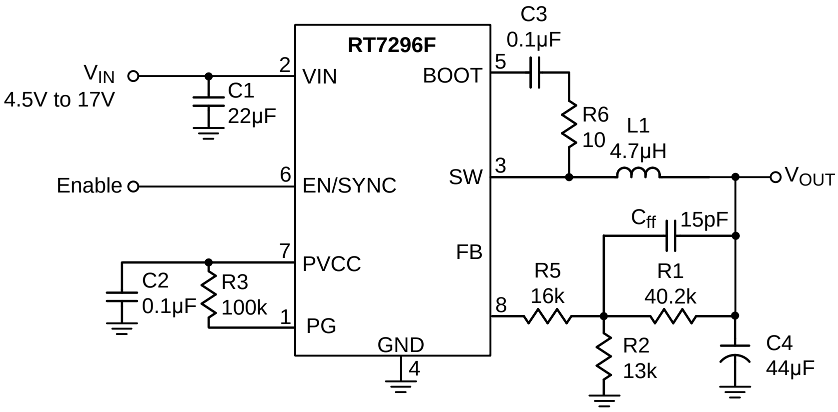
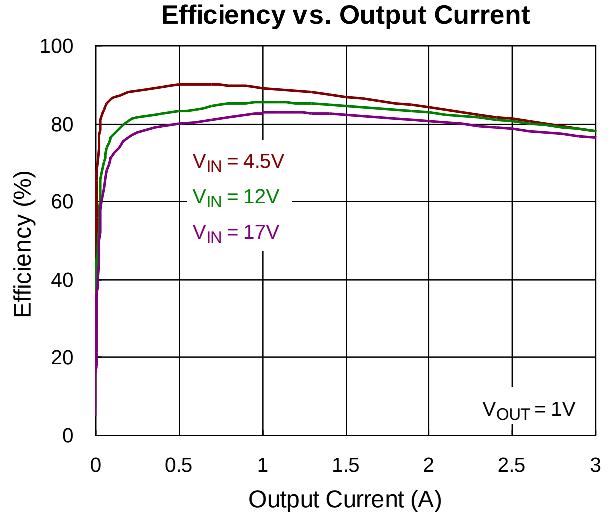


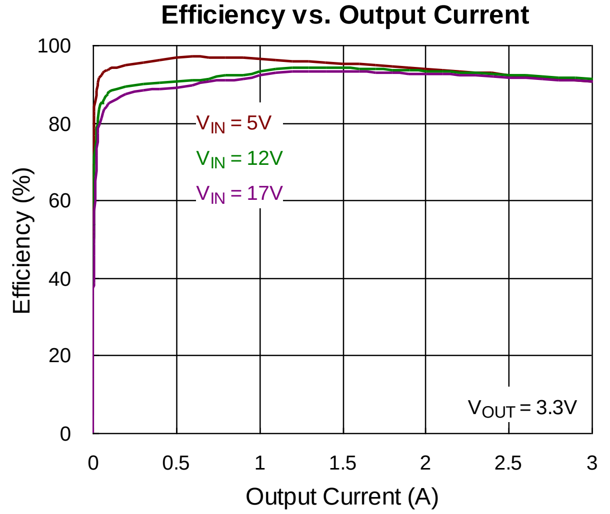
Table 1. Suggested Component Values

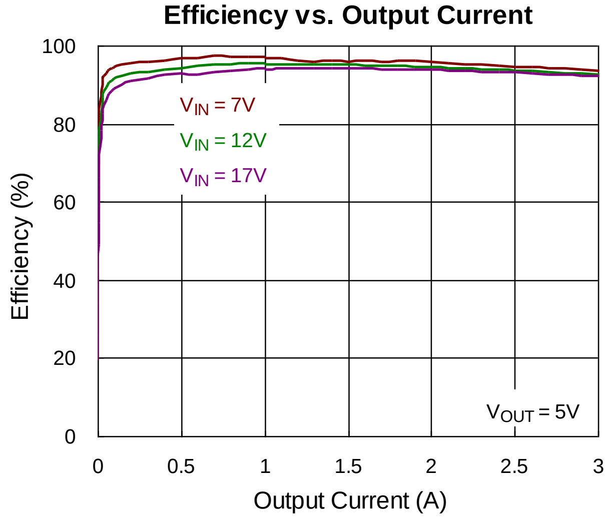
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R5 (kΩ)	C_{ff} (pF)	C2 (μF)	C4 (μF)	L1 (μH)
1.0	20.5	84.5	82	15	0.1	44	2.2
3.3	40.2	13	16	15	0.1	44	4.7
5.0	40.2	7.68	16	15	0.1	44	4.7

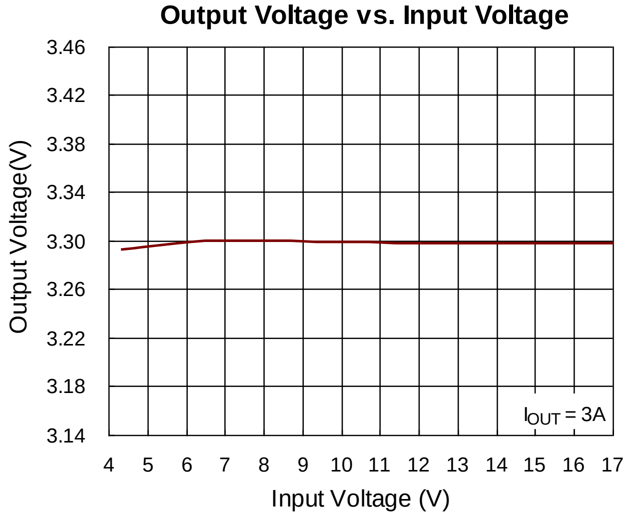
Note : Where the C4 value means the effective output capacitance. Design engineer must be aware that ceramic capacitance varies a great deal with the size, operating voltage and temperature. The variation should be taken into the design consideration of control loop bandwidth. A rule-of-the-thumb is to design the RT7296F control loop bandwidth below 60kHz by changing the value of R5. Generally, increase the value of R5 if a de-rated capacitance is used.

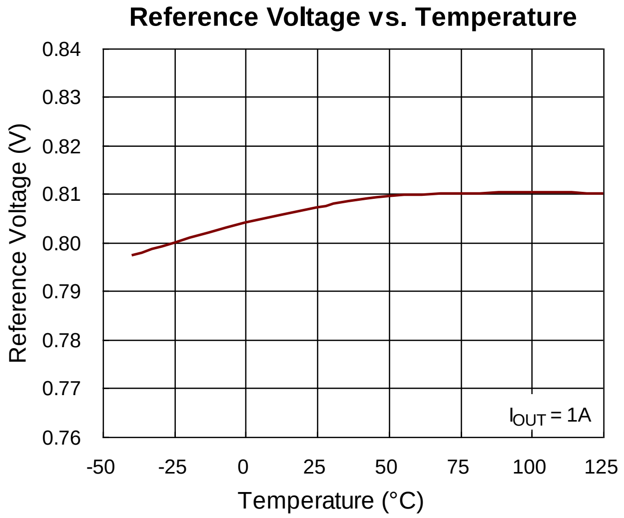
Typical Operating Characteristics

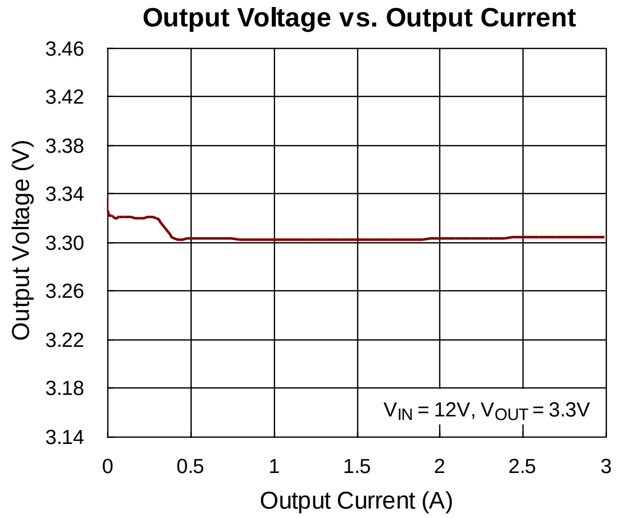




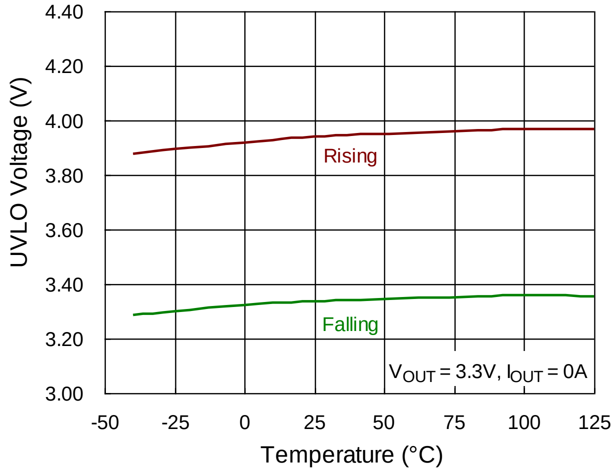




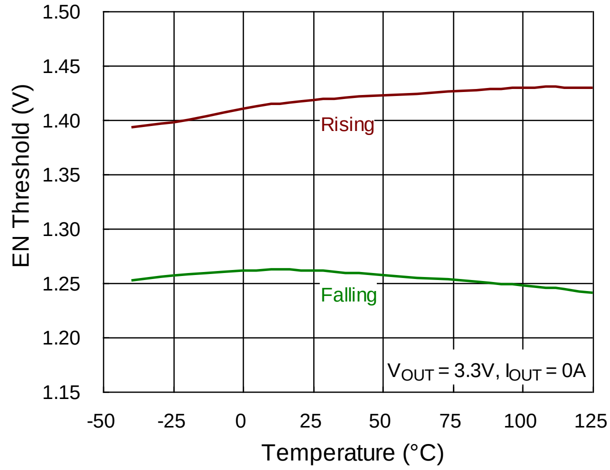




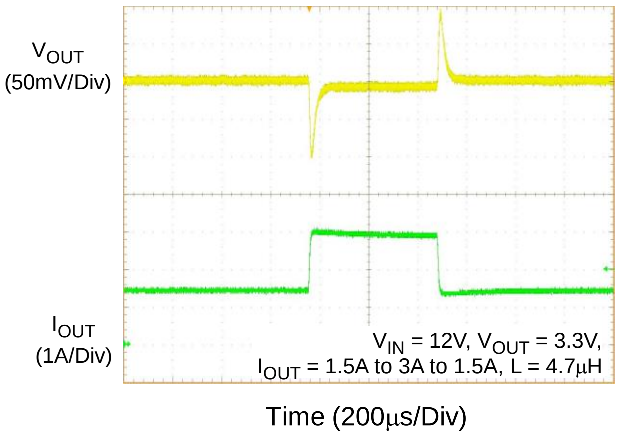
UVLO Voltage vs. Temperature



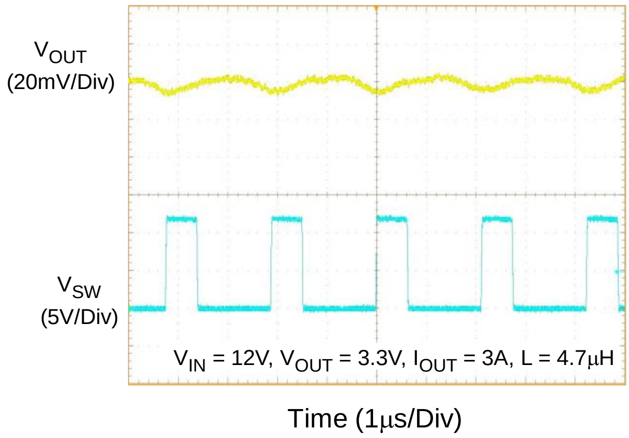
EN Threshold vs. Temperature



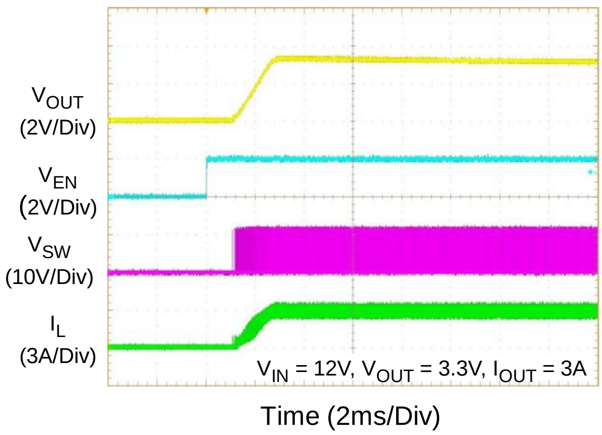
Load Transient Response



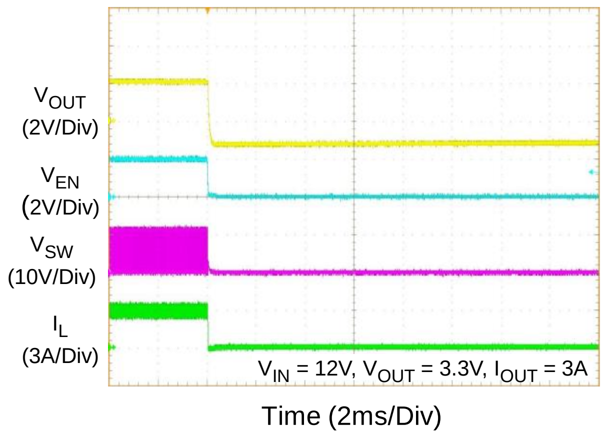
Output Ripple Voltage



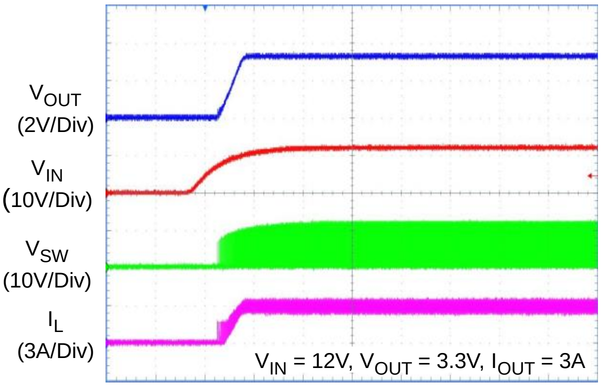
Power On from EN



Power Off from EN

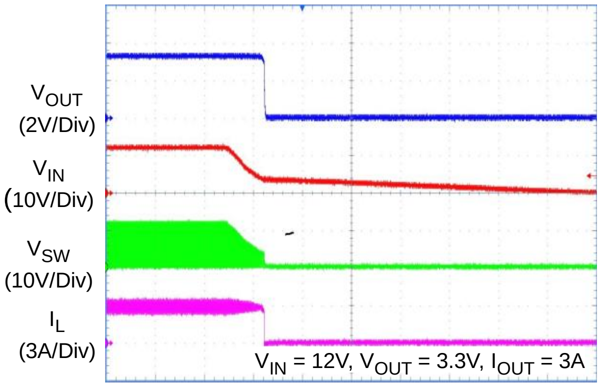


Power On from VIN



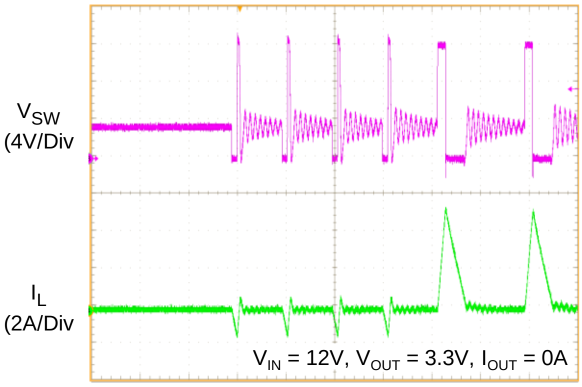
Time (5ms/Div)

Power Off from VIN



Time (5ms/Div)

BOOT UVLO



Time (2μs/Div)

Application Information

The RT7296F is a high voltage buck converter that can support the input voltage range from 4.5V to 17V and the input voltage range from 4.5V to 17V and the output current can be up to 3A.

Output Voltage Selection

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

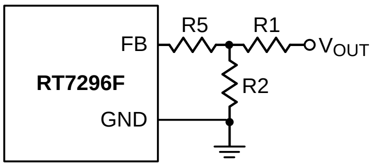


Figure 3. Output Voltage Setting

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

Where V_{FB} is the feedback reference voltage (0.8V typ.). Table 2 lists the recommended resistors value for common output voltages.

Table 2. Recommended Resistors Value

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R5 (kΩ)
1.0	20.5	84.5	82
3.3	40.2	13	16
5.0	40.2	7.68	16

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and BOOT pin, as shown as Figure 4, for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output (PVCC) of the RT7296F.

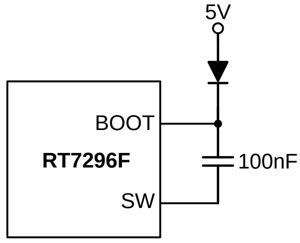


Figure 4. External Bootstrap Diode

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L = 0.3 (I_{MAX}) will be a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left(\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right) \times \left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = $2V_{OUT}$, where I_{RMS} = I_{OUT} / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. The selection of C_{OUT} is determined by the required Effective Series Resistance (ESR) to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \times \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 70°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (70°C/W) = 1.428W for TSOT-23-8 (FC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

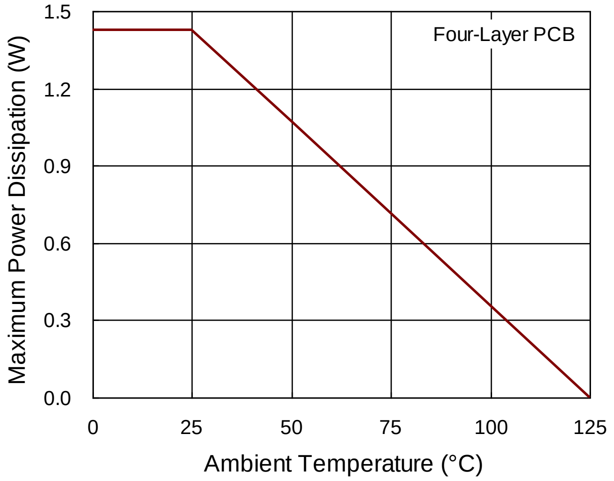


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT7296F, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close to the IC as possible.
- SW should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- Keep VIN, GND and SW traces connected to pin as wide as possible for improving thermal dissipation.

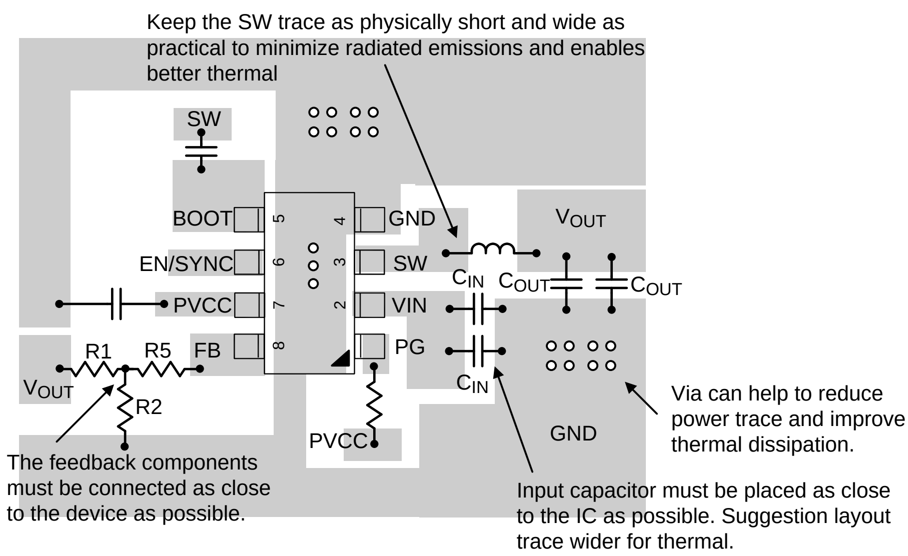


Figure 6. PCB Layout Guide