500mA, Low Dropout, Low Noise, Ultra-Fast Linear Regulator

General Description

The RT9065 is designed for portable RF and wireless applications with demanding performance and space requirements. The RT9065 performance is optimized for battery powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The RT9065 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand held wireless devices. The RT9065 consumes less than 0.01μA in shutdown mode. The other features include low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. The RT9065 is available in the SOT-23-6 package.

Features

- **Ultra-Low-Noise for RF Application**
- **Ultra-Fast Response in Line/Load Transient**
- **0.01μA Shutdown Current**
- **Low Dropout : 370mV @ 500mA**
- **Wide Input Voltage Range : 2.2V to 5.5V**
- **Adjustable Output Voltage**
- **TTL Logic Controlled Shutdown Input**
- **Low Temperature Coefficient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **Only 1μF Output Capacitor Required for Stability**
- **High Power Supply Rejection Ratio**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT9065 □□

- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

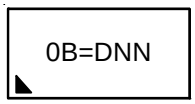
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

- CDMA/GSM Cellular Handsets
- Battery Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand Held Instruments
- PCMCIA Cards
- Portable Information Appliances

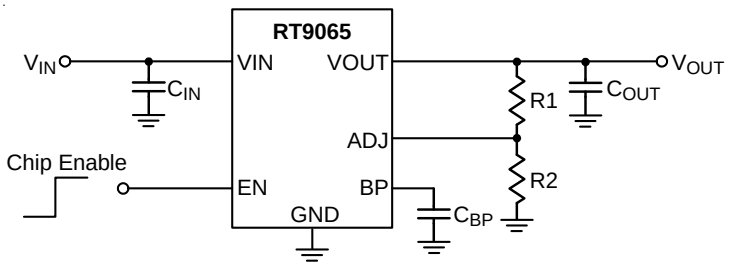
Marking Information



0B= : Product Code

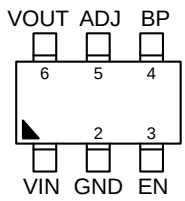
DNN : Date Code

Simplified Application Circuit



Pin Configuration

(TOP VIEW)

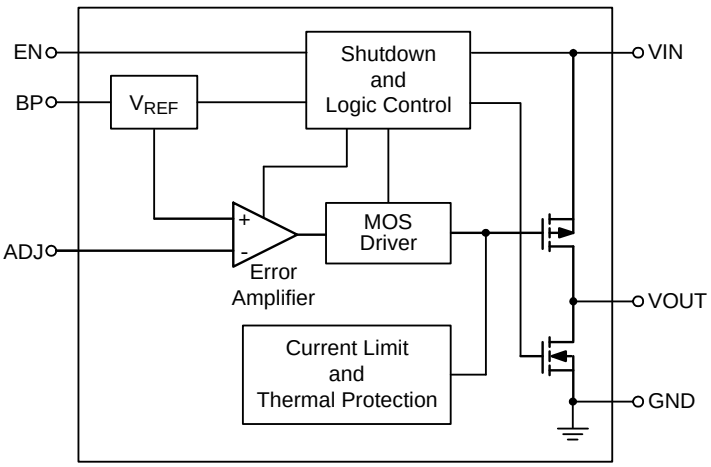


SOT-23-6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Power input.
2	GND	Ground.
3	EN	Chip enable (active high). Note that this pin is high impedance. There should be a pull-low 100kΩ resistor connected to GND when the control signal is floating.
4	BP	Reference noise bypass.
5	ADJ	Feedback input. Connect a resistive divider to adjust the output voltage.
6	VOUT	Output of the regulator.

Functional Block Diagram



Operation

The RT9065 is a low dropout voltage linear regulator designed for RF and wireless applications which require low noise and high PSRR performance. The RT9065 builds in a P-type P-MOSFET with current capability up to 500mA. In normal operation, the Error Amplifier adjusts the gate voltage of the power MOSFET to regulate the ADJ voltage being equal to the internal 0.8V reference voltage.

P-MOSFET current is detected and current limit function will work to limit the output current to a designed value when short circuit happens. Furthermore, the P-MOSFET will be shutdown if the junction temperature is higher than typically 165°C, and released to normal operation until the temperature falls below typically 135°C.

Start-Up

This function is defined as chip start up time which is from V_{EN} > V_{IH} to the 95% of V_{OUT}.

Shutdown and Logic Control

This function block includes chip Enable/Disable and UVLO circuits. When chip is disabled, VOUT is pulled to GND through the auto-discharge MOSFET.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 6V
- Chip Enable Input Voltage, EN ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to 6V
- Adjust Output, ADJ ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.48W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 208.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 2.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = 2.2µF, C_{OUT} = 1µF, C_{BP} =22nF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
ADJ Reference Voltage		V_{ADJ}	V_{IN} = 5V, I_{OUT} = 100mA	0.788	0.8	0.812	V
Shutdown Current		I_{SHDN}	V_{EN} = GND	--	0.01	1	µA
Quiescent Current		I_Q	I_{OUT} = 0mA	--	90	120	µA
Dropout Voltage		V_{DROP}	I_{OUT} = 300mA	--	220	300	mV
			I_{OUT} = 500mA	--	370	500	
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA	--	--	0.3	%
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 500mA	--	--	0.6	%
EN Input Bias Current		I_{IBSD}	V_{EN} = GND or V_{IN}	--	0	100	nA
EN Input Voltage	Logic-High	V_{IH}		1.2	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Start-Up Time	t_{START}	From V_{EN} > V_{IH} to V_{OUT} = 95% of V_{OUT}	V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10μF	35	60	80	μs
			V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 20μF	60	80	120	
			V_{IN} = 3.3V, V_{OUT} = 2.9V, C_{OUT} = 30μF	130	175	240	
			V_{IN} = 3.3V, V_{OUT} = 2.9V, C_{OUT} = 60μF	250	340	450	
			V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 30μF	140	180	250	
			V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 60μF	270	350	480	
EN Start-Up Delay Time	t_{EN_Delay}	From V_{EN} > V_{IH} to V_{OUT} = 0% of V_{OUT}	V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10μF	5	15	30	μs
			V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 20μF	5	15	30	
			V_{IN} = 3.3V, V_{OUT} = 2.9V, C_{OUT} = 30μF	5	15	30	
			V_{IN} = 3.3V, V_{OUT} = 2.9V, C_{OUT} = 60μF	5	15	30	
			V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 30μF	5	10	20	
			V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 60μF	5	10	20	
Output Noise Voltage	eNO	10kHz to 100kHz, I_{OUT} = 200mA, C_{OUT} = 1μF		--	100	--	μVRMS
Power Supply Rejection Rate f = 100Hz	PSRR	C_{OUT} = 1μF, I_{OUT} = 10mA		--	70	--	dB
Power Supply Rejection Rate f = 10kHz				--	50	--	
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising		1.6	1.8	2	V
Under Voltage Lockout Hysteresis	ΔV_{UVLO}			0.1	0.15	--	V
Current Limit	I_{LIM}	R_{LOAD} = 1Ω		500	650	--	mA
Thermal Shutdown Threshold	T_{SD}			--	165	--	°C
Hysteresis	ΔT_{SD}			--	30	--	°C

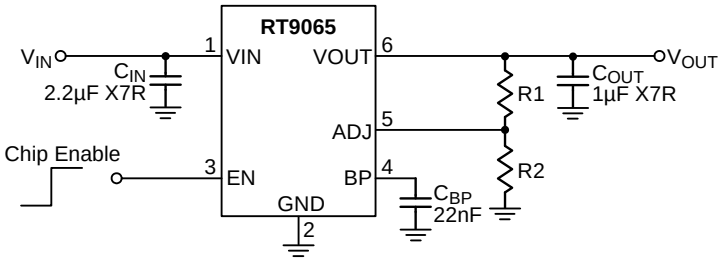
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

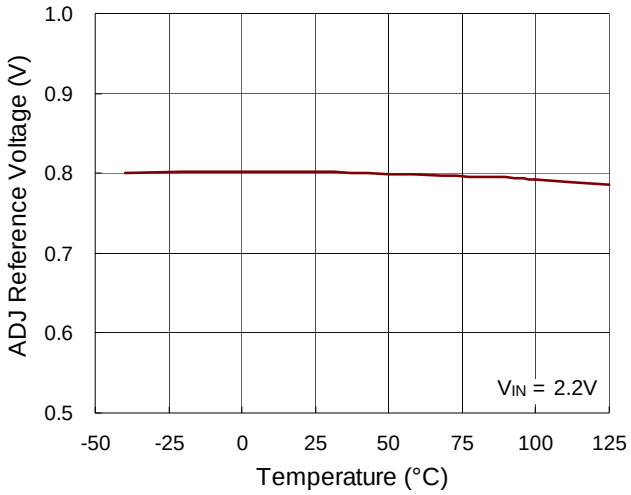
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

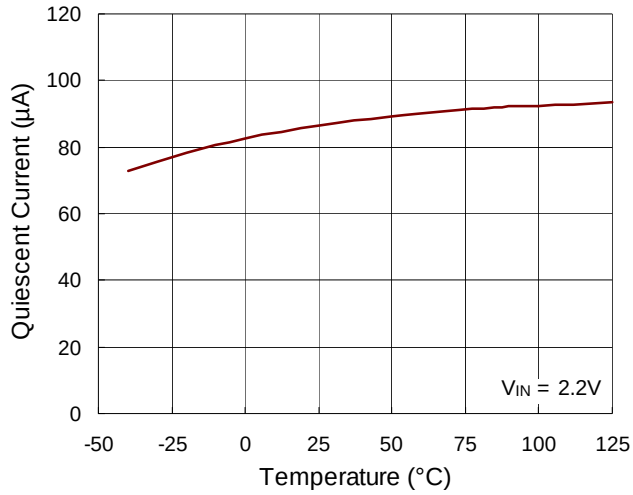


Typical Operating Characteristics

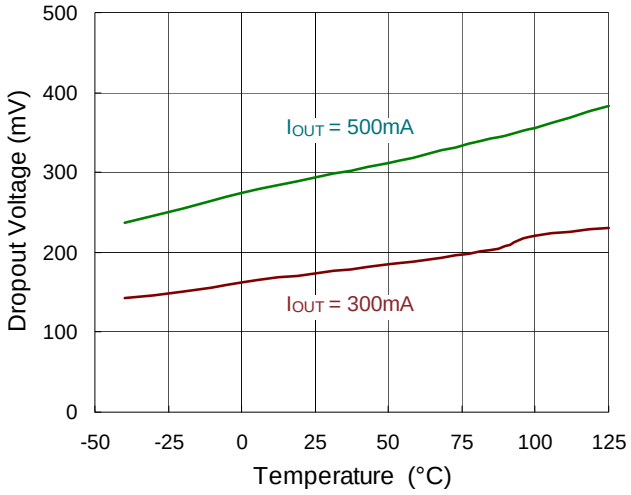
ADJ Reference Voltage vs. Temperature



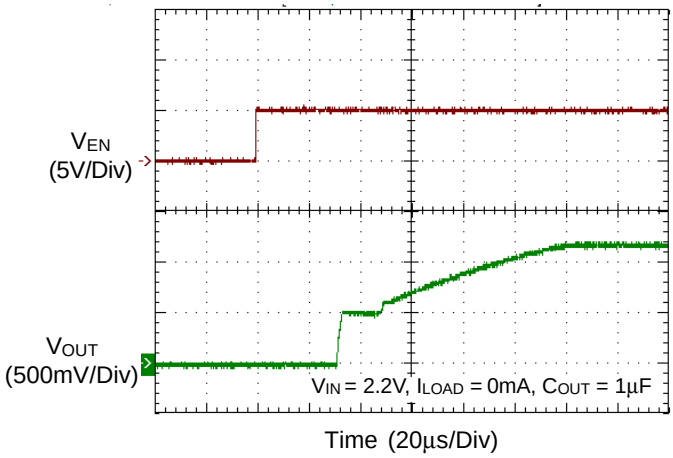
Quiescent Current vs. Temperature



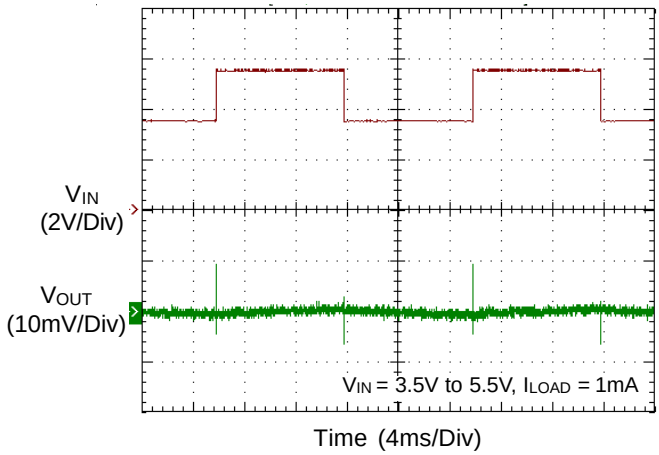
Dropout Voltage vs. Temperature



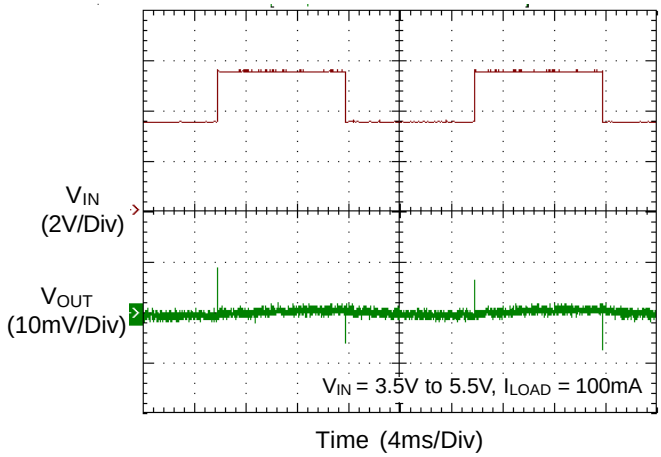
Start-Up



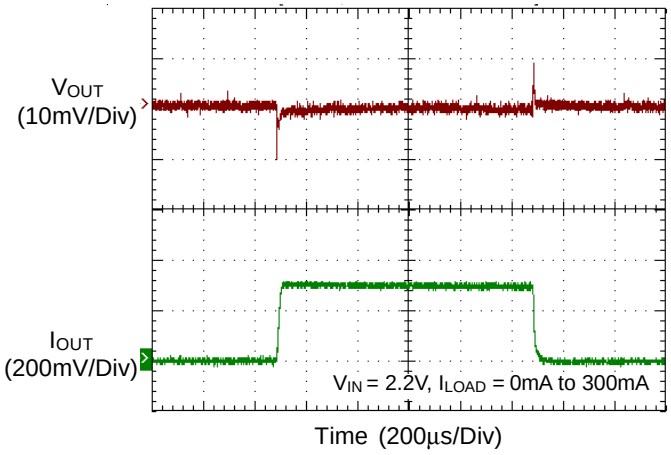
Line Transient Response



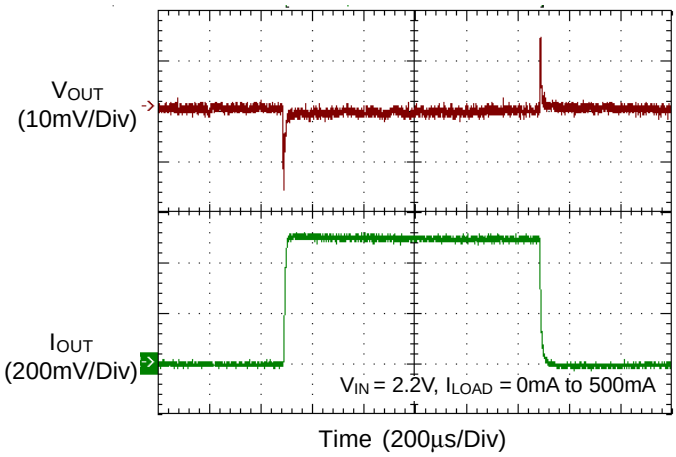
Line Transient Response



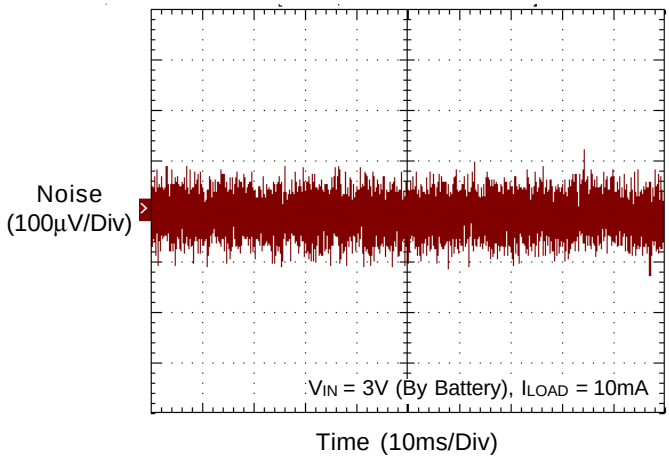
Load Transient Response



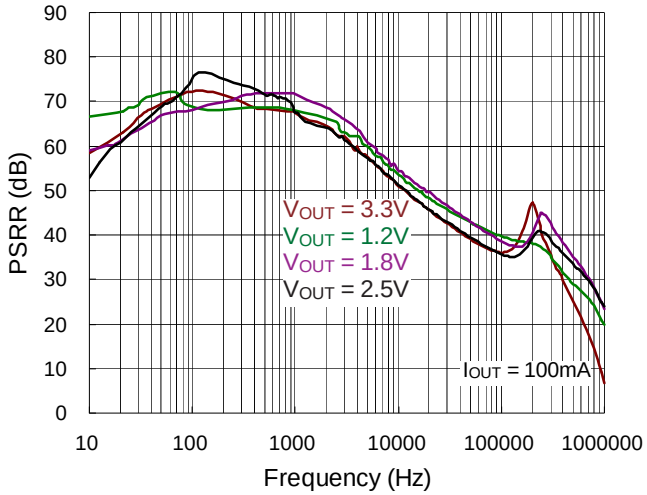
Load Transient Response



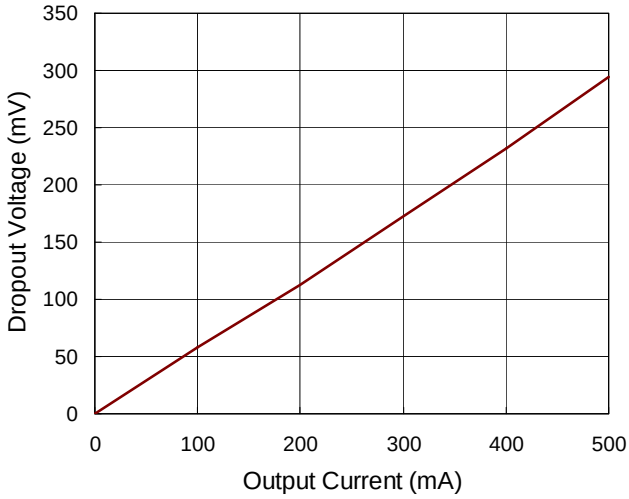
Noise



PSRR



Dropout Voltage vs. Output Current



Application Information

The RT9065 requires input and output decoupling capacitors. These capacitors must be correctly selected for good performance and insufficient decoupling capacitance may cause oscillation.

Input Capacitor

The value of input capacitor should be ≥ 2.2μF. The input capacitor must be placed within 1cm from the device to assure input stability. There are no requirements for the ESR (equivalent series resistance) on the input capacitor, but low-ESR ceramic capacitor with larger value provides better PSRR and line transient response.

Output Capacitor

The output capacitor must meet both requirements for minimum amount of capacitance and ESR for the LDO application. The RT9065 is designed specifically to work with low-ESR ceramic output capacitor in consideration of space-saving and performance. To ensure the stability, the value of ceramic capacitor should be at least 1μF and ESR should be > 5mΩ. The RT9065 can also work well with other types of output capacitors. Figure 1 shows the stable range of ESR as a function of load current for various output capacitor values. Output capacitor with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located no more than 0.5 inches from the VOUT pin.

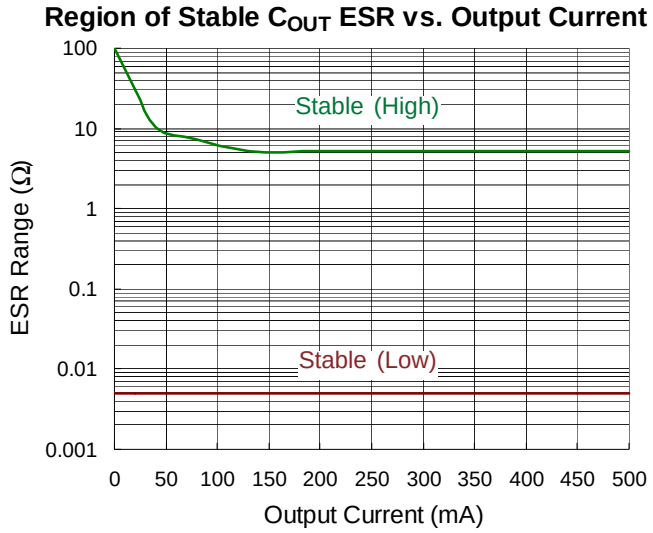


Figure 1. Region of Stable C_{OUT} ESR

Adjustable Output Voltage

The output voltage is set by the ratio of two external resistors as follow :

$V_{OUT} = 0.8 \times (1 + R1 / R2)$

Bypass Capacitor and Low Noise

Connecting a 22nF capacitor between the BP pin and the GND pin significantly reduces noise on the regulator output, and it is critical that the capacitor should be placed close to the IC and PCB traces should be as short as possible. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

Enable Function

The RT9065 features an enable/disable function. The enable control level must be greater than 1.2V to turn-on the device. When the voltage on the EN pin falls below 0.4V, the LDO will be shut down and will reduce quiescent current to less than 1μA. If the enable function is not needed in a specific application, it should be tied to VIN to keep the LDO in a continuously on state.

Current Limit

The RT9065 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.65A (typ.). The output can be shorted to ground without damaging the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to SOT-23-6 package, the thermal resistance, θ_{JA}, is 208.2°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (208.2°C/W) = 0.48W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

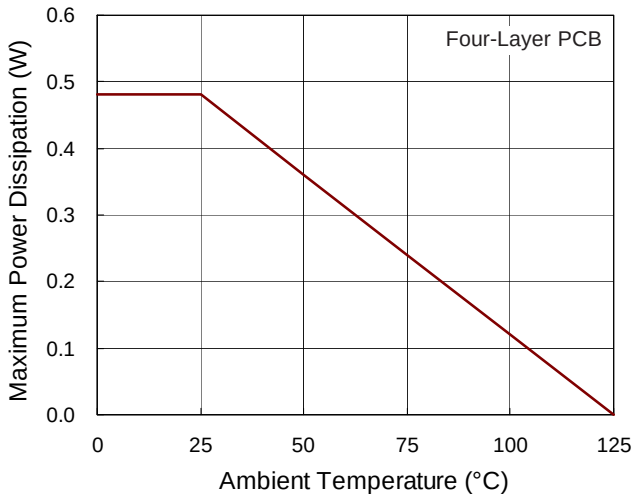


Figure 2. Derating Curve of Maximum Power Dissipation