20V, 1A, Rail-to-Rail Operational Amplifier

General Description

The RT9146/7 consists of a low power, high slew rate, single supply rail-to-rail input and output operational amplifier.

The RT9146 contains a single amplifier and the RT9147 contains two amplifiers in one package.

The RT9146/7 has a high slew rate (35V/μs), 1A peak output current and offset voltage below 15mV. The RT9146/7 is ideal for Thin Film Transistor Liquid Crystal Displays (TFT-LCD) .

The RT9146 is available in the WDFN-8L 3x3 package, and the RT9147 is available in the WQFN-16L 4x4 package. The RT9146/7 are specified for operation over the full –40°C to 85°C temperature range.

Ordering Information

RT9146 □□

- Package Type
  - QW : WDFN-8L 3x3
  - QWA : WDFN-8SL 3x3
- Lead Plating System
  - Z : ECO (Ecological Element with Halogen Free and Pb free)

RT9147 □□

- Package Type
  - QW : WQFN-16L 4x4
- Lead Plating System
  - Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

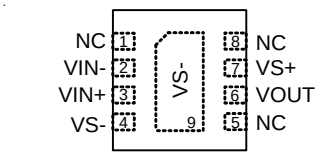
- **Rail-to-Rail Output Swing**
- **Supply Voltage : 6V to 20V**
- **Peak Output Current : 1A**
- **High Slew Rate : 35V/μs**
- **Unity Gain Stable**
- **RoHS Compliant and Halogen Free**

Applications

- TFT-LCD Panels
- Notebook Computers
- Monitors
- LCD TVs

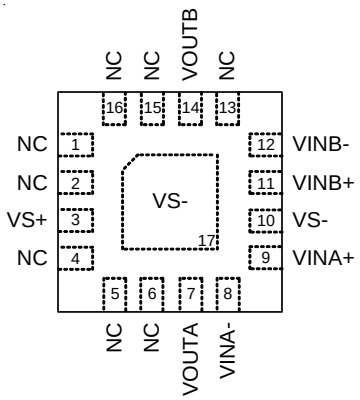
Pin Configurations

(TOP VIEW)



WDFN-8L 3x3 / WDFN-8SL 3x3

RT9146

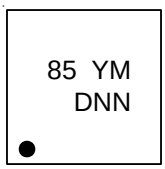


WQFN-16L 4x4

RT9147

Marking Information

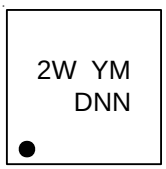
RT9146ZQW



85 : Product Code

YMDNN : Date Code

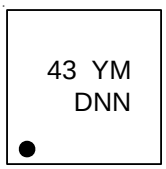
RT9146ZQWA



2W : Product Code

YMDNN : Date Code

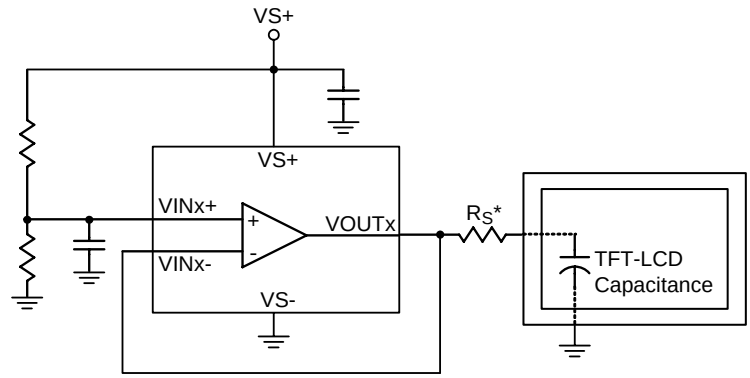
RT9147ZQW



43 : Product Code

YMDNN : Date Code

Typical Application Circuit



* : R_S may be needed for some applications.

Functional Pin Description

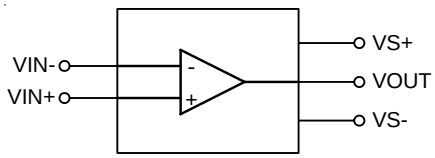
RT9146

Pin No.		Pin Name	Pin Function
WDFN-8L 3x3	WDFN-8SL 3x3		
1, 5, 8		NC	No Internal Connection.
2		VIN–	Negative Input.
3		VIN+	Positive Input.
4, 9 (Exposed Pad)		VS–	Negative Supply Input. The exposed pad must be soldered to a large PCB and connected to VS– for maximum power dissipation.
6		VOUT	Output.
7		VS+	Positive Supply Input. Bypass VS+ to VS– with a 0.1μF capacitor placed as close as possible to the device.

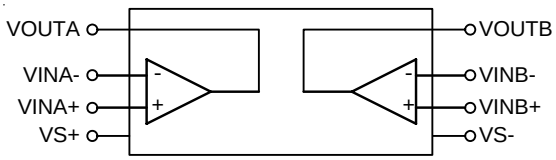
RT9147

Pin No.	Pin Name	Pin Function
1, 2, 4, 5, 6, 13, 15, 16	NC	No Internal Connection.
3	VS+	Positive Supply Input. Bypass VS+ to VS– with a 0.1μF capacitor placed as close as possible to the device.
7	VOUTA	Output of Amplifier A.
8	VINA–	Positive Input of Amplifier A.
9	VINA+	Negative Input of Amplifier A.
10, 17 (Exposed Pad)	VS–	Negative Supply Input. The exposed pad must be soldered to a large PCB and connected to VS– for maximum power dissipation.
11	VINB+	Positive Input of Amplifier B.
12	VINB–	Negative Input of Amplifier B.
14	VOUTB	Output of Amplifier B.

Function Block Diagram



RT9146



RT9147

Absolute Maximum Ratings (Note 1)

- Supply Voltage, (VS+ to VS–) ---------- 24V
- VINx+, VINx– to VS– ---------- –0.3V to 24V
- VINx+ to VINx– ---------- ±5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8L 3x3 ---------- 3.22W
  - WDFN-8SL 3x3 ---------- 3.22W
  - WQFN-16L 4x4 ---------- 3.51W
- Package Thermal Resistance (Note 2)
  - WDFN-8L 3x3, θ_{JA} ---------- 31°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
  - WDFN-8SL 3x3, θ_{JA} ---------- 31°C/W
  - WDFN-8SL 3x3, θ_{JC} ---------- 8°C/W
  - WQFN-16L 4x4, θ_{JA} ---------- 28.5°C/W
  - WQFN-16L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VS– = 0V, VS+ ---------- 6V to 20V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{S+} = 16V, V_{S-} = 0V, V_{INx+} = V_{OUTx} = V_{S+} / 2, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}	V_{CM} = V_{S+} / 2	--	2	15	mV
Input Bias Current	I_B	V_{CM} = V_{S+} / 2	--	2	50	nA
Load Regulation	ΔV_{LOAD}	I_{OUTx} = 0 to –80mA	--	0.1	--	mV/mA
		I_{OUTx} = 0 to 80mA	--	–0.1	--	
Common Mode Input Range	CMIR		0.5	--	V_{S+} –0.5	V
Common Mode Rejection Ratio	CMRR	0.5V ≤ V_{OUTx} ≤ V_{S+} – 0.5V	--	95	--	dB
Open Loop Gain	A_{VOL}	0.5V ≤ V_{OUTx} ≤ V_{S+} – 0.5V	--	118	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Characteristics						
Output Swing Low	V_{OL}	I_L = –50mA	--	0.6	1.5	V
Output Swing High	V_{OH}	I_L = 50mA	V_{S+} – 1.5	V_{S+} – 0.3	--	V
Transient Peak Output Current	I_{PK}		800	1000	1400	mA
Power Supply						
Power Supply Rejection Ratio	PSRR	V_{S+} = 6V to 20V, V_{CM} = V_{OUTx} = V_{S+} / 2	--	96	--	dB
Quiescent Current	I_{DD}	No Load	--	4	--	mA
Dynamic Performance						
Slew Rate	SR	4V step, 20% to 80%, A_V = 1	--	35	--	V/μs
Setting to ±0.1% (AV = 1)	t_S	A_V = 1, V_{OUTx} = 2V step R_L = 10kΩ, C_L = 10pF	--	270	--	ns
–3dB Bandwidth	BW	R_L = 10kΩ, C_L = 10pF	--	16	--	MHz
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L = 10pF	--	12	--	MHz
Phase Margin	PM	R_L = 10kΩ, C_L = 10pF	--	50°	--	--
Thermal Shutdown Temperature	T_S	Temperature Rising	--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_S		--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

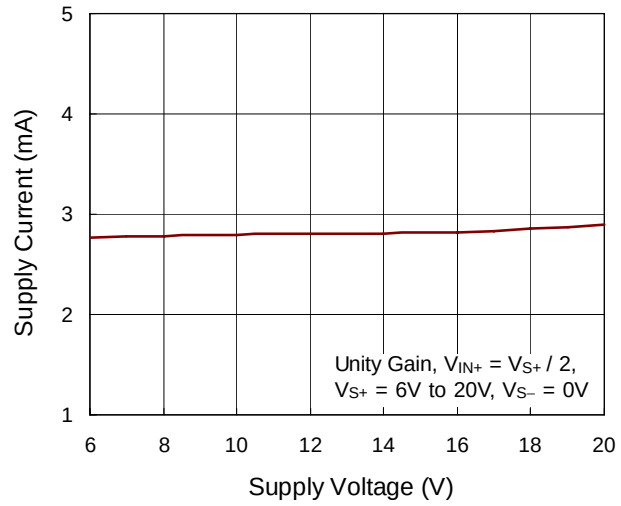
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

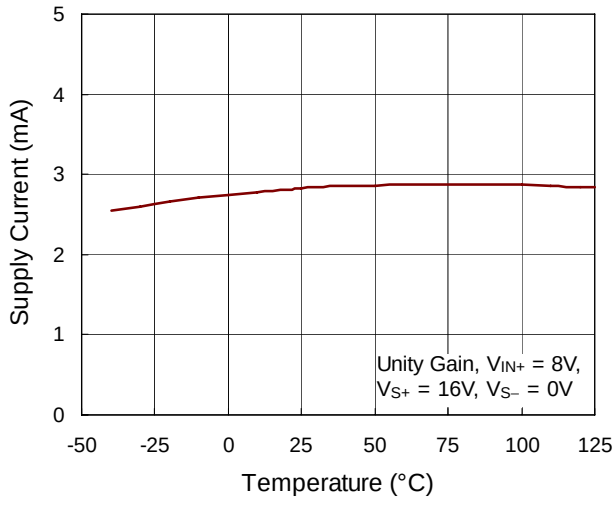
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

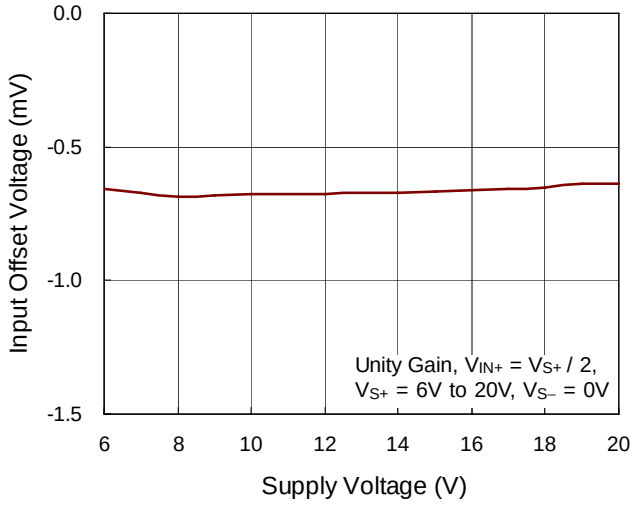
Supply Current vs. Supply Voltage



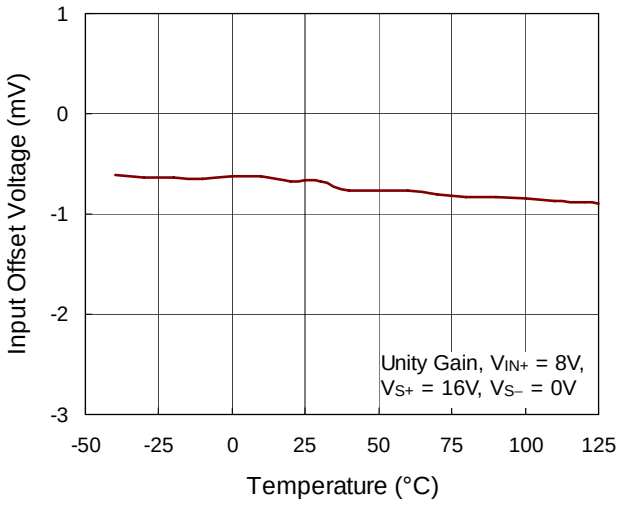
Supply Current vs. Temperature



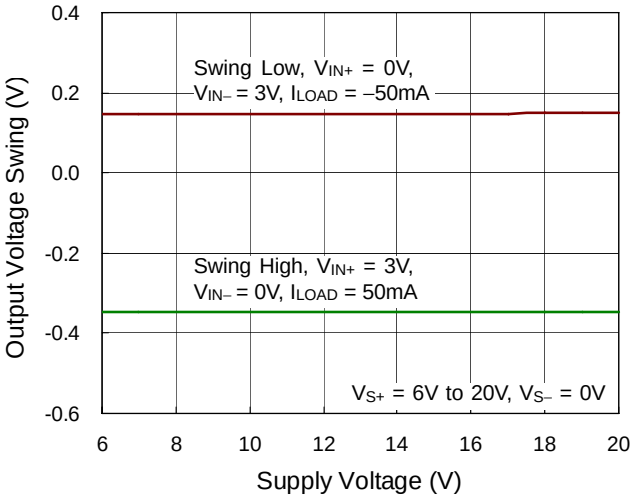
Input Offset Voltage vs. Supply Voltage



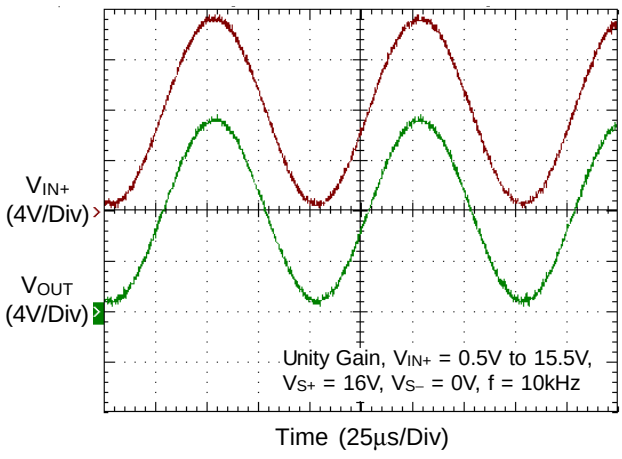
Input Offset Voltage vs. Temperature



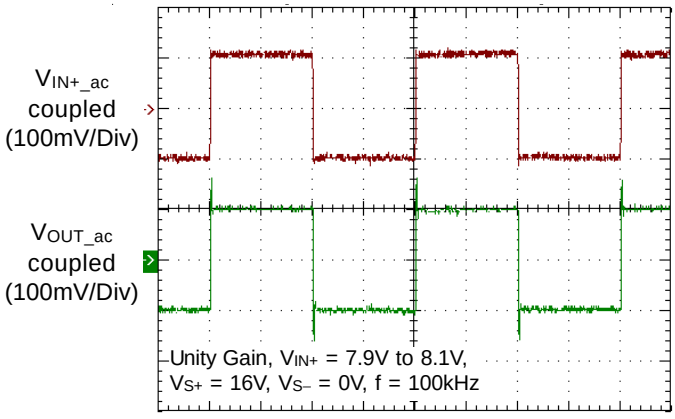
Output Voltage Swing vs. Supply Voltage



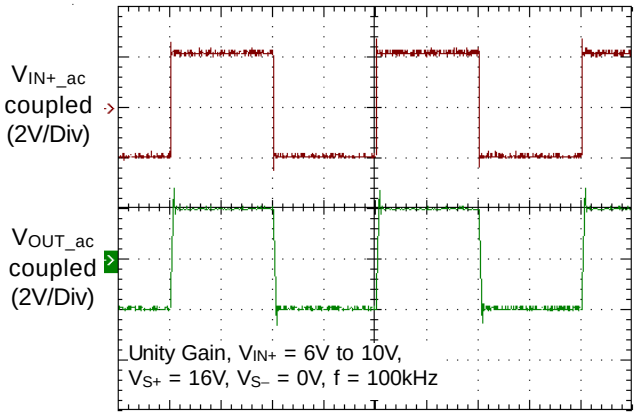
Rail to Rail



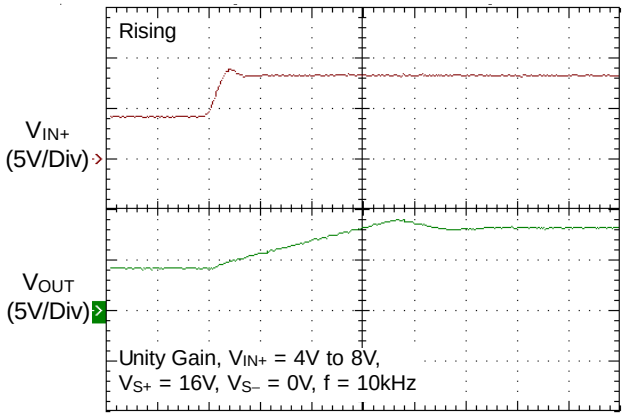
Small Signal Response



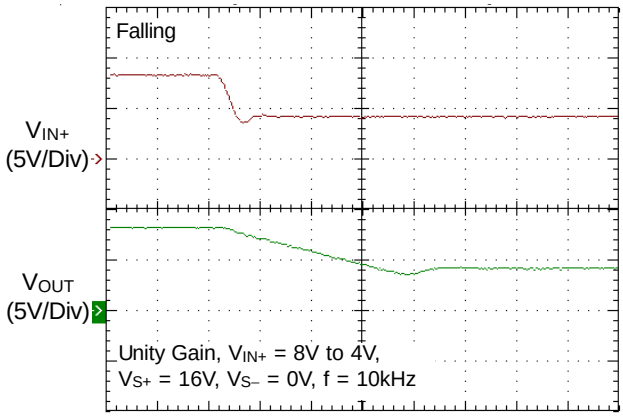
Large Signal Response



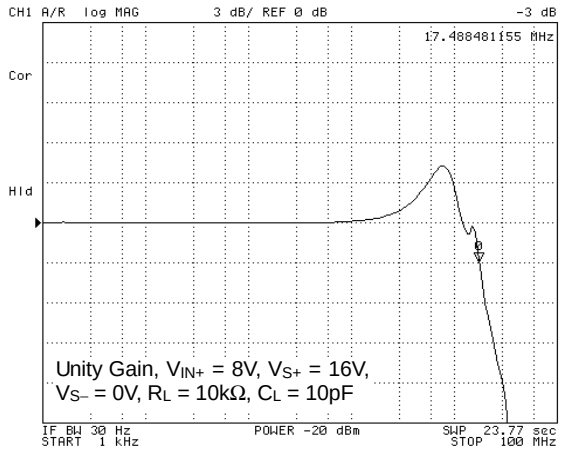
Slew Rate



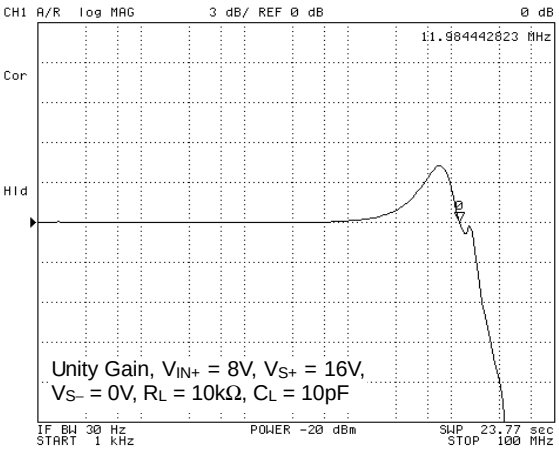
Slew Rate



–3dB Bandwidth



Gain Bandwidth Product



Applications Information

The RT9146/7 is a high performance operational amplifier capable of driving large loads for different applications. A high slew rates, rail-to-rail input and output capability, and low power consumption are the features which make the RT9146/7 ideal for LCD applications. The RT9146/7 also has wide bandwidth and phase margin to drive a load with 10kΩ resistance and 10pF capacitance.

Operating Voltage

The RT9146/7 total supply voltage range is guaranteed from 6V to 20V. The specifications are stable over both full supply range and operating temperatures from –40°C to 85°C. The output swing of the RT9146/7 typically extends to within 1.5V of positive/negative supply rails with 50mA load current source/sink. Decreasing the load current will obtain an output swing even closer to the supply rails.

Short-Circuit Condition

An internal short-circuit protection is implemented to protect the device from output short-circuit. The RT9146/7 limits the short-circuit current to ±1A if the output is directly shorted to positive/negative supply rails.

LCD Panel Applications

The RT9146/7 is mainly designed for LCD V-com buffer. The operational amplifier has 1A instantaneous source/sink peak current.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 3x3 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-8SL 3x3 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WQFN-16L 4x4 package, the thermal resistance, θ_{JA}, is 28.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.22W for WDFN-8L 3x3 package

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.22W for WDFN-8SL 3x3 package

$P_{D(MAX)}$ = (125°C – 25°C) / (28.5°C/W) = 3.51W for WQFN-16L 4X4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

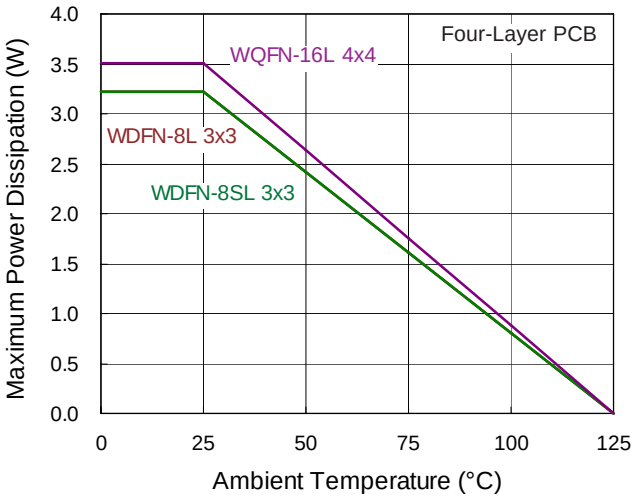


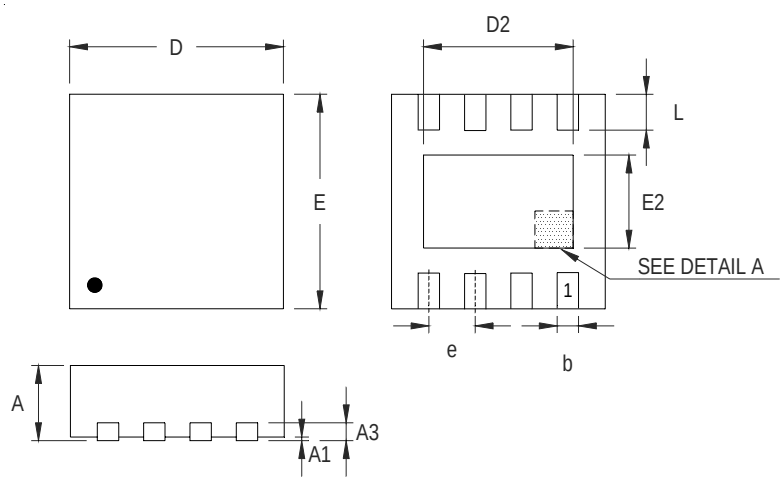
Figure 1. Derating Curve of Maximum Power Dissipation

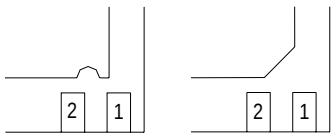
Layout Consideration

PCB layout is very important for designing power converter circuits. The following layout guidelines should be strictly followed for best performance of the RT9146/7.

- Place the power components as close to the IC as possible. The traces should be wide and short, especially for the high current loop.
- A series resistance may be needed at the output for some applications.
- Connect a 0.1µF capacitor from VINx+ to ground and place it as close to the IC as possible for better performance.
- The exposed pad of the chip should be connected to a large PCB plane for maximum thermal consideration.

Outline Dimension





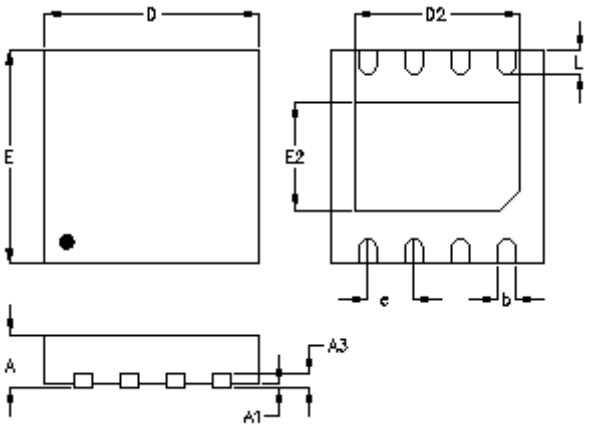
DETAIL A

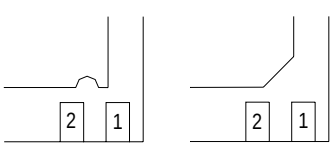
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.250	2.350	0.089	0.093
E	2.900	3.100	0.114	0.122
E2	1.450	1.550	0.057	0.061
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 8SL DFN 3x3 Package