Smart Multi-Voltage Detector

General Description

The RT9824C is an integrated smart multi-voltage detector supervising three power supply voltage levels including 5V, 5.4V and additional 3.3V, 12V or other voltage which can be determined by external divided resisters.

The RT9824C performs supervisory function by sending out $\overline{\text{RESET}}$ and CTR signals whenever the monitored voltages fall below 80% of voltage levels. The $\overline{\text{RESET}}$ and CTR signals will last the whole period before VCC recovering. Once the supervising voltages are recovered to higher than 80% of the voltage levels, the $\overline{\text{RESET}}$ and CTR signal will be released after 60ms delay time.

MR (Manual Reset) controls CTR signal during three monitored power supply voltages at normal voltage levels. When MR signal is in logic high, the CTR signal will be pulled low immediately. However the $\overline{\text{RESET}}$ will not be interfered and will be kept at high level.

The RT9824C is available in the TSOT-23-8 package.

Ordering Information

RT9824C□ □

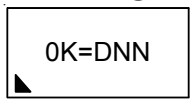
- Package Type
  J8 : TSOT-23-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0K= : Product Code

DNN : Date Code

Features

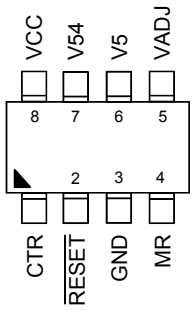
- **Capable of Monitoring Three Inputs Precisely**
- **Detection Threshold Voltages**
  - **VCC Connect to 5V or 3.3V Standby Power**
  - **V5 : 5V x 80%**
  - **V54 : 5.4V x 80%**
  - **VADJ : 1V (Using Resistor Divider)**
- **Accuracy : ±2%**
- **$\overline{\text{RESET}}$ (Open Drain Output Active Low)**
- **Built-in Recovery Delay 60ms**
- **CTR (Open Drain Output Active Low)**
- **Manual Reset (MR) Function**
- **TSOT-23-8 Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD TV or Monitors
- Consumer Electronic Products
- System Voltage Detector

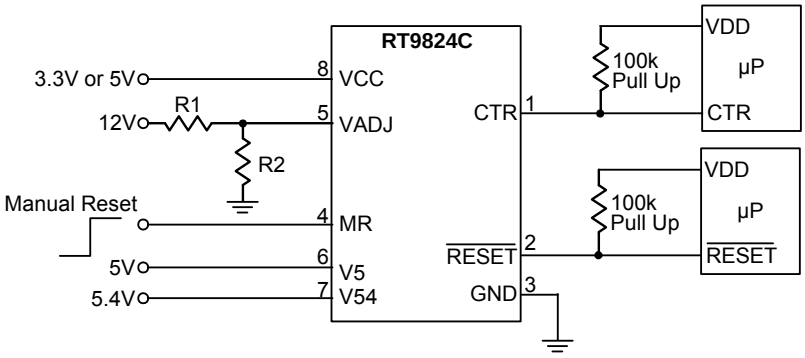
Pin Configurations

(TOP VIEW)



TSOT-23-8

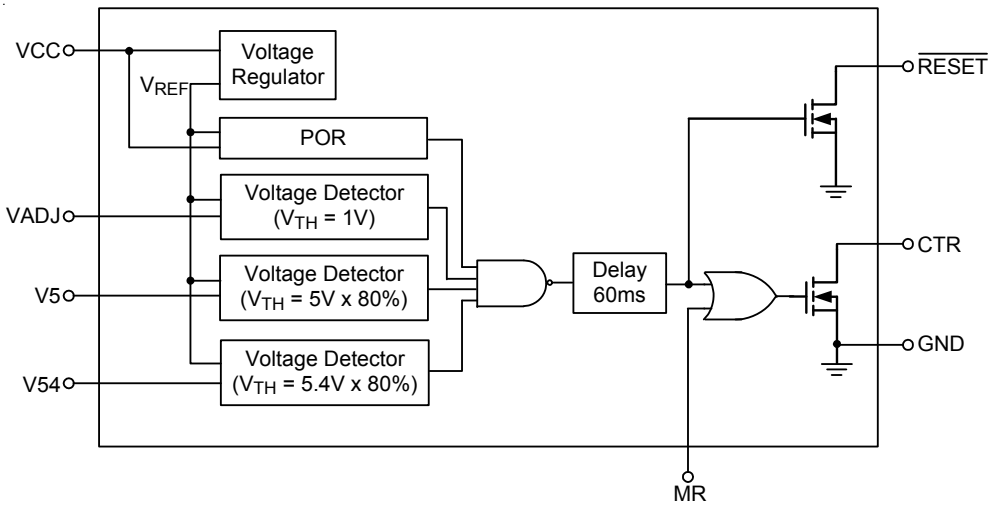
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CTR	Control Output (Open Drain, Active-Low). Only when V_{CC} is > POR, V5 is > 80%, V54 is > 80%, and V_{ADJ} is > 1V, the CTR will delay 60ms and become high. Once V5 or V54 or V_{ADJ} is <80%, the signal will become low. When MR is high, CTR will become low.
2	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output (Open Drain, Active-Low). Only when V_{CC} is > POR, V5 is > 80%, V54 is > 80%, and V_{ADJ} is > 1V, the $\overline{\text{RESET}}$ will delay 60ms and become high. Once V5 or V54 or V_{ADJ} is < 80%, the signal will become low.
3	GND	Ground.
4	MR	Manual Reset Input. Manual reset with internal pull high resister (1MΩ), H : CTR = Low; L : CTR signal is dependent on voltage detector output.
5	VADJ	Voltage Detection Input. Connect 12V or other power with external resister divider to this pin. The V_{ADJ} logic-high threshold voltage is 1V.
6	V5	5V Voltage Detection Input. The detection threshold is 5V x 80%.
7	V54	54V Voltage Detection Input. The detection threshold is 5.4V x 80%.
8	VCC	Connect this Pin to Standby Power from system.

Function Block Diagram



Operation

The RT9824 smart voltage detector monitors three voltage levels at the same time to ensure the micro-processor is operated within the recommended input voltage range. In conventional reset IC application, to monitor one power rail needs one reset IC. The RT9824 can monitor three power rails simultaneously, by using just one reset IC. The RT9824 also provides a Manual Reset (MR) function for application easily. Glitch-rejection is implemented in the RT9824 to prevent it from false operation and to eliminate the additional de-bouncing circuitry.

POR Protection

To protect the chip from operating at insufficient supply voltage, the POR is needed. When the input voltage of VIN is lower than the POR falling threshold voltage, the device will be lockout.

Absolute Maximum Ratings (Note 1)

- VCC, CTR, MR, $\overline{\text{RESET}}$, V5, V54, VADJ ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 ---------- 0.435W
- Package Thermal Resistance (Note 2)
  TSOT-23-8, θ_{JA} ---------- 230°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Current	I_{VCC}	Without load	--	--	200	μA
VCC Operating Voltage	V_{CC}		2.97	5	5.94	V
VCC POR Rising	V_{POR}		--	2.8	--	V
VCC POR Hysteresis	V_{POR_Hys}		--	0.15	--	V
Voltage Detector & MUTE Threshold						
V5 High Threshold Voltage	$V5_{TH}$		3.92	4	4.08	V
V54 High Threshold Voltage	$V54_{TH}$		4.23	4.32	4.41	V
VADJ High Threshold Voltage	$VADJ_{TH}$		0.98	1	1.02	V
Manual Reset High Voltage	V_{IH}		2	--	--	V
Manual Reset Low Voltage	V_{IL}		--	--	0.8	V
Voltage Detector Deglitch and Delay						
Voltage Detectors Delay Time	T_{DELAY}		45	60	80	ms
Voltage Detectors Deglitch Time	$T_{DEGLITCH}$		--	20	--	μs
Output : Open Drain						
$\overline{\text{RESET}}$ Output Low Voltage	$V_{OL\_\overline{RESET}}$	V_{CC} = 3.3V, 5mA sinking current at $\overline{\text{RESET}}$ output	--	--	0.3	V
CTR Output Low Voltage	V_{OL_CTR}	V_{CC} = 3.3V, 5mA sinking current at CTR output	--	--	0.3	V

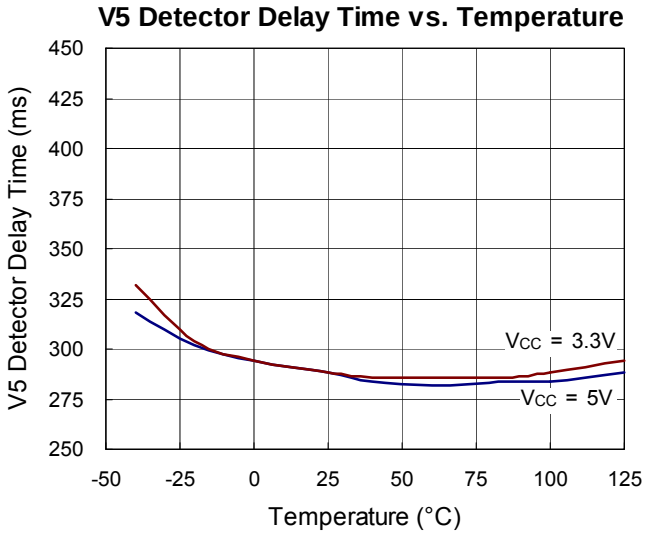
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

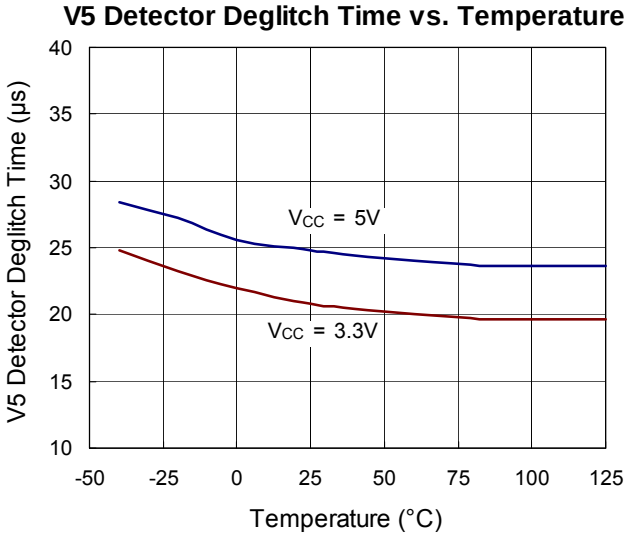
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

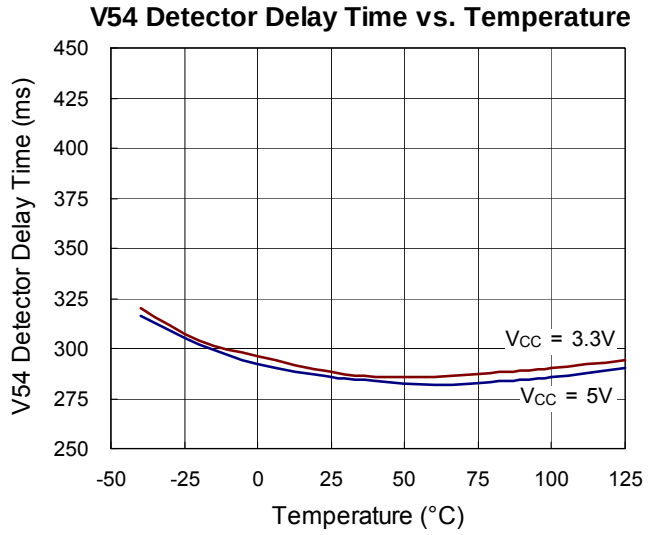
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

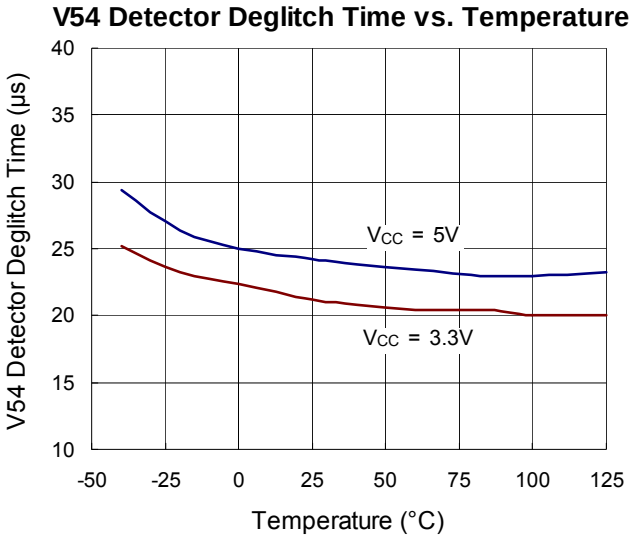
Note 4. The device is not guaranteed to function outside its operating conditions.

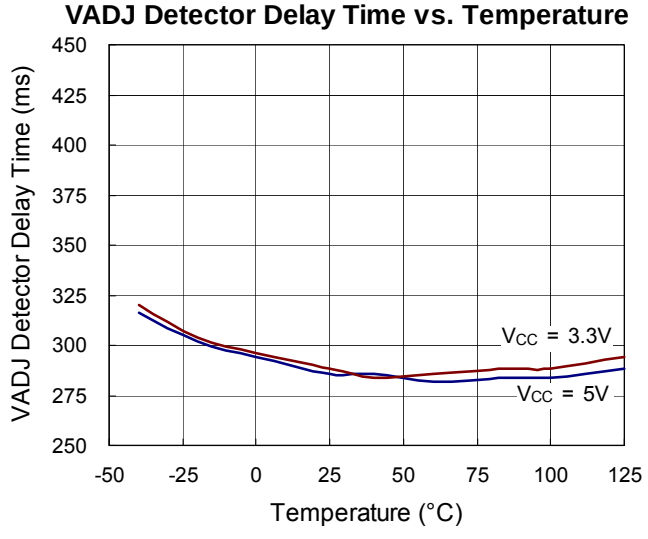
Typical Operating Characteristics

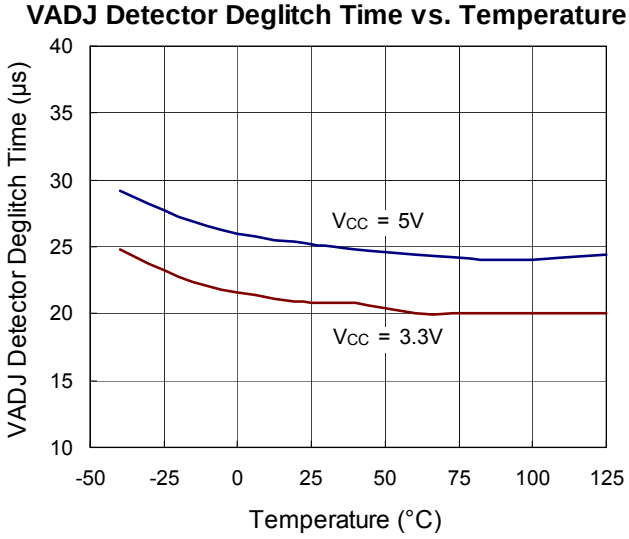




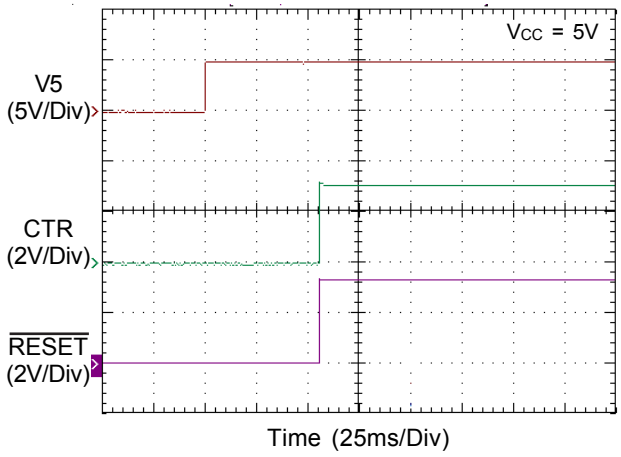




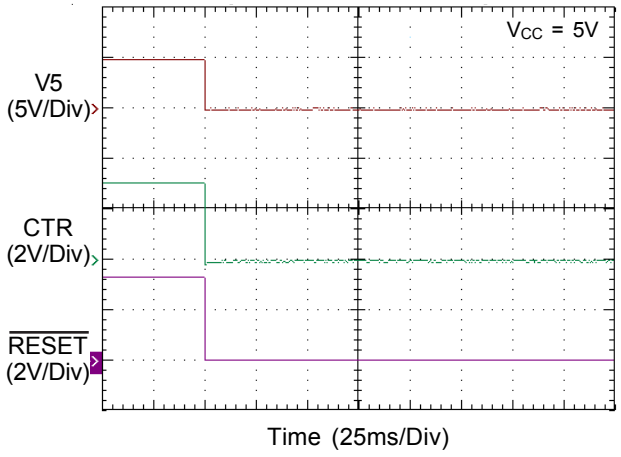




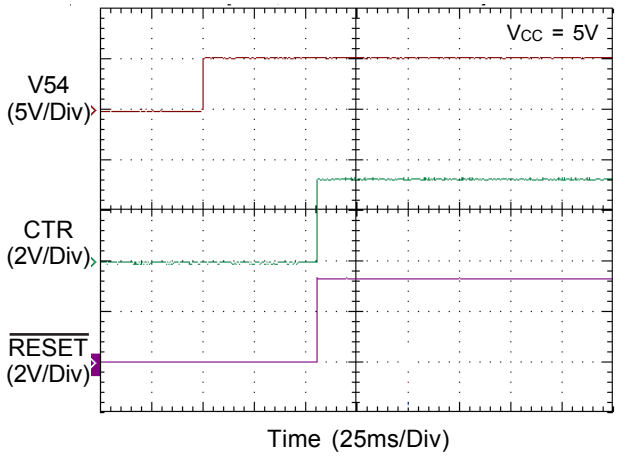
Power On from V5



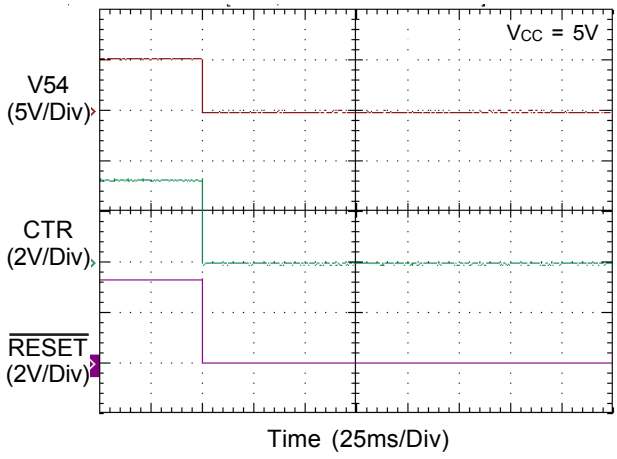
Power Off from V5



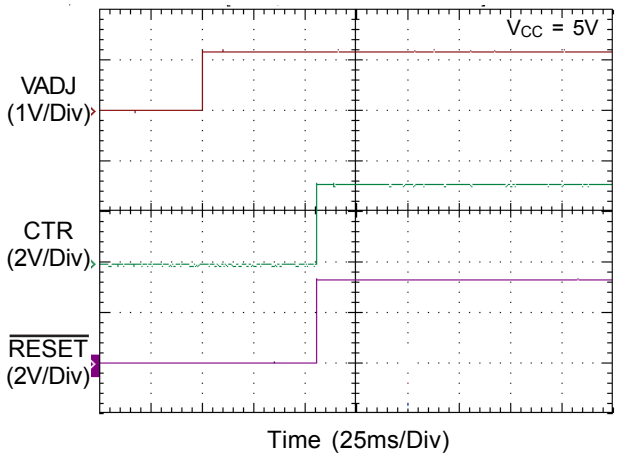
Power On from V54



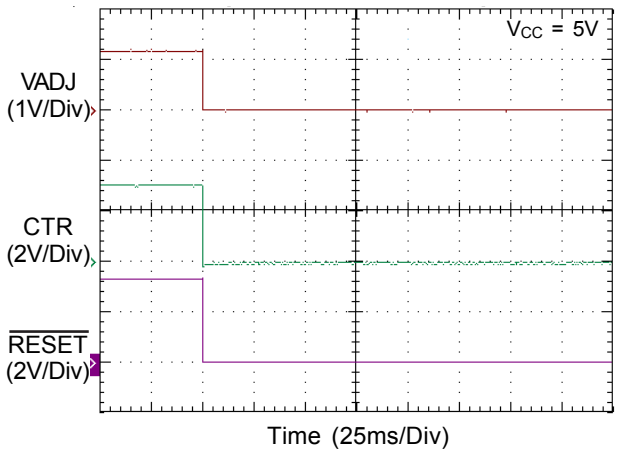
Power Off from V54



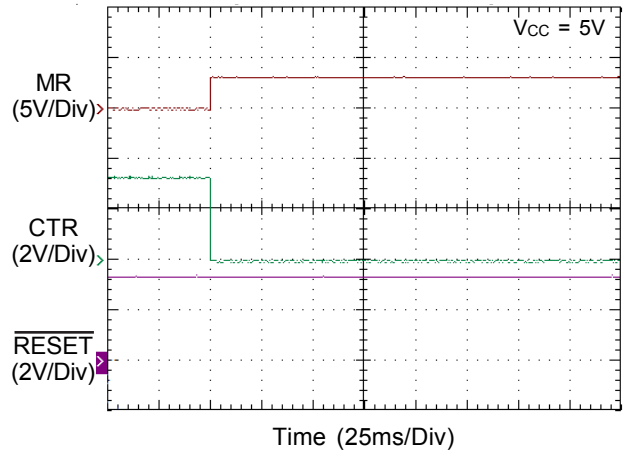
Power On from VADJ



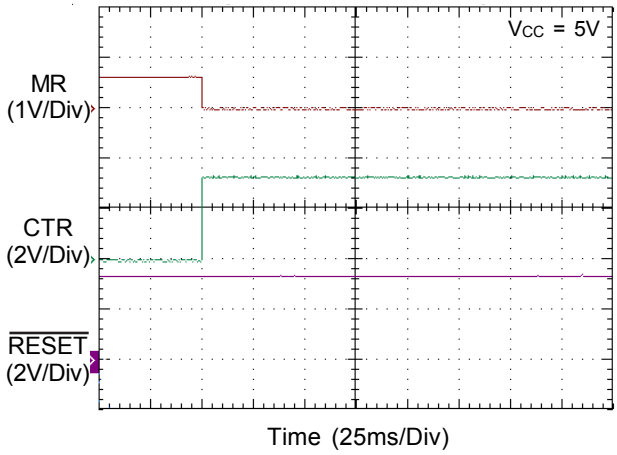
Power Off from VADJ



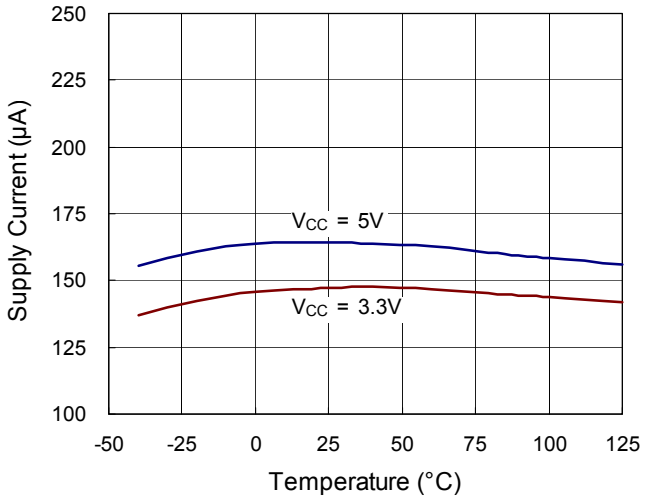
Power On from MR



Power Off from MR



Supply Current vs. Temperature



Application Information

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Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For TSOT-23-8 package, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A= 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (230°C/W) = 0.435W for TSOT-23-8 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 1 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

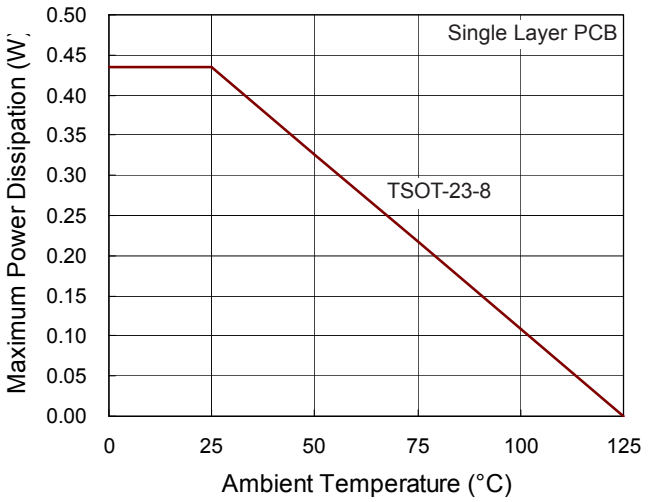

Figure 1. Derating Curve of Maximum Power Dissipation