

RA6T2 Group

MCK-RA6T2 User's Manual

Renesas RA Family RA6 Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas RA Family

MCK-RA6T2 User's Manual

Contents

| | |
|--|----|
| 1. Overview | 4 |
| 1.1 Presupposition and precautions of this document | 4 |
| 2. Product Contents | 5 |
| 3. Product Order Information | 5 |
| 4. Hardware Configuration and Default Setting | 6 |
| 4.1 Hardware configuration | 6 |
| 4.2 Block diagram | 10 |
| 4.3 Board Layout | 11 |
| 4.4 Standoffs and Screws | 12 |
| 4.5 Jumper pin setting | 13 |
| 4.5.1 Inverter Board | 13 |
| 4.5.2 CPU Board | 14 |
| 4.5.3 Communication Board | 16 |
| 4.6 Hardware Setup | 17 |
| 4.6.1 Board Connection | 17 |
| 4.6.2 Power Supply | 18 |
| 5. Inverter Board Specification | 20 |
| 5.1 Functions | 20 |
| 5.1.1 Inverter control circuit block | 20 |
| 5.1.2 Current detection circuit | 21 |
| 5.1.3 Overcurrent detection circuit | 22 |
| 5.1.4 Output voltage detection circuit | 23 |
| 5.1.5 Voltage generation circuit | 23 |
| 5.1.6 LED | 24 |
| 5.1.7 Toggle switch and push switch | 24 |
| 5.1.8 Variable resistor | 24 |
| 5.2 Pin assignment | 25 |
| 5.2.1 CPU board connector | 25 |
| 5.2.2 Hall sensor signal input | 27 |
| 5.2.3 Encoder/Inductive position sensor signal input | 27 |
| 6. CPU Board Specification | 28 |
| 6.1 Functions | 28 |
| 6.1.1 Power supply | 28 |

| | | |
|-------|--|----|
| 6.1.2 | Onboard debugger | 28 |
| 6.1.3 | Inverter board connector | 29 |
| 6.1.4 | Serial communication | 31 |
| 6.1.5 | Reset circuit..... | 31 |
| 6.1.6 | LED..... | 32 |
| 6.1.7 | CAN Communication..... | 32 |
| 6.1.8 | SPI communication | 32 |
| 6.2 | RA6T2 pin function list | 33 |
| 7. | Communication Board Specification | 36 |
| 7.1 | Functions | 36 |
| 7.1.1 | Power supply | 36 |
| 7.1.2 | USB communication..... | 36 |
| 7.1.3 | Serial communication | 36 |
| 8. | Design and Manufacture Information | 37 |
| 9. | Website and Support | 37 |

Figure of contents

| | | |
|-------------|--|----|
| Figure 2-1 | Product contents | 5 |
| Figure 4-1 | MCK-RA6T2 block diagram | 10 |
| Figure 4-2 | Inveter Board..... | 11 |
| Figure 4-3 | CPU Board | 11 |
| Figure 4-4 | Communication board | 12 |
| Figure 4-5 | Standoffs and Screws assembly | 12 |
| Figure 4-6 | Default jumper pin setting | 13 |
| Figure 4-7 | Default jumper pin setting of CPU board | 15 |
| Figure 4-8 | Default jumper pin setting of communication board..... | 16 |
| Figure 4-9 | Board connection | 17 |
| Figure 4-10 | Power supply from DC jack..... | 18 |
| Figure 4-11 | Power supply from terminal block | 18 |
| Figure 4-12 | Power supply from USB connector | 19 |
| Figure 5-1 | Illustration of inverter control circuit block | 20 |
| Figure 5-2 | Current detection circuit | 21 |
| Figure 5-3 | Overcurrent detection circuit | 22 |
| Figure 5-4 | Output voltage detection circuit..... | 23 |
| Figure 6-1 | Connection for CPU board and inverter board..... | 31 |

Table of contents

| | |
|--|----|
| Table 4-1 MCK-RA6T2 specification (1/4)..... | 6 |
| Table 4-2 MCK-RA6T2 specification (2/4)..... | 7 |
| Table 4-3 MCK-RA6T2 specification (3/4)..... | 8 |
| Table 4-4 MCK-RA6T2 specification (4/4)..... | 9 |
| Table 4-5 Jumper pin setting of inverter board..... | 13 |
| Table 4-6 Jumper pin setting of CPU board | 14 |
| Table 4-7 Jumper pin setting of communication board | 16 |
| Table 4-8 Power supply and driving voltage generation | 19 |
| Table 5-1 Voltage generation | 23 |
| Table 5-2 LED..... | 24 |
| Table 5-3 Toggle switch and push switch..... | 24 |
| Table 5-4 Variable resistance specification | 24 |
| Table 5-5 CPU board connector (CN3) | 25 |
| Table 5-6 CPU board connector (CN4) | 26 |
| Table 5-7 Connector for hall sensor signal input (CN6) pin assignment..... | 27 |
| Table 5-8 Pins for encoder/inductive position sensor signal input (CN7) pin assignment | 27 |
| Table 6-1 1st Inverter board connector (CN4) pin assignment | 29 |
| Table 6-2 1st Inverter board connector (CN5) pin assignment | 29 |
| Table 6-3 2nd Inverter board connector (CN7) pin assignment | 30 |
| Table 6-4 2nd Inverter board connector (CN6) pin assignment | 30 |
| Table 6-5 SCI connector (CN10) pin assignment..... | 31 |
| Table 6-6 LED pin assignment | 32 |
| Table 6-7 CAN communication pin assignment (CN8)..... | 32 |
| Table 6-8 SPI communication pin assignment (CN9) | 32 |
| Table 6-9 RA6T2 pin function list | 33 |
| Table 7-1 SCI connector (CN5) pin assignment..... | 36 |
| Table 7-2 SCI connector (CN4) pin assignment..... | 36 |

1. Overview

MCK-RA6T2 is a motor control evaluation kit. By using this product, motor control with RA6T2 can be performed easily.

MCK-RA6T2 has characteristics shown below.

- (1) Supports Brushless DC motor.
- (2) Supports 1-/2-/3-shunt current detection.
- (3) Supports Motor Control Development Support Tool.
- (4) Provides overcurrent protection function using overcurrent detection circuit.

1.1 Presupposition and precautions of this document

1. Experience of using tools: This document assumes that the user has used terminal emulation program of Integrated Development Environment (IDE) such as e2 studio before.
2. Knowledge about the development subject: This document assumes that the user has a basic knowledge to modify the sample project regarding MCU and embedded system.
3. Before using this product, wear an antistatic wrist strap. If you touch this product with static charge on your body, a device failure may occur, or operation may become unstable
4. All screen shots provided in this document is for reference. Actual screen displays may differ depending on the software and development tool version which you use.

2. Product Contents

This kit consists of the following parts.

1. Inverter Board (RTK0EM0000B12020BJ) x1
2. CPU Board (RTK0EMA270C00000BJ) x1
3. Communication Board (RTK0EMXC90Z00000BJ) x1
4. Brushless DC Motor (R42BLD30L3) x1
5. Communication Cable x1
6. USB Cable x2
7. Screw x12
8. Standoff x12

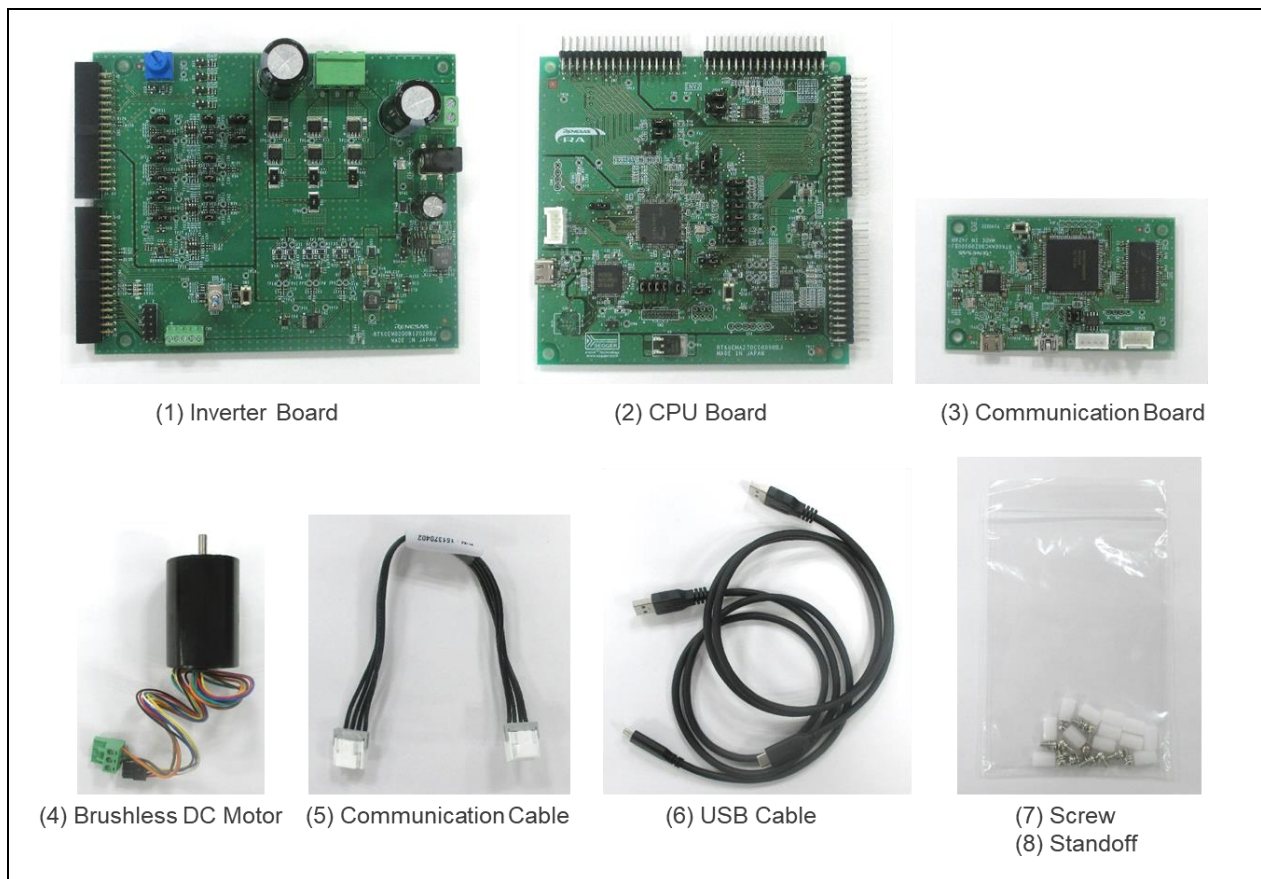


Figure 2-1 Product contents

3. Product Order Information

Product number to order MCK-RA6T2 : RTK0EMA270S00020BJ

4. Hardware Configuration and Default Setting

4.1 Hardware configuration

MCK-RA6T2 consists of the inverter board, the CPU board and the communication board. Specifications as a kit and for the relevant boards are listed below.

Table 4-1 MCK-RA6T2 specification (1/4)



| Item | Specification | |
|-----------------------|---|---|
| Kit product name | MCK-RA6T2 | |
| Kit product No. | RTK0EMA270S00020BJ | |
| Kit configuration | Inverter Board | RTK0EM0000B12020BJ |
| | CPU Board | RTK0EMA270C00000BJ |
| | Communication Board | RTK0EMXC90Z00000BJ |
| | Brushless DC Motor | R42BLD30L3 (MOONS') Rated voltage : 36[V] Rated current : 1.67[A] |
| Isolation | Inverter board - CPU board : Non-isolated Communication board - CPU board : Isolated | |
| External view |  <p style="text-align: center;">Note: The actual product may differ from this photo.</p> | |
| Board size | Inverter board : 133 mm (W) x 109 mm (L) CPU board : 109 mm (W) x 109 mm (L) Communication board : 89 mm (W) x 52 mm (L) | |
| Operating temperature | Room temperature | |
| Operating humidity | No condensation allowed | |
| EMC Directive | Europe : EN61326-1 : 2013 Class A | |

Table 4-2 MCK-RA6T2 specification (2/4)

| Item | Specification |
|---|--|
| Product name | Inverter board |
| Board part No. | RTK0EM0000B12020BJ |
| External view |  <p>Note: The actual product may differ from this photo.</p> |
| Power supply | 2 ways <ul style="list-style-type: none"> • From DC jack or Power supply connector (DC 12~48V) *1 • From CPU board (DC 5V) |
| Rated output current | AC 10 A (RMS value) *2 |
| Switching frequency | 20 kHz (typical) |
| Current detection method | 1- / 2- / 3-shunt detection |
| Shunt resistor | 10 mohm |
| PWM logic | Lower arm, Upper arm : Positive logic |
| DC bus voltage detection (bus voltage detection) | Detection by resistance division (0 V ~ 48 V) |
| 3-phase output voltage detection | Detection by resistance division (0 V ~ 48 V) |
| 3-phase output current detection | With shunt resistor (-16.5 A ~ +16.5 A) |
| Overcurrent detection function | 21.4 A |
| Supporting sensor | HALL sensor, Encoder |
| Connector | <ul style="list-style-type: none"> • CPU card connector • Motor connector • Power input connector • HALL sensor connector • Encoder/Inductive position sensor connector |
| Switch | <ul style="list-style-type: none"> • Toggle switch x1 • Push switch x1 |
| LED | <ul style="list-style-type: none"> • LED x3 • Power LED |

*1 The polarity of the DC jack (J1) is center positive. The compatible plug has an inner diameter of 2.1 mm and an outer diameter of 5.5 mm.

*2 It is strongly recommended to attach a heat sink to the MOSFET when using over 5A.

Table 4-3 MCK-RA6T2 specification (3/4)

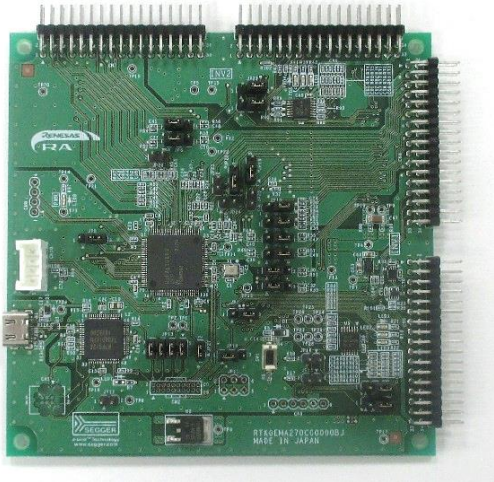
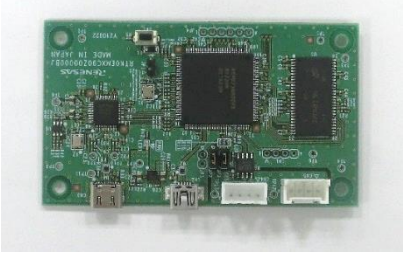
| item | | Specification |
|---------------------------|---------------------------------|---|
| Product name | | CPU Board |
| Board part No. | | RTK0EMA270C00000BJ |
| Compatible inverter board | | RTK0EM0000B12020BJ |
| External view | |  <p>Note: The actual product may differ from this photo.</p> |
| Mounted MCU | Product group | RA6T2 group |
| | Product No. | R7FA6T2BD3CFP |
| | CPU maximum operating frequency | 240MHz |
| | Bit count | 32 bit |
| | Package / Pin number | LFQFP / 100 pin |
| | RAM | 64K byte |
| MCU input clock | | 10MHz (Generate with external crystal oscillator) |
| Power supply | | DC 5V Select one way automatically from the below <ul style="list-style-type: none"> • Power is supplied from compatible inverter board • Power is supplied from USB connector |
| Debugger | | J-Link-OB (Onboard debugger circuit) |
| Connector | | <ul style="list-style-type: none"> • Inverter board connector (2 sets) • USB connector for J-Link OB • SCI connector for Renesas Motor Workbench communication • Through hole for CAN communication • Through hole for SPI communication • 20 pin through hole for Arm debugger |
| Switch | | MCU reset switch |
| LED | | User-controllable LED x6, Power LED x1 |

Table 4-4 MCK-RA6T2 specification (4/4)

| item | | Specification |
|-----------------|---------------------------------|---|
| Product name | | Communication Board |
| Board part No. | | RTK0EMXC90Z00000BJ |
| External view | |  <p>Note: The actual product may differ from this photo.</p> |
| Mounted MCU | Product group | RX72N group |
| | Product No. | R5F572NNDDFB |
| | CPU maximum operating frequency | 240MHz |
| | Bit count | 32 bit |
| | Package / Pin number | LFQFP / 144 pin |
| | RAM | 1M byte |
| MCU input clock | | 20MHz (Generate with external crystal oscillator) |
| Power supply | | DC 5V <ul style="list-style-type: none"> Power is supplied from USB connector |
| Connector | | <ul style="list-style-type: none"> USB Type-C connector for PC SCI connector for CPU board USB miniB connector (not available for users) |
| Isolation | | <ul style="list-style-type: none"> Between SCI connector and MCU Isolation device Si8622BC-B-IS (Skyworks Solutions Inc.) or ISO7421FED (Texas Instruments) |
| Switch | | MCU external reset switch |

4.2 Block diagram

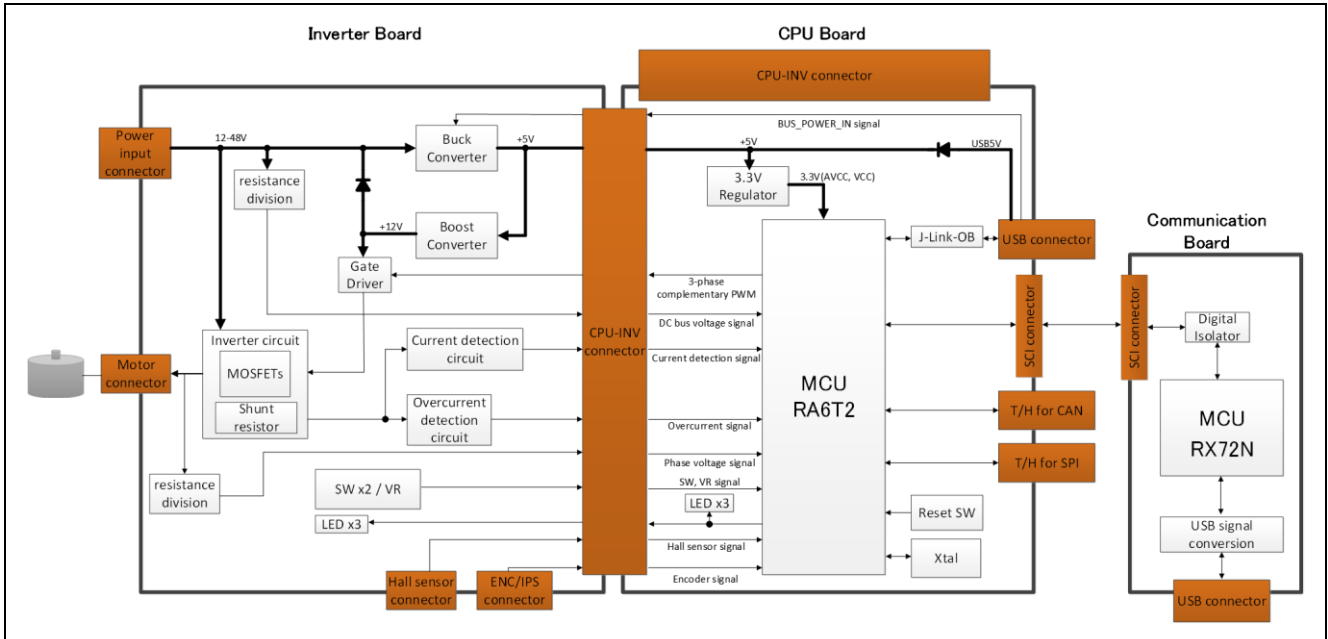


Figure 4-1 MCK-RA6T2 block diagram

4.3 Board Layout

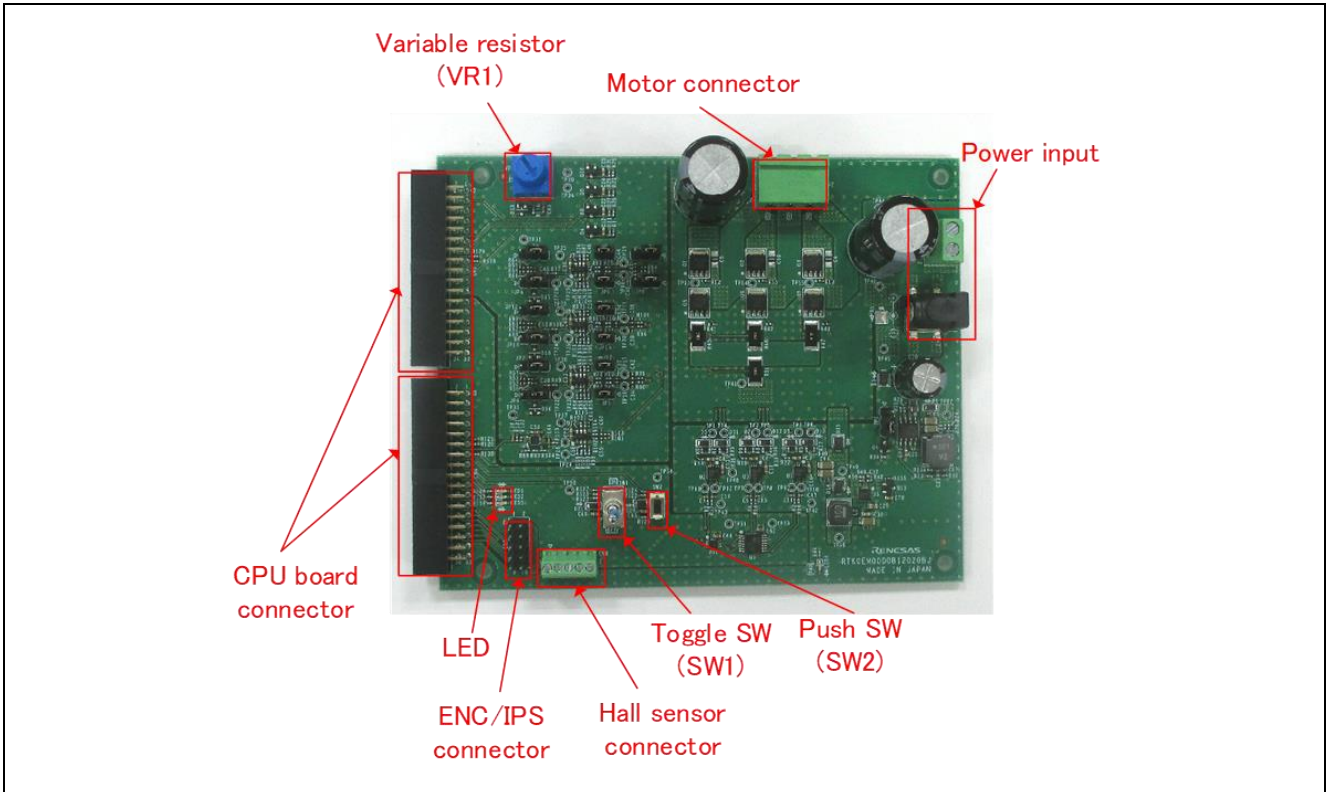


Figure 4-2 Inverter Board

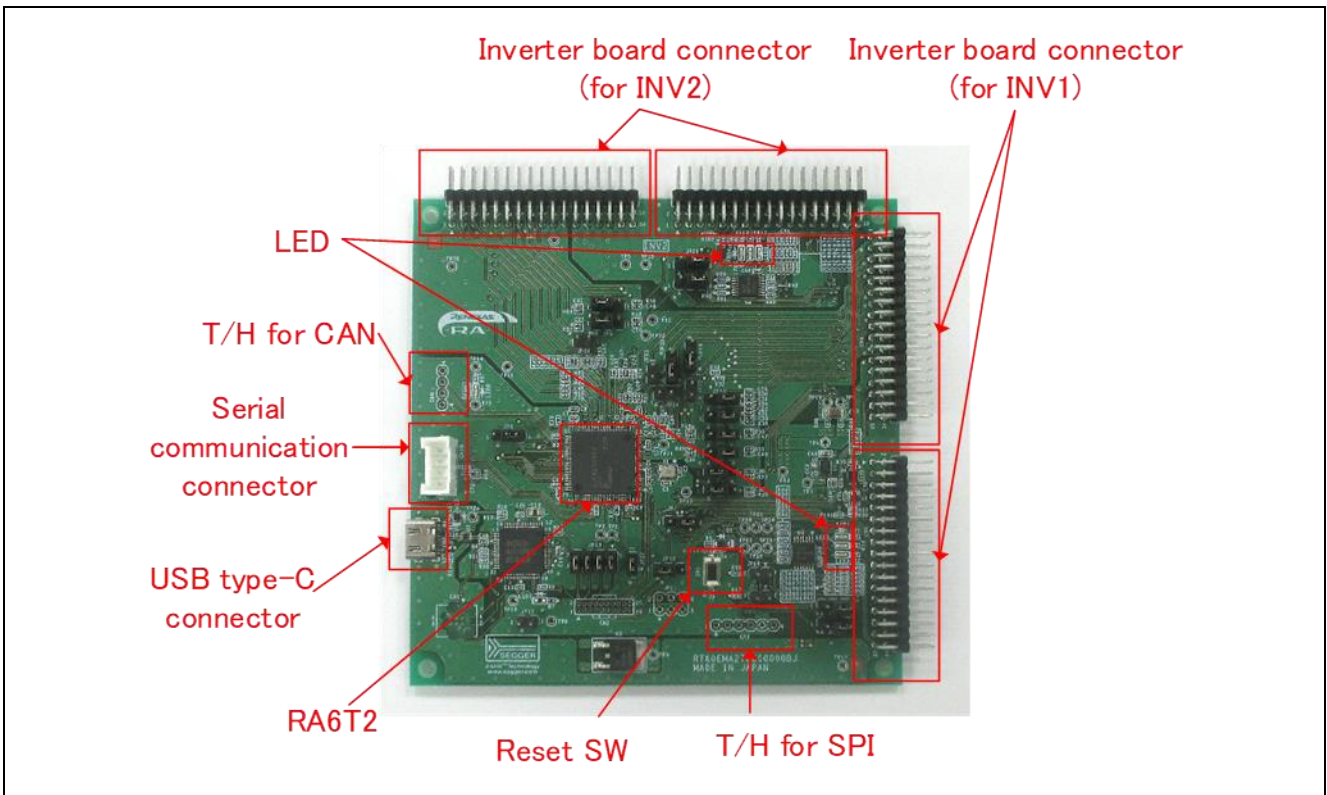


Figure 4-3 CPU Board

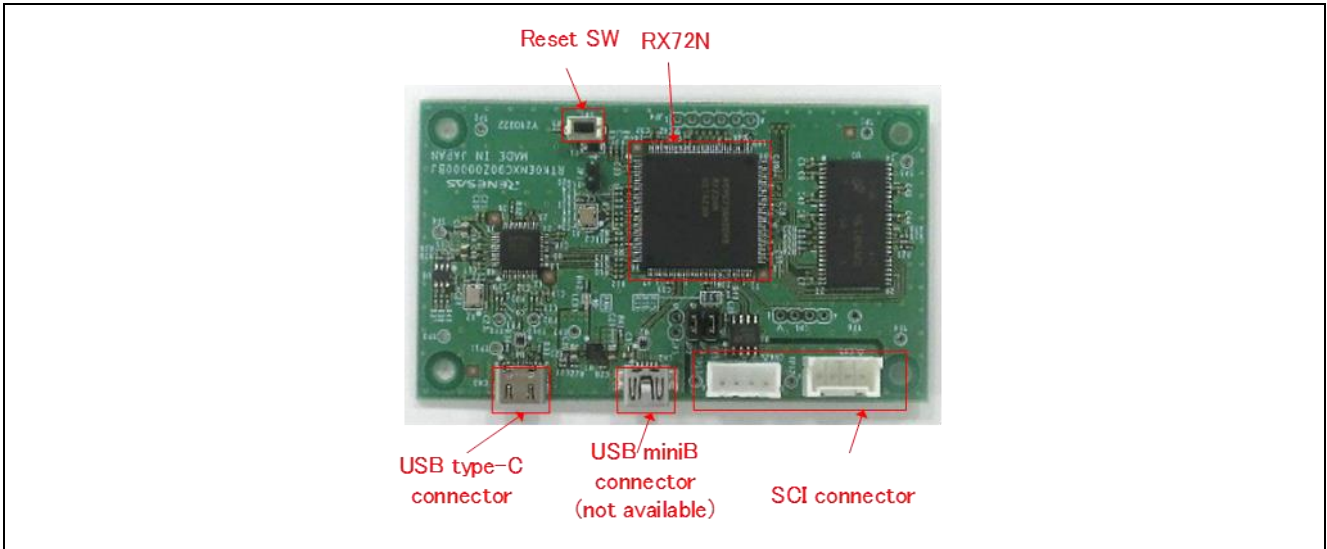


Figure 4-4 Communication board

4.4 Standoffs and Screws

Before using this product, assemble the included standoffs and screws as shown below.

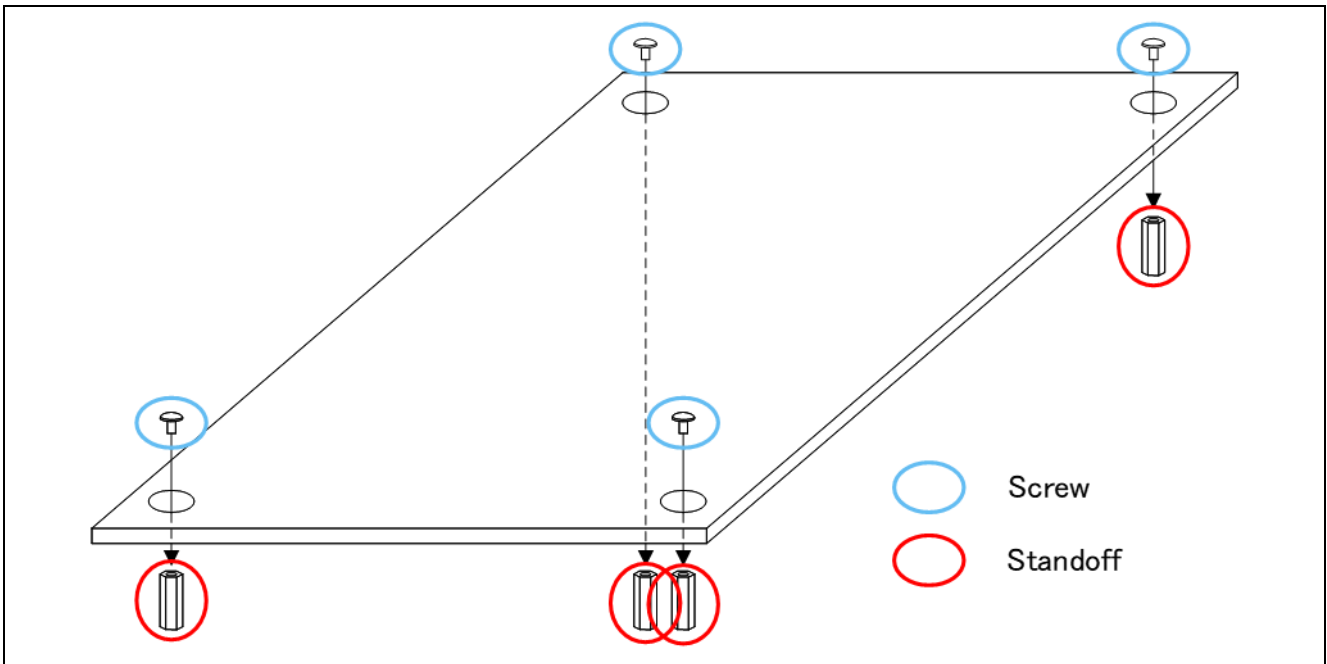


Figure 4-5 Standoffs and Screws assembly

4.5 Jumper pin setting

4.5.1 Inverter Board

Default settings and functions of the jumper pins (JP1~JP15) are as follows.

Table 4-5 Jumper pin setting of inverter board

| Jumper pin | Default setting | Function |
|---------------------------------|-----------------|---|
| JP1 | 2-3pin short | 1-2pin short : Disable 5V regulator 2-3pin short : Enable 5V regulator |
| JP2, JP3, JP4, JP6, JP12, JP13 | 2-3pin short | 1-2pin short : Disable current detection amplifiers 2-3pin short : Enable current detection amplifiers |
| JP5, JP7, JP9, JP10, JP14, JP15 | 1-2pin short | 1-2pin short : Current detection amplifier gain = 20 1-2pin open : Current detection amplifier gain = 10 |
| JP8, JP11 | 1-2pin short | 1-2pin short : 2-/3-shunt current detection 2-3pin short : 1-shunt current detection |

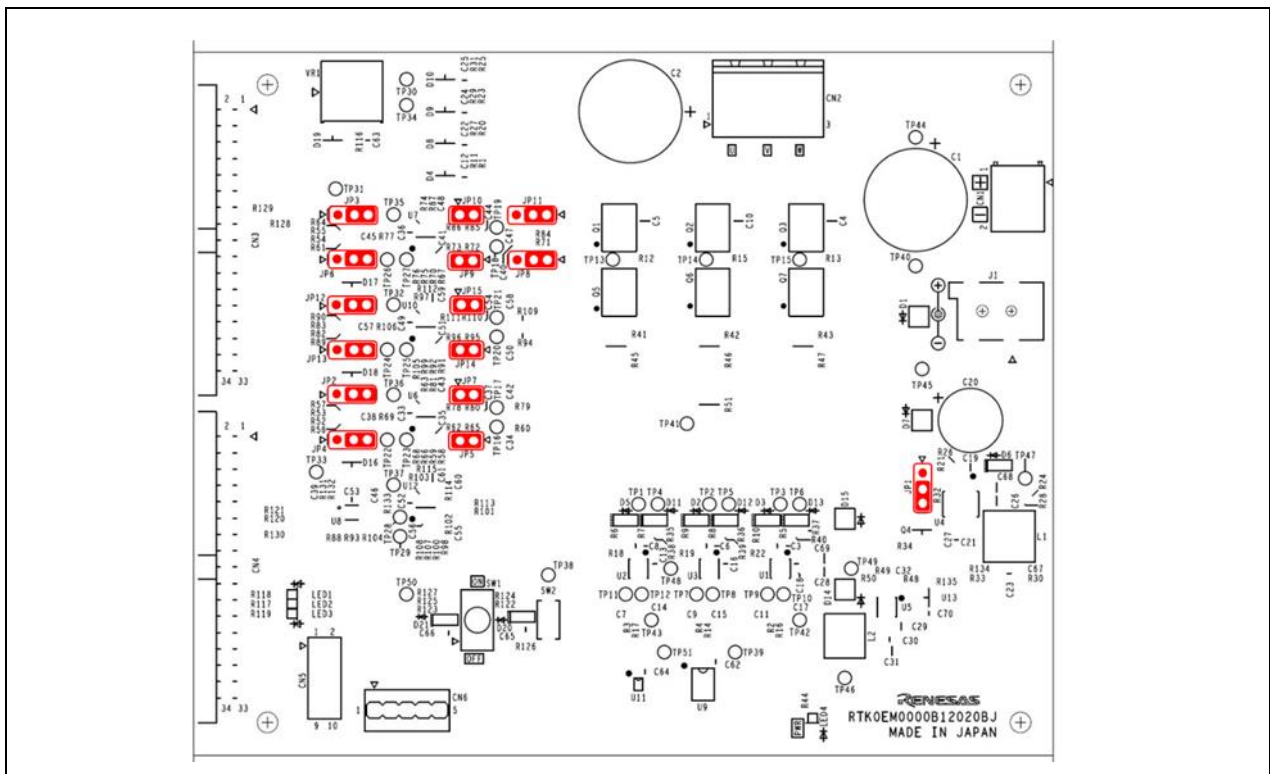


Figure 4-6 Default jumper pin setting

4.5.2 CPU Board

Default settings and functions of the jumper pins (JP1~JP25) are as follows.

Table 4-6 Jumper pin setting of CPU board

| Jumper pin | Default setting | Function |
|------------------|--|---|
| JP1 | 2-3pin short | 1-2pin short : INV1 IPS CSN_IRQN 2-3pin short : INV1 Encoder Z |
| JP2 | 2-3pin short | 1-2pin short : INV2 PFC current detection (for HV INV) 2-3pin short : INV2 IPS A |
| JP3 | 2-3pin short | 1-2pin short : INV2 AC input voltage detection (for HV INV) 2-3pin short : INV2 IPS A#/Encoder A# |
| JP4 | 1-2pin short | 1-2pin short : INV1 HALL U 2-3pin short : INV1 IPS A |
| JP5 | 1-2pin short | 1-2pin short : INV1 HALL V 2-3pin short : INV1 IPS A#/Encoder A# |
| JP6 | 1-2pin short | 1-2pin short : INV2 V-phase voltage detection 2-3pin short : INV2 IPS B |
| JP7 | 2-3pin short | 1-2pin short : INV1 PFC current detection (for HV INV) 2-3pin short : INV1 IPS B# |
| JP8 | 2-3pin short | 1-2pin short : INV2 IPS CSN_IRQN 2-3pin short : INV2 Encoder Z |
| JP9 | 1-2pin short | 1-2pin short : INV2 W-phase voltage detection 2-3pin short : INV2 IPS B#/Encoder B# |
| JP10 | 2-3pin short | 1-2pin short : INV1 AC input voltage detection (for HV INV) 2-3pin short : INV1 IPS B#/Encoder B# |
| JP11 | 1-2pin open 3-4pin open 5-6pin open | |
| JP12 | 1-2pin open | 1-2pin short : Disable J-Link OB 1-2pin open : Enable J-Link OB |
| JP13 | 1-2pin short 3-4pin short 5-6pin short 7-8pin short | |
| JP14 | 1-2pin short | 1-2pin short : Enable RA6T2 2-3pin short : Disable RA6T2 |
| JP15, JP16 | 1-2pin open | 1-2pin short : Enable pull-up for I2C 1-2pin open : Disable pull-up for I2C |
| JP17 | 2-3pin short | 1-2pin short : INV1 IPS A 2-3pin short : INV1 Encoder A |
| JP18 | 2-3pin short | 1-2pin short : INV1 IPS B 2-3pin short : INV1 Encoder B |
| JP19 | 1-2pin short | 1-2pin short : INV1 W-phase voltage detection 2-3pin short : INV1 W-phase current detection (PGAVSS) |
| JP20 | 1-2pin short | 1-2pin short : INV1 V-phase voltage detection 2-3pin short : INV1 V-phase current detection (PGAVSS) |
| JP21 | 2-3pin short | 1-2pin short : INV2 IPS A 2-3pin short : INV2 Encoder A |
| JP22 | 2-3pin short | 1-2pin short : INV2 IPS B 2-3pin short : INV2 Encoder B |
| JP23, JP24, JP25 | 1-2pin open | 1-2pin open : Enable LPF for current sensing 1-2pin short : Disable LPF for current sensing |

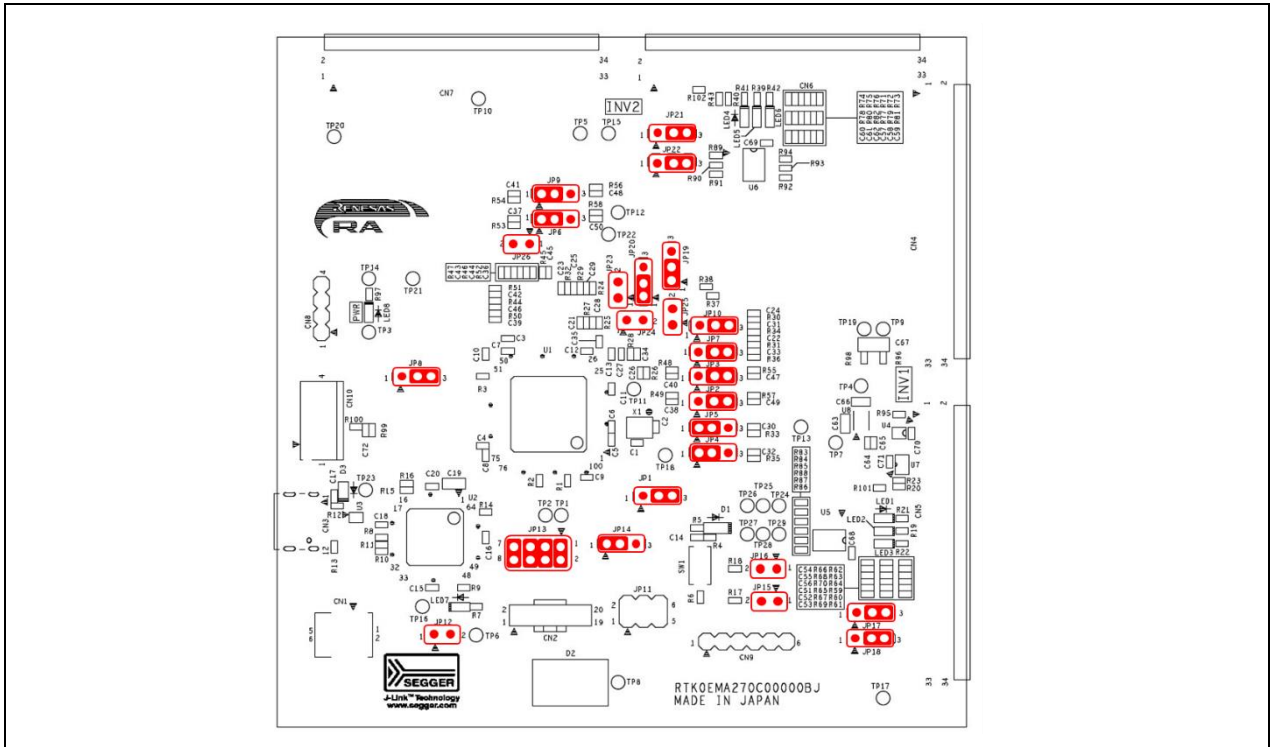


Figure 4-7 Default jumper pin setting of CPU board

4.5.3 Communication Board

Default settings and functions of the jumper pins (JP1~JP3) are as follows.

Table 4-7 Jumper pin setting of communication board

| Jumper pin | Default setting | Function |
|------------|-----------------|---|
| JP1 | 1-2pin open | 1-2pin short : Enable pull-up for MD port (Not available) 1-2pin open : Enable pull-up for MD port |
| JP2 | 1-2pin short | 1-2pin short : Disable pull-up for GPIO(PC6) 1-2pin open : Enable pull-up for GPIO(PC6) |
| JP3 | 1-2pin short | 1-2pin short : Disable pull-up for GPIO(PC5) 1-2pin open : Enable pull-up for GPIO(PC5) |

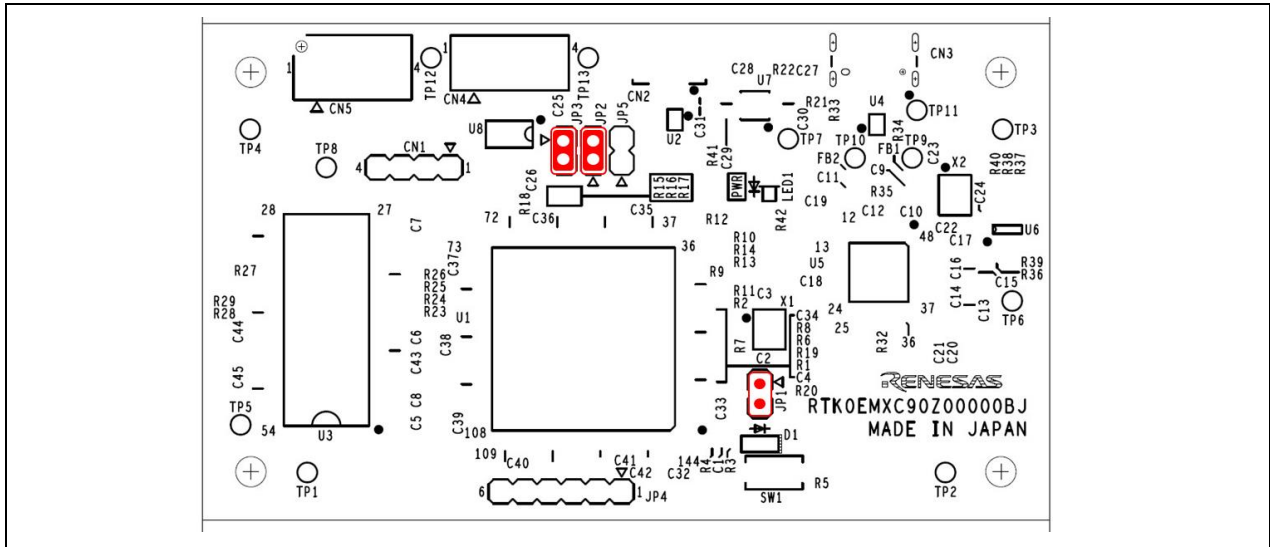


Figure 4-8 Default jumper pin setting of communication board

4.6 Hardware Setup

4.6.1 Board Connection

When using this product for motor control evaluation, connect the boards as shown in Figure 4-9. Note that the connector between the CPU board and the inverter board is a tight fit, so be careful not to bend the pins when connecting or disconnecting.

Please refer to 4.6.2 for the power supply method. In Figure 4-9, the power is supplied from the AC adapter. The RA6T2 CPU board supports a maximum of two-motor control and can be connected as shown in Fig. 6.1 shown later, if you prepare an additional inverter board and motor.

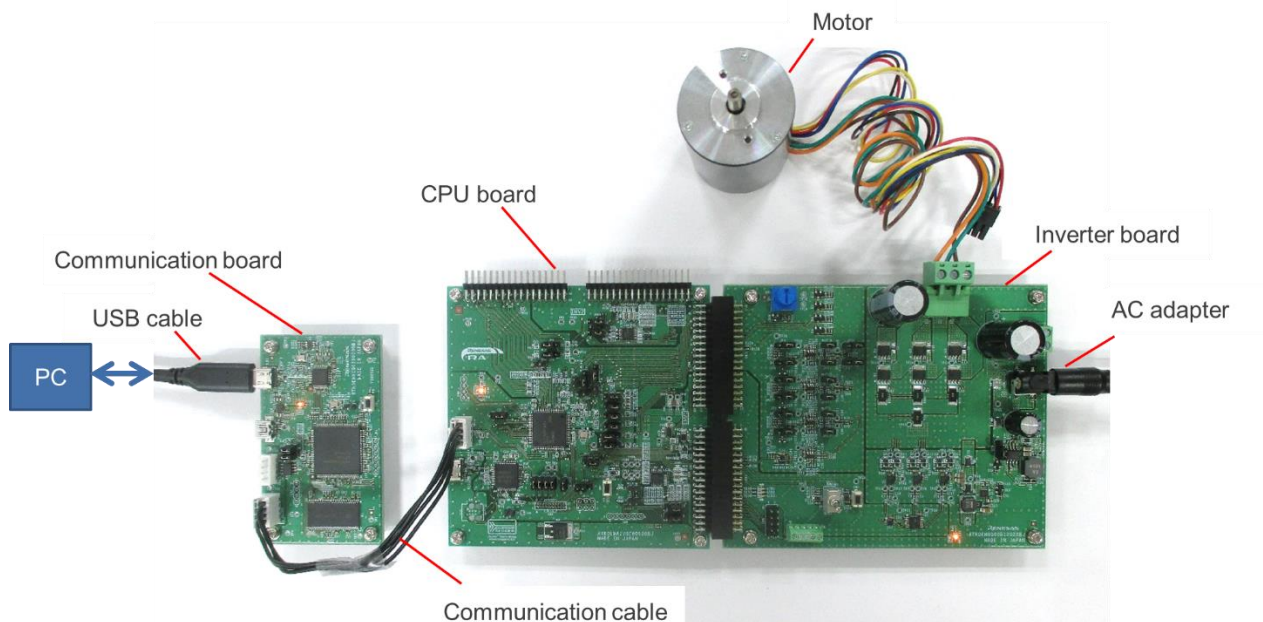


Figure 4-9 Board connection

4.6.2 Power Supply

There are three ways to supply power to the CPU board and inverter board, and the power supply for the communication board is independent of the CPU board and inverter board and is supplied at 5V from the USB connector.

(1) From DC jack

Use an AC adapter or something similar to supply power from the DC jack (J1) on the inverter board. The compatible plug has an outer diameter of 5.5 mm, an inner diameter of 2.1 mm, and a polarity of center positive. The input voltage range is 12 to 48V.

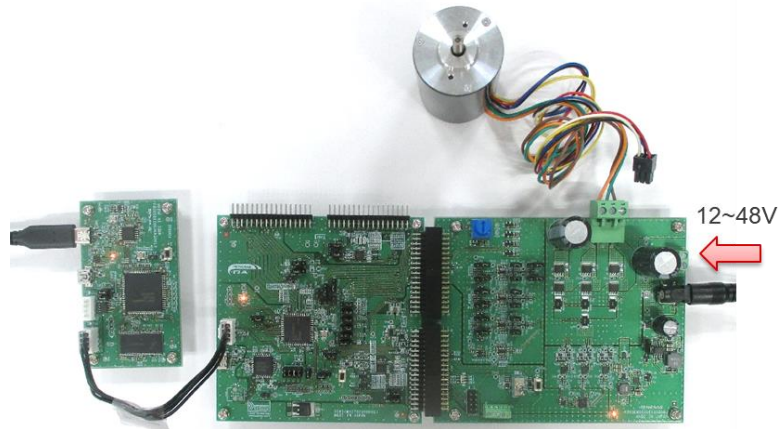


Figure 4-10 Power supply from DC jack

(2) From terminal block

Supply power from the terminal block (CN1) of the inverter board using a DC stabilized power supply or the like. The polarity should follow the silk indication (“+”, “-”) on the board. The input voltage range is 12 to 48V.

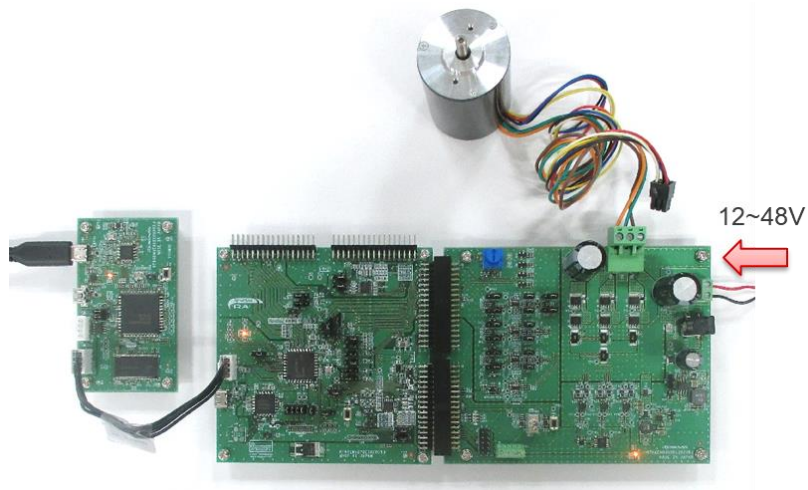


Figure 4-11 Power supply from terminal block

(3) From USB connector

5V power is supplied from the USB connector (Type-C) on the CPU board. Use a USB adapter capable of outputting 1A or more so that the motor can be driven sufficiently.

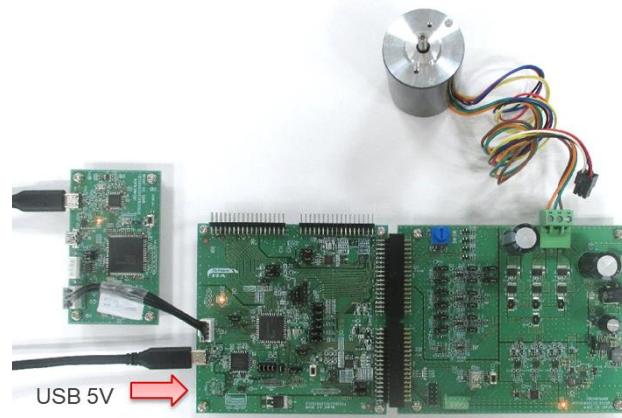


Figure 4-12 Power supply from USB connector

It is also possible to supply power from the USB connector on the CPU board and the DC jack or terminal block on the inverter board at the same time. In this case, the MCU drive voltage of 3.3V and the gate driver drive voltage are generated from the USB supply of 5V, while the motor drive voltage is supplied from the DC jack or terminal block. Please refer to Table 4-8 for the power supply conditions and each voltage generation.

Table 4-8 Power supply and driving voltage generation

| | | | Case 1 | Case 2 | Case 3 |
|------------------------|----------------|-------------------------------|--------|--------|--------|
| Power supply condition | CPU board | USB 5V *1 | ✓ | - | ✓ |
| | Inverter board | External power (12~48V) *2 | - | ✓ | ✓ |
| Power source for | CPU board | I/O (VCC, 3.3V) | [A] | [B] | [A] |
| | | BUS (5V) | [A] | [B] | [A] |
| | Inverter board | I/O (VCC, 3.3V) | [A] | [B] | [A] |
| | | BUS (5V) | [A] | [B] | [A] |
| | | Gate driver (11.4V) | [A] | [B] | [A] |
| | | Motor drive (11.4V or 12~48V) | [A] | [B] | [B] |

Power supply condition:

- ✓: supplied
- : not supplied

Driving voltage generation

- [A]: generated from USB 5V on CPU board
- [B]: generated from external power on inverter board

*1 Motor drive current of 1 A or more may be required for each inverter board.

*2 When connecting two inverter boards to the CPU board and also inputting an external power supply to INV2, it is necessary to supply an external power supply (which can be different from INV2) to INV1 as well, or to supply USB 5V to the CPU board.

5. Inverter Board Specification

This section describes inverter board specification.

5.1 Functions

5.1.1 Inverter control circuit block

The inverter board has the inverter control circuit block which controls the motor with 6 POWER MOSFETs. POWER MOSFET is controlled with 6-phase timer output of MCU.

The inverter control circuit block outputs DC bus voltage, U, V and W phase voltage and shunt current to the connectors (CN3, CN4). By inputting these output voltages to A/D of MCU on the CPU card, analog values of the voltage and the shunt current of each phase can be measured. Refer to 5.1.2 and 5.1.4 for the current detection and the voltage detection, respectively. Also function to detect overcurrent from the input current is available. Refer to 5.1.3 for details.

An illustration of the inverter control circuit block is shown in Figure 5-1. In the actual circuit, some inputs on the A/D pins are via voltage dividers and offsets and so on. Refer to the circuit diagram for details.

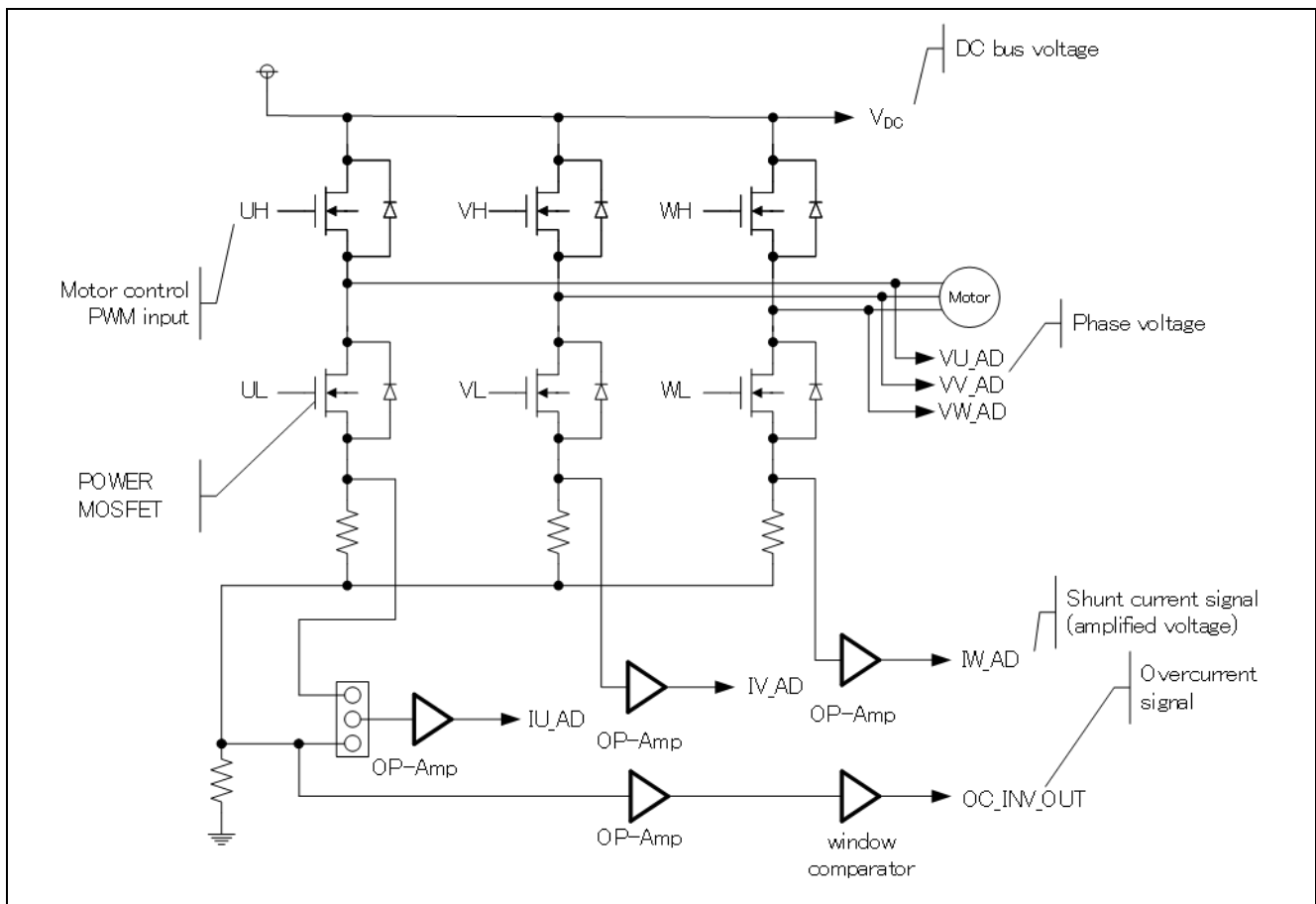


Figure 5-1 Illustration of inverter control circuit block

5.1.2 Current detection circuit

The inverter board has the current detection circuit to measure the current at the U, V and W phase. The current detection circuit uses shunt resistor at each phase. Voltage drop caused by the current flowing through the shunt resistor is amplified by the current detection amplifier to output. The default gain of the current detection amplifier is set to 20x, but the gain can be changed to 10x by setting JP5, JP7, JP9, JP10, JP14, and JP15 to open. The relationship between the current I_{in} flowing through the shunt resistor and the voltage V_{out} output from the current detection circuit is shown in equations (1) and (2). In addition, by switching JP8 and JP11 to 2-3 pin short circuit, one shunt current detection can be supported.

$$\text{Amplifier gain } 10x : V_{out}[V] = I_{in}[A] \times R_s[\Omega] \times 10 + AVCC/2 \quad (1)$$

$$\text{Amplifier gain } 20x : V_{out}[V] = I_{in}[A] \times R_s[\Omega] \times 20 + AVCC/2 \quad (2)$$

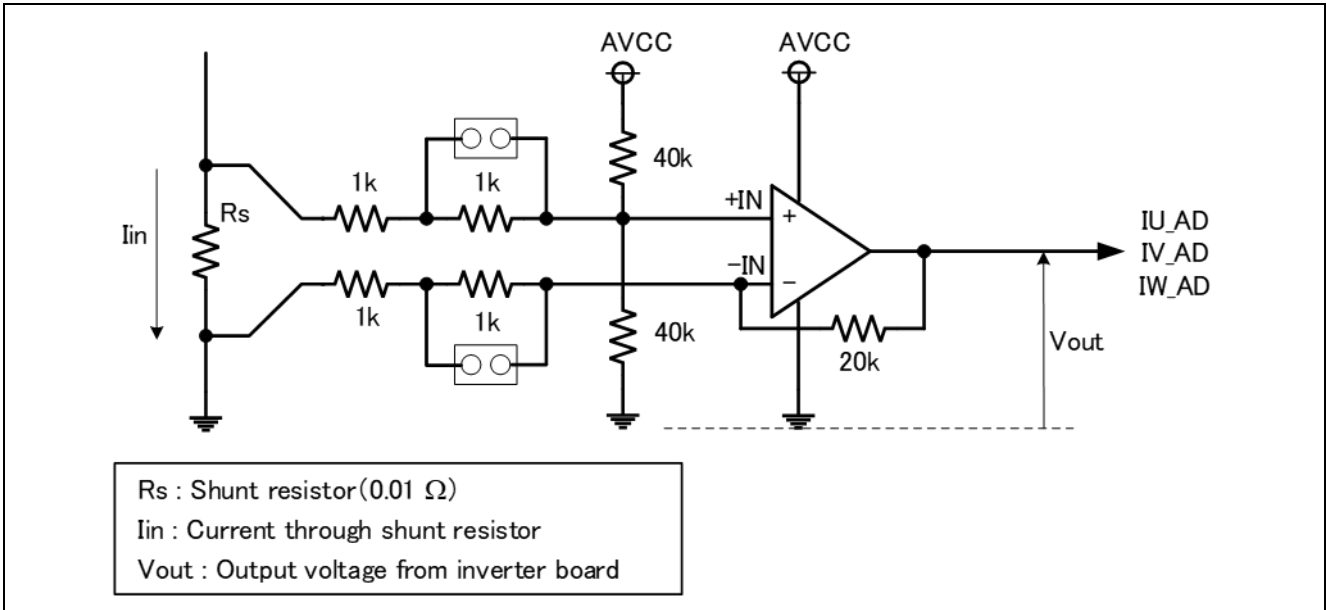


Figure 5-2 Current detection circuit

5.1.3 Overcurrent detection circuit

Detect the overcurrent from the input current, using the overcurrent detection circuit illustrated in Figure 5-3. If the current value is within the range of threshold, OC_INV_OUT is HIGH, and this changes to LOW if overcurrent is detected. Therefore, you can protect the board and motor by monitoring the over current detection signal and setting PWM signals for gate driver to LOW or Hi-Z if the over current detection signal changes to LOW.

The overcurrent detection circuit does not directly protect the board and motor. Protect them by performing appropriate processing with equipment such as microcontroller.

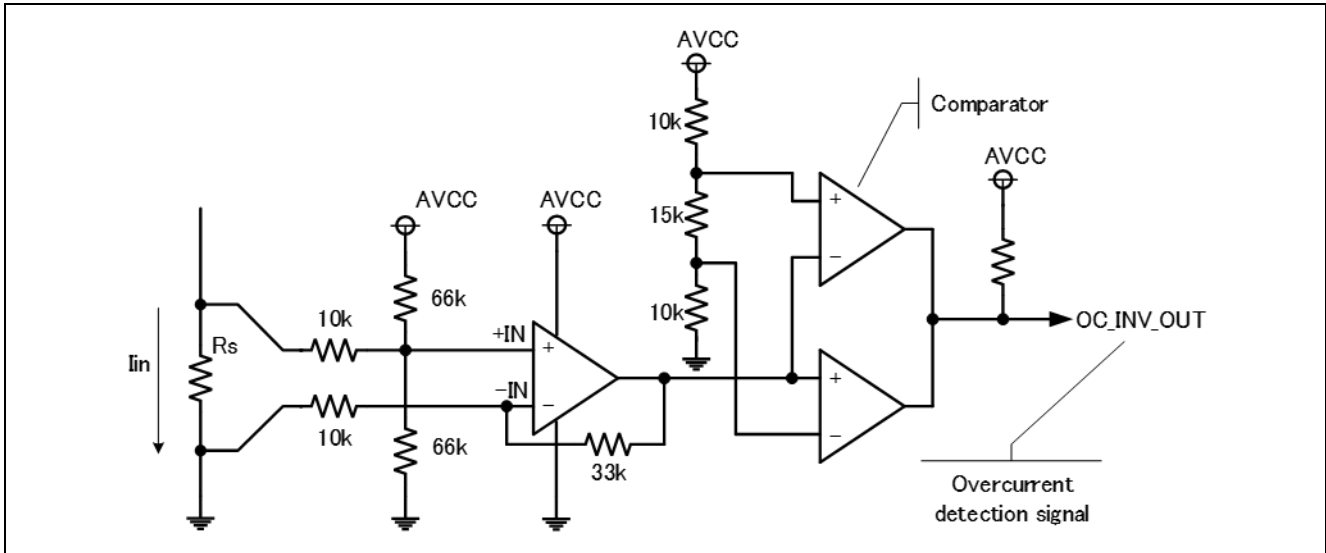


Figure 5-3 Overcurrent detection circuit

5.1.4 Output voltage detection circuit

The INV-BRD has the circuit that inputs bus voltage and three-phase output voltage (U, V and W phase) into the AD pin of the microcontroller through resistive voltage divider. Relation between the three-phase output voltage, the bus voltage and the detection voltage is described by the below equation (3).

$$V_{out}[V] = \frac{470}{10 \times 10^3 + 470} \times V_{in}[V] \quad (3)$$

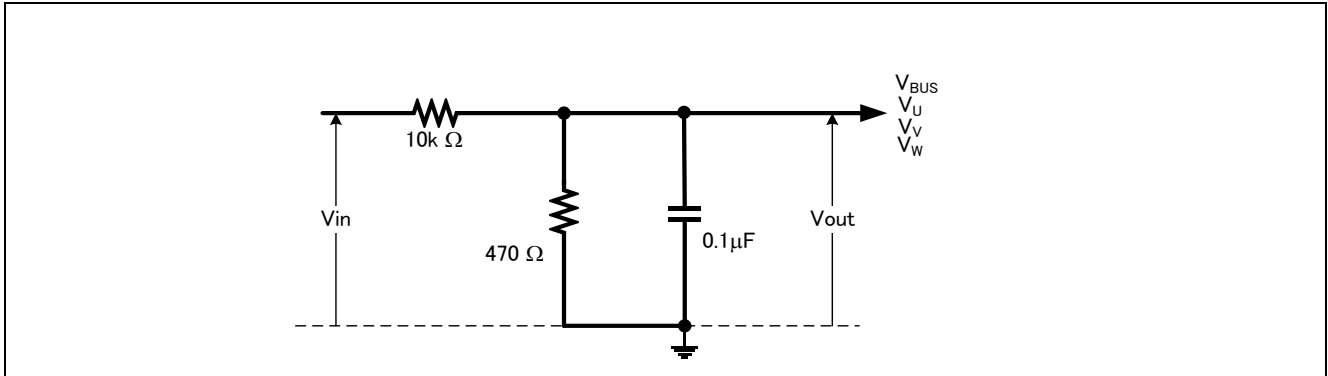


Figure 5-4 Output voltage detection circuit

5.1.5 Voltage generation circuit

On the INV-BRD, the gate driver voltage (" +12V" in the schematic) is generated from the 5V power supply (" +5V" in the schematic) with the boost converter. If 5V is not supplied from the CPU board, the buck converter on the INV-BRD generates 5V from the voltage input (12 to 48V) from the DC jack or terminal block.

Table 5-1 Voltage generation

| Item | Input voltage [V] | Output voltage (TYP.) [V] | Output current (Max) [A] |
|--------------------------------|-------------------|---------------------------|--------------------------|
| 5V generation | 12~48 | 5 | 0.6 |
| Gate driver voltage generation | 5 | 11.4 | - |

5.1.6 LED

The INV-BRD has three LEDs which the user can control. The LED ON/OFF is controlled by the pin state.

Table 5-2 LED

| Connector pin | | LED1 | LED2 | LED3 |
|---------------|------|------|------|------|
| CN4-18 | HIGH | OFF | - | - |
| | LOW | ON | - | - |
| CN4-19 | HIGH | - | OFF | - |
| | LOW | - | ON | - |
| CN4-20 | HIGH | - | - | OFF |
| | LOW | - | - | ON |

5.1.7 Toggle switch and push switch

The INV-BRD has toggle switch (SW1) and push switch (SW2). The pin voltage is controlled by the state of them.

Table 5-3 Toggle switch and push switch

| Connector pin | | SW1 | SW2 |
|---------------|------|-----|---------|
| CN4-16 | HIGH | ON | - |
| | LOW | OFF | - |
| CN4-17 | HIGH | - | RELEASE |
| | LOW | - | PUSH |

5.1.8 Variable resistor

The INV-BRD has a variable resistor (VR1). If turning the variable resistor clockwise, terminal voltage of the variable resistor (CN3-17) becomes low. If turning it counterclockwise, the voltage becomes high.

Table 5-4 Variable resistance specification

| Item | Specification |
|-------------------------|----------------|
| Input voltage range | 0~AVCC |
| Variable resistor range | 0~10k Ω |

5.2 Pin assignment

5.2.1 CPU board connector

Table 5-5 CPU board connector (CN3)

| Pin No. | Output direction | Signal |
|---------|------------------|------------------------------------|
| 1 | - | SPARE1 |
| 2 | - | AGND |
| 3 | To CPU | DC bus voltage detection |
| 4 | - | AGND |
| 5 | To CPU | U-phase current detection |
| 6 | To CPU | U-phase current detection (PGAVSS) |
| 7 | To CPU | V-phase current detection |
| 8 | To CPU | V-phase current detection (PGAVSS) |
| 9 | To CPU | W-phase current detection |
| 10 | To CPU | W-phase current detection (PGAVSS) |
| 11 | To CPU | U-phase voltage detection |
| 12 | To CPU | V-phase voltage detection |
| 13 | To CPU | W-phase voltage detection |
| 14 | - | AGND |
| 15 | To CPU | VPFC_AD |
| 16 | To CPU | IPFC_AD |
| 17 | To CPU | VR1 |
| 18 | - | AGND |
| 19 | - | AVCC |
| 20 | - | AVCC |
| 21 | - | AGND |
| 22 | - | AGND |
| 23 | - | VCC |
| 24 | - | VCC |
| 25 | - | DGND |
| 26 | - | DGND |
| 27 | To INV | PWM U-phase (Lower) |
| 28 | - | DGND |
| 29 | To INV | PWM U-phase (Upper) |
| 30 | - | DGND |
| 31 | To INV | PWM V-phase (Lower) |
| 32 | - | DGND |
| 33 | To INV | PWM V-phase (Upper) |
| 34 | - | DGND |

Table 5-6 CPU board connector (CN4)

| Pin No. | Output direction | Signal |
|---------|------------------|---------------------------------|
| 1 | To INV | PWM W-phase (Lower) |
| 2 | - | DGND |
| 3 | To INV | PWM W-phase (Upper) |
| 4 | - | DGND |
| 5 | - | SPARE2 |
| 6 | - | SPARE3 |
| 7 | - | SPARE4 |
| 8 | - | SPARE5 |
| 9 | To INV | Bus power signal from CPU board |
| 10 | To CPU | Inverter connected signal |
| 11 | To CPU | Save interlock signal |
| 12 | To CPU | Over current detection |
| 13 | To CPU | OC_PFC_OUT |
| 14 | To INV | PWM_IN |
| 15 | To INV | RELAY_IN |
| 16 | To CPU | SW1 |
| 17 | To CPU | SW2 |
| 18 | To INV | LED1 |
| 19 | To INV | LED2 |
| 20 | To INV | LED3 |
| 21 | To CPU | HALL U |
| 22 | To CPU | HALL V |
| 23 | To CPU | HALL W |
| 24 | To CPU | IPS_SIO_SDA |
| 25 | To CPU | IPS_SCK_SCL |
| 26 | To CPU | IPS_CSN_IRQN/Encoder Z |
| 27 | To CPU | IPS_A/ Encoder A |
| 28 | To CPU | IPS_A#/ Encoder A# |
| 29 | To CPU | IPS_B/ Encoder B# |
| 30 | To CPU | IPS_B#/ Encoder B# |
| 31 | - | AGND |
| 32 | - | AGND |
| 33 | - | +5V |
| 34 | - | +5V |

5.2.2 Hall sensor signal input

This product has connector for hall sensor signal input. Pin assignment of it is listed in Table 5-7.

Table 5-7 Connector for hall sensor signal input (CN6) pin assignment

| Pin No. | Pin Function |
|---------|--------------|
| 1 | DGND |
| 2 | +5V |
| 3 | HALL_W |
| 4 | HALL_V |
| 5 | HALL_U |

5.2.3 Encoder/Inductive position sensor signal input

This product has pins for encoder/inductive position sensor signal input. Pin assignment for them is listed in Table 5-8

Table 5-8 Pins for encoder/inductive position sensor signal input (CN7) pin assignment

| Pin No. | Pin function |
|---------|----------------|
| 1 | VCC |
| 2 | +5V |
| 3 | CSN_IRQN/ENC_Z |
| 4 | SIO_SDA |
| 5 | SCK_SCL |
| 6 | IPS_A/ENC_A |
| 7 | IPS_A#/ENC_A# |
| 8 | IPS_B/ENC_B |
| 9 | IPS_B#/ENC_B# |
| 10 | DGND |

6. CPU Board Specification

This section describes the specification of the CPU Board.

6.1 Functions

6.1.1 Power supply

When not connected to the inverter board, power should be supplied from the USB connector. When connecting to the inverter board, power supply from the USB connector or from the inverter board will be automatically selected. USB power supply has priority.

6.1.2 Onboard debugger

This product has the onboard debugger circuit, J-Link On-Board (hereinafter called "J-Link-OB"). You can write a program (firmware) of RA6T2 with it. When you write a program, connect the CPU board to PC with USB cable. J-Link-OB operates as debugger equivalent to J-Link. If connecting from Integrated Development Environment or flash programming tool (e.g. J-Flash Lite by SEGGER), set the type of debugger (tool) to "J-Link".

6.1.3 Inverter board connector

Two inverter boards can be connected to this board: the 1st inverter board is connected with CN4 and CN5, and the 2nd inverter board is connected with CN6 and CN7. The pin assignments of the connectors are shown in Table 6-1, Table 6-2, Table 6-3 and Table 6-4. Note that these tables show default connection setting for the ports with jumper switches.

Table 6-1 1st Inverter board connector (CN4) pin assignment

| Pin No | Pin Function | RA6T2 Pin | Pin No | Pin Function | RA6T2 Pin |
|--------|--------------|----------------|--------|--------------|--------------|
| 1 | SPARE1 | - | 2 | AGND | -(AVSS) |
| 3 | VPN | PA06/AN006 | 4 | AGND | -(AVSS) |
| 5 | IU | PA04/AN004 | 6 | PGAVSSU | PA05/PGAVSS2 |
| 7 | IV | PA02/AN002 | 8 | PGAVSSV | PA03/AN003 |
| 9 | IW | PA00/AN000 | 10 | PGAVSSW | PA01/AN001 |
| 11 | VU | PA07/AN007 | 12 | VV | PA03/AN003 |
| 13 | VW | PA01/AN001 | 14 | AGND | -(AVSS) |
| 15 | VAC | PB10/AN028 | 16 | IPFC | PE15/AN027 |
| 17 | VR | PB00/AN008 | 18 | AGND | -(AVSS) |
| 19 | AVCC | -(AVCC) | 20 | AVCC | -(AVCC) |
| 21 | AGND | -(AVSS) | 22 | AGND | -(AVSS) |
| 23 | VCC | -(VCC) | 24 | VCC | -(VCC) |
| 25 | GND | -(VSS) | 26 | GND | -(VSS) |
| 27 | UN | PB05/GTIOC4B_B | 28 | GND | -(VSS) |
| 29 | UP | PB04/GTIOC4A_B | 30 | GND | -(VSS) |
| 31 | VN | PB07/GTIOC5B_B | 32 | GND | -(VSS) |
| 33 | VP | PB06/GTIOC5A_B | 34 | GND | -(VSS) |

Table 6-2 1st Inverter board connector (CN5) pin assignment

| Pin No | Pin Function | RA6T2 Pin | Pin No | Pin Function | RA6T2 Pin |
|--------|----------------|------------------------|--------|----------------|--------------|
| 1 | WN | PB09/GTIOC6B_B | 2 | GND | -(VSS) |
| 3 | WP | PB08/GTIOC6A_B | 4 | GND | -(VSS) |
| 5 | SPARE2 | - | 6 | SPARE3 | - |
| 7 | SPARE4 | - | 8 | SPARE5 | - |
| 9 | BUS_POWER_IN | - | 10 | INV_CONNECTED | - |
| 11 | SAFE_LOCK | - | 12 | OC# | PC13/GTETRGD |
| 13 | PFCERROR | P001/IRQ2 | 14 | PFCPWM | PB14/GTIOC1A |
| 15 | VRL | PE01 | 16 | SW1 | PD04 |
| 17 | SW2 | PD07 | 18 | LED1 | PD01 |
| 19 | LED2 | PD02 | 20 | LED3 | PD03 |
| 21 | HALL_U | PC04/IRQ10_B | 22 | HALL_V | PC05/IRQ11_B |
| 23 | HALL_W | PB01/IRQ1_B | 24 | MISO0/SIO_SDA | PC11/MISOB_B |
| 25 | SCK0/SCK_SCL | PC10 | 26 | CSN_IRQN/ENC_Z | PE00/GTETRGA |
| 27 | IPS_A ENC_A | PC04 PC14/GTIOC3A_D | 28 | IPS_A#/ENC_A# | PC05/IRQ11_B |
| 29 | IPS_B ENC_B | PE15 PC15/GTIOC3B_D | 30 | IPS_B#/ENC_B# | PB10/AN028 |
| 31 | GND | -(VSS) | 32 | GND | -(VSS) |
| 33 | +5V | - | 34 | +5V | - |

Table 6-3 2nd Inverter board connector (CN7) pin assignment

| Pin No | Pin Function | RA6T2 Pin | Pin No | Pin Function | RA6T2 Pin |
|--------|--------------|----------------|--------|--------------|--------------|
| 1 | SPARE1 | - | 2 | AGND | - (AVSS) |
| 3 | VPN | PE13/AN025 | 4 | AGND | - (AVSS) |
| 5 | IU | PB02/AN018 | 6 | PGAVSSU | P002/PGAVSS3 |
| 7 | IV | PE08/AN020 | 8 | PGAVSSV | - |
| 9 | IW | PE09/AN021 | 10 | PGAVSSW | - |
| 11 | VU | PE10/AN022 | 12 | VV | PE11/AN023 |
| 13 | VW | PE12/AN024 | 14 | AGND | - (AVSS) |
| 15 | VAC | PC03/AN015 | 16 | IPFC | PC02/AN014 |
| 17 | VR | PE14/AN026 | 18 | AGND | - (AVSS) |
| 19 | AVCC | - (AVCC) | 20 | AVCC | - (AVCC) |
| 21 | AGND | - (AVSS) | 22 | AGND | - (AVSS) |
| 23 | VCC | - (VCC) | 24 | VCC | - (VCC) |
| 25 | GND | - (VSS) | 26 | GND | - (VSS) |
| 27 | UN | PC09/GTIOC7B_A | 28 | GND | - (VSS) |
| 29 | UP | PC08/GTIOC7A_A | 30 | GND | - (VSS) |
| 31 | VN | PA09/GTIOC8B_A | 32 | GND | - (VSS) |
| 33 | VP | PA08/GTIOC8A_A | 34 | GND | - (VSS) |

Table 6-4 2nd Inverter board connector (CN6) pin assignment

| Pin No | Pin Function | RA6T2 Pin | Pin No | Pin Function | RA6T2 Pin |
|--------|----------------|------------------------|--------|----------------|----------------|
| 1 | WN | PA11/GTIOC9B_A | 2 | GND | - (VSS) |
| 3 | WP | PA10/GTIOC9A_A | 4 | GND | - (VSS) |
| 5 | SPARE2 | - | 6 | SPARE3 | - |
| 7 | SPARE4 | - | 8 | SPARE5 | - |
| 9 | BUS_POWER_IN | - | 10 | INV_CONNECTED | - |
| 11 | SAFE_LOCK | - | 12 | OC# | PA12/GTETRGB |
| 13 | PFCERROR | P000/IRQ0 | 14 | PFCPWM | PB15/GTIOC1B_A |
| 15 | VRL | PD11 | 16 | SW1 | PC00 |
| 17 | SW2 | PC01 | 18 | LED1 | PD15 |
| 19 | LED2 | PC06 | 20 | LED3 | PC07 |
| 21 | HALL_U | PD12/IRQ12_B | 22 | HALL_V | PD13/IRQ13_B |
| 23 | HALL_W | PD14/IRQ13_B | 24 | MISO0/SIO_SDA | PC11/MISOB_B |
| 25 | SCK0/SCK_SCL | PC10 | 26 | CSN_IRQN/ENC_Z | PD10/GTETRGC |
| 27 | IPS_A ENC_A | PC02 PD08/GTIOC2A_A | 28 | IPS_A#/ENC_A# | PC03/AN015 |
| 29 | IPS_B ENC_B | PE11 PD09/GTIOC2B_A | 30 | IPS_B#/ENC_B# | PE12/AN024 |
| 31 | GND | - (VSS) | 32 | GND | - (VSS) |
| 33 | +5V | - | 34 | +5V | - |

The connection for CPU board and inverter board is shown in Figure 6-1. Please refer to 4.6.2 for the power supply method.

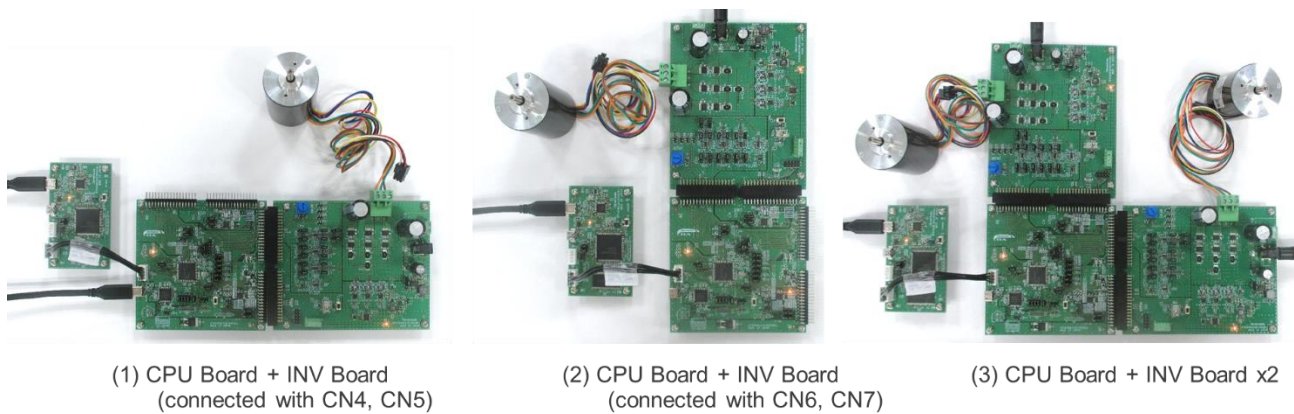


Figure 6-1 Connection for CPU board and inverter board

6.1.4 Serial communication

For serial communication using Renesas Motor Workbench, the CPU board has SCI connector. Pin assignment for SCI connector is listed in Table 6-5.

Table 6-5 SCI connector (CN10) pin assignment

| Pin No. | Pin Function | RA6T2 Connection Pin |
|---------|--------------|----------------------|
| 1 | GND | - |
| 2 | MCU RXD | PD06/RXD9_A |
| 3 | MCU TXD | PD05/TXD9_A |
| 4 | VCC | - |

6.1.5 Reset circuit

This product has a reset circuit to enable power-on reset or external reset on MCU. Push the tact switch (SW1) to externally reset MCU.

6.1.6 LED

This product has six ports and LEDs, so that they can be used for program debug and the system. LED switches on when output from the corresponding port is "LOW" and switches off when output is "HIGH". Pin assignment for corresponding LEDs is listed in Table 6-6.

Table 6-6 LED pin assignment

| RA6T2 port | | LED1 | LED2 | LED3 | LED4 | LED5 | LED6 |
|------------|-------------|------|------|------|------|------|------|
| PD01 | Output HIGH | OFF | - | - | - | - | - |
| | Output LOW | ON | - | - | - | - | - |
| PD02 | Output HIGH | - | OFF | - | - | - | - |
| | Output LOW | - | ON | - | - | - | - |
| PD03 | Output HIGH | - | - | OFF | - | - | - |
| | Output LOW | - | - | ON | - | - | - |
| PD15 | Output HIGH | - | - | - | OFF | - | - |
| | Output LOW | - | - | - | ON | - | - |
| PC06 | Output HIGH | - | - | - | - | OFF | - |
| | Output LOW | - | - | - | - | ON | - |
| PC07 | Output HIGH | - | - | - | - | - | OFF |
| | Output LOW | - | - | - | - | - | ON |

6.1.7 CAN Communication

This product has through holes for CAN communication. Note that CAN driver is not equipped. Pin assignment for CAN communication connector is listed in Table 6-7.

Table 6-7 CAN communication pin assignment (CN8)

| Pin No | RA6T2 pin |
|--------|-------------|
| 1 | VCC |
| 2 | PB13/CTX0_E |
| 3 | PB12/CRX0_E |
| 4 | VSS |

6.1.8 SPI communication

This product has through holes for SPI communication. Pin Assignment for SPI communication connector is listed in Table 6-8.

Table 6-8 SPI communication pin assignment (CN9)

| Pin No | RA6T2 pin |
|--------|--------------------|
| 1 | PD00_SS0 |
| 2 | PC12_MOSI0 |
| 3 | PC11_MISO0/SIO_SDA |
| 4 | PC10_SCK0/SCK_SCL |
| 5 | VSS |
| 6 | VCC |

6.2 RA6T2 pin function list

Table 6-9 RA6T2 pin function list

| Pin number | RA6T2 pin function | Signal function |
|------------|--|--|
| 1 | PE02/TRCLK/CMPOUT0_C/GTOVLO_C/GTIOC7B_B/GTIOC8A_E/GT CPPO8/SCK0_B/DE0_D/SCK3_A/DE3_A/RSPCKB_C/CLKOUT_C | ARM debugger |
| 2 | PE03/TRDATA0/CMPOUT1_C/GTOWLO_C/GTIOC8A_B/GTIOC9A_E/ GTCPP06/RXD0_B/CTS3_A/SSLB0_C/GTODFMA | ARM debugger |
| 3 | PE04/TRDATA1/CMPOUT2_C/GTOUUP_C/GTIOC8B_B/GTIOC7B_E/ GTCPP09/TXD0_B/SS_CTS_RTS3_A/DE3_A/SSLB1_C/GTODFMB | ARM debugger |
| 4 | PE05/TRDATA2/CMPOUT3_C/GTOVUP_C/GTIOC9A_B/GTIOC8B_E/ GTCPP02/SS_CTS_RTS0_B/DE0_B/RXD3_A/MISOB_C/GTODFMC | ARM debugger |
| 5 | PE06/TRDATA3/GTOWUP_C/GTIOC9B_B/GTCPP03/CTS0_B/TXD3_ A/MOSIB_C/GTODFMD | ARM debugger |
| 6 | VCC | Power |
| 7 | PC13/GTETRGD/NMI | INV1 over current |
| 8 | PC14/ADTRG0_C/CMPOUT012_B/AGTWIO0_C/GTETRGA/GTIOC3A _D/GTCPP00/GTADSM0/GTCPP04/IRQ14_A/GTODFMC | INV1 Encoder_A |
| 9 | PC15/ADTRG1_C/CMPOUT345_B/AGTWIO1_C/GTETRGB/GTIOC3B _D/GTCPP01/GTADSM1/GTCPP07/IRQ15_A/GTODFMD | INV1 Encoder_B |
| 10 | VSS | Power |
| 11 | VCC | Power |
| 12 | P212/EXTAL | Xtal |
| 13 | P213/XTAL/IRQ0_C | Xtal |
| 14 | RES | ARM debugger |
| 15 | PC00/AN012 (AN012)/PGAOUT0/IVCMP00/IRQ11DS | INV2 SW1 |
| 16 | PC01/AN013 (AN013)/PGAOUT1/IVCMP10/IRQ12DS | INV2 SW2 |
| 17 | PC02/AN014 (AN014)/PGAOUT2/IVCMP20/IRQ13DS | INV2 PFC current detection/IPS_A |
| 18 | PC03/AN015 (AN015)/PGAOUT3/IVCMP30/IRQ14DS | INV2 PFC current detection/IPS_A # |
| 19 | P000/AN016 (AN016)/IVREF0/IRQ0_D | INV2 PFC over current detection |
| 20 | VREFL0 | Power |
| 21 | VREFH0 | Power |
| 22 | P001/AN017 (AN017)/IVREF1/IRQ2_C | INV1 PFC over current detection |
| 23 | PA00/AN000 (AN000)/PGAIN0/IVCMP02 / IVCMP03/IRQ0DS | INV1 W-phase current detection |
| 24 | PA01/AN001 (AN001)/PGAVSS0/IRQ1_A | INV1 W-phase voltage detection/PGAVSS_ W |
| 25 | PA02/AN002 (AN002)/PGAIN1/IVCMP12 / IVCMP13/IRQ2_A | INV1 V-phase current detection |
| 26 | PA03/AN003 (AN003)/PGAVSS1/IRQ3_A | INV1 V-phase voltage detection/PGAVSS_ V |
| 27 | AVSS0 | Power |
| 28 | AVCC0 | Power |
| 29 | PA04/AN004 (AN004)/PGAIN2/IVCMP22 / IVCMP23/IRQ4_A | INV1 U-phase current detection |
| 30 | PA05/AN005 (AN005)/PGAVSS2/IRQ5_A | INV1 PGAVSS_U |
| 31 | PA06/AN006 (AN106)/DA0/IRQ6_A | INV1 bus voltage detection |
| 32 | PA07/AN007 (AN107)/DA1/IRQ7_A | INV1 W-phase voltage detection |
| 33 | PC04/AN010 (AN110)/DA2/IRQ10_B | INV1 HALL_U/IPS_A |
| 34 | PC05/AN011 (AN111)/DA3/IRQ11_B | INV1 HALL_V/IPS_A# |
| 35 | PB00/AN008 (AN108)/PGAOUT0 / PGAOUT2/IRQ0_A | INV1 VR1 voltage detection |
| 36 | PB01/AN009 (AN109)/PGAOUT1 / PGAOUT3/IRQ1_B | INV1 HALL_W |

| Pin number | RA6T2 pin function | Signal function |
|------------|---|---------------------------------------|
| 37 | PB02/AN018 (AN118)/PGAIN3/IVCMP32 / IVCMP33/IRQ15DS | INV2 U-phase current detection |
| 38 | P002/AN019 (AN119)/PGAVSS3 | INV2 PGAVSS_U |
| 39 | PE08/AN020/AN120/ADTRG0_E/CMPOUT012_C/GTIV_B/GTIOC3A_B/GTETRGC/GTADSM0/SSLA3_C/KR00_E/GTODFMON | INV2 V-phase current detection |
| 40 | PE09/AN021/AN121/ADTRG1_E/CMPOUT345_C/GTIW_B/GTIOC3B_B/GTETRGD/GTADSM1/CACREF_F/SSLA2_C/KR01_E | INV2 W-phase current detection |
| 41 | PE10/AN022/AN122/GTOULO_B/GTIOC2A_B/GTIOC4A_C/GTIOC7A_D/SSLA1_C/KR02_E | INV2 U-phase voltage detection |
| 42 | PE11/AN023/AN123/GTOUUP_B/GTIOC2B_B/GTIOC5A_C/GTIOC8A_D/SSLA0_C/KR03_E | INV2 V-phase voltage detection /IPS_B |
| 43 | PE12/AN024/AN124/GTOVLO_B/GTIOC1A_B/GTIOC6A_C/GTIOC9A_D/RSPCKA_C/KR04_E | INV2 V-phase voltage detection/IPS_B# |
| 44 | PE13/AN025/AN125/GTOVUP_B/GTIOC1B_B/GTIOC4B_C/GTIOC7B_D/MISOA_C/KR05_E | INV2 bus voltage detection |
| 45 | PE14/AN026/AN126/GTOWLO_B/GTIOC0A_B/GTIOC5B_C/GTIOC8B_D/MOSIA_C/KR06_E | INV2 VR1 voltage detection |
| 46 | PE15/AN027/AN127/GTOWUP_B/GTIOC0B_B/GTIOC6B_C/GTIOC9B_D/RXD4_A/KR07_E | INV1 PFC current detection/IPS_B |
| 47 | PB10/AN028/AN128/GTIU_C/GTETRGA/GTETRGB/GTCPPO4/GTCPPO7/CACREF_C/TXD4_A/CTS3_B/IRQ10DS/VCOUT | INV1 PFC voltage detection/IPS_B# |
| 48 | VCL1 | Power |
| 49 | VSS | Power |
| 50 | VCC | Power |
| 51 | PB12/ADTRG0_B/GTETRGA/GTIOC0A_A/GTIOC4A_F/CRX0_E/SCK4_A/DE4_A/RXD3_B/SSLB0_A/IRQ2_B | CAN_RX |
| 52 | PB13/GTOULO_A/GTIOC0B_A/GTIOC7A_C/GTIOC5A_F/CTX0_E/CTS4_A/TXD3_B/RSPCKB_A/IRQ3_B | CAN_TX |
| 53 | PB14/GTOVLO_A/GTIOC1A_A/GTIOC8A_C/GTIOC6A_F/SS_CTS_RT S4_A/DE4_A/SCK3_B/DE3_B/SDA0_C/MISOB_A/IRQ4_B | INV2 PFCPWM1 |
| 54 | PB15/GTOWLO_A/GTIOC1B_A/GTIOC9A_C/GTIOC4B_F/RXD4_A/SS_CTS_RTS3_B/DE3_B/SCL0_C/MOSIB_A/IRQ5_B | INV1 PFCPWM2 |
| 55 | PD08/GTIOC2A_A/CTS2_B/TXD1_A/SSLB1_A/KR00_D | INV2 Encoder_A |
| 56 | PD09/GTIOC2B_A/SS_CTS_RTS2_B/DE2_B/RXD1_A/SSLB2_A/KR01_D | INV2 Encoder_B |
| 57 | PD10/GTETRGC/GTIOC3A_A/SCK2_C/DE2_C/SCK1_A/DE1_A/SSLB3_A/KR02_D | INV2 Encoder_Z |
| 58 | PD11/GTIOC3B_A/RXD2_C/CTS1_A/KR03_D | INV2 Relay control |
| 59 | PD12/GTIOC4A_A/TXD2_C/SS_CTS_RTS1_A/DE1_A/SCL1_D/KR04_D/IRQ12_B/GTODFMA | INV2 HALL_U |
| 60 | PD13/GTIOC4B_A/SCK4_C/DE4_C/SCK9_C/DE9_C/SDA1_D/KR05_D/IRQ13_B/GTODFMB | INV2 HALL_V |
| 61 | PD14/GTIOC5A_A/RXD4_C/RXD9_C/SCL0_F/KR06_D/IRQ14_B/GTODFMC | INV2 HALL_W |
| 62 | PD15/GTIOC5B_A/TXD4_C/TXD9_C/DE9_C/SDA0_F/KR07_D/IRQ15_B/GTODFMD | INV2 LED1 |
| 63 | PC06/AGTWO0_B/GTETRGD/GTIOC6A_A/GTIOC5B_F/TXD2_B/SS_CTS_RTS9_C/DE9_C/SCL1_E/IRQ6_B | INV2 LED2 |
| 64 | PC07/AGTWEE0_B/GTETRGA/GTIOC6B_A/RXD2_B/CTS9_C/SDA1_E/IRQ7_B | INV2 LED3 |
| 65 | PC08/AGTWOA0_B/GTIV_C/GTIOC7A_A/CACREF_D/SCK2_B/DE2_B/SS_CTS_RTS3_C/DE3_C/SCL0_D (SCL0_E)/SSLA3_B/IRQ8_B | INV2 PWM U-phase (Upper) |
| 66 | PC09/AGTWOB0_B/GTIW_C/GTIOC7B_A/GTIOC8A_F/SS_CTS_RTS2_B/DE2_B/CTS3_C/SDA0_D (SDA0_E)/SSLA2_B/IRQ9_B/CLKOUT_B | INV2 PWM U-phase (Lower) |
| 67 | PA08/CMPOUT2_A/AGTWIO0_B/GTOUUP_A/GTIOC8A_A/GTIOC7B_C/GTIOC2A_C/GTIOC9A_F/SCK0_A/DE0_A/SCK1_C/DE1_C/SCL0_D/SSLA1_B/KR00_B/IRQ8_A/CLKOUT_A | INV2 PWM V-phase (Upper) |
| 68 | PA09/CMPOUT3_A/GTOVUP_A/GTIOC8B_A/GTIOC8B_C/GTIOC2B_C/GTIOC7B_F/TXD0_A/SCL1_C/SSLA0_B/KR01_B/IRQ9_A | INV2 PWM V-phase (Lower) |
| 69 | PA10/CMPOUT0_A/GTOWUP_A/GTIOC9A_A/GTIOC9B_C/GTIOC3A | INV2 PWM W-phase |

| Pin number | RA6T2 pin function | Signal function |
|------------|---|--|
| | _C/GTIOC8B_F/RXD0_A/SDA1_C/RSPCKA_B/KR02_B/IRQ10_A | (Upper) |
| 70 | PA11/CMPOUT1_A/GTETRGD/GTIOC9B_A/GTETRGC/GTIOC3B_C/CTX0_A/CTS0_A/RXD1_C/MOSIA_B/KR03_B/IRQ11_A | INV2 PWM W-phase (Lower) |
| 71 | PA12/ADTRG1_A/GTETRGB/GTCPPO0/GTCPPO2/GTADSM0/GTCPPO7/CACREF_A/CRX0_A/SS_CTS_RTS0_A/DE0_A/TXD1_C/MISOA_B/KR04_B/IRQ12_A/GTODFMA | INV2 over current detection/PFC over current detection |
| 72 | PA13/TMS/SWDIO/TMS/SWDIO/AGTWO0_A/SCK0_C/DE0_C/SS_CTS_RTS1_C/DE1_C | ARM debugger |
| 73 | VCL2 | Power |
| 74 | VSS | Power |
| 75 | VCC | Power |
| 76 | PA14/TCK/SWCLK/AGTWO1_A/TXD0_C/SCK9_B/DE9_B | ARM debugger |
| 77 | PA15/TDI/ADTRG0_A/CMPOUT012_A/GTETRGB/GTADSM1/GTCPPO4/RXD0_C/RXD9_B/SSLA0_A/KR02_A/IRQ1_C/GTODFMB | ARM debugger |
| 78 | PC10/CMPOUT0_B/AGTWIO1_B/TXD1_B/SCL0_B[w/5VToI]/RSPCKB_B/KR05_B/IRQ6DS | SS |
| 79 | PC11/CMPOUT1_B/AGTWOA1_B/RXD1_B/SDA0_B[w/5VToI]/MISOB_B/KR06_B/IRQ7DS | MOSI |
| 80 | PC12/CMPOUT2_B/AGTWOB1_B/GTCPPO6/GTCPPO9/TXD4_B/SCK1_B/DE1_B/MOSIB_B/KR07_B/IRQ8DS/GTODFMON | MISO/SIO_SDA |
| 81 | PD00/GTADSM0/GTCPPO4/CRX0_F/CTS2_A/RXD3_C/SSLB0_B/KR00_C | SCK0/SCK_SCL |
| 82 | PD01/GTADSM1/GTCPPO7/CTX0_F/SS_CTS_RTS2_A/DE2_A/TXD3_C/SSLB1_B/KR01_C | INV1 LED1 |
| 83 | PD02/CMPOUT3_B/AGTWEE1_B/GTCPPO0/GTCPPO2/RXD4_B/SCK3_C/DE3_C/KR02_C/IRQ9DS/CLKOUT_D | INV1 LED2 |
| 84 | PD03/CMPOUT0_D/GTCPPO5/GTCPPO0/SCK4_B/DE4_B/CTS9_A/SSLB2_B/KR03_C | INV1 LED3 |
| 85 | PD04/CMPOUT1_D/GTCPPO8/GTCPPO1/SS_CTS_RTS4_B/DE4_B/SS_CTS_RTS9_A/DE9_A/SSLB3_B/KR04_C | INV1 SW1 |
| 86 | PD05/GTADSM0/GTCPPO3/TXD9_A/SDA1_B[w/5VToI]/SSLA3_A/KR05_C | RMW communication |
| 87 | PD06/GTCPPO4/RXD9_A/SCL1_B[w/5VToI]/SSLA2_A/KR06_C | RMW communication |
| 88 | PD07/GTADSM1/GTCPPO7/SCK9_A/DE9_A/SSLA1_A/KR07_C | INV1 SW2 |
| 89 | PB03/TDO/TRACESWO/ADTRG1_B/CMPOUT345_A/AGTWO1_B/GTIOC4A_D/GTCPPO1/GTCPPO3/CRX0_D/TXD2_A/TXD9_B/RSPCKA_A/KR03_A/IRQ0_B/GTODFMON | ARM debugger |
| 90 | PB04/AGTWOA0_A/GTIOC4A_B/GTIOC5A_D/GTIOC0A_C/CACREF_B/CTX0_D/RXD2_A/RXD3_D/MISOA_A/KR04_A/IRQ13_A/VCOUT | INV1 PWM U-phase (Upper) |
| 91 | PB05/AGTWOB0_A/GTIU_A/GTIOC4B_B/GTIOC6A_D/GTIOC0B_C/CRX0_B/SCK2_A/DE2_A/TXD3_D/MOSIA_A/KR05_A/IRQ3DS/GTODFMON | INV1 PWM U-phase (Lower) |
| 92 | PB06/AGTWOA1_A/GTIV_A/GTIOC5A_B/GTIOC4B_D/GTIOC1A_C/CTX0_B/TXD0_D/SS_CTS_RTS3_D/DE3_D/SCL0_A[HSw/5VToI]/KR06_A/IRQ4DS/GTODFMA | INV1 PWM V-phase (Upper) |
| 93 | PB07/AGTWOB1_A/GTIW_A/GTIOC5B_B/GTETRGC/GTIOC1B_C/RXD0_D/SS_CTS_RTS1_D/DE1_D/SDA0_A[HSw/5VToI]/KR07_A/IRQ5DS/GTODFMB | INV1 PWM V-phase (Lower) |
| 94 | P201/MD | ARM debugger |
| 95 | PB08/AGTWIO0_A/GTIOC6A_B/GTIOC5B_D/GTIOC2A_D/CRX0_C/RXD4_C/RXD1_D/SCL1_A[w/5VToI]/KR00_A/IRQ1DS/GTODFMC | INV1 PWM W-phase (Upper) |
| 96 | PB09/AGTWIO1_A/GTIOC6B_B/GTIOC2B_D/CTX0_C/TXD4_C/TXD1_D/SDA1_A[w/5VToI]/KR01_A/IRQ2DS/GTODFMD | INV1 PWM W-phase (Lower) |
| 97 | PE00/ADTRG0_D/AGTWEE0_A/GTETRGA/GTIOC4A_F/GTADSM0/GTCPPO5/CACREF_E/TXD0_E/TXD9_D/SSLB3_ | INV1 Encoder_Z |
| 98 | PE01/ADTRG1_D/AGTWEE1_A/GTOULO_C/GTIOC7A_B/GTIOC4B_F/GTADSM1/RXD0_E/RXD9_D/SSLB2_C | INV1 Relay control |
| 99 | VSS | Power |
| 100 | VCC | Power |

7. Communication Board Specification

This section describes the specification of the communication board.

7.1 Functions

7.1.1 Power supply

Power of this product is supplied at 5V from USB connector.

7.1.2 USB communication

This product is equipped with a USB type-C connector for communication with a PC when using Renesas Motor Workbench, etc.

7.1.3 Serial communication

This board has two SCI connectors for serial communication with the target MCU when using Renesas Motor Workbench, etc. The pin assignments are shown in Table 7-1 and Table 7-2. When using the communication cable bundled with this product, use CN5.

The serial communication connector and the MCU (RX72N) are connected via a digital isolator, so the communication board and the CPU board with the target MCU are isolated.

Table 7-1 SCI connector (CN5) pin assignment

| Pin No. | Function | Note |
|---------|----------|------------------------------|
| 1 | VCC | |
| 2 | RXD | Connect to TXD of target MCU |
| 3 | TXD | Connect to RXD of target MCU |
| 4 | GND | |

Table 7-2 SCI connector (CN4) pin assignment

| Pin No. | Function | Note |
|---------|----------|------------------------------|
| 1 | VCC | |
| 2 | RXD | Connect to TXD of target MCU |
| 3 | TXD | Connect to RXD of target MCU |
| 4 | GND | |

8. Design and Manufacture Information

You can obtain information on the design and manufacture of this product from [renesas.com](https://www.renesas.com).

9. Website and Support

In order to learn, download tools and documents, apply technical support for RA family MCU and its kit, visit the below Web site.

- RA Product Information [renesas.com/ra](https://www.renesas.com/ra)
- Renesas Support [renesas.com/support](https://www.renesas.com/support)

| | |
|------------------|-------------------------|
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| 1.10 | March 31, 2022 | 31 | Modified Table 6-5 |
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