User's Manual

32

RX66T Group

Renesas Starter Kit User's Manual

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

Rev. 1.10 Nov 2019

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK), the user accepts the following terms:

The RSK is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK is assumed by the User. The RSK is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK product, but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX66T Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the CPU Board hardware.	RSKRX66T User's Manual	R20UT4150EG
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	RSKRX66T Tutorial Manual	CS+: R20UT4151EG e^2 studio: R20UT4154EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.	RSKRX66T Quick Start Guide	CS+: R20UT4152EG e^2 studio: R20UT4155EG
Smart Configurator Tutorial Manual	Provides a guide to code generation and importing into the e^{2}studio/CS+ IDE.	RSKRX66T Smart Configurator Tutorial Manual	CS+: R20UT4153EG e^2 studio: R20UT4156EG
Schematics	Full detail circuit schematics of the RSK.	RSKRX66T Schematics	R20UT4149EG
Hardware Manual	Provides technical details of the RX66T microcontroller.	RX66T Group Hardware Manual	R01UH0749EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1/E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GPT	General PWM Timer
GLCDC	Graphic LCD Controller
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK	Renesas Starter Kit
RTC	Real time Clock
SAU	Serial Array Unit
SCI	Serial Communications Interface
SFR	Special Function Registers
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TAU	Timer Array Unit
TPU	Timer Pulse Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

Table of Contents

1. Overview

1.1 Purpose

This CPU Board is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the CPU Board hardware.

1.2 Board specification

Board specification was shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microcontroller	Part No : R5F566TEADFP *1
	Package : 100-pin LFQFP
	On-Chip Memory : ROM 512KB+32KB, RAM 64KB+16KB
On-Board Memory	I²C EEPROM: 2Kbit
Input Clock	RX66T Main : 8MHz
	RL78/G1C Main: 12MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC : 5V Input, 3.3V Output
Debug Interface	E1/E2 Lite 14-pin box header
DIP Switch	Mode Configuration : 2-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer (for ADC)	Single-turn, 10kΩ
LED	Power indicator: green x 1
	User : green x 1, orange x 1, red x 2
CAN	Connector : 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
LIN	Connector : 2.54mm pitch, 3-pin x 1 *2
	LIN Driver x 1
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 *2 : Straight type, 12-pin Connector
Application Board Interface *2	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: The product of Trusted Secure IP Lite version mounted R5F566TEEDFP.

*2: The connector is not included to a product.

2. Power Supply

2.1 Requirements

This RSK is supplied with an E1 debugger or E2 Lite debugger. The debugger is able to power the RSK board with up to 200mA. When the RSK is connected to another system then that system should supply power to the RSK. This board has an optional centre positive supply connector using a 2.0mm barrel power jack.

Details of the external power supply requirements for the RSK, and configuration are shown in **Table 2-1 and Table 2-2** below. The default RSK power configuration is shown in **bold, blue text.**

Table 2-1: PWR connector Requirements

Connector	Supply voltage
PWR	Input 5VDC

Table 2-2: Main Power Supply Requirements

J8 Setting	R173 *1 Setting	J7 Setting	Supply Source	Board_3V3	Board_5V	Board_VCC UC_VCC
All Open	Fit	Open	E1(3V3) / E2 Lite (3V3) / JA1-3V3	3.3V	-	3.3V *3
		Shorted	PWR Connector / JA1-5V / Unregulated_VCC	3.3V	5V	3.3V *3
Pin1-2 Shorted	**DNF**	**Open**	**E1(3V3) / E2 Lite (3V3) / JA1-3V3**	**3.3V**	**-**	**3.3V *3**
		Shorted	PWR Connector / JA1-5V / Unregulated_VCC	3.3V	5V	3.3V *3
Pin2-3 Shorted	**DNF**	**Open**	PWR Connector / JA1-5V / Unregulated_VCC / E1(5V)	-	5V	5V *2
		Shorted	PWR Connector / JA1-5V / Unregulated_VCC / E1(5V)	3.3V	5V	5V *2

*1: R173 is not included to a product.

*2: 3.3V Pmod™ interface and Pmod™ LCD module can't be used.

*3: 5V Pmod™ interface and CAN, LIN can't be used.

The main power supply connected to PWR should supply a minimum of 5W to ensure full functionality.

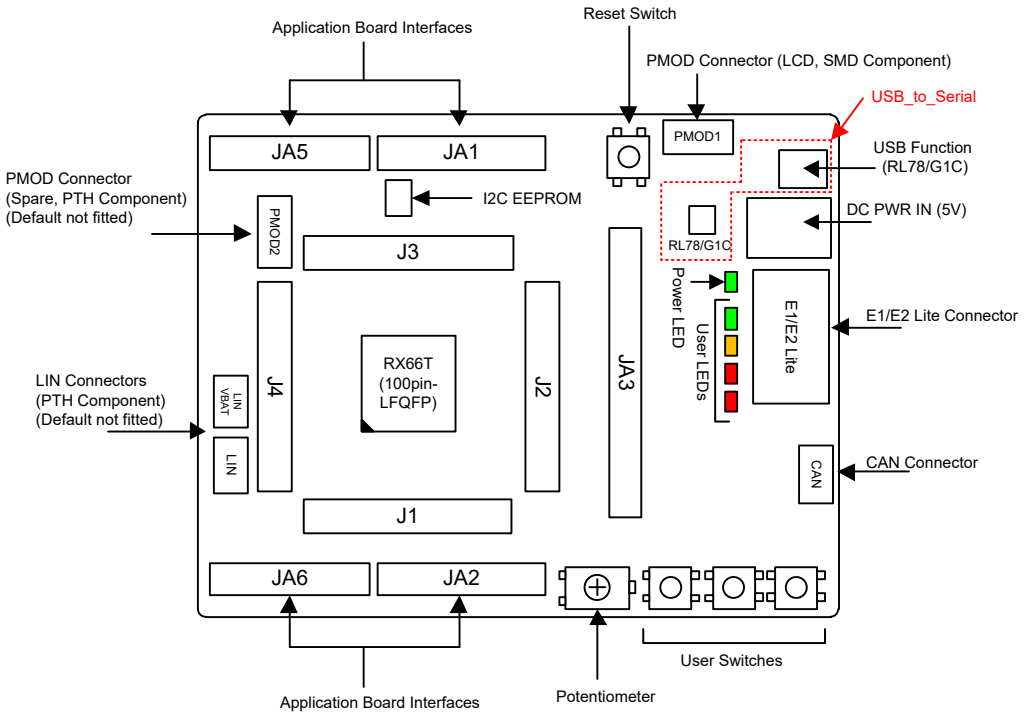
2.2 Power-Up Behaviour

When the RSK is purchased, the RSK board has the 'Release' build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit Smart Configurator Tutorial Manual' for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.



* J1 to J4 : 36-pin Micon Pin Headers

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

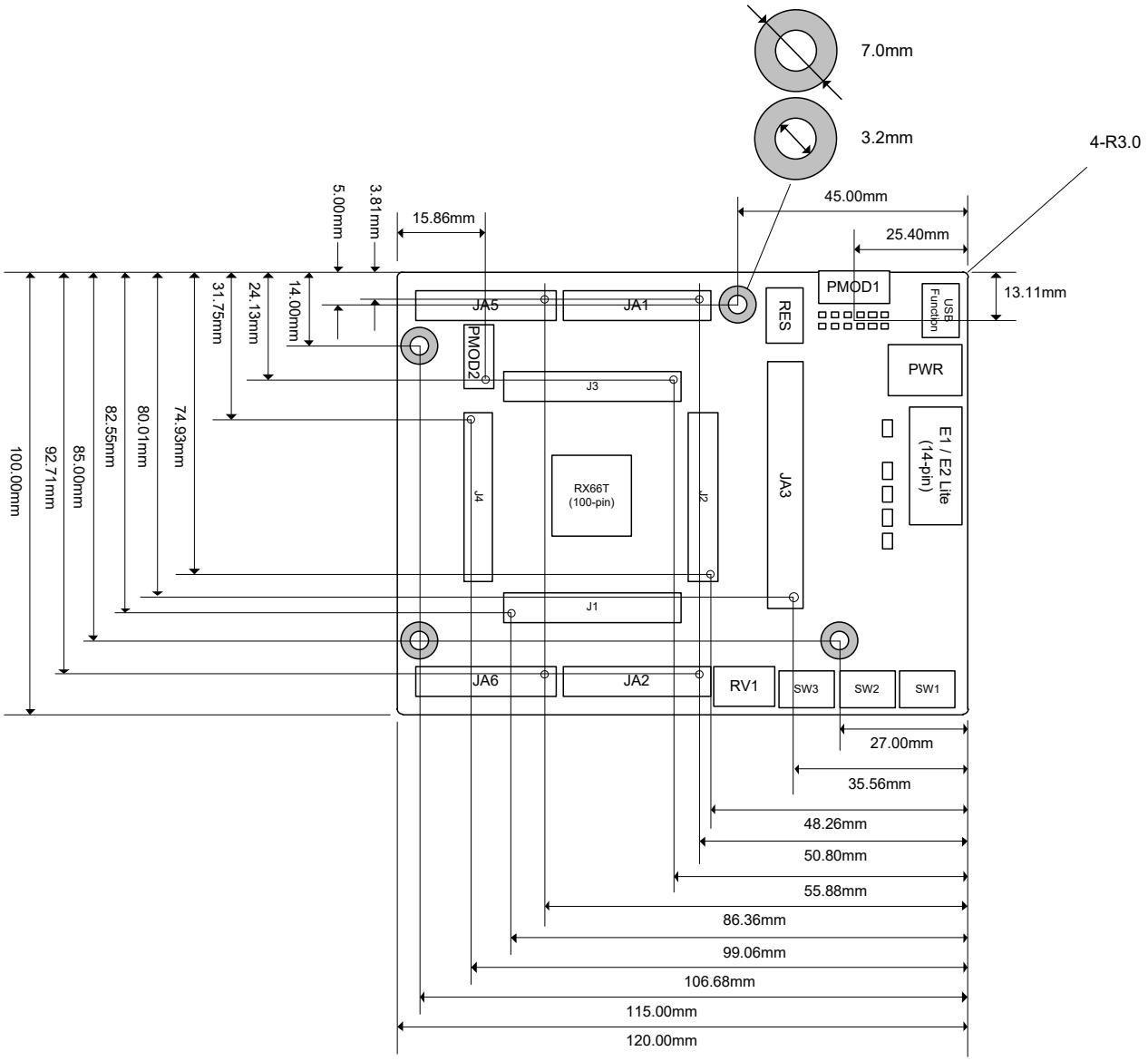


Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values are shown on the board schematics.

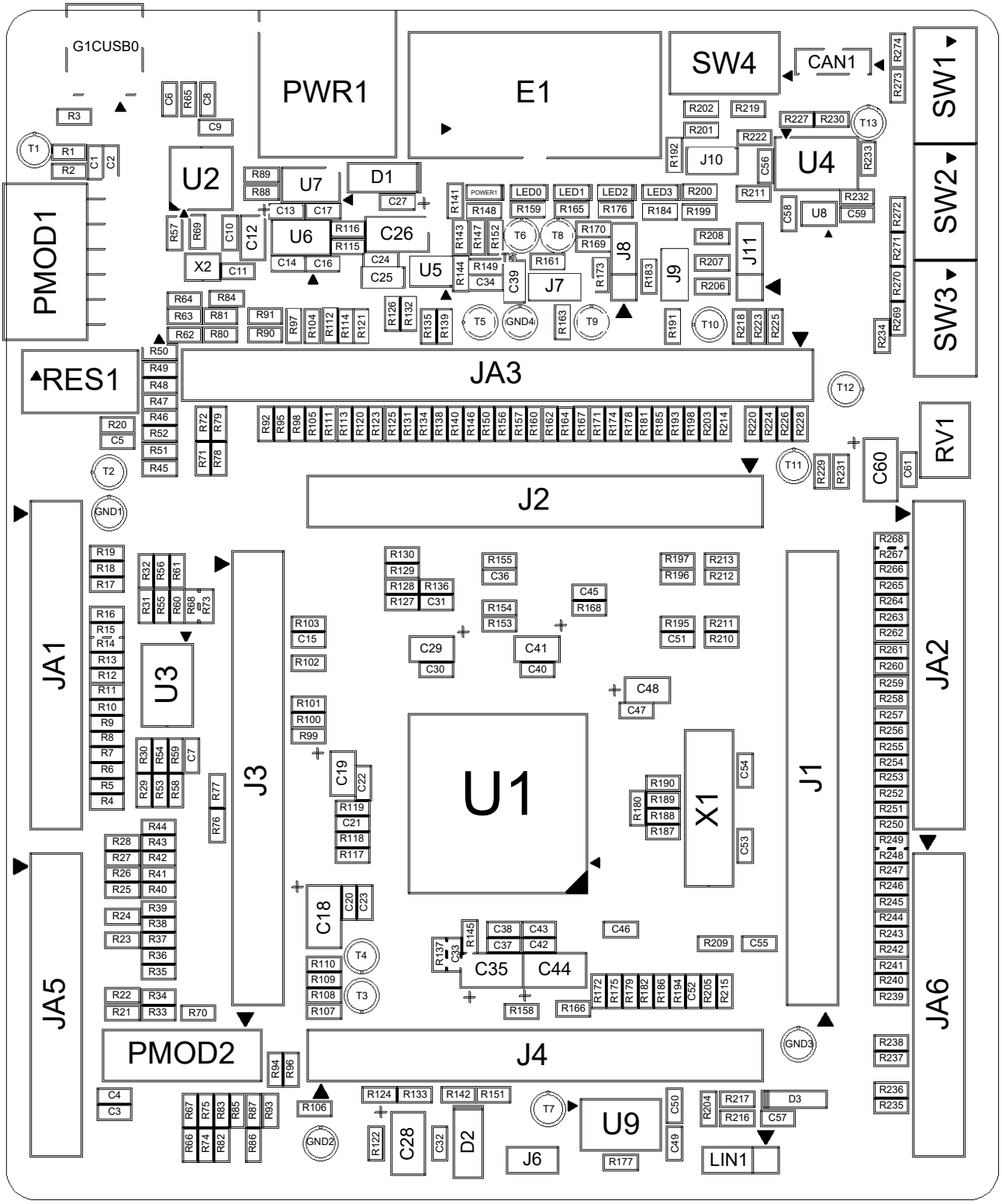


Figure 3-3: Top-Side Component Placement

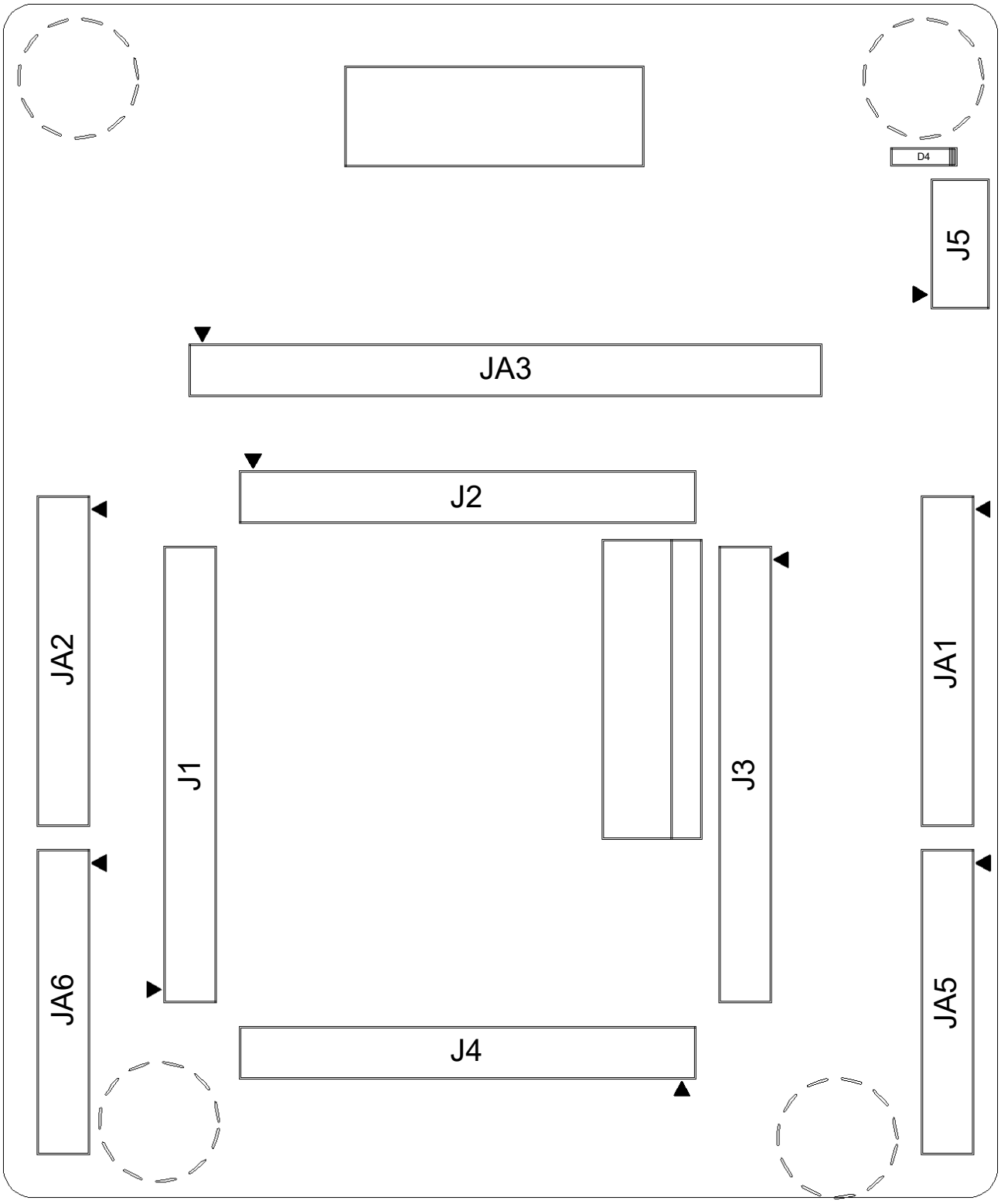


Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.

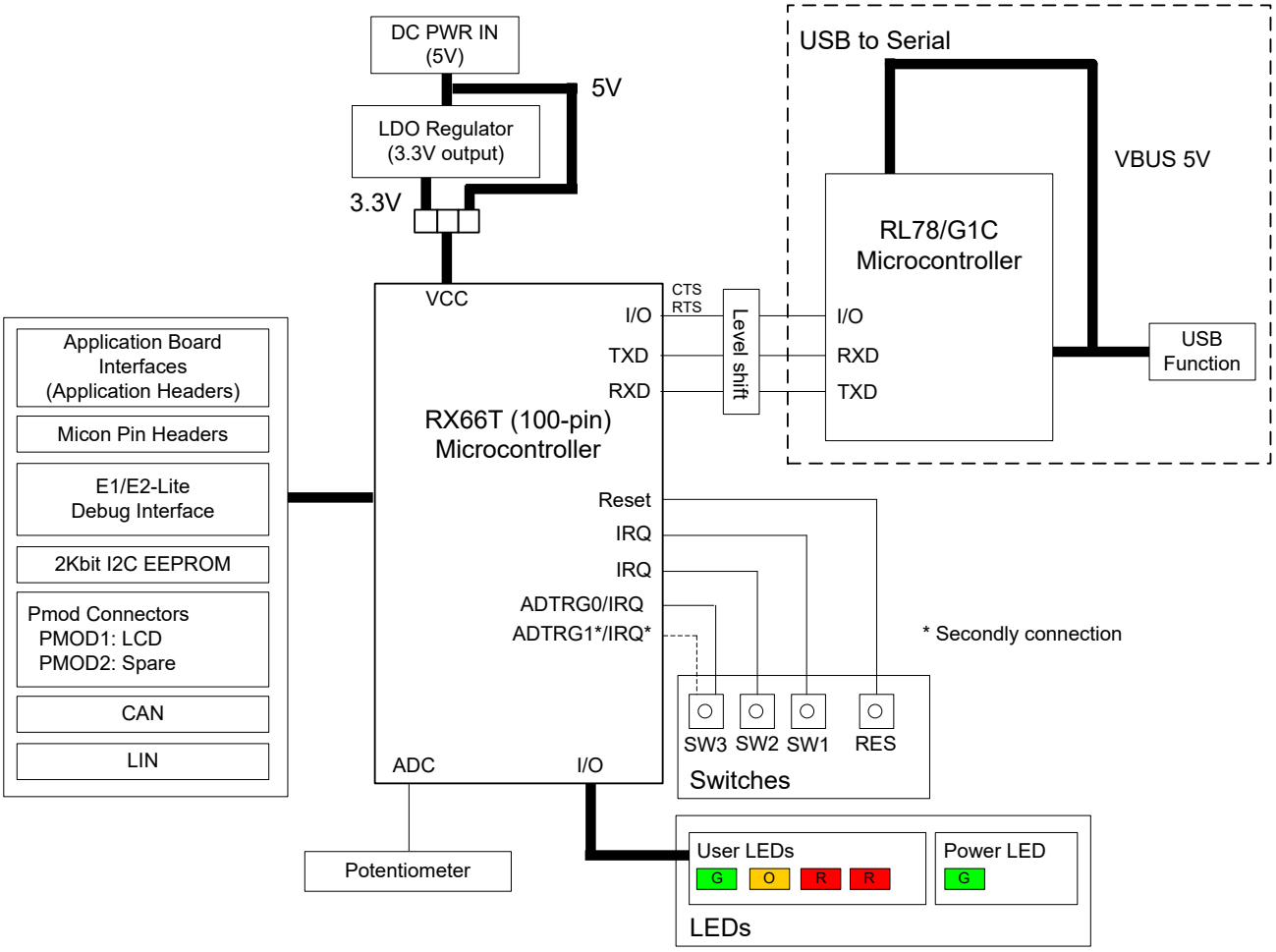


Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E1/E2 Lite debugger and the host PC.

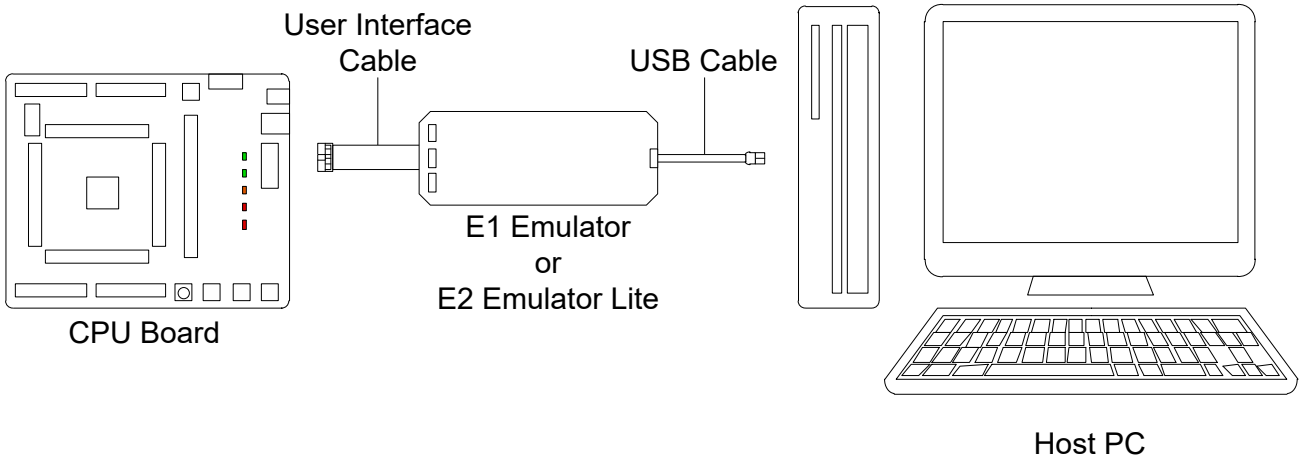


Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX66T Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX66T Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX66T	Fitted	8MHz	Encapsulated, SMT
X2	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT

5.3 Switches

There are four switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Switch Connections

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	10
SW1	Connects to an IRQ0_DS input for user controls.	P10	100
SW2	Connects to an IRQ9 input for user controls.	PB3	32
SW3	Connects to an IRQ7_DS input for user controls. Connects to an ADTRG0 input for ADC controls.	P20	69
	Connects to an IRQ6_DS input for user controls. Connects to an ADTRG1 input for ADC controls.	P21	68

5.4 LEDs

There are 5 LEDs on the CPU board. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

Table 5-3: LED Connections

LED	Colour	Function	MCU	
			Port	Pin
POWER1	Green	Indicates the status of the Board_VCC power rail.	NC	NC
LED0	Green	User operated LED.	P95	45
LED1	Orange	User operated LED.	P94	46
LED2	Red	User operated LED.	P93	47
LED3	Red	User operated LED.	PE0	17

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 90. The potentiometer can be used to create a voltage between Board_VCC and ground.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX66T Group User's Manual: Hardware for further details.

5.6 Pmod™

The CPU board are equipped with connectors for Digilent Pmod™ interface. Please connect the PMOD1 connector that is compatible with LCD module.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4 and Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

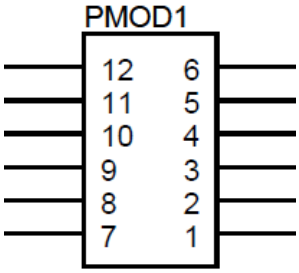


Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-4: Pmod™1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD1-CS	PA2	39	7	PMOD1-IO0	P55	78
2	PMOD1-MOSI	PB0	35	8	PMOD1-IO1	P61	76
3	PMOD1-MISO	PA5	36	9	PMOD1-IO2	P62	75
4	PMOD1-SCK	PA4	37	10	PMOD1-IO3	P63	74
5	GROUND	-	-	11	GROUND	-	-
6	Board_VCC	-	-	12	Board_VCC	-	-

Table 5-5: Pmod™2 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD2-CS	P24	65	7	PMOD2-IO0	P11	99
2	PMOD2-MOSI	P23	66	8	PMOD2-IO1	P27	64
3	PMOD2-MISO	P22	67	9	PMOD2-IO2	P54	79
4	PMOD2-SCK	P30	63	10	PMOD2-IO3	P60	77
5	GROUND	-	-	11	GROUND	-	-
6	Board_VCC	-	-	12	Board_VCC	-	-

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX66T Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI11 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Table 5-6: Serial Port Connections

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. *1	PD3	22
	SCI11 Transmit Signal.	PB5	28
	External RS232 Transmit Signal. *1	-	-
SERIAL-RXD	SCI1 Receive Signal. *1	PD5	20
	SCI11 Receive Signal.	PB6	27
	External RS232 Receive Signal. *1	-	-
SERIAL-CTS	Clear To Send. *2	P32	59
SERIAL-RTS	Request To Send. *2	P31	61

*1: This connection is a not available in the default RSK configuration - refer to §6 for the required modifications.

*2: CTS & RTS control is not supported on this RSK.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/en-eu/software/D6000699.html

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the CPU board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX66T Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

Table 5-7: CAN Connections

CAN Signal	Function	MCU	
		Port	Pin
CAN1TX JA5-CAN1TX *1	CAN Data Transmission.	PA0	41
CAN1RX JA5-CAN1RX *1	CAN Data Reception.	PA1	40

*1: This connection is a not available in the default RSK configuration - refer to §6 for the required modifications.

5.9 External Bus

The RX66T features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-8** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-8: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0(JA3-CSa)	JA3	Application Header	FFE00000h - FFFFFFFFh (2Mbyte)
CS1(JA3-CSb)	JA3	Application Header	07E00000h - 07FFFFFFh (2Mbyte)
CS2(JA3-CSc)	JA3	Application Header	06E00000h - 06FFFFFFh (2Mbyte)
CS3	-	Unused	05E00000h - 05FFFFFFh (2Mbyte)

5.10 I²C Bus (Inter-IC Bus)

The RX66T features one I²C (Inter-IC Bus) interface modules. RIIC0 is connected to a 2Kbit EEPROM. Specific details of the EEPROM device and the connections can be found in the board schematics.

5.11 Local-Interconnect Network (LIN)

A LIN transceiver IC is fitted to the CPU board, and connected to the LIN MCU peripheral. For further details regarding the LIN protocol and supported modes of operation, please refer to the RX66T Group User's Manual: Hardware. The connections for the LIN microcontroller signals are listed in **Table 5-9** below.

Table 5-9: LIN Connections

CAN Signal	Function	MCU	
		Port	Pin
LINTXD	LIN Data Transmission.	P23	66
LINRXD	LIN Data Reception.	P22	67
LINNSLP	LIN Transceiver Device Sleep Control.	P24	65

6. Configuration

6.1 Modifying the RSK

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX66T Group User's Manual: Hardware and CPU board schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU Operating Modes.

Table 6-1: MCU Operating Modes Switch Settings

Pin1	Pin2	Explanation	Related Ref.
OFF	**OFF(don't care)**	**Single Chip Mode**	
ON	OFF	User Boot Mode	**R201, R6,** R191, J10[*1]
ON	ON	SCI Boot Mode	**R201, R6,** R191, J10[*1]

[*1]: Jumpers J10 are not mounted on the board at the time of product shipment.

6.3 E1/E2 Lite Debugger Configuration

Table 6-2 below details the function of the option links associated with E1/E2 Lite Debugger Configuration.

Table 6-2: E1/E2 Lite Debugger Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P00	4	P00	**E1-UB**	**R6, R201** or J10(Short)	**R191**	**E1/E2 Lite.10**	-	-
			DSW-UB			**SW4.2**	-	-
			JA1-IRQd_M2HSIN0	**R6, R201** or J10(Short)	**R191**	**JA1.23**	-	-
			JA3-A11	R191	R6, R201, **J10(Open)**	JA3.12	-	-
PD7	18	PD7	**E1-TRSTn**	-	-	**E1/E2 Lite.3**	-	-
PD6	19	PD6	**E1-TMS**	-	-	**E1/E2 Lite.9**	-	-
PD5	20	PD5	**E1-TDI_RXD**	**R170**	**R196, R241**	**E1/E2 Lite.11**	-	-
			SERIAL-RXD	R196	R170, **R241**	U7.3	-	R197, **R242**
			JA6-RXDb	R241	R170, **R196**	JA6.7	-	
PD4	21	PD4	**E1-TCK_FINEC**	**R211, R195**	**R210**	**E1/E2 Lite.1**	-	-
			JA6-SCKb	R210, **R195**	R211	JA6.10	-	-
PD3	22	PD3	**E1-TDO_TXD**	**R147**	**R218, R240**	**E1/E2 Lite.5**		
			SERIAL-TXD	R218	R147, **R240**	U6.3	-	R223, **R243**
			JA6-TXDb	R240	R147, **R218**	JA6.8		
RESn	10	-	**E1-RESn**	-	-	**E1/E2 Lite.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-
EMLE	2	-	**E1-EMLE**	-	-	**E1/E2 Lite.4**	-	-
			JP-EMLE	-	-	**J11.2**	**R207**	-
MD_FINED	6	-	**E1-MD_FINED**	-	-	**E1/E2 Lite.7**	-	-
			DSW-MD_FINED	-	-	**SW4.1**	-	-

Table 6-3 below details the function of the jumpers associated with the E1/E2 Lite Debugger.

Table 6-3: E1/E2 Lite Debugger Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J11(DNF) *1	Shorted Pin1-2	Enable E1/E2 Lite debugging with Hot plug-in function.	-
	Shorted Pin2-3	**Enable E1/E2 Lite normal debugging and MCU single operation (without E1/E2 Lite).**	**R207**
	All open	DO NOT SET.	-

*1: Jumper J11 is not fitted on the default CPU board. Same as Jumper Position “Shorted pin2-3” setting by resistor R207.

6.4 Power Supply Configuration

Table 6-4 below details the function of the jumpers associated with the Power Supply Configuration.

Table 6-4: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J7	Shorted	Regulator output(3.3V) to Board_3V3.	**U5**
	Open *2	**Disconnects regulator output(3.3V) from Board_3V3.**	
J8	**Shorted Pin1-2**	**Board_3V3 power rail to Board_VCC.**	**U5**, R173
	Shorted Pin2-3 *3	Board_5V power rail to Board_VCC.	
	All Open	DO NOT SET.	
J9(DNF) *1	**Shorted**	**Board_VCC power rail to UC_VCC.**	**U5, R183**
	Open	Enable current probe for measurement MCU current consumption.	

*1: Jumper J9 is not fitted on the default CPU board. Same as Jumper Position “Shorted” setting by resistor R183.
*2: When the 3.3 V power supply source is the E1 / E2 Lite emulator or JA1-3V3, be sure to release it.
*3: When 5V power supply source is the E1 emulator, be sure to short Pin 2-3.

Table 6-5 below details the function of the option links associated with Power Supply Configuration.

Table 6-5: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
PWR	**Connects PWR power rail to Board_5V.**	-	-	**JA1.1, U5, R122,** J8.3, Simple IIC pull-up resistor
JA1-5V	**Connects JA1-5V power rail to Board_5V.**	**R126**	-	**JA1.1, U5, R122,** J8.3, Simple IIC pull-up resistor
	Disconnects JA1-5V power rail to Board_5V.	-	R126	
Unregulated_VCC	**Connects Unregulated_VCC power rail to Board_5V.**	**R132**	-	**JA6.23, U5, R122,** J8.3, Simple IIC pull-up resistor
	Disconnects Unregulated_VCC power rail to Board_5V.	-	R132	
JA1-3V3	**Connects JA1-3V3 power rail to Board_3V3.**	**R163**	-	**JA1.3**
	Disconnects JA1-3V3 power rail to Board_3V3.	-	R163	
Board_3V3	**Connects Board_3V3 power rail to Board_VCC.**	**J8(1-2Short)** or R173	-	**Simple IIC pull-up resistor**
	Disconnects Board_3V3 power rail to Board_VCC.	-	J8(2-3Short)	
Board_VCC	**Connects Board_VCC power rail to UC_VCC.**	J9(Short) or **R183**	-	**U1, R108, R110**
	Enable current probe for measurement MCU current consumption.	-	**J9(Open),** R183	
Board_5V	**Connects Board_5V power rail to VBAT.**	**R122**	-	J6
	Disconnects Board_5V power rail to VBAT.	-	R122	

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with Clock Configuration.

Table 6-6: Clock Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
XTAL, EXTAL	**Connects 8MHz crystal (X1) to RX66T.**	**R188, R189**	**R187, R190**	**U1.11, U1.13**
	Connects JA2-EXTAL to RX66T.	R190	R188, R189	U1.13

6.6 Analog Power & ADC & DAC Configuration

Table 6-7 below details the function of the option links associated with Analog Power & ADC & DAC Configuration.

Table 6-7: Analog Power & ADC & DAC Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P21	68	P21	**JA3-D14**	**R113**	**R269, R18**	**JA3.35**	-	-
			SW3	R269	R113, **R18**	SW3	-	-
			JA1-ADTRG	R18	R113, **R269**	JA1.8	R18	R17
P20	69	P20	**SW3**	**R234, R17**	**R120**	**SW3**	-	-
			JA1-ADTRG	**R234, R17**	**R120**	**JA1.8**	**R17**	**R18**
			JA3-D15	R120	R234, R17	JA3.36		
JA5-ADC7	82	P47	**JA5-ADC7**	-	-	**JA5.4**	-	-
JA5-ADC6	83	P46	**JA5-ADC6**	-	-	**JA5.3**	-	-
JA5-ADC5	84	P45	**JA5-ADC5**	-	-	**JA5.2**	-	-
JA5-ADC4	85	P44	**JA5-ADC4**	-	-	**JA5.1**	-	-
JA1-ADC3	87	P43	**JA1-ADC3**	-	-	**JA1.12**	-	-
JA1-ADC2	88	P42	**JA1-ADC2**	-	-	**JA1.11**	-	-
JA1-ADC1	89	P41	**JA1-ADC1**	-	-	**JA1.10**	-	-
P40	90	P40	**RV1-ADC**	**R145**	**R137**	**RV1(Board_VCC)**	**R231**	**R229**
						RV1(AVCC0-2)	R229	R231
			JA1-ADC0	R137	R145	JA1.9		
P65	70	P65	**JA1-DAC1**	**R15**	**R77**	**JA1.14**	-	-
			JA3-A12	R77	R15	JA3.13	-	-
P64	71	P64	**JA1-DAC0**	**R16**	**R76**	**JA1.13**	-	-
			JA3-A13	R76	R16	JA3.14	-	-
AVCC0-2	93, 92, 72	-	**UC_VCC**	**R108**	**R229** or R231, **R107**	-	-	-
			JA1-AVCC	R107	**R229** or R231, R108	JA1.5	-	-
AVSS0-2	94, 95, 73	-	**GROUND**	**R110**	**R109**	-	-	-
			JA1-AVSS	R109	R110	JA1.6	-	-

6.7 BUS Configuration

Table 6-8 to Table 6-10 below details the function of the option links associated with BUS Configuration.

Table 6-8: BUS Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	7	P01	**JA5-M2HSIN2**	**R40**	**R193**	**JA5.10**	-	-
			JA3-A10	R193	R40	JA3.11	-	-
P00	4	P00	**E1-UB**	**R6, R201** or J10(Short)	**R191**	**E1/E2 Lite.10**	-	-
			DSW-UB			**SW4.2**	-	-
			JA1-IRQd_M2HSIN0	**R6, R201** or J10(Short)	**R191**	**JA1.23**	-	-
			JA3-A11	R191	R6, R201, **J10(Open)**	JA3.12	-	-
P11	99	P11	**JA6-M1TOGGLE**	**R237**	**R172, R166**	**JA6.13**	-	-
			JA3-RDn	R172	R237, R166	JA3.25	-	-
			PMOD2-IO0	R166	R237, R172	PMOD2.7	-	-
P24	65	P24	**LINNSLP**	**R158**	**R131, R96**	**U9.2**	-	-
			JA3-D11	R131	R158, **R96**	JA3.32	-	-
			PMOD2-CS	R96	R158, **R131**	PMOD2.1	-	-
P23	66	P23	**LINTXD**	**R124**	**R123, R239, R86**	**U9.4**	-	-
			JA3-D12	R123	R124, **R239, R86**	JA3.33	-	-
			JA6-TXDc	R239	R124, **R123, R86**	JA6.9	-	-
			PMOD2-MOSI	R86	R124, **R123, R239**	PMOD2.2	-	-
P22	67	P22	**LINRXD**	**R142**	**R125, R238, R82**	**U9.1**	-	-
			JA3-D13	R125	R142, **R238, R82**	JA3.34	-	-
			JA6-RXDc	R238	R142, **R125, R82**	JA6.12	-	-
			PMOD2-MISO	R82	R142, **R125, R238**	PMOD2.3	-	-
P21	68	P21	**JA3-D14**	**R113**	**R269, R18**	**JA3.35**	-	-
			SW3	R269	R113, **R18**	SW3	-	-
			JA1-ADTRG	R18	R113, **R269**	JA1.8	R18	R17
P20	69	P20	**SW3**	**R234, R17**	**R120**	**SW3**	-	-
			JA1-ADTRG	**R234, R17**	**R120**	**JA1.8**	**R17**	**R18**
			JA3-D15	R120	R234, R17	JA3.36		
P33	58	P33	**JA2-M1TRCCLK**	**R245**	**R160**	**JA2.25**	-	-
			JA3-D7	R160	R245	JA3.24	-	-
P32	59	P32	**JA2-M1TRDCLK**	**R244**	**R134, R102**	**JA2.26**	-	-
			JA3-D8	R134	R244, **R102**	JA3.29	-	-
			SERIAL-CTS	R102	R244, **R134**	U7.2	-	-
P31	61	P31	JA3-D9	R139	R135	JA3.30	-	-
			SERIAL-RTS	**R135**	**R139**	**U6.2**	-	-
P30	63	P30	JA3-D10	R118, **R119**	R117	JA3.31	-	-
			PMOD2-SCK	**R117, R119**	**R118**	**PMOD2.4**	-	-
P55	78	P55	**PMOD1-IO0**	**R45**	**R95**	**PMOD1.7**	-	-
			JA3-A18	R95	R45	JA3.39	-	-
P54	79	P54	JA3-A19	R98	R74	JA3.40	-	-
			PMOD2-IO2	**R74**	**R98**	**PMOD2.9**	-	-
P53	80	P53	**JA2-M1UD**	**R261**	**R92**	**JA2.11**	-	-
			JA3-A20	R92	R261	JA3.41	-	-

Table 6-9: BUS Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P65	70	P65	**JA1-DAC1**	**R15**	**R77**	**JA1.14**	-	-
			JA3-A12	R77	R15	JA3.13	-	-
P64	71	P64	**JA1-DAC0**	**R16**	**R76**	**JA1.13**	-	-
			JA3-A13	R76	R16	JA3.14	-	-
P63	74	P63	**PMOD1-IO3**	**R49**	**R185**	**PMOD1.10**	-	-
			JA3-A14	R185	R49	JA3.15	-	-
P62	75	P62	**PMOD1-IO2**	**R47**	**R181**	**PMOD1.9**	-	-
			JA3-A15	R181	R47	JA3.16	-	-
P61	76	P61	**PMOD1-IO1**	**R52**	**R105**	**PMOD1.8**	-	-
			JA3-A16	R105	R52	JA3.37	-	-
P60	77	P60	JA3-A17	R111	R66	JA3.38	-	-
			PMOD2-IO3	**R66**	**R111**	**PMOD2.10**	-	-
P76	51	P76	**JA2-M1WN**	**R254**	**R7, R178**	**JA2.18**	-	-
			JA1-IO6	R7	R254, **R178**	JA1.21	-	-
			JA3-D0	R178	R254, **R7**	JA3.17		
P75	52	P75	**JA2-M1VN**	**R256**	**R8, R174**	**JA2.16**	-	-
			JA1-IO5	R8	R256, **R174**	JA1.20	-	-
			JA3-D1	R174	R256, **R8**	JA3.18		
P74	53	P74	**JA2-M1UN**	**R258**	**R9, R10**	**JA2.14**	-	-
			JA1-IO4	R9	R258, **R10**	JA1.19	-	-
			JA3-D2	R10	R258, **R9**	JA3.19		
P73	54	P73	**JA2-M1WP**	**R255**	**R11, R171**	**JA2.17**	-	-
			JA1-IO3	R11	R255, **R171**	JA1.18	-	-
			JA3-D3	R171	R255, **R11**	JA3.20		
P72	55	P72	**JA2-M1VP**	**R257**	**R12, R167**	**JA2.15**	-	-
			JA1-IO2	R12	R257, **R167**	JA1.17	-	-
			JA3-D4	R167	R257, **R12**	JA3.21		
P71	56	P71	**JA2-M1UP**	**R259**	**R13, R164**	**JA2.13**	-	-
			JA1-IO1	R13	R259, **R164**	JA1.16	-	-
			JA3-D5	R164	R259, **R13**	JA3.22	-	-
P70	57	P70	**JA2-M1POE**	**R246, R103**	**R14, R162**	**JA2.24**	-	-
			JA1-IO0	R14, **R103**	R246, **R162**	JA1.15	-	-
			JA3-D6	R162, **R103**	R246, **R14**	JA3.23	-	-
P82	96	P82	**JA5-M2UIN**	**R186, R194**	**R182, R179, R205, R215**	**JA5.12**	-	-
			JA3-ALE	R182, **R194**	R186, **R179, R205, R215**	JA3.46	-	-
			JA3-WAIT	R179, **R194**	R186, **R182, R205, R215**	JA3.45	R79	R112
			JA6-M1UIN	R205, **R194**	R186, **R182, R179, R215**	JA6.14	-	-
			JA6-SCKc	R215, **R194**	R186, **R182, R179, R205**	JA6.11	-	-
P81	97	P81	**JA5-M2VIN**	**R39**	**R121, R236**	**JA5.13**	-	-
			JA3-CSc	R121	R39, R236	JA3.45	**R112**	**R79**
			JA6-M1VIN	R236	R39, R121	JA6.15	-	-
P80	98	P80	**JA5-M2WIN**	**R24**	**R146, R235**	**JA5.14**	-	-
			JA3-CSb	R146	R24, R235	JA3.28	-	-
			JA6-M1WIN	R235	R24, R146	JA6.16	-	-
P96	43	P96	**JA5-M2POE**	**R37, R136**	**R140**	**JA5.16**	-	-
			JA3-CSa	R140, **R136**	R37	JA3.27	-	-
PA2	39	PA2	**PMOD1-CS**	**R80**	**R226**	**PMOD1.1**	-	-
			JA3-A0	R226	R80	JA3.1	-	-

Table 6-10: BUS Configuration Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PB7	26	PB7	**JA2-SCKa**	**R212, R168**	**R213**	**JA2.10**	-	-
			JA3-A4	R213, **R168**	R212	JA3.5	-	-
PB6	27	PB6	**SERIAL-RXD**	**R197, R264**	**R224**	**U7.3**	-	**R196, R242**
			JA2-RXDa	**R197, R264**	**R224**	**JA2.8**	-	-
			JA3-A3	R224	R197, R264	JA3.4	-	-
PB5	28	PB5	**SERIAL-TXD**	**R223, R267**	**R225**	**U6.3**	-	**R218, R243**
			JA2-TXDa	**R223, R267**	**R225**	**JA2.6**	-	-
			JA3-A2	R225	R223, R267	JA3.3	-	-
PB4	30	PB4	**JA2-CTSaRTSa**	**R260**	**R228**	**JA2.12**	-	-
			JA3-A1	R228	R260	JA3.2	-	-
PD2	23	PD2	**JA3-A7**	-	-	**JA3.8**	-	-
PD1	24	PD1	**JA2-TIMOUT1**	**R252**	**R214**	**JA2.20**	-	-
			JA3-A6	R214	R252	JA3.7	-	-
PD0	25	PD0	**JA2-TIMIN1**	**R250**	**R220**	**JA2.22**	-	-
			JA3-A5	R220	R250	JA3.6	-	-
JA3-BCLK	1	PE5	**JA3-BCLK**	**R209**	-	**JA3.44**	-	-
PE4	8	PE4	**JA5-M2TRCCLK**	**R36, R209**	**R203**	**JA5.17**	-	-
			JA3-A9	R203, **R209**	R36	JA3.10	-	-
PE3	9	PE3	**JA5-M2TRDCLK**	**R35**	**R198**	**JA5.18**	-	-
			JA3-A8	R198	R35	JA3.9	-	-
PE1	16	PE1	**JA3-WRLn**	**R72**	**R156**	**JA3.48**	-	-
			JA3-WRn	R156	R72	JA3.26	-	-
PE0	17	PE0	**LED3**	**R199**	**R184**	**LED3.K**	**R192**	-
			JA3-WRHn	R184	R199	JA3.47	-	-

6.8 CAN Configuration

Table 6-11 below details the function of the option links associated with CAN Configuration.

Table 6-11: CAN Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PA1	40	PA1	**CAN1RX**	**R232**	**R28, R38**	**U8.3**	-	-
			JA5-CAN1RX	R28	R232, **R38**	JA5.6	-	-
			JA5-M2TOGGLE	R38	R232, **R28**	JA5.15	-	-
PA0	41	PA0	**CAN1TX**	**R222**	**R44**	**U4.1**	-	-
			JA5-CAN1TX	R44	R222	JA5.5	-	-

6.9 General IO & LED Configuration

Table 6-12 below details the function of the option links associated with General IO & LED Configuration.

Table 6-12: General IO & LED Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P11	99	P11	**JA6-M1TOGGLE**	**R237**	**R172, R166**	**JA6.13**	-	-
			JA3-RDn	R172	R237, R166	JA3.25	-	-
			PMOD2-IO0	R166	R237, R172	PMOD2.7	-	-
P27	64	P27	**JA2-M1ENC**	**R100**	**R99**	**JA2.23**	**R249**	**R248**
			PMOD2-IO1	R99	R100	PMOD2.8	-	-
P55	78	P55	**PMOD1-IO0**	**R45**	**R95**	**PMOD1.7**	-	-
			JA3-A18	R95	R45	JA3.39	-	-
P54	79	P54	JA3-A19	R98	R74	JA3.40	-	-
			PMOD2-IO2	**R74**	**R98**	**PMOD2.9**	-	-
P63	74	P63	**PMOD1-IO3**	**R49**	**R185**	**PMOD1.10**	-	-
			JA3-A14	R185	R49	JA3.15	-	-
P62	75	P62	**PMOD1-IO2**	**R47**	**R181**	**PMOD1.9**	-	-
			JA3-A15	R181	R47	JA3.16	-	-
P61	76	P61	**PMOD1-IO1**	**R52**	**R105**	**PMOD1.8**	-	-
			JA3-A16	R105	R52	JA3.37	-	-
P60	77	P60	JA3-A17	R111	R66	JA3.38	-	-
			PMOD2-IO3	**R66**	**R111**	**PMOD2.10**	-	-
P76	51	P76	**JA2-M1WN**	**R254**	**R7, R178**	**JA2.18**	-	-
			JA1-IO6	R7	R254, **R178**	JA1.21	-	-
			JA3-D0	R178	R254, **R7**	JA3.17		
P75	52	P75	**JA2-M1VN**	**R256**	**R8, R174**	**JA2.16**	-	-
			JA1-IO5	R8	R256, **R174**	JA1.20	-	-
			JA3-D1	R174	R256, **R8**	JA3.18		
P74	53	P74	**JA2-M1UN**	**R258**	**R9, R10**	**JA2.14**	-	-
			JA1-IO4	R9	R258, **R10**	JA1.19	-	-
			JA3-D2	R10	R258, **R9**	JA3.19		
P73	54	P73	**JA2-M1WP**	**R255**	**R11, R171**	**JA2.17**	-	-
			JA1-IO3	R11	R255, **R171**	JA1.18	-	-
			JA3-D3	R171	R255, **R11**	JA3.20		
P72	55	P72	**JA2-M1VP**	**R257**	**R12, R167**	**JA2.15**	-	-
			JA1-IO2	R12	R257, **R167**	JA1.17	-	-
			JA3-D4	R167	R257, **R12**	JA3.21		
P71	56	P71	**JA2-M1UP**	**R259**	**R13, R164**	**JA2.13**	-	-
			JA1-IO1	R13	R259, **R164**	JA1.16	-	-
			JA3-D5	R164	R259, **R13**	JA3.22	-	-
P70	57	P70	**JA2-M1POE**	**R246, R103**	**R14, R162**	**JA2.24**	-	-
			JA1-IO0	R14, **R103**	R246, **R162**	JA1.15	-	-
			JA3-D6	R162, **R103**	R246, **R14**	JA3.23	-	-
P95	45	P95	**LED0**	**R127**	-	**LED0.K**	**R192**	-
			JA5-M2UP	**R22**	-	**JA5.19**	-	-
P94	46	P94	**LED1**	**R128**	-	**LED1.K**	**R192**	-
			JA5-M2VP	**R34**	-	**JA5.21**	-	-
P93	47	P93	**LED2**	**R129**	-	**LED2.K**	**R192**	-
			JA5-M2WP	**R33**	-	**JA5.23**	-	-
PE0	17	PE0	**LED3**	**R199**	**R184**	**LED3.K**	**R192**	-
			JA3-WRHn	R184	R199	JA3.47	-	-

6.10 I2C & EEPROM Configuration

Table 6-13 and Table 6-14 below detail the function of the option links associated with I2C & EEPROM Configuration.

Table 6-13: I2C & EEPROM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PB2	33	PB2	**E2P-SDA**	-	-	**U3.5**	-	-
			JA1-SDA			**JA1.25**	-	-
PB1	34	PB1	**E2P-SCL**	**R4**	**R262**	**U3.6**	-	-
			JA1-SCL			**JA1.26**	-	-
			JA2-IRQb_M1HSIN1	R262	R4	JA2.9	-	-

Table 6-14: I2C & EEPROM Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
SDA, SCL	**Connects pull-up resistor to Board_3V3.**	**R73**	**R68**	**U3**
	Connects pull-up resistor to Board_5V.	R68	R73	**U3**
WP	EEPROM Write protect.	R59	-	**U3**
A0	**Device address (0xA6).**	**R60**	-	**U3**
	Device address (0xA4).	-	R60	**U3**

6.11 IRQ & Switch Configuration

Table 6-15 and Table 6-16 below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-15: IRQ & Switch Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	7	P01	**JA5-M2HSIN2**	**R40**	**R193**	**JA5.10**	-	-
			JA3-A10	R193	R40	JA3.11	-	-
P00	4	P00	**E1-UB**	**R6, R201** or J10(Short)	**R191**	**E1/E2 Lite.10**	-	-
			DSW-UB			**SW4.2**	-	-
			JA1-IRQd_M2HSIN0	**R6, R201** or J10(Short)	**R191**	**JA1.23**	-	-
			JA3-A11	R191	R6, R201, **J10(Open)**	JA3.12	-	-
P11	99	P11	**JA6-M1TOGGLE**	**R237**	**R172, R166**	**JA6.13**	-	-
			JA3-RDn	R172	R237, R166	JA3.25	-	-
			PMOD2-IO0	R166	R237, R172	PMOD2.7	-	-
P10	100	P10	**SW1**	**R273, R43**	-	**SW1**	-	-
			JA5-IRQe_M2HSIN1	**R273, R43**	-	JA5.9	R42	R41
P27	64	P27	**JA2-M1ENC**	**R100**	**R99**	**JA2.23**	**R249**	**R248**
			PMOD2-IO1	R99	R100	PMOD2.8	-	-
P21	68	P21	**JA3-D14**	**R113**	**R269, R18**	**JA3.35**	-	-
			SW3	R269	R113, **R18**	SW3	-	-
			JA1-ADTRG	R18	R113, **R269**	JA1.8	R18	R17
P20	69	P20	**SW3**	**R234, R17**	**R120**	**SW3**	-	-
			JA1-ADTRG	**R234, R17**	**R120**	**JA1.8**	**R17**	**R18**
			JA3-D15	R120	R234, R17	JA3.36		
P32	59	P32	**JA2-M1TRDCLK**	**R244**	**R134, R102**	**JA2.26**	-	-
			JA3-D8	R134	R244, **R102**	JA3.29	-	-
			SERIAL-CTS	R102	R244, **R134**	U7.2	-	-
P55	78	P55	**PMOD1-IO0**	**R45**	**R95**	**PMOD1.7**	-	-
			JA3-A18	R95	R45	JA3.39	-	-

Table 6-16: IRQ & Switch Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P61	76	P61	PMOD1-IO1	R52	R105	PMOD1.8	-	-
			JA3-A16	R105	R52	JA3.37	-	-
PB3	32	PB3	SW2	R271	R266	SW2	-	-
			JA2-IRQa_M1HSIN0	R266	R271	JA2.7	-	-
PB1	34	PB1	E2P-SCL	R4	R262	U3.6	-	-
			JA1-SCL			JA1.26	-	-
			JA2-IRQb_M1HSIN1	R262	R4	JA2.9	-	-
PB0	35	PB0	PMOD1-MOSI	R91	R97	PMOD1.2	-	-
			JA2-IRQc_M1HSIN2	R97	R91	JA2.23	R248	R249
PE2	15	PE2	JA2-NMIn	-	-	JA2.3	-	-
RESn	10	-	E1-RESn	-	-	E1/E2 Lite.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-

6.12 LIN Configuration

Table 6-17 and Table 6-18 below details the function of the option links associated with LIN Configuration.

Table 6-17: LIN Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P24	65	P24	LINNSLP	R158	R131, R96	U9.2	-	-
			JA3-D11	R131	R158, R96	JA3.32	-	-
			PMOD2-CS	R96	R158, R131	PMOD2.1	-	-
P23	66	P23	LINTXD	R124	R123, R239, R86	U9.4	-	-
			JA3-D12	R123	R124, R239, R86	JA3.33	-	-
			JA6-TXDc	R239	R124, R123, R86	JA6.9	-	-
			PMOD2-MOSI	R86	R124, R123, R239	PMOD2.2	-	-
P22	67	P22	LINRXD	R142	R125, R238, R82	U9.1	-	-
			JA3-D13	R125	R142, R238, R82	JA3.34	-	-
			JA6-RXDc	R238	R142, R125, R82	JA6.12	-	-
			PMOD2-MISO	R82	R142, R125, R238	PMOD2.3	-	-

Table 6-18: LIN Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
U9.6	Master	R204, R216	-	U9
	Slave	-	R204, R216	U9

6.13 MTU & POE Configuration

Table 6-19 and Table 6-20 below details the function of the option links associated with MTU & POE Configuration.

Table 6-19: MTU & POE Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	7	P01	**JA5-M2HSIN2**	**R40**	**R193**	**JA5.10**	-	-
			JA3-A10	R193	R40	JA3.11	-	-
P00	4	P00	**E1-UB**	**R6, R201** or J10(Short)	**R191**	**E1/E2 Lite.10**	-	-
			DSW-UB			**SW4.2**	-	-
			JA1-IRQd_M2HSIN0	**R6, R201** or J10(Short)	**R191**	**JA1.23**	-	-
			JA3-A11	R191	R6, R201, **J10(Open)**	JA3.12	-	-
P11	99	P11	**JA6-M1TOGGLE**	**R237**	**R172, R166**	**JA6.13**	-	-
			JA3-RDn	R172	R237, R166	JA3.25	-	-
			PMOD2-IO0	R166	R237, R172	PMOD2.7	-	-
P10	100	P10	**SW1**	**R273, R43**	-	**SW1**	-	-
			JA5-IRQe_M2HSIN1	**R273, R43**	-	JA5.9	R42	R41
P27	64	P27	**JA2-M1ENC**	**R100**	**R99**	**JA2.23**	**R249**	**R248**
			PMOD2-IO1	R99	R100	PMOD2.8	-	-
P33	58	P33	**JA2-M1TRCCLK**	**R245**	**R160**	**JA2.25**	-	-
			JA3-D7	R160	R245	JA3.24	-	-
P32	59	P32	**JA2-M1TRDCLK**	**R244**	**R134, R102**	**JA2.26**	-	-
			JA3-D8	R134	R244, **R102**	JA3.29	-	-
			SERIAL-CTS	R102	R244, **R134**	U7.2	-	-
P53	80	P53	**JA2-M1UD**	**R261**	**R92**	**JA2.11**	-	-
			JA3-A20	R92	R261	JA3.41	-	-
P52	81	P52	**JA5-M2UD**	-	-	**JA5.11**	-	-
P76	51	P76	**JA2-M1WN**	**R254**	**R7, R178**	**JA2.18**	-	-
			JA1-IO6	R7	R254, **R178**	JA1.21	-	-
			JA3-D0	R178	R254, **R7**	JA3.17		
P75	52	P75	**JA2-M1VN**	**R256**	**R8, R174**	**JA2.16**	-	-
			JA1-IO5	R8	R256, **R174**	JA1.20	-	-
			JA3-D1	R174	R256, **R8**	JA3.18		
P74	53	P74	**JA2-M1UN**	**R258**	**R9, R10**	**JA2.14**	-	-
			JA1-IO4	R9	R258, **R10**	JA1.19	-	-
			JA3-D2	R10	R258, **R9**	JA3.19		
P73	54	P73	**JA2-M1WP**	**R255**	**R11, R171**	**JA2.17**	-	-
			JA1-IO3	R11	R255, **R171**	JA1.18	-	-
			JA3-D3	R171	R255, **R11**	JA3.20		
P72	55	P72	**JA2-M1VP**	**R257**	**R12, R167**	**JA2.15**	-	-
			JA1-IO2	R12	R257, **R167**	JA1.17	-	-
			JA3-D4	R167	R257, **R12**	JA3.21		
P71	56	P71	**JA2-M1UP**	**R259**	**R13, R164**	**JA2.13**	-	-
			JA1-IO1	R13	R259, **R164**	JA1.16	-	-
			JA3-D5	R164	R259, **R13**	JA3.22	-	-
P70	57	P70	**JA2-M1POE**	**R246, R103**	**R14, R162**	**JA2.24**	-	-
			JA1-IO0	R14, **R103**	R246, **R162**	JA1.15	-	-
			JA3-D6	R162, **R103**	R246, **R14**	JA3.23	-	-

Table 6-20: MTU & POE Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P82	96	P82	**JA5-M2UIN**	**R186, R194**	**R182, R179, R205, R215**	**JA5.12**	-	-
			JA3-ALE	R182, **R194**	R186, **R179, R205, R215**	JA3.46	-	-
			JA3-WAIT	R179, **R194**	R186, **R182, R205, R215**	JA3.45	R79	R112
			JA6-M1UIN	R205, **R194**	R186, **R182, R179, R215**	JA6.14	-	-
			JA6-SCKc	R215, **R194**	R186, **R182, R179, R205**	JA6.11	-	-
P81	97	P81	**JA5-M2VIN**	**R39**	**R121, R236**	**JA5.13**	-	-
			JA3-CSc	R121	R39, R236	JA3.45	**R112**	**R79**
			JA6-M1VIN	R236	R39, R121	JA6.15	-	-
P80	98	P80	**JA5-M2WIN**	**R24**	**R146, R235**	**JA5.14**	-	-
			JA3-CSb	R146	R24, R235	JA3.28	-	-
			JA6-M1WIN	R235	R24, R146	JA6.16	-	-
P96	43	P96	**JA5-M2POE**	**R37, R136**	**R140**	**JA5.16**	-	-
			JA3-CSa	R140, **R136**	R37	JA3.27	-	-
P95	45	P95	**LED0**	**R127**	-	**LED0.K**	**R192**	-
			JA5-M2UP	**R22**	-	**JA5.19**	-	-
P94	46	P94	**LED1**	**R128**	-	**LED1.K**	**R192**	-
			JA5-M2VP	**R34**	-	**JA5.21**	-	-
P93	47	P93	**LED2**	**R129**	-	**LED2.K**	**R192**	-
			JA5-M2WP	**R33**	-	**JA5.23**	-	-
P92	48	P92	**JA5-M2UN**	**R130**	**R253**	**JA5.20**	-	-
			JA2-TIMOUT0	R253	R130	JA2.19	-	-
P91	49	P91	**JA5-M2VN**	**R21**	**R251**	**JA5.22**	-	-
			JA2-TIMIN0	R251	R21	JA2.21	-	-
JA5-M2WN	50	P90	**JA5-M2WN**	-	-	**JA5.24**	-	-
JA5-M2ENC	38	PA3	**JA5-M2ENC**	-	-	**JA5.9**	**R41**	**R42**
PA1	40	PA1	**CAN1RX**	**R232**	**R28, R38**	**U8.3**	-	-
			JA5-CAN1RX	R28	R232, **R38**	JA5.6	-	-
			JA5-M2TOGGLE	R38	R232, **R28**	JA5.15	-	-
PB3	32	PB3	**SW2**	**R271**	**R266**	**SW2**	-	-
			JA2-IRQa_M1HSIN0	**R266**	**R271**	**JA2.7**	-	-
PB1	34	PB1	**E2P-SCL**	**R4**	**R262**	**U3.6**	-	-
			JA1-SCL			**JA1.26**	-	-
			JA2-IRQb_M1HSIN1	R262	R4	JA2.9	-	-
PB0	35	PB0	**PMOD1-MOSI**	**R91**	**R97**	**PMOD1.2**	-	-
			JA2-IRQc_M1HSIN2	R97	R91	JA2.23	R248	R249
PD1	24	PD1	**JA2-TIMOUT1**	**R252**	**R214**	**JA2.20**	-	-
			JA3-A6	R214	R252	JA3.7	-	-
PD0	25	PD0	**JA2-TIMIN1**	**R250**	**R220**	**JA2.22**	-	-
			JA3-A5	R220	R250	JA3.6	-	-
PE4	8	PE4	**JA5-M2TRCCLK**	**R36, R209**	**R203**	**JA5.17**	-	-
			JA3-A9	R203, **R209**	R36	JA3.10	-	-
PE3	9	PE3	**JA5-M2TRDCLK**	**R35**	**R198**	**JA5.18**	-	-
			JA3-A8	R198	R35	JA3.9	-	-
RESn	10	-	**E1-RESn**	-	-	**E1/E2 Lite.13**	-	-
			SW-RESn	-	-	**RES1(Switch)**	-	-
			JA2-RESn	-	-	**JA2.1**	-	-

6.14 PMOD1 Configuration

Table 6-21 below details the function of the option links associated with PMOD1 Configuration.

Table 6-21: PMOD1 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P55	78	P55	**PMOD1-IO0**	**R45**	**R95**	**PMOD1.7**	-	-
			JA3-A18	R95	R45	JA3.39	-	-
P63	74	P63	**PMOD1-IO3**	**R49**	**R185**	**PMOD1.10**	-	-
			JA3-A14	R185	R49	JA3.15	-	-
P62	75	P62	**PMOD1-IO2**	**R47**	**R181**	**PMOD1.9**	-	-
			JA3-A15	R181	R47	JA3.16	-	-
P61	76	P61	**PMOD1-IO1**	**R52**	**R105**	**PMOD1.8**	-	-
			JA3-A16	R105	R52	JA3.37	-	-
PMOD1-MISO	36	PA5	**PMOD1-MISO**	-	-	**PMOD1.3**	-	-
PMOD1-SCK	37	PA4	**PMOD1-SCK**	**R155**	-	**PMOD1.4**	-	-
PA2	39	PA2	**PMOD1-CS**	**R80**	**R226**	**PMOD1.1**	-	-
			JA3-A0	R226	R80	JA3.1	-	-
PB0	35	PB0	**PMOD1-MOSI**	**R91**	**R97**	**PMOD1.2**	-	-
			JA2-IRQc_M1HSIN2	R97	R91	JA2.23	R248	R249

6.15 PMOD2 Configuration

Table 6-22 below details the function of the option links associated with PMOD2 Configuration.

Table 6-22: PMOD2 Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P11	99	P11	**JA6-M1TOGGLE**	**R237**	**R172, R166**	**JA6.13**	-	-
			JA3-RDn	R172	R237, R166	JA3.25	-	-
			PMOD2-IO0	R166	R237, R172	PMOD2.7	-	-
P27	64	P27	**JA2-M1ENC**	**R100**	**R99**	**JA2.23**	**R249**	**R248**
			PMOD2-IO1	R99	R100	PMOD2.8	-	-
P24	65	P24	**LINNSLP**	**R158**	**R131, R96**	**U9.2**	-	-
			JA3-D11	R131	R158, **R96**	JA3.32	-	-
			PMOD2-CS	R96	R158, **R131**	PMOD2.1	-	-
P23	66	P23	**LINTXD**	**R124**	**R123, R239, R86**	**U9.4**	-	-
			JA3-D12	R123	R124, **R239, R86**	JA3.33	-	-
			JA6-TXDc	R239	R124, **R123, R86**	JA6.9	-	-
			PMOD2-MOSI	R86	R124, **R123, R239**	PMOD2.2	-	-
P22	67	P22	**LINRXD**	**R142**	**R125, R238, R82**	**U9.1**	-	-
			JA3-D13	R125	R142, **R238, R82**	JA3.34	-	-
			JA6-RXDc	R238	R142, **R125, R82**	JA6.12	-	-
			PMOD2-MISO	R82	R142, **R125, R238**	PMOD2.3	-	-
P30	63	P30	JA3-D10	R118, **R119**	R117	JA3.31	-	-
			PMOD2-SCK	**R117, R119**	**R118**	**PMOD2.4**	-	-
P54	79	P54	JA3-A19	R98	R74	JA3.40	-	-
			PMOD2-IO2	**R74**	**R98**	**PMOD2.9**	-	-
P60	77	P60	JA3-A17	R111	R66	JA3.38	-	-
			PMOD2-IO3	**R66**	**R111**	**PMOD2.10**	-	-

6.16 Serial & USB to Serial Configuration

Table 6-23 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-23: Serial & USB to Serial Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P23	66	P23	**LINTXD**	**R124**	**R123, R239, R86**	**U9.4**	-	-
			JA3-D12	R123	R124, **R239, R86**	JA3.33	-	-
			JA6-TXDc	R239	R124, **R123, R86**	JA6.9	-	-
			PMOD2-MOSI	R86	R124, **R123, R239**	PMOD2.2	-	-
P22	67	P22	**LINRXD**	**R142**	**R125, R238, R82**	**U9.1**	-	-
			JA3-D13	R125	R142, **R238, R82**	JA3.34	-	-
			JA6-RXDc	R238	R142, **R125, R82**	JA6.12	-	-
			PMOD2-MISO	R82	R142, **R125, R238**	PMOD2.3	-	-
P32	59	P32	**JA2-M1TRDCLK**	**R244**	**R134, R102**	**JA2.26**	-	-
			JA3-D8	R134	R244, **R102**	JA3.29	-	-
			SERIAL-CTS	R102	R244, **R134**	U7.2	-	-
P31	61	P31	JA3-D9	R139	R135	JA3.30	-	-
			SERIAL-RTS	**R135**	**R139**	**U6.2**	-	-
P82	96	P82	**JA5-M2UIN**	**R186, R194**	**R182, R179, R205, R215**	**JA5.12**	-	-
			JA3-ALE	R182, **R194**	R186, **R179, R205, R215**	JA3.46	-	-
			JA3-WAIT	R179, **R194**	R186, **R182, R205, R215**	JA3.45	R79	R112
			JA6-M1UIN	R205, **R194**	R186, **R182, R179, R215**	JA6.14	-	-
			JA6-SCKc	R215, **R194**	R186, **R182, R179, R205**	JA6.11	-	-
PB7	26	PB7	**JA2-SCKa**	**R212, R168**	**R213**	**JA2.10**	-	-
			JA3-A4	R213, **R168**	R212	JA3.5	-	-
PB6	27	PB6	**SERIAL-RXD**	**R197, R264**	**R224**	**U7.3**	-	**R196, R242**
			JA2-RXDa	**R197, R264**	**R224**	**JA2.8**	-	-
			JA3-A3	R224	R197, R264	JA3.4	-	-
PB5	28	PB5	**SERIAL-TXD**	**R223, R267**	**R225**	**U6.3**	-	**R218, R243**
			JA2-TXDa	**R223, R267**	**R225**	**JA2.6**	-	-
			JA3-A2	R225	R223, R267	JA3.3	-	-
PB4	30	PB4	**JA2-CTSaRTSa**	**R260**	**R228**	**JA2.12**	-	-
			JA3-A1	R228	R260	JA3.2	-	-
PD5	20	PD5	**E1-TDI_RXD**	**R170**	**R196, R241**	**E1/E2 Lite.11**	-	-
			SERIAL-RXD	R196	R170, **R241**	U7.3	-	R197, **R242**
			JA6-RXDb	R241	R170, **R196**	JA6.7	-	
PD4	21	PD4	**E1-TCK_FINEC**	**R211, R195**	**R210**	**E1/E2 Lite.1**	-	-
			JA6-SCKb	R210, **R195**	R211	JA6.10	-	-
PD3	22	PD3	**E1-TDO_TXD**	**R147**	**R218, R240**	**E1/E2 Lite.5**		
			SERIAL-TXD	R218	R147, **R240**	U6.3	-	R223, **R243**
			JA6-TXDb	R240	R147, **R218**	JA6.8		

7. Headers

7.1 Application Headers

This CPU board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA1					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V JA1-5V	-	2	0V GROUND	-
3	3V3 JA1-3V3	-	4	0V GROUND	-
5	AVCC JA1-AVCC	93, 92, 72	6	AVSS JA1-AVSS	94, 95, 73
7	AVREF NC	NC	8	ADTRG JA1-ADTRG	69, 68
9	ADC0 JA1-ADC0	90	10	ADC1 JA1-ADC1	89
11	ADC2 JA1-ADC2	88	12	ADC3 JA1-ADC3	87
13	DAC0 JA1-DAC0	71	14	DAC1 JA1-DAC1	70
15	IO_0 JA1-IO0	57	16	IO_1 JA1-IO1	56
17	IO_2 JA1-IO2	55	18	IO_3 JA1-IO3	54
19	IO_4 JA1-IO4	53	20	IO_5 JA1-IO5	52
21	IO_6 JA1-IO6	51	22	IO_7 NC	NC
23	IRQd / IRQAEC / M2_HSIN0 JA1-IRQd_M2HSIN0	4 / NC / 4	24	IIC_EX NC	NC
25	IIC_SDA JA1-SDA	33	26	IIC_SCL JA1-SCL	34

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections

Application Header JA2					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	RESET JA2-RESn	10	2	EXTAL JA2-EXTAL	13
3	NMI JA2-NMIn	15	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX JA2-TXDa	28
7	IRQa / WKUP / M1_HSIN0 JA2-IRQa_M1HSIN0	32 / NC / 32	8	SCIaRX JA2-RXDa	27
9	IRQb / M1_HSIN1 JA2-IRQb_M1HSIN1	34 / 34	10	SCIaCK JA2-SCKa	26
11	M1_UD JA2-M1UD	80	12	CTSaRTSa JA2-CTSaRTSa	30
13	M1_UP JA2-M1UP	56	14	M1_UN JA2-M1UN	53
15	M1_VP JA2-M1VP	55	16	M1_VN JA2-M1VN	52
17	M1_WP JA2-M1WP	54	18	M1_WN JA2-M1WN	51
19	TimerOut0 JA2-TIMOUT0	48	20	TimerOut1 JA2-TIMOUT1	24
21	TimerIn0 JA2-TIMIN0	49	22	TimerIn1 JA2-TIMIN1	25
23	IRQc / M1_EncZ / M1_HSIN2 JA2-23PIN	35 / 64 / 35	24	M1_POE JA2-M1POE	57
25	M1_TRCCLK JA2-M1TRCCLK	58	26	M1_TRDCLK JA2-M1TRDCLK	59

Table 7-3 below lists the connections of the BUS application header, JA3.

Table 7-3: Application Header JA3 Connections

Application Header JA3					
Pin	Header Name Circuit Net Name	MCU Pin	Pin	Header Name Circuit Net Name	MCU Pin
1	A0 JA3-A0	39	2	A1 JA3-A1	30
3	A2 JA3-A2	28	4	A3 JA3-A3	27
5	A4 JA3-A4	26	6	A5 JA3-A5	25
7	A6 JA3-A6	24	8	A7 JA3-A7	23
9	A8 JA3-A8	9	10	A9 JA3-A9	8
11	A10 JA3-A10	7	12	A11 JA3-A11	4
13	A12 JA3-A12	70	14	A13 JA3-A13	71
15	A14 JA3-A14	74	16	A15 JA3-A15	75
17	D0 JA3-D0	51	18	D1 JA3-D1	52
19	D2 JA3-D2	53	20	D3 JA3-D3	54
21	D4 JA3-D4	55	22	D5 JA3-D5	56
23	D6 JA3-D6	57	24	D7 JA3-D7	58
25	RDn JA3-RDn	99	26	WR / SDWE JA3-WRn	16 / NC
27	CSa JA3-CSa	43	28	CSb JA3-CSb	98
29	D8 JA3-D8	59	30	D9 JA3-D9	61
31	D10 JA3-D10	63	32	D11 JA3-D11	65
33	D12 JA3-D12	66	34	D13 JA3-D13	67
35	D14 JA3-D14	68	36	D15 JA3-D15	69
37	A16 JA3-A16	76	38	A17 JA3-A17	77
39	A18 JA3-A18	78	40	A19 JA3-A19	79
41	A20 JA3-A20	80	42	A21 NC	NC
43	A22 NC	NC	44	SDCLK JA3-BCLK	1
45	CSc / Wait JA3-45PIN	97 / 96	46	ALE / SDCKE JA3-ALE	96 / NC
47	HWRn / DQMH JA3-WRHn	17 / NC	48	LWRn / DQML JA3-WRLn	16 / NC
49	CAS NC	NC	50	RAS NC	NC

Table 7-4 below lists the connections of the application header, JA5.

Table 7-4: Application Header JA5 Connections

Application Header JA5					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	ADC4 JA5-ADC4	85	2	ADC5 JA5-ADC5	84
3	ADC6 JA5-ADC6	83	4	ADC7 JA5-ADC7	82
5	CAN1TX JA5-CAN1TX	41	6	CAN1RX JA5-CAN1RX	40
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 JA5-9PIN	100 / 38 / 100	10	IRQf / M2_HSIN2 JA5-M2HSIN2	7
11	M2_UD JA5-M2UD	81	12	M2_Uin JA5-M2UIN	96
13	M2_Vin JA5-M2VIN	97	14	M2_Win JA5-M2WIN	98
15	M2_Toggle JA5-M2TOGGLE	40	16	M2_POE JA5-M2POE	43
17	M2_TRCCLK JA5-M2TRCCLK	8	18	M2_TRDCLK JA5-M2TRDCLK	9
19	M2_UP JA5-M2UP	45	20	M2_Un JA5-M2UN	48
21	M2_VP JA5-M2VP	46	22	M2_Vn JA5-M2VN	49
23	M2_WP JA5-M2WP	47	24	M2_Wn JA5-M2WN	50

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	DREQ NC	NC	2	DACK NC	NC
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX JA6-RS232TX	NC	6	RS232RX JA6-RS232RX	NC
7	SCIbRX JA6-RXDb	20	8	SCIbTX JA6-TXDb	22
9	SCIcTX JA6-TXDc	66	10	SCIbCK JA6-SCKb	21
11	SCIcCK JA6-SCKc	96	12	SCIcRX JA6-RXDc	67
13	M1_Toggle JA6-M1TOGGLE	99	14	M1_Uin JA6-M1UIN	96
15	M1_Vin JA6-M1VIN	97	16	M1_Win JA6-M1WIN	98
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

7.2 Microcontroller Pin Headers

This RSK is fitted with MCU pin headers, which are used to access all the MCU's pins.
Table 7-6 below lists the connections of the microcontroller pin header, J1.

Table 7-6: Microcontroller Pin Header, J1

Microcontroller Pin Header J1					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	JA3-BCLK	1	2	EMLE	2
3	GROUND	-	4	P00	4
5	NC	NC	6	MD_FINED	6
7	P01	7	8	PE4	8
9	PE3	9	10	RESn	10
11	P37	11	12	GROUND	-
13	JA2-EXTAL	13	14	UC_VCC	-
15	JA2-NMIn	15	16	PE1	16
17	PE0	17	18	E1-TRSTn	18
19	E1-TMS	19	20	PD5	20
21	PD4	21	22	PD3	22
23	JA3-A7	23	24	PD1	24
25	PD0	25	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-7 below lists the connections of the microcontroller pin header, J2.

Table 7-7: Microcontroller Pin Header, J2

Microcontroller Pin Header J2					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	PB7	26	2	PB6	27
3	PB5	28	4	UC_VCC	-
5	PB4	30	6	GROUND	-
7	PB3	32	8	PB2	33
9	PB1	34	10	PB0	35
11	PMOD1-MISO	36	12	PMOD1-SCK	37
13	JA5-M2ENC	38	14	PA2	39
15	PA1	40	16	PA0	41
17	UC_VCC	-	18	P96	43
19	GROUND	-	20	P95	45
21	P94	46	22	P93	47
23	P92	48	24	P91	49
25	JA5-M2WN	50	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-8 below lists the connections of the microcontroller pin header, J3.

Table 7-8: Microcontroller Pin Header, J3

Microcontroller Pin Header J3					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	P76	51	2	P75	52
3	P74	53	4	P73	54
5	P72	55	6	P71	56
7	P70	57	8	P33	58
9	P32	59	10	UC_VCC	-
11	P31	61	12	GROUND	-
13	P30	63	14	P27	64
15	P24	65	16	P23	66
17	P22	67	18	P21	68
19	P20	69	20	P65	70
21	P64	71	22	AVCC0-2	72
23	AVSS0-2	73	24	P63	74
25	P62	75	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

Table 7-9 below lists the connections of the microcontroller pin header, J4.

Table 7-9: Microcontroller Pin Header, J4

Microcontroller Pin Header J4					
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	P61	76	2	P60	77
3	P55	78	4	P54	79
5	P53	80	6	JA5-M2UD	81
7	JA5-ADC7	82	8	JA5-ADC6	83
9	JA5-ADC5	84	10	JA5-ADC4	85
11	PH4	86	12	JA1-ADC3	87
13	JA1-ADC2	88	14	JA1-ADC1	89
15	P40	90	16	PH0	91
17	AVCC0-2	92	18	AVCC0-2	93
19	AVSS0-2	94	20	AVSS0-2	95
21	P82	96	22	P81	97
23	P80	98	24	P11	99
25	P10	100	26	NC	NC
27	NC	NC	28	NC	NC
29	NC	NC	30	NC	NC
31	NC	NC	32	NC	NC
33	NC	NC	34	NC	NC
35	NC	NC	36	NC	NC

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK board must be connected to a PC via an E1/E20/E2 Lite debugger. An E1/E2 Lite debugger is supplied with this RSK product.

For further information regarding the debugging capabilities of the E1/E20/E2 Lite debuggers, refer to E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot Modes (SCI), which are configured on the RSK board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX66T Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 Emulator or E2 Emulator Lite (as supplied with this RSK) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer RX Family E1/E20 Emulator User's Manual (R20UT0398EJ) or E2 Emulator Lite User's Manual (R20UT3240EJ).

8.5 Address Space

For the MCU address space details, refer to the 'Address Space' section of RX66T Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX66T Group microcontrollers refer to the RX66T Group Hardware Manual.

For information about the RX assembly language, refer to the RX Family Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 8 of the "*Quick Start Guide*"

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

Trademarks

All brand or product names used in this manual are trademarks or registered trademarks of their respective companies or organisations.

Copyright

REVISION HISTORY	RX66T Group Renesas Starter Kit for RX66T User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Sep 30, 2018	—	First Edition issued
1.10	Nov 29, 2019	20	5.7 SERIAL-TXD SCI1 Transmit Signal and SCI11 Transmit Signal port and pin corrected
			5.7 SERIAL-RXD SCI1 Receive Signal and SCI11 Receive Signal port and pin corrected

RX66T Group
Renesas Starter Kit for RX66T User’s Manual

Publication Date: Rev.1.00 Sep 30, 2018
Rev.1.10 Nov 29, 2019

Published by: Renesas Electronics Corporation