User's Manual

Target Board Kit S3A1 (TB-S3A1)

User's Manual

Renesas Synergy™ Platform
Synergy Tools & Kits
Kits: TB-S3A1 v1.0

Renesas Electronics
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This Renesas Synergy™ Development Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Renesas Synergy™ Development Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Renesas Synergy™ Platform

Target Board Kit S3A1 (TB-S3A1)

Contents

1. Overview

The Target Board Kit S3A1 (TB-S3A1) enables developers get started with initial firmware development and evaluation of the Synergy Software Package (SSP) on the S3A1 MCU Group.

- Renesas Synergy™ S3A1 Microcontroller Group
  - R7FS3A17C3A01CFB
  - 144-pin Quad Flat Pack package
  - 48 MHz Arm® Cortex® M4 core with FPU
  - 192 KB SRAM
  - 1 MB code flash memory
  - 8 KB data flash memory
- Connectivity
  - A Device USB connector for the Main MCU
  - SEGGER J-Link® On-Board interface for debugging and programming of the S3A1 MCU. A 10-pin JTAG/SWD interface is also provided for connecting optional external debuggers and programmers.
  - Two PMOD connectors, allowing use of appropriate PMOD compliant peripheral plug-in modules for rapid prototyping
  - Pin headers for access to power and signals for the Main MCU
- Multiple clock sources
  - Main MCU oscillator crystals, providing precision 12.000 MHz and 32,768 Hz reference clocks
  - Additional low-precision clocks are available internal to the Main MCU
- MCU reset push button switch
- MCU boot configuration jumper
- General Purpose I/O ports
  - One jumper to allow measuring Main MCU current
  - Copper jumpers on PCB bottom side for configuration and access to a selected MCU signals
- Operating voltage
  - External 5V input through the Debug USB connector supplies the on-board power regulator to power the Target Board logic and interfaces. Alternatively, 5 V or 3.3 V may be supplied through alternate locations on the Target Board.
- A two-color board status LED indicating availability of regulated power and connection status of the J-Link interface
- A red User LED, controlled by the Main MCU firmware
- A User Push-Button switch, User Capacitive Touch sensor (button), and an optional User Potentiometer, all of which are controlled by the Main MCU firmware

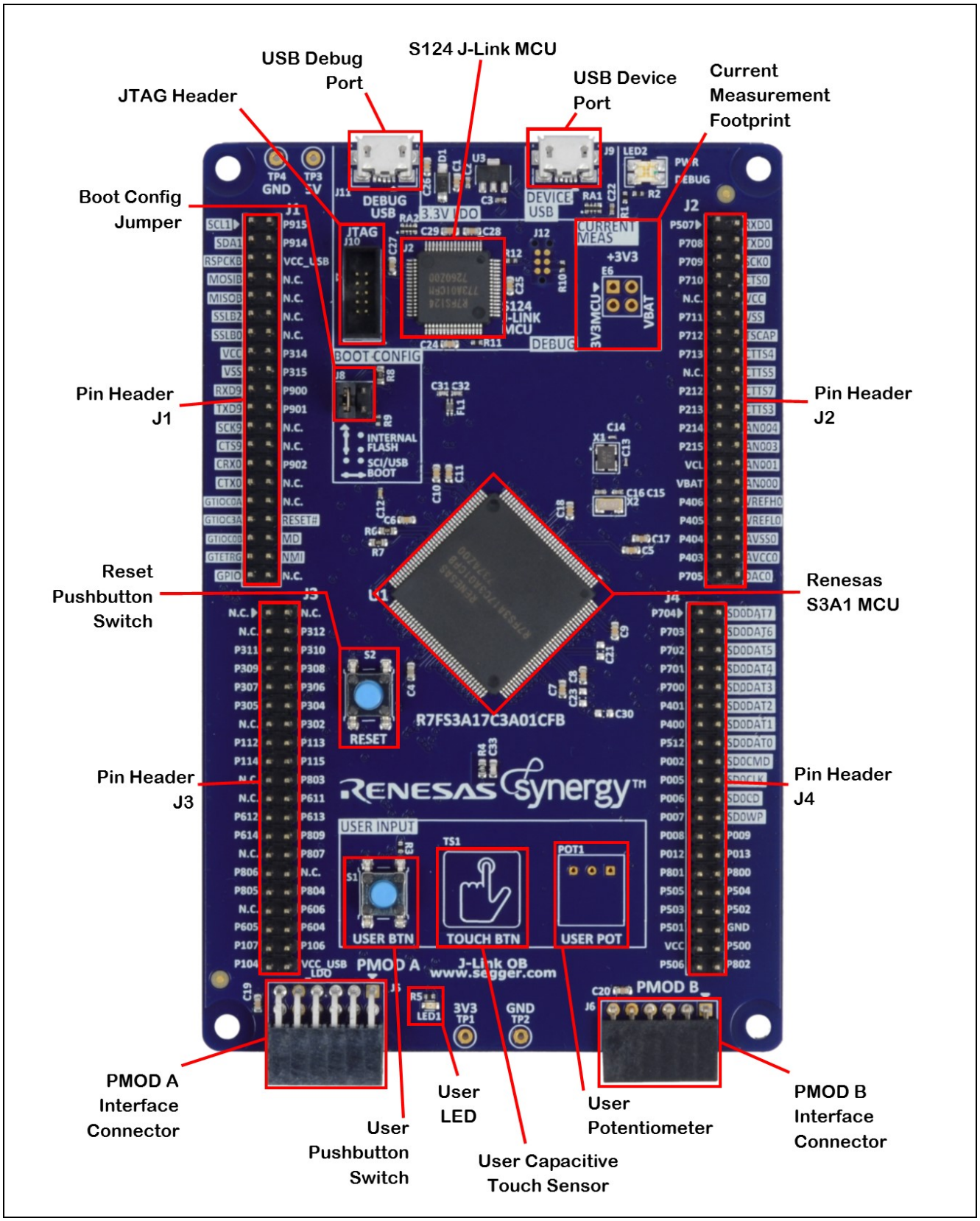


Figure 1. TB-S3A1 Top Side

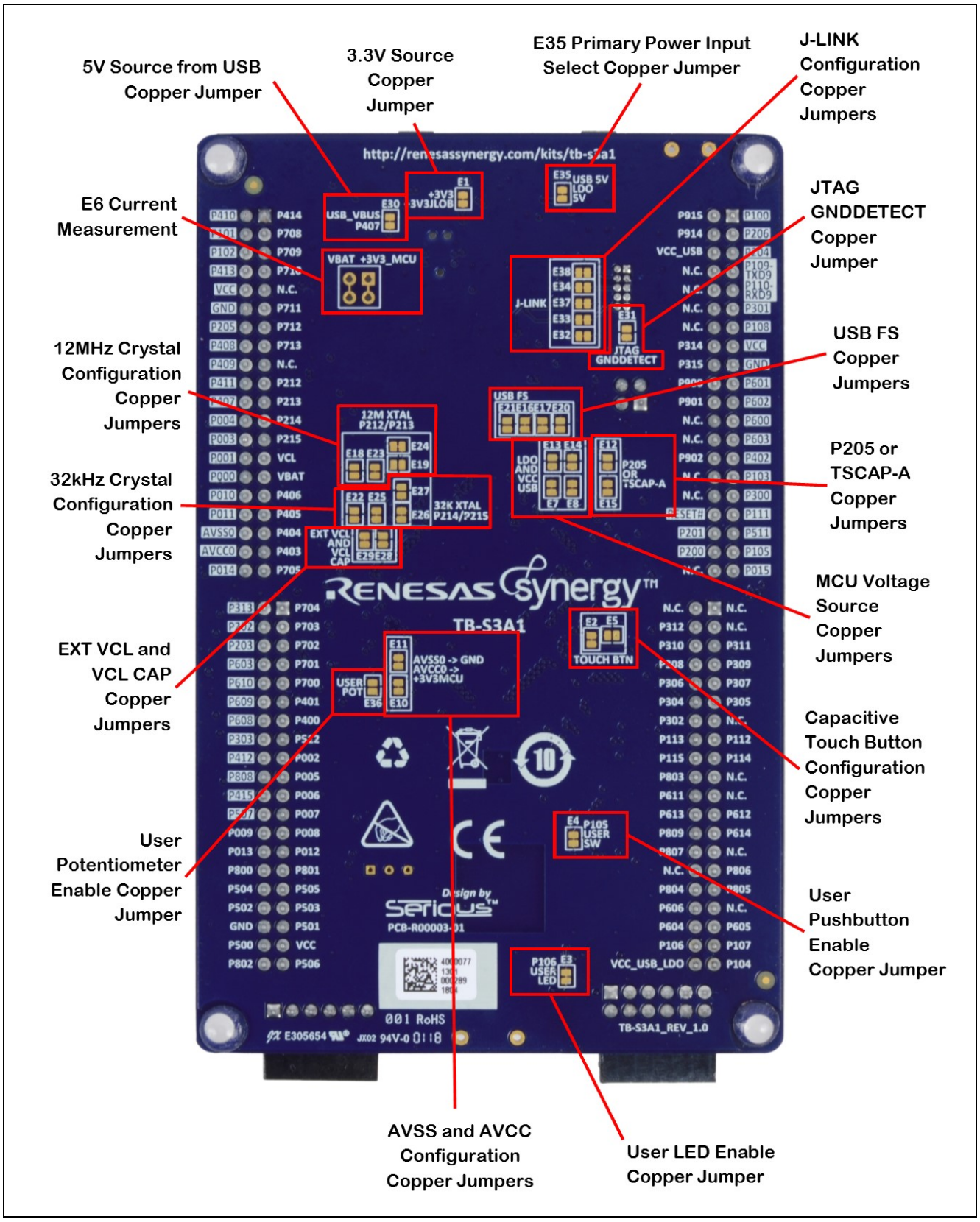


Figure 2. TB-S3A1 Bottom Side

2. Kit Contents

The following components are included in the Target Board Kit (TB-S3A1):

- 1x TB-S3A1 board
- 1x USB Type-A to USB Micro-B cable

3. Getting Started with Embedded Application Development on TB-S3A1

To develop and execute embedded applications on the TB-S3A1 using the Synergy Platform, Synergy Software Package and development tools are required to be installed on your computer.

Step 1: Create My Renesas Account (if you do not have one already)

You need a **My Renesas** account to download software, development tools, and application projects. Log in to or Sign up for a **My Renesas** account at www.update.renesas.com/SSO/login.

Step 2: Download and Install Synergy Software Package and Development Tools

The Synergy Software Package, J-Link USB drivers, and one of the two supported tool chains are bundled and available as single downloadable file as follows:

A. **IAR Platform Installer** installs Synergy Software Package and IAR Embedded Workbench® for Renesas Synergy™ IDE with IAR complier and J-Link USB drivers.
Download from www.renesas.com/synergy/ewsynergy.

B. **e² studio Platform Installer** installs Synergy Software Package and e² studio for Synergy IDE with IAR complier and J-Link USB drivers.
Download from www.renesas.com/synergy/e2studio.

Note: The TB-S3A1 uses J-Link® On-Board (OB) debug interface. While J-Link drivers are necessary to establish debug connection between the host PC and the TB-S3A1, they are not required to run the Out-of-Box (OoB) Demonstration (Blinky) Application that the TB-S3A1 comes pre-programmed with. Refer to the *TB-S3A1 Quick Start Guide* for more details.

Step 3: Explore Existing Application Projects for the TB-S3A1

Renesas provides several application projects to demonstrate different capabilities of the S3A1 MCU Group. These application projects can also serve as a good starting point for you to develop your custom applications. Application projects available for the TB-S3A1 are listed at http://www.renesas.com/synergy/tb-s3a1.

Notes: 1. Every application project includes the project files, an application note, and instructions to import the application project.
2. On downloading the application project from the website to your computer, the application projects have to be built using one of the two supported tool chains before they can be downloaded on to the TB-S3A1 board.

4. TB-S3A1 Hardware Details

4.1 Jumpers and DIP Switch Settings

4.1.1 Copper Jumpers

Copper jumpers are of two types, designated **trace-cut** and **solder-bridge**.

A **trace-cut jumper** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **solder-bridge jumper** is provided with two isolated pads that may be joined together by one of three methods:

- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMT resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-Ohm resistor shorts the pads together.

The silk screen overlay printing around a solder-bridge jumper is a box with a gap in the lines adjacent to the isolation region between the pads.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for trace-cut jumpers.) The connection is considered **open** if there is no electrical connection between the pads (default for the solder-bridge jumpers.)

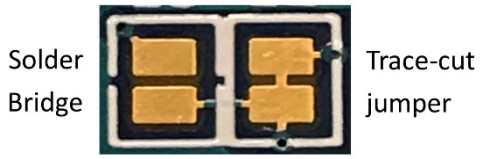


Figure 3. Copper Jumpers

4.1.2 Default Board Configuration

The following table describes the default settings for each jumper on the TB-S3A1 Target Board. This includes traditional pin jumpers (J*x* designation) and copper jumpers (E*x* designation.)

The Circuit Group for each jumper is the designation found in the board schematic. Functional details for many of the listed jumpers may be found in section 5.4, Connectivity and Settings and section 5.6, Additional Features.

Table 1. Default Jumper Settings

Location	Circuit Group	Default Open/Closed	Function
J8	MCU Mode Config	Shunt on pins 1-2	Sets the MCU Mode to boot from Internal Flash
E18	12M Crystal	Open	Connects signal P213 to MCU
E19		Open	Connects signal P212 to MCU
E23		Closed	Connects 12.000 MHz Crystal to MCU
E24		Closed	Connects 12.000 MHz Crystal to MCU
E1	3.3V Linear Regulator	Closed	Alternate 3.3V source (+3V3JLOB)
E22	32K Crystal	Open	Connects signal P215 to MCU
E25		Closed	Connects 32.768 kHz Crystal to MCU
E26		Closed	Connects 32.768 kHz Crystal to MCU
E27		Open	Connects signal P214 to MCU

Location	Circuit Group	Default Open/Closed	Function
E10	AVCC0-> +3V3MCU	Closed	Connects +3V3MCU to AVCC0
E11	AVSS0->GND	Closed	Connects AVSS0 to Ground
E2	Capacitive Touch Button	Closed	Enable/Disable Capacitive Touch Button
E5		Open	Connects signal P115J to Capacitive Touch Button
E28	EXT VCL and VCL CAP	Open	Connects VCL to MCU
E29		Closed	Connects MCU pin 15 (VCL) to capacitor
E32	J-Link	Closed	Connects the S124 MCU to the J-Link signal JLED
E33		Closed	Connects the S124 MCU to the J-Link signal RESET#
E34		Closed	Connects the S124 MCU to the J-Link signal TDO(/SWO) P109
E37		Closed	Connects the S124 MCU to the J-Link signal P108/SWDIO
E38		Closed	Connects the S124 MCU to the J-Link signal P300/SWCLK
E35	J-Link OB USB	Closed	Connects the J-Link OB USB 5V input to the primary 5V->3.3V voltage regulator
E31	JTAG Connector	Open	JTAG Ground Detect. Connects the JTAG connector pin 9 to Ground.
E13	LDO and VCC USB	Open	Connects VCC_USB_LDO to MCU pin 41
E14		Open	Connects VCC_USB_LDO to MCU pin 40
E7		Closed	Connects +3V3MCU to MCU pin 41
E8		Closed	Connects +3V3MCU to MCU pin 40
E12	P205 or TSCAP-A	Open	Connects MCU pin 43 to signal P205
E15		Closed	Connects MCU pin 43 to capacitor
E30	USB Device Interface	Closed	Connects the Device USB 5 V input to the MCU
E16	USB FS	Closed	Connects MCU pin 38 to signal USB_N
E17		Closed	Connects MCU pin 39 to signal USB_P
E20		Open	Connects MCU pin 39 to signal USBPH_P
E21		Open	Connects MCU pin 38 to signal USBPH_N
E3	User LED	Closed	Enable/Disable User LED
E36	User Potentiometer	Open	Enable/Disable User Potentiometer
E4	User Push-Button	Closed	Enable/Disable User Push-Button switch
E6	VBAT +3V3_MCU	Closed	Dual Jumper. Pins 1-3 connect +3V3 to +3V3MCU. Pins 2-4 connect +3V3 to VBAT.

5. Hardware Layout

5.1 System Block Diagram

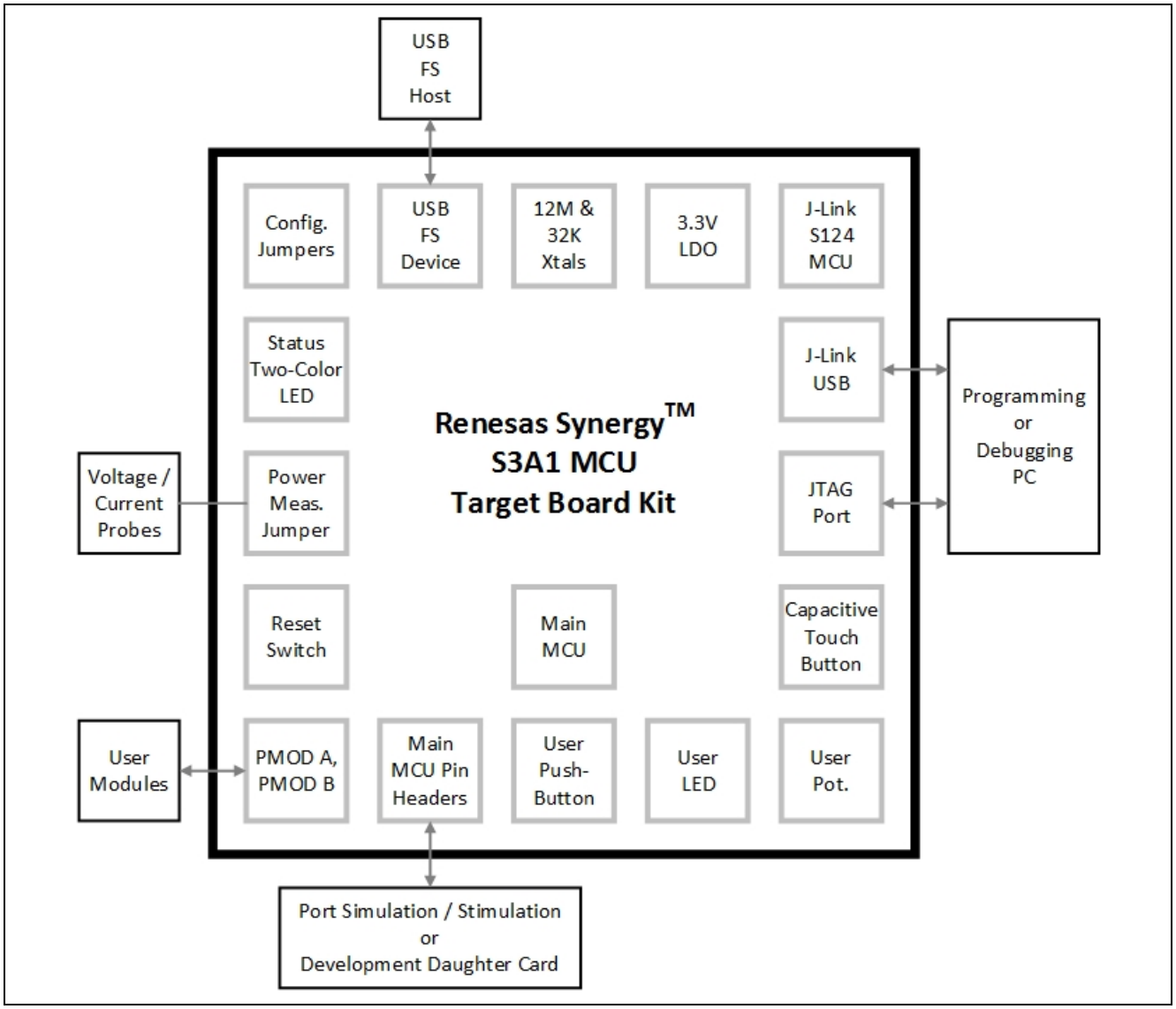


Figure 4. TB-S3A1 Block Diagram

5.2 Power Requirements

TB-S3A1 is designed for 3.3 V operation. Please note that this also means that 5 V PMOD devices cannot be used together with the TB-S3A1 unless they are powered separately.

The total current available from the LDO regulator for all connected circuits is 600 mA or less, depending the 5 V power source used.

5.2.1 Power Supply Options

TB-S3A1 can be powered in several different methods as described in this section.

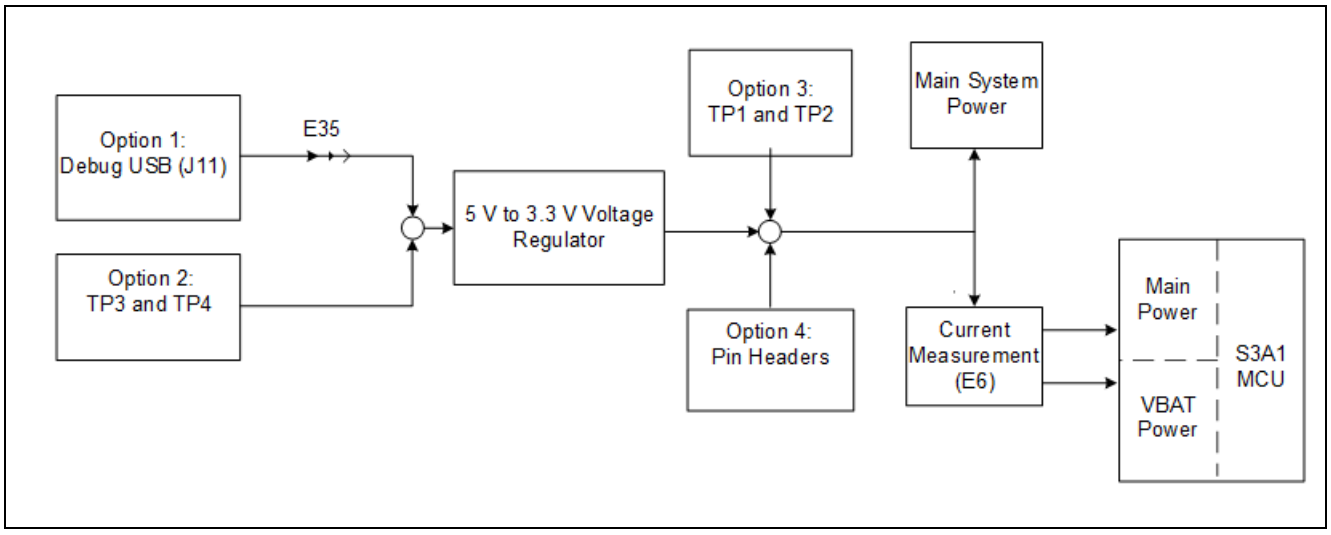


Figure 5. Power Supply Options

5.2.1.1 Option 1: Debug USB (Default)

The default power source is 5 V supplied from an external USB host to the USB Debug connector labelled **DEBUG USB** on the top surface of the board. A low drop-out regulator (LDO) is used to convert the 5 V signal to 3.3 V, and is used to power the MCU and any connected devices.

Copper jumper E35 selects the source for the primary power input to the LDO regulator. By default, this jumper is configured to provide power through the Debug USB connector. Copper jumper E35 is closed for this configuration.

5.2.1.2 Option 2: Test Points TP3 and TP4

TB-S3A1 can also be powered by installing a 5 V power source across TP3 (positive input) and TP4 (negative input). Copper jumper E35 must be opened to enable powering the board using these test points.

The on-board Low Dropout Regulator (see section 5.3, Major Components) has an input voltage range of +3.3 V to +5.5 V, and a built-in current limit of 600 mA. Make sure any external power source connected to TP3 and TP4 meets these requirements.

Figure 6. USB Debug Connector (J11), TP3, and TP4 on Target Board

5.2.1.3 Option 3: Test Points TP1 and TP2

TB-S3A1 can also be powered by installing a 3.3 V source across TP1 (positive input) and TP2 (negative input). Copper jumper E35 must be open to enable powering the board using these test points.

Figure 7. TP1, TP2 and LED1 on Target Board

These test points supply voltage directly to the S3A1 MCU, the S124 J-Link MCU, and other on-board circuitry. Use caution to ensure that any voltage connected in this manner meets the power requirements for the active features. Power sources that are outside of the published operating range for the active devices may cause degraded performance or damage the board.

5.2.1.4 Option 4: Pin Headers

TB-S3A1 can also be powered through the following pin-headers on the board.

- J1 (pin J1-15 for +3.3 V, pin J1-17 for Return)
- J2 (pin J2-10 for +3.3 V, pin J2-12 for Return)
- J4 (pin J4-37 for +3.3 V, pin J4-36 for Return)

Copper jumper E35 must be open for any of these configurations.

The pin headers supply voltage directly to the S3A1 MCU, the S124 J-Link MCU, and other on-board circuitry. Use caution to ensure that any voltage connected in this manner meets the power requirements for the active features. Power sources that are outside of the published operating range for the active devices may cause degraded performance or damage the board.

See Section 4.5, Target board pin headers for more information on the Pin Headers.

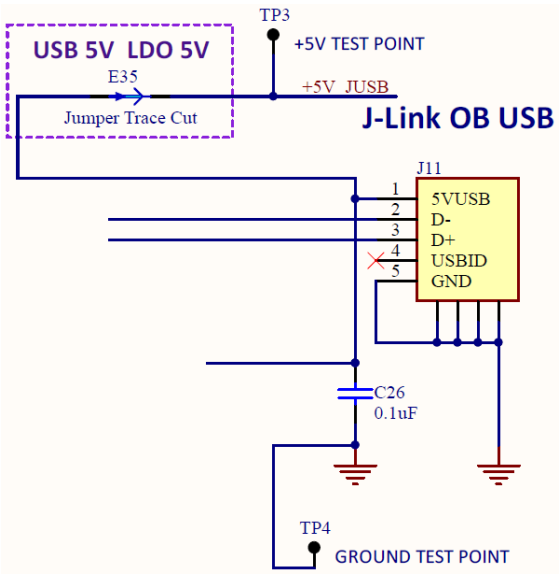


Figure 8. 5 V Power Input Circuit

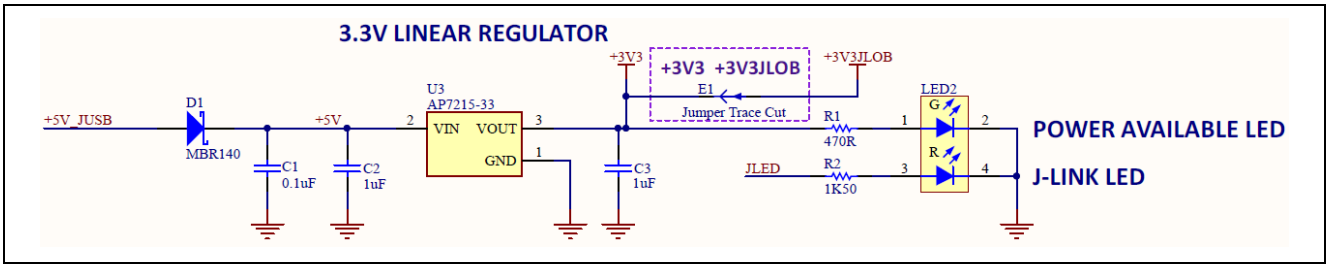


Figure 9. 3.3 V Power Regulator Circuit

5.2.2 Powering up the Board

When powered, the green LED to the right of the DEVICE USB connector (LED2) lights up.

The red LED in the same LED package functions as a status indicator for the J-Link On-Board debug interface on the board. If both LEDs in the LED2 package are lit, LED2 appears orange.

Figure 10. LED2 on Target Board (Top Side)

5.2.3 Battery Supply Configuration

An external battery may be connected according to the methods outlined in Section 4.2.1, Power supply options, providing it meets the minimum voltage and current requirements.

An external battery source may be connected to VBAT at Pin Header location J2-29 (J2-12 ground return) to maintain the MCU Real Time Clock (RTC) when other main power sources are disconnected from TB-S3A1.

5.2.4 Measuring Current Consumption

Pad 1 and 3 of copper jumper E6, which is a dual trace-cut jumper, allow measurement of +3V3 MCU supply current. Pad 2 and 4 of E6 allow measurement of VBAT supply current. Both traces are connected by default. These traces should be cut to enable power measurement. Care must be taken when cutting the trace to not cause damage to PCB layers below the trace.

Note that the actual current consumed by the S3A1 MCU is dependent on many factors, including ambient temperature, internal clock speed, input voltage level, and device activity. The actual current consumed by the MCU can vary from less than 1 mA to nearly 40 mA. Refer to the *S3A1 User's Manual* for more information on the electrical characteristics of the MCU.

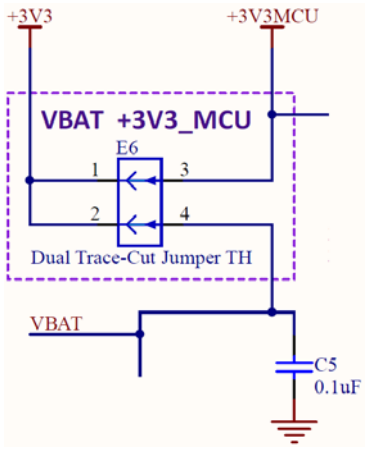


Figure 11. MCU Current Measurement Circuit

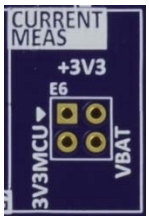


Figure 12. E6 on Target Board (Top Side)

Figure 13. E6 on Target Board (Bottom Side)

Once the shorting traces have been removed, there are several options to measure current:

- Pins can be installed that allow connection of a precision multi-meter or bench meter, or leaded current shunt to allow oscilloscope or data logger connection. When not measuring current, this allows easily installed and removed shunts to be used to short the jumper terminals.
- Another option is to install current sense resistors between pads 1 and 3 for +3V3 MCU, and between pads 2 and 4 for VBAT. Precision non-inductive film or foil resistors are recommended for use in this application, and the value of each resistor should be carefully considered.
  For example, if the expected current requirement for the +3V3 MCU supply voltage is 10 mA, and you would expect to measure a 10 mV drop across the current measurement resistor, then a 1.0 ohm resistor should be selected and installed.
  The actual value selected should be based on the operating conditions of the MCU for the specific application you are working on and the sensitivity of the measurement equipment used.

5.3 Major Components

- Main MCU
  - Renesas Synergy™ S3A1 MCU device, part number R7FS3A17C3A01CFB#AA0 (U1)
- J-Link MCU
  - Renesas Synergy™ S124 MCU device, part number R7FS124773A01CFM#AA0 (U2)
- USB Connectors
  - FCI, part number 10118192-0001LF (J9, J11)
    - Micro USB 2.0 Female connector
    - Primary communication with Main MCU and J-Link MCU
- Push-Buttons
  - C&K, part number PTS645SM43SMTR92 LFS (S1, S2)
    - Momentary push-button switch
    - Used for system reset and user defined functions
- LDO Regulator
  - Diodes Inc., part number AP7215-33YG-13 (U3)
    - Low-drop out linear regulator
    - Generates system 3.3 V from J-Link USB 5 V input
- PMOD A Connector
  - Samtec, part number SSW-106-02-F-D-RA (J5)
    - 12 pin right angle connector for PMOD A
- PMOD B Connector
  - Samtec, part number SSW-106-02-FM-S-RA (J6)
    - 6 pin right angle connector for PMOD B
- Pin Headers
  - Sullins, part number PRPC020DAAN-RC (J1, J2, J3, J4)
    - 40 position pin header, 0.1” pitch
    - Provides signal breakout and access for Main MCU signals
- System LED
  - Dialight, part number 598-8610-207F (LED2)
    - Dual color Red/Green LED
    - System status indicator for power and J-Link status
- User LED
  - Lite-On, part number LTST-C191KRKT (LED1)
    - User defined
    - Single color red LED as needed for user environment
- User Potentiometer
  - Bourns, part number 3352T-1-1-3LF (POT1)
    - User defined
    - Provides variable resistance as needed for user environment

5.4 Connectivity and Settings

Throughout this section, feature configuration using copper jumpers are described. See Section 4.1.1, Copper Jumpers for information on using copper jumpers.

5.4.1 Device USB

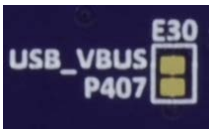
The Device USB Micro-B connection jack connects the Main MCU to an external USB Host, FS capable, allowing communications for testing and use of the Main MCU firmware. Power for the Target Board cannot be received from this connector. The DEVICE USB interface can detect the presence of power from the USB Host PC. USB Host power received at the DEVICE USB interface is not connected to the Target Board 5 V power bus.

Table 2. Device USB Connector (J9)

USB Device Connector		TB-S3A1
Pin	**Description**	**Signal/Bus**
1	+5VDC, connected to a sense voltage 2/3 divider to allow Main MCU sensing of Host presence	+5VUSB P407/USB_VBUS = 2/3(5VUSB)
2	Data-	P915/USB_DM
3	Data+	P914/USB_DP
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

Connections in Table 2 are based on the condition of copper jumpers E16, E17, E20, E21, and E30 matching their as-manufactured status. As-manufactured, E16 and E17 are closed, E20 and E21 are open, and E30 is closed.

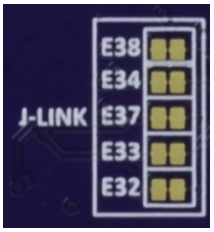
Alternatively, the Device USB signals to the Main MCU may be connected to MCU Pin Header J1. To enable this configuration, copper jumpers E16 and E17 should be open, E20 and E21 should be closed.



5.4.2 Debug USB

The Debug USB Micro-B connection jack connects the S124 J-Link MCU to an external USB Host, FS capable, allowing re-programming and debugging of the Main MCU firmware. Power for the Target Board may be received from this connector.

The J-Link OB interface is multiplexed with the JTAG interface, and can collectively be referred to as the Programming Interface. While the J-Link OB interface and the JTAG interface do not conflict, the J-Link OB signals may be isolated from the programming interface by changing the associated copper jumpers.



J-Link Disconnect Copper Jumpers E32, E33, E34, E37, and E38 connect the J-Link signals to the MCU programming interface. To isolate the J-Link signals from the JTAG interface, the copper jumpers must be open. To allow use of the J-Link interface, each copper jumper must be closed.

J-Link MCU Power Copper Jumper, E1, connects the main +3.3 V power to the J-Link +3.3 V power. The default condition for E1 is closed, which connects the J-Link MCU power to the main +3.3 V power. If J-Link signals are disconnected, the power to the J-Link MCU should also be removed by changing E1 to open.

Table 3. Debug USB Connector (J11)

DEBUG USB Connector		TB-S3A1
Pin	**Description**	**Signal/Bus**
1	+5VDC	+5V_JUSB
2	Data-	U2 USB_DM (U2-18)
3	Data+	U2 USB_DP (U2-19)
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

Three of the J-Link ports (P108, P109, and P300) conflict with the SPI interface, as shown in the following table.

Table 4. J-Link interface conflicts

Programming Interface		Conflicting Interface	
Port	**Use**	**Interface**	**Use**
P108	SWDIO/JTAG TMS	SPI	SSLB0 fixed function, J113
P109	SWO/JTAG TDO	SPI	MOSIB fixed function, J17
P300	SWCLK/JTAG TCK	GPT	GTIOC0A fixed function, J131

5.4.3 JTAG/SWD

A 10-pin Cortex Debug Connector is provided at J10.

Table 5. JTAG/SWD Connector (J10)

JTAG Connector			TB-S3A1
Pin	**JTAG pin name**	**SWD pin name**	**Signal/Bus**
1	VTref	VTref	+3V3
2	TMS	SWDIO	U1 P108/SWDIO (U1-51)
3	GND	GND	GND
4	TCK	SWCLK	U1 P300/SWCLK (U1-50)
5	GND	GND	GND
6	TDO	SWO	U1 P109 (U1-52)
7	Key	Key	N.C.
8	TDI	NC/EXTb	U1 P110 (U1-53)
9	GNDDetect	GNDDetect	N.C. (short E31 to connect to GND)
10	nSRST	nSRST	U1 RESET# (U1-38)

The Cortex® Debug Connector is fully described in the Arm® CoreSight™ Architecture Specification.

The J-Link MCU Power copper jumper and J-Link Disconnects copper jumpers may be open for proper operation of the JTAG interface to prevent interactions with the J-Link MCU. See Section 5.4.2, Debug USB for details.

If a JTAG adapter is in use that properly interprets the Arm® Cortex® 10-pin Debug connector assignment of pin 9 to GND, JTAG GNDDetect-copper jumper E31 should be closed. If the JTAG adapter used is one of several that may be confused or damaged by the presence of GND at pin 9, E31 should be open (as shipped).

The J-Link OB interface is multiplexed with the JTAG interface, and can collectively be referred to as the Programming Interface. While the J-Link OB interface and the JTAG interface do not conflict, the J-Link OB signals may be isolated from the programming interface by changing the copper jumpers as described in Section 5.4.2, Debug USB.

Four of the JTAG ports (P108, P109, P110 and P300) conflict with the SPI interface, as shown in the following table.

Table 6. JTAG Interface Conflicts

Programming Interface		Conflicting Interface	
Port	**Use**	**Interface**	**Use**
P108	TMS/J-Link SWDIO	SPI	SSLB0_B fixed function, J113
P109	TDO/J-Link SWO	SPI	MOSIB_B fixed function, J17
P110	TDI	SPI	MISOB_B fixed function, J19
P300	SWCLK	GPT	GTIOC0A_A fixed function, J131

5.4.4 LEDs

Two LEDs are provided on the TB-S3A1 Target Board. Target Board U1 is the Main MCU, and directly controls LED1. See Figure 6 for LED1 location, Figure 9 for LED2 location, and Figure 8 for LED2 circuit. Target Board U2 is the J-Link MCU, and controls the Red LED in LED2.

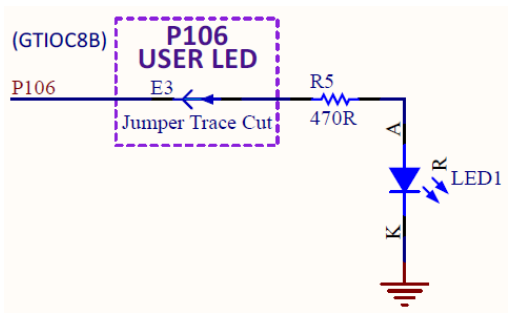


Figure 14. LED1 Control Circuit

The behavior of the LEDs is described in the following table.

Table 7. Target Board LED Functions

Designator	Color	Function	MCU control port	MCU pin
LED1	Red	User LED	U1 P106	U1-102
LED2	Red	J-Link Indicator	JLED (U2 P103)	U2-45
LED2	Green	3.3V Power Available	+3V3	N.A.

To disconnect the User LED from the MCU signal P106, copper jumper E3 must be open.

5.4.5 Switches

Two miniatures, momentary, mechanical push-button type SMT switches are mounted on the Target Board. Pressing the RESET Switch generates a reset signal to restart the Main MCU.

To disconnect the User Switch from the MCU signal P105/IRQ0, copper jumper E4 must be open.

Table 8. Target Board Switches

Designator	Function	MCU Control Port	MCU Pin
S1	User Switch	U1 P105/IRQ0	U1-103
S2	MCU Reset Switch	RESET#	U1-55

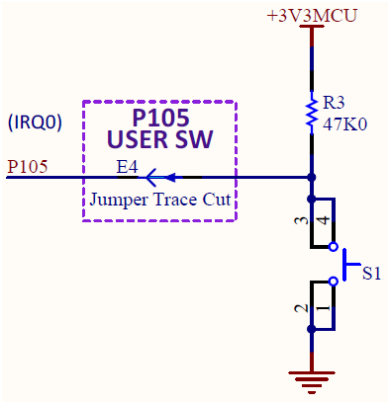


Figure 15. User Switch Circuit

Figure 16. User Switch (S1) on Target Board

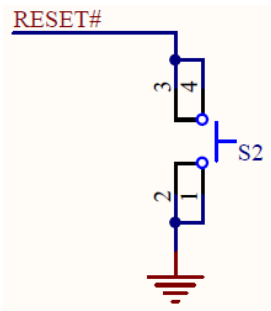


Figure 17. Reset Switch Circuit

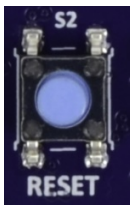


Figure 18. Reset Switch (S2) on Target Board

5.4.6 PMOD A

A 12-pin PMOD type 2A connector is provided at PMOD A. The interface is powered for 3.3 V modules only. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

Please note that signals on PMOD A are shared with Main MCU pin header J1 and J2. Care must be taken to ensure shared signals are not used concurrently.

Table 9. PMOD A Connector (J5)

PMOD A connector		**TB-S3A1**
Pin	**Description**	**Signal/Bus**
1	SS (low to select slave)	U1 P103, SSLA0_A (U1-72)
2	MOSI	U1 P101, MOSIA_A (U1-74)
3	MISO	U1 P100, MISOA_A (U1-75)
4	SCK	U1 P102, RSPCKA_A (U1-73)
5	GND	GND
6	VCC	+3V3
7	INT (slave to master)	U1 P104, IRQ1 (U1-71)
8	RESET (master to slave)	U1 P107, GPIO (U1-68)
9	Not Specified	U1 P111, GPIO (U1-54)
10	Not Specified	U1 P112, GPIO (U1-55)
11	GND	GND
12	VCC	+3V3

Limits of the 3.3 V regulator on the Target Board, and limits of the power source supplying that regulator (especially for USB Host devices), including the to-be-connected PMOD device, must be considered prior to connecting a module to a PMOD connector.

5.4.7 PMOD B

A 6-pin PMOD type 4 connector is provided at PMOD B. The interface is powered for 3.3 V modules only. The Main MCU acts as the UART DCE, and the connected module acts as the UART DTE. This interface may additionally be re-configured in firmware as some other PMOD types.

Please note that signals on PMOD B are shared with the Main MCU pin header J1 and J2. Care must be taken to ensure shared signals are not used concurrently.

Table 10. PMOD B Connector (J6)

PMOD B connector		**TB-S3A1**
Pin	**Description**	**Signal/Bus**
1	CTS (from module)	U1 P403, CTS1 (U1-4)
2	TXD	U1 P401, TXD1 (U1-2)
3	RXD	U1 P402, RXD1 (U1-3)
4	RTS (from Main MCU)	U1 P400, GPIO (U1-1) (for RTS by Main MCU firmware)
5	GND	GND
6	VCC	+3V3

Limits of the 3.3 V regulator on the Target Board, and limits of the power source supplying that regulator (especially for USB Host devices), including the to-be-connected PMOD device, must be considered prior to connecting a module to a PMOD connector.

5.4.8 User Capacitive Touch Button

A capacitive sensor region for use as a Capacitive Touch button is provided in the board USER INPUT region. A support circuit, TSCAP, is required for proper operation of Capacitive Touch button(s) by the Main MCU.

To disconnect the Capacitive Touch Button from the MCU, copper jumper E2 must be open.

To connect MCU signal P115 to pin header J3, copper jumper E5 must be closed.

Note: Capacitor C33 is optional. This design does not include a dielectric overlay, so C33 is added to reduce the sensitivity of the Capacitive Touch Button. This capacitor is not required by the MCU specification.

Table 11. Target Board Capacitive Touch Button Sensor

Designator	**Function**	**MCU Control Port**	**MCU Pin**
TS1	Capacitive Touch Button	U1 P115 (TS35)	U1-80
-	TSCAP Support	U1 P205 (TSCAP-A)	U1-43

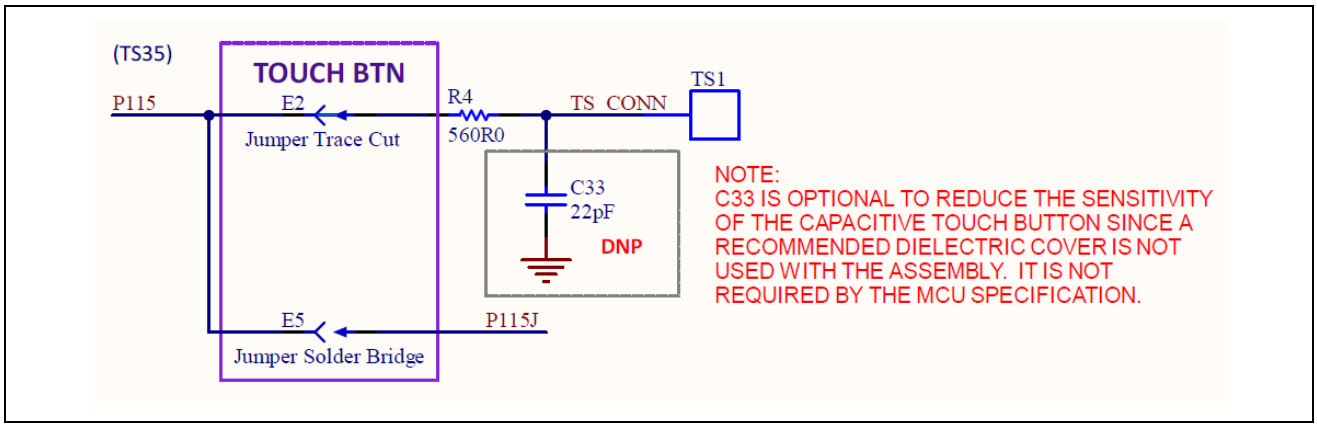


Figure 19. Capacitive Touch Button Circuit

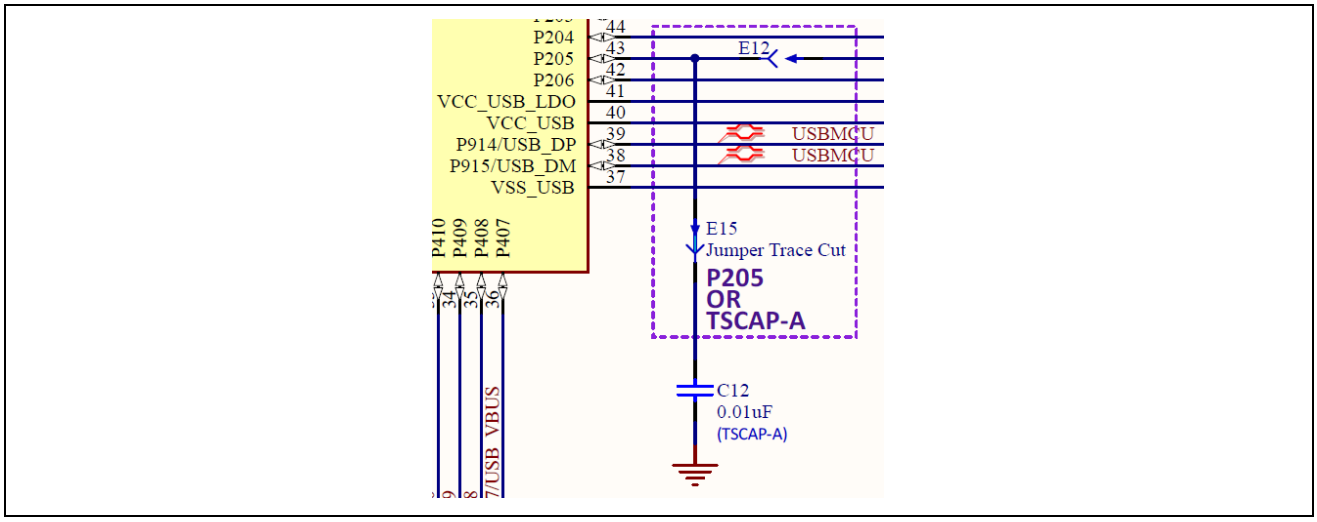


Figure 20. Capacitive Touch TSCAP Circuit

Figure 21. Capacitive Touch Button on Target Board (Top)

5.5 Pin Headers

The Target Board pin headers, J1, J2, J3, and J4, provide access to all Main MCU interface signals, and to voltages for all Main MCU power ports.

Fixed Function Pin Assignments

For consistency across all Synergy Target Board Kits, some pin assignments on the headers have **fixed function** signal assignments. This provides specific signals and functions to be at a common pin header location on all Target Boards for a particular Synergy MCU Group (For example, S1/S3/S5/S7) and where possible, across all Synergy Target Boards.

On the TB-S3A1, 40 pins of the pin headers are set aside for **fixed function** assignment. These pins are odd-numbered pins of J1 and even-numbered pins of J2.

Pin Header Fixed Function Pins are labeled on the Target Board with dark text on a white background. Pins that are not Fixed Function pins are labeled with white text on a dark background. On the top side of the board is the functional label for the fixed location. On the bottom side of the board is the port information for the same pin.

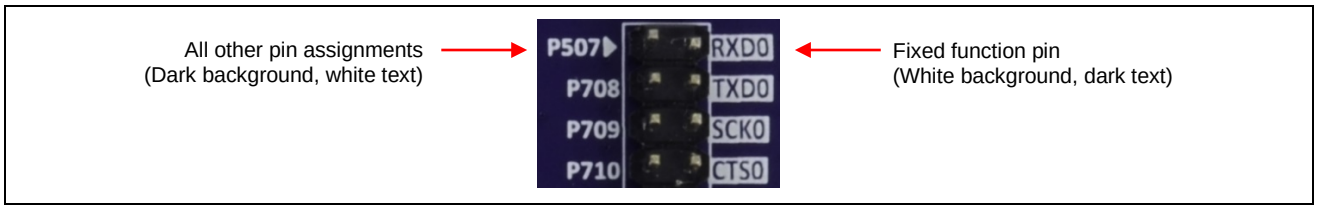


Figure 22. Fixed Function Pin Label Example

There are several pins in the headers that are secondary fixed function pins. These secondary fixed function pins share common pin assignments with other Target Boards having the Main MCUs with the same functionality. The secondary fixed function pins are also labeled with the top side having a functional label, and bottom side having a port label.

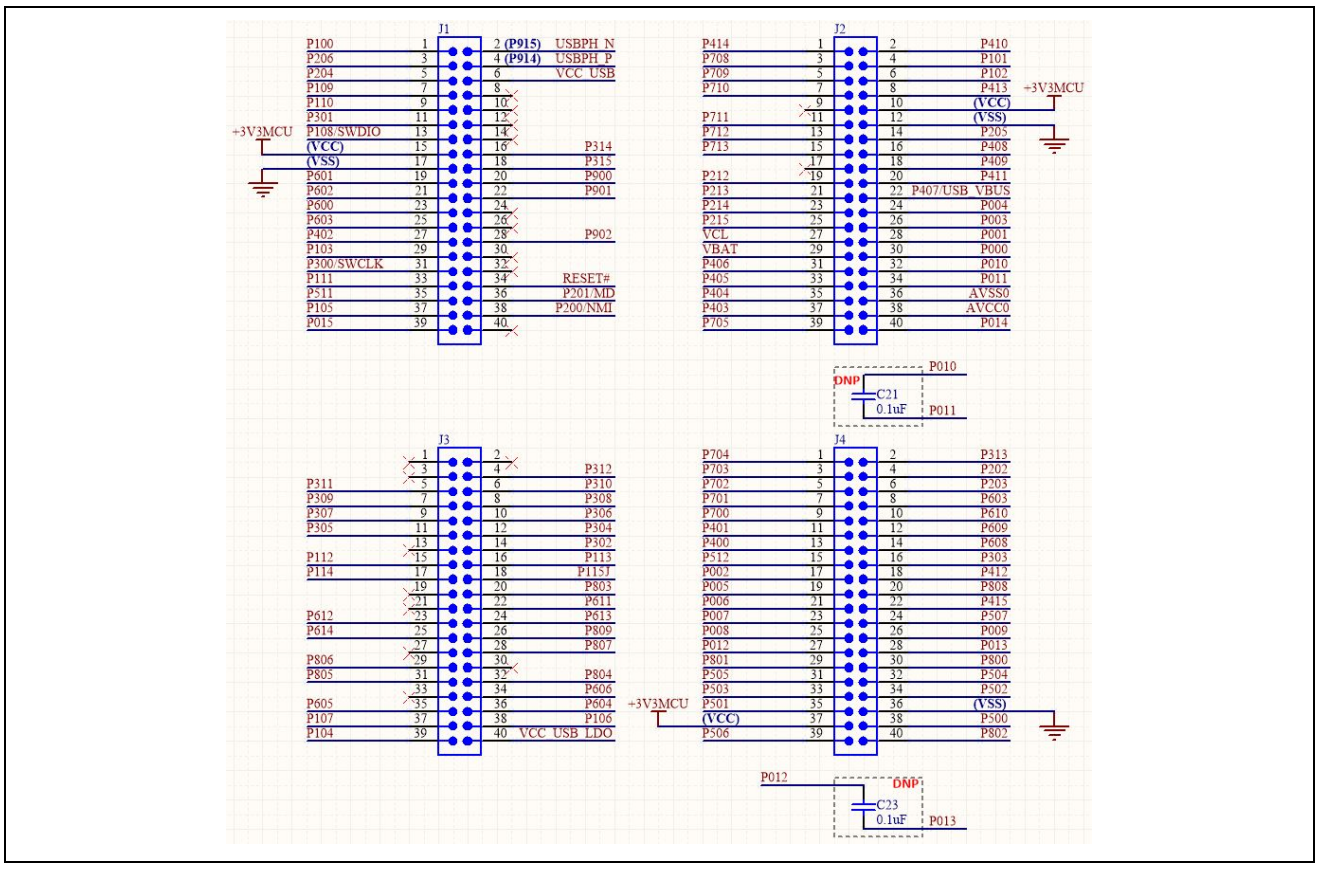


Figure 23. TB-S3A1 Pin Headers Circuit

5.5.1 Pin Header J1

Pin header J1 is a 2-column by 20-row through-hole pin header on 2.54 mm centers.

Table 12. Pin Header J1 Pin Assignment

144p S3A1 Pin	S3A1 Signal	J1 Pins		S3A1 Signal	144p S3A1 Pin
108	P100	1	2	P915/USB_DM	38
42	P206	3	4	P914/USB_DP	39
44	P204	5	6	VCC_USB	40
74	P109/TDO/SWO	7	8	(None)	NC
75	P110/TDI	9	10	(None)	NC
71	P301	11	12	(None)	NC
73	P108/TMS/SWDIO	13	14	(None)	NC
90	VCC	15	16	P314	48
91	VSS	17	18	P315	49
97	P601	19	20	P900	50
96	P602	21	22	P901	51
98	P600	23	24	(None)	NC
95	P603	25	26	(None)	NC
3	P402	27	28	P902	52
105	P103	29	30	(None)	NC
72	P300/TCK/SWCLK	31	32	(None)	NC
76	P111	33	34	RES	55
144	P511	35	36	P201/MD	56
103	P105	37	38	P200	57
123	P015	39	40	(None)	NC

Color Key:

Primary Fixed Function Pins
Secondary Fixed Function Pins

5.5.2 Pin Header J2

Pin header J2 is a 2-column by 20-row through-hole pin header on 2.54 mm centers.

Table 13. Pin Header J2 Pin Assignment

144p S3A1 Pin	S3A1 Signal	J2 Pins		S3A1 Signal	144p S3A1 Pin
29	P414	1	2	P410	33
27	P708	3	4	P101	107
26	P709	5	6	P102	106
25	P710	7	8	P413	30
NC	(None)	9	10	VCC	21
24	P711	11	12	VSS	18
23	P712	13	14	P205	43
22	P713	15	16	P408	35
NC	(None)	17	18	P409	34
20	P212/EXTAL	19	20	P411	32
19	P213/XTAL	21	22	P407	36
17	P214/XCOUT	23	24	P004	136
16	P215/XCIN	25	26	P003	137
15	VCL	27	28	P001	139
14	VBATT	29	30	P000	140
7	P406	31	32	P010/VREFH0	130
6	P405	33	34	P011/VREFL0	129
5	P404	35	36	AVSS0	128
4	P403	37	38	AVCC0	127
13	P705	39	40	P014	124

Color Key:

Primary Fixed Function Pins
Secondary Fixed Function Pins

5.5.3 Pin Header J3

Pin header J3 is a 2-column by 20-row through-hole pin header on 2.54 mm centers.

Table 14. Pin Header J3 Pin Assignment

144p S3A1 Pin	S3A1 Signal	J3 Pins		S3A1 Signal	144p S3A1 Pin
NC	(None)	1	2	(None)	NC
NC	(None)	3	4	P312	58
59	P311	5	6	P310	60
61	P309	7	8	P308	62
63	P307	9	10	P306	64
65	P305	11	12	P304	66
NC	(None)	13	14	P302	70
77	P112	15	16	P113	78
79	P114	17	18	P115	80
NC	(None)	19	20	P803	112
NC	(None)	21	22	P611	86
87	P612	23	24	P613	88
89	P614	25	26	P809	68
NC	(None)	27	28	P807	82
81	P806	29	30	(None)	NC
99	P805	31	32	P804	100
NC	(None)	33	34	P606	92
93	P605	35	36	P604	94
101	P107	37	38	P106	102
104	P104	39	40	VCC_USB_LDO	41

Color Key:

Secondary Fixed Function Pins

5.5.4 Pin Header J4

Pin header J4 is a 2-column by 20-row through-hole pin header on 2.54 mm centers.

Table 15. Pin Header J4 Pin Assignment

144p S3A1 Pin	S3A1 Signal	J4 Pins		S3A1 Signal	144p S3A1 Pin
12	P704	1	2	P313	47
11	P703	3	4	P202	46
10	P702	5	6	P203	45
9	P701	7	8	P603	95
8	P700	9	10	P610	85
2	P401	11	12	P609	84
1	P400	13	14	P608	83
143	P512	15	16	P303	69
138	P002	17	18	P412	31
135	P005	19	20	P808	67
134	P006	21	22	P415	28
133	P007	23	24	P507	120
132	P008	25	26	P009	131
126	P012/VREFH	27	28	P013/VREFL	125
110	P801	29	30	P800	109
118	P505	31	32	P504	117
116	P503	33	34	P502	115
114	P501	35	36	VSS	122
121	VCC	37	38	P500	113
119	P506	39	40	P802	111

Color Key:

Secondary Fixed Function Pins

5.6 Additional Features

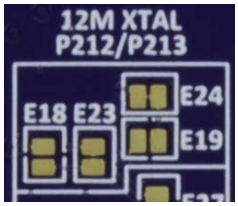
5.6.1 Analog Reference Voltages

A footprint for installation of capacitors C21 and C23 is provided on the Target Board. These two capacitors provide noise-bypass capability for ports P010/P011 and for ports P012/P013 respectively. See Figure 22 for the circuit design.

Port pair P010/P011 may be assigned as GPIO, where bypass capacitor C21 would damage signal quality. When P010/P011 are to be assigned as VREFH0/VREFL0, installation of capacitor C21 can reduce reference voltage noise and improve ADC measurement and DAC output quality. The Target Board was designed for Samsung P/N CL10B104KB8NNNC, or similar, noise-bypass capacitors.

Port pair P012/P013 may be assigned as GPIO, where bypass capacitor C23 would damage signal quality. When P012/P013 are to be assigned as VREFH/VREFL, installation of capacitor C23 may reduce reference voltage noise and improve ADC measurement and DAC output quality. The Target Board was designed for Samsung P/N CL10B104KB8NNNC, or similar, noise-bypass capacitors.

5.6.2 On-Board Clock Crystals



The TB-S3A1 includes two precision crystal clock sources. A precision 12.000 MHz crystal is installed at location X1, and a precision 32.768 kHz crystal is installed at location X2. These crystal clock sources are connected to the Main MCU by default.

The MCU pins for the 12 MHz clock crystal may be connected to P212 and P213. To disconnect the 12 MHz crystal, open copper jumpers E23 and E24, and close copper jumpers E18 and E19.

The MCU pins for the 32.768 kHz clock crystal may be connected to P214 and P215. To disconnect the 32.768 kHz crystal, open copper jumpers E25 and E26, and close copper jumpers E22 and E27.

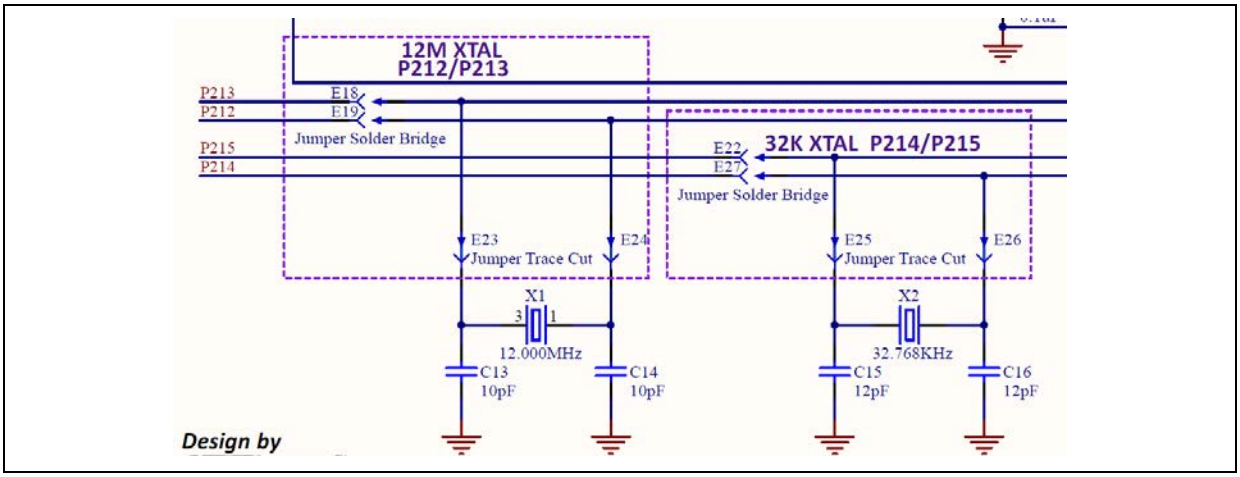


Figure 24. Crystal Clock Sources

5.6.3 User Potentiometer

A footprint for installation of a potentiometer and a recommended noise-bypass capacitor are provided on the Target Board. The footprint was designed for installation of a Bourns P/N 3352T-1-103LF, or equivalent, as the potentiometer, and a Samsung P/N CL10B104KB8NNNC, or similar, as the noise-bypass capacitor.

When the User Potentiometer is installed, copper jumper E36 must be closed to connect the User Potentiometer to the MCU.

Table 16. Target Board User Potentiometer

Designator	Function	MCU Control Port	MCU Pin
POT1	User Potentiometer	U1 P004 (AN004)	U1-136

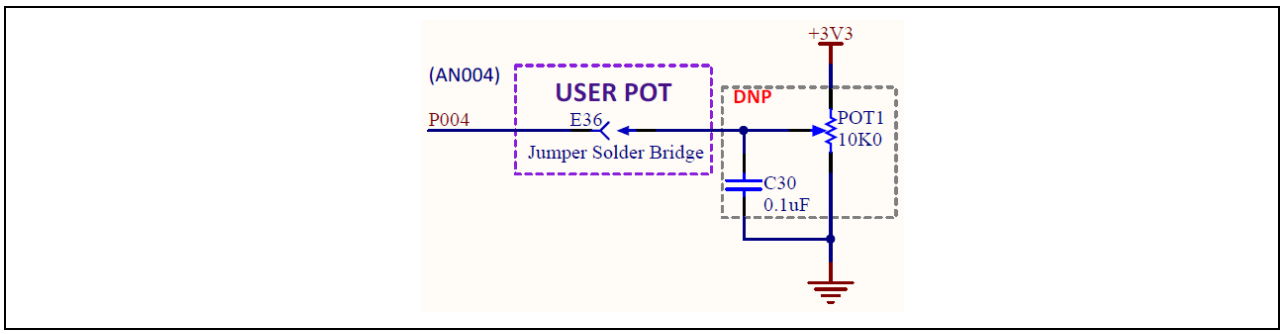


Figure 25. User Potentiometer Circuit

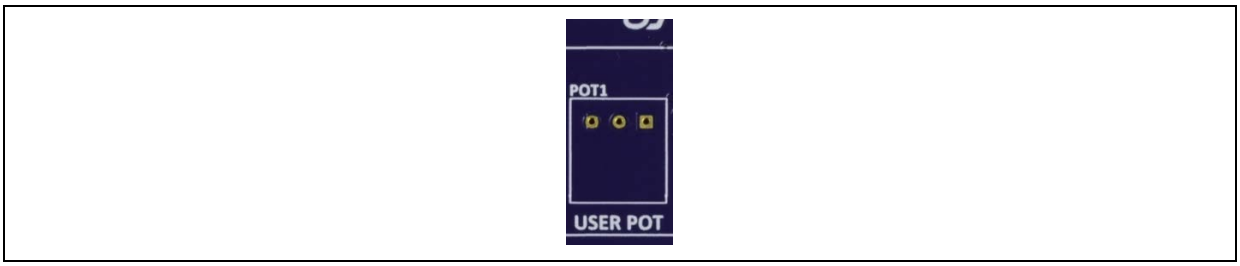


Figure 26. User Potentiometer on Target Board (Top)

5.6.4 Boot configuration

The BOOT CONFIG jumper, J8, is used to configure the operating mode of the S3A1 MCU at boot.

Table 17. Boot Configuration

Boot Configuration	J8 Shunt Location
Normal Boot (default)	Pins 1 and 2
SCI/USB Boot	Pins 1 and 3

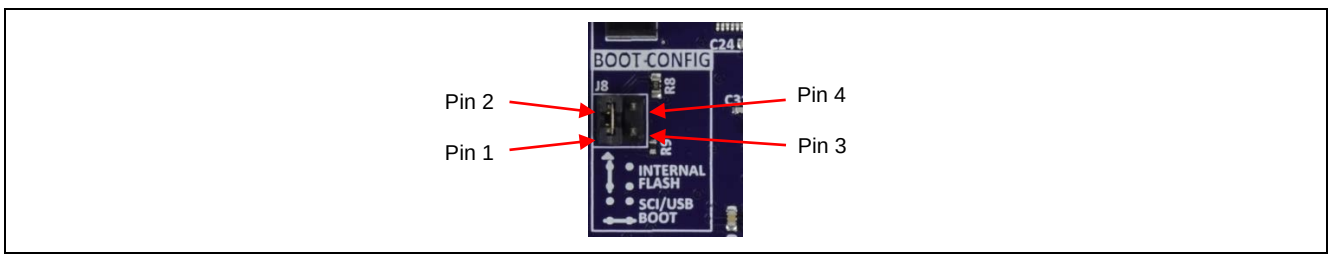


Figure 27. Boot Config Jumper J8

5.6.5 Miscellaneous Signals

5.6.5.1 AVCC0/AVSS0

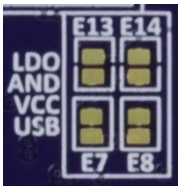
By default, AVCC0 is connected to +3V3 MCU, and AVSS0 is connected to the system ground. To disconnect these references from the AVCC0 and AVSS0 lines, copper jumpers E10 and E11 must be open.

5.6.5.2 VCL

By default, the Main MCU pin VCL is connected to reference capacitor C17. To connect this pin to MCU pin header J2, solder bridge E28 must be closed. To disconnect the reference capacitor C17, copper jumper E29 must be open.

5.6.5.3 VCC_USB_LDO

By default, the Main MCU pin VCC_USB_LDO is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU pin header J3. To do this, copper jumper E7 must be open, and copper jumper E13 must be closed.



5.6.5.4 VCC_USB

By default, the Main MCU pin VCC_USB is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU pin header J1. To do this, copper jumper E8 must be open and copper jumper E14 must be closed.

5.6.5.5 Signal P205

By default, the Main MCU pin P205 is connected to a TSCAP-A capacitor. This pin may be connected to MCU pin header J2. To do this, copper jumper E12 must be closed. The TSCAP-A capacitor may be disconnected by making copper jumper E15 open.

5.7 Additional Features

5.7.1 Analog Reference Voltages

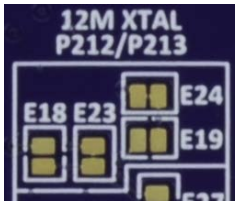
A footprint for installation of capacitors C21 and C23 is provided on the Target Board. These two capacitors provide noise-bypass capability for ports P010/P011 and for ports P012/P013 respectively. See Figure 22 for the circuit design.

Port pair P010/P011 may be assigned as GPIO, where bypass capacitor C21 would damage signal quality. When P010/P011 are to be assigned as VREFH0/VREFL0, installation of capacitor C21 can reduce reference voltage noise and improve ADC measurement and DAC output quality. The Target Board was designed for Samsung P/N CL10B104KB8NNNC, or similar, noise-bypass capacitors.

Port pair P012/P013 may be assigned as GPIO, where bypass capacitor C23 would damage signal quality. When P012/P013 are to be assigned as VREFH/VREFL, installation of capacitor C23 may reduce reference voltage noise and improve ADC measurement and DAC output quality. The Target Board was designed for Samsung P/N CL10B104KB8NNNC, or similar, noise-bypass capacitors.

5.7.2 On-Board Clock Crystals

The TB-S3A1 includes two precision crystal clock sources. A precision 12.000 MHz crystal is installed at location X1, and a precision 32.768 kHz crystal is installed at location X2. These crystal clock sources are connected to the Main MCU by default.



The MCU pins for the 12 MHz clock crystal may be connected to P212 and P213. To disconnect the 12 MHz crystal, open copper jumpers E23 and E24, and close copper jumpers E18 and E19.

The MCU pins for the 32.768 kHz clock crystal may be connected to P214 and P215. To disconnect the 32.768 kHz crystal, open copper jumpers E25 and E26, and close copper jumpers E22 and E27.

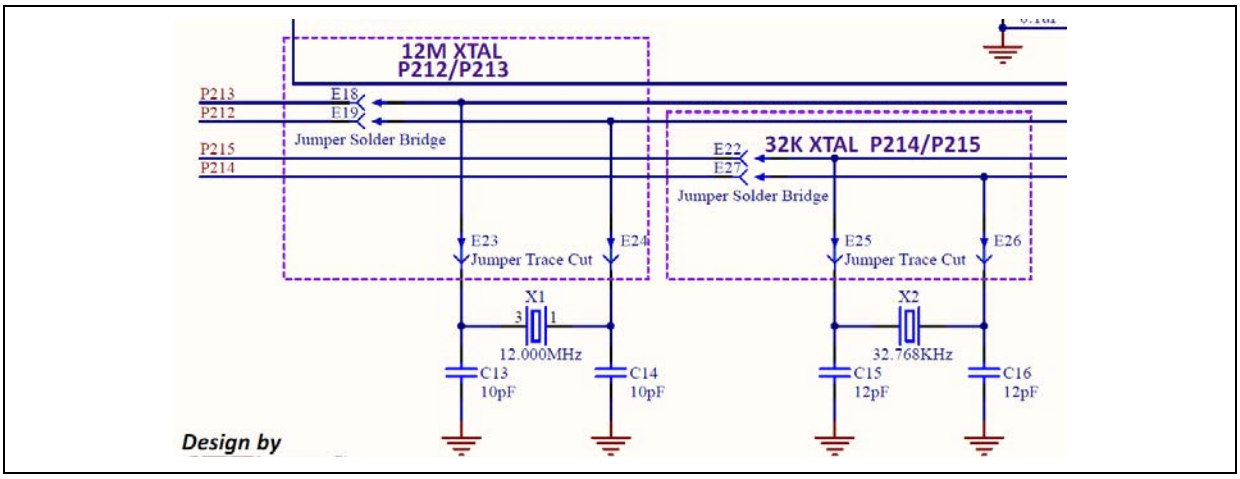


Figure 28. Crystal Clock Sources

5.7.3 User Potentiometer

A footprint for installation of a potentiometer and a recommended noise-bypass capacitor are provided on the Target Board. The footprint was designed for installation of a Bourns P/N 3352T-1-103LF, or equivalent, as the potentiometer, and a Samsung P/N CL10B104KB8NNNC, or similar, as the noise-bypass capacitor.

When the User Potentiometer is installed, copper jumper E36 must be closed to connect the User Potentiometer to the MCU.

Table 18. Target Board User Potentiometer

Designator	Function	MCU Control Port	MCU Pin
POT1	User Potentiometer	U1 P004 (AN004)	U1-136

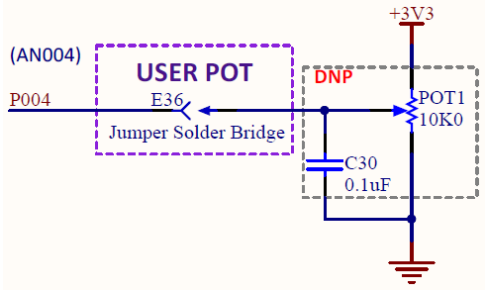


Figure 29. User Potentiometer Circuit

Figure 30. User Potentiometer on Target Board (Top)

5.7.4 Boot Configuration

The BOOT CONFIG jumper, J8, is used to configure the operating mode of the S3A1 MCU at boot.

Table 19. Boot Configuration

Boot Configuration	J8 Shunt Location
Normal Boot (default)	Pins 1 and 2
SCI/USB Boot	Pins 1 and 3

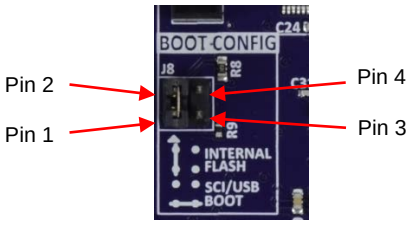


Figure 31. Boot Config Jumper J8

5.7.5 Miscellaneous Signals

5.7.5.1 AVCC0/AVSS0

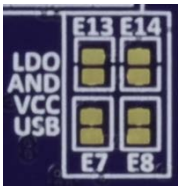
By default, AVCC0 is connected to +3V3 MCU, and AVSS0 is connected to the system ground. To disconnect these references from the AVCC0 and AVSS0 lines, copper jumpers E10 and E11 must be open.

5.7.5.2 VCL

By default, the Main MCU pin VCL is connected to reference capacitor C17. To connect this pin to MCU pin header J2, solder bridge E28 must be closed. To disconnect the reference capacitor C17, copper jumper E29 must be open.

5.7.5.3 VCC_USB_LDO

By default, the Main MCU pin VCC_USB_LDO is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU pin header J3. To do this, copper jumper E7 must be open, and copper jumper E13 must be closed.



5.7.5.4 VCC_USB

By default, the Main MCU pin VCC_USB is connected to the +3V3 MCU supply voltage. Alternatively, this pin may be connected to MCU pin header J1. To do this, copper jumper E8 must be open and copper jumper E14 must be closed.

5.7.5.5 Signal P205

By default, the Main MCU pin P205 is connected to a TSCAP-A capacitor. This pin may be connected to MCU pin header J2. To do this, copper jumper E12 must be closed. The TSCAP-A capacitor may be disconnected by making copper jumper E15 open.

6. Certifications

The TB-S3A1 v1 meets the following certifications/standards. See page 3 of this user's manual for the disclaimer and precautions.

6.1 EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/television technician for help.

- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirmeents set out in the Council Directives on the Approximation of the laws of the Member States relating to electromagnetic Compatibility Directive 2004/108/EEC.

  Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be requried to take adequate measures to correct this interference.

6.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS

- China SJ/T 113642014, 10-year environmental protection use period.

6.3 Safety Standards

- UL 94V-0

7. Design and Manufacturing Information

The design and manufacturing information about TB-S3A1 v1 board are available in the "TB-S3A1 v1 Design Package" available on renesas.com/synergy/tb-s3a1 under the Downloads tab.

- Design package file name: tb-s3a1-v1.2-designpackage.zip
- Design package contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	tb-s3a1-v1.2-schematics
File (PDF)	Mechanical Drawing	tb-s3a1-v1.2-mechdwg
File (PDF)	3D Drawing	tb-s3a1-v1.2-3d
File (PDF)	BOM	tb-s3a1-v1.2-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files - Altium

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

TB-S3A1 Resources	renesas.com/synergy/tb-s3a1
Synergy Software	renesas.com/synergy/software
Synergy Software Package	renesas.com/synergy/ssp
Software add-ons	renesas.com/synergy/addons
Software glossary	renesas.com/synergy/softwareglossary
Development tools	renesas.com/synergy/tools
Synergy Hardware	renesas.com/synergy/hardware
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MCU glossary	renesas.com/synergy/mcuglossary
Parametric search	renesas.com/synergy/parametric
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Partner projects	renesas.com/synergy/partnerprojects
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Knowledgebase	renesas.com/synergy/knowledgebase
Forums	renesas.com/synergy/forum
Training	renesas.com/synergy/training
Videos	renesas.com/synergy/videos
Chat and web ticket	renesas.com/synergy/resourcelibrary

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan.01.19	—	First release document
1.01	Apr.21.20	—	Updated sections 5.4.8, 6, and 7

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