

RTKA212831DR0000BU

The RTKA212831DR0000BU provides a simple platform to demonstrate the performances of the [RAA212831](#). The RAA212831 is an integrated 72V input voltage, 0.5A output load one synchronous buck regulator with fixed switching frequency from 350kHz and two 100mA, and 50mA output load linear regulators LDOs. The buck can support a wide input voltage range of 14V to 72V and adjusted output voltage from 1.25V to  $V_{IN} \times D_{max}$ . The LDO\_3V3 can support a wide input voltage range of 6V to 12V, and the output voltage is fixed at 3.3V. The LDO\_5 can support a wide input voltage range of 6V to 12V, and the output voltage is fixed at 5V. It is designed for small size and high integration electric-bike control board power management. Integrated buck and LDOs minimize the system components.

The Buck converter adopts peak current mode control, providing 500mA current for load and downstream LDO regulators, while the following LDOs provide 5V and 3.3V regulated power sources to the system. The current-mode buck converter provides a fast transient response and cycle-by-cycle switching current limit. All output voltages are fixed internally with few external components.

The RAA212831 has a fixed frequency operation, even the output terminal is light load condition, therefore, the switching frequency is fixed during the load variation. The RAA212831 can also use external components to achieve standby function to control buck output voltage as 6V or 12V. When the chip wants to save more energy with LDOs operations only, the external component can control buck output voltage from 12V to 6V.

Features

- Buck Converter:
  - 4.5V to 72V input voltage
  - Adjustable output voltage from 1.25V to  $V_{IN} \times D_{max}$
  - 500mA output load capability
  - 0.6Ω high-side MOSEFT  $r_{DS(ON)}$
  - Fixed switching frequency 350kHz operation
  - High side OCP, UVP, UVLO, OTP fault protection
- 5V LDO Regulator:
  - 6V to 12V input voltage
  - Fixed output voltage 5V
  - 100mA output load capability
  - Current limit foldback function
- 3.3V LDO Regulator:
  - 6V to 12V input voltage
  - Fixed output voltage 3.3V
  - 50mA output load capability
  - Current limit foldback function

Specifications

This board is configured and optimized for the following operating conditions:

- $V_{IN} = 14V$  to  $72V$  (For  $V_{OUT}$  is operated at 6V~12V)
- $V_{OUT} = 6V \sim 12V$  (For LDOs normal operations)
- $I_{OUT\_MAX} = 0.5A$
- $VLDO\_5V = 5V$
- $LDO\_5V\_MAX = 0.1A$
- $VLDO\_3V3 = 3.3V$
- $ILDO\_3V3\_MAX = 0.05A$

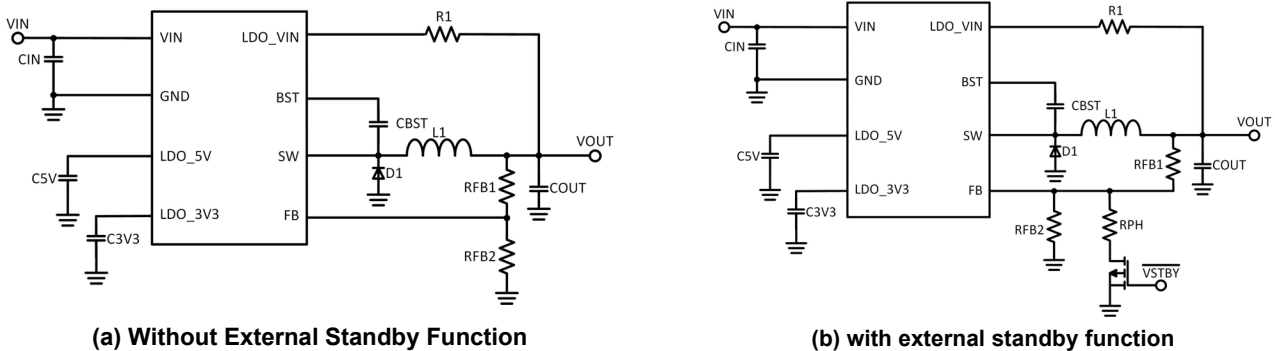


Figure 1. Typical Application Diagrams

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# 1. Functional Description

The RTKA212831DR0000BU demonstration board provides a simple platform to demonstrate the features of the RAA212831. The RTKA212831DR0000BU has a functionally optimized RAA212831 circuit layout that allows efficient operation up to the maximum output current.

The RTKA212831DR0000BU demonstration board is shown in Figure 3 and Figure 4. Figure 5 shows the schematic. The bill of materials and PCB layout information are also provided for your reference. Figure 8 through Figure 31 show performance data taken using this hardware.

## 1.1 Operation Range

The RTKA212831DR0000BU demonstration board input voltage range is 14V to 72V. The output voltage is fixed at 12V when the EXTFB test point is high and 6V when the EXTFB test point is low. It is a simple setting for use. For the LDO\_5V rail, the output voltage is 5V (default) with a 100mA maximum output current. For the LDO\_3V3 rail, the output voltage is 3.3V (default) with a 50mA maximum output current.

## 1.2 Setup and Configuration

See Figure 2 and complete the following steps:

1. Connect the power supply to the input terminals VIN (J1) and GND (J6). Connect the load to the output terminals, VOUT (J3) and GND (T2). Connect the load to the LDO\_5V output terminals, LDO\_5V (J2) and GND(J8). Connect the load to the LDO\_3V3 output terminals, LDO\_3V3 (J2) and GND (J8).
2. Ensure the setup is correctly connected before applying any power or load to the board.
3. Turn on the power supply and the part should start operating.
4. Verify that the buck output voltage is 12V with the EXTFB test point high, and phase node waveforms can be monitored at TP1. Verify that the LDO\_5V output voltage is 5V and the LDO\_3V3 output voltage is 3.3V.

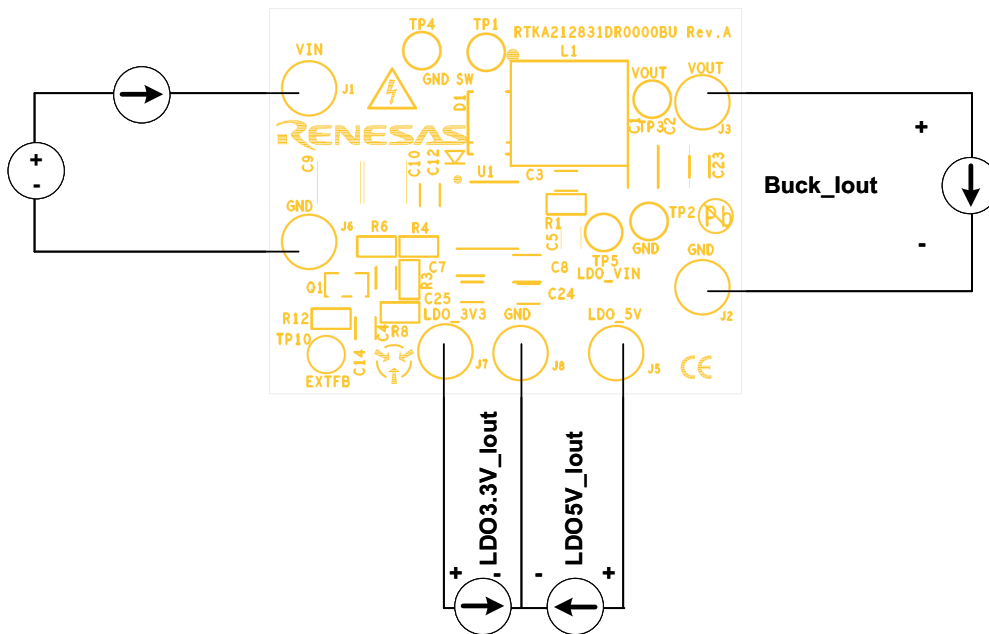


Figure 2. RTKA212831DR0000BU Board Setup

## 2. Board Design

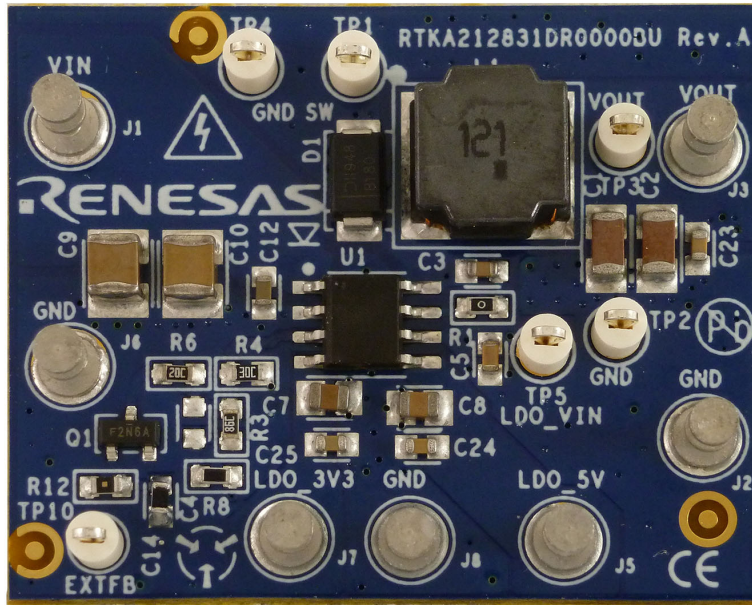


Figure 3. RTKA212831DR0000BU Demonstration Board (Top)



Figure 4. RTKA212831DR0000BU Demonstration Board (Bottom)

### 2.1 Layout Guidelines

A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. Place the LDO\_VIN pin trace away from noisy planes and traces. The via pattern under the RAA212831 is connected to a large ground copper plane on the bottom layer for effective thermal dissipation.



## 2.3 Bill of Materials

| Qty | Ref Des      | Description   | Manufacturer | Part Number          |
|-----|--------------|---|--------------|----------------------|
| 1   | U1           | IC SWITCHING REGULATOR, 8P, PSOP-8E, ROHS                 | Renesas      | RAA212831GSP#AA0     |
| 1   | L1           | COIL PWR INDUCTOR, SM, 8mm, 120μH, 20%, 1.15A, ROHS       | Würth        | 74404084121          |
| 1   | D1           | 1A 80V SCHOTTKY BARRIER RECTIFIER                         | Diodes       | B180-13-F            |
| 1   | Q1           | 6A, 8V, N-Channel (D-S) MOSFET                            | Vishay       | SI2342DS             |
| 2   | C1, C2       | CAP, SMD, 1206, 10μF, 35V, 10%, X7R, ROHS                 | TDK          | CGA5L1X7R1V106K160AC |
| 4   | C3, C23-C25  | CAP, SMD, 0603, 0.1μF, 16V, 10%, X7R, ROHS                | Murata       | GCM188R71C104KA37D   |
| 2   | C7, C8       | CAP, SMD, 0805, 4.7μF, 10V, 10%, X7R, ROHS                | Murata       | GRM21BR71A475KA73    |
| 1   | C5           | CAP, SMD, 0603, 1μF, 25V, 10%, X7R, ROHS                  | Murata       | GCM188R71E105KA64D   |
| 2   | C9, C10      | CAP, SMD, 1210, 10μF, 100V, 10%, X7S, ROHS                | Murata       | GRM32EC72A106KE05L   |
| 1   | C12          | CAP, SMD, 0603, 0.1μF, 100V, 10%, X7R, ROHS               | Murata       | GRM188R72A104KA35J   |
| 1   | C14          | CAP, SMD, 0603, 0.068μF, 25V, 10%, X7R, ROHS              | Kemet        | C0603C683K3RACTU     |
| 1   | R2           | RES, SMD, 0603, 1.5Ω, 1/10W, 1%, ROHS                     | Various      | Generic              |
| 1   | R1           | RES, SMD, 0603, 0Ω, 1/10W, 1%, ROHS                       | Various      | Generic              |
| 1   | R12          | RES, SMD, 0603, 10Ω, 1/10W, 1%, ROHS                      | Various      | Generic              |
| 1   | R6           | RES, SMD, 0603, 15.8kΩ, 1/10W, 1%, ROHS                   | Various      | Generic              |
| 1   | R4           | RES, SMD, 0603, 20kΩ, 1/10W, 1%, ROHS                     | Various      | Generic              |
| 1   | R3           | RES, SMD, 0603, 76.8kΩ, 1/10W, 1%, ROHS                   | Various      | Generic              |
| 1   | R8           | RES, SMD, 0603, 20Ω, 1/10W, 1%, ROHS                      | Various      | Generic              |
| 6   | TP1-TP6      | CONN MINI TEST POINT, VERTICAL, WHITE, ROHS               | Keystone     | 5002                 |
| 7   | J1-J3, J5-J8 | CONN DBL TURRET, TH, 0.218x0.078 PCB MNT, TIN/BRASS, ROHS | Keystone     | 1502-2               |

## 2.4 Board Layout

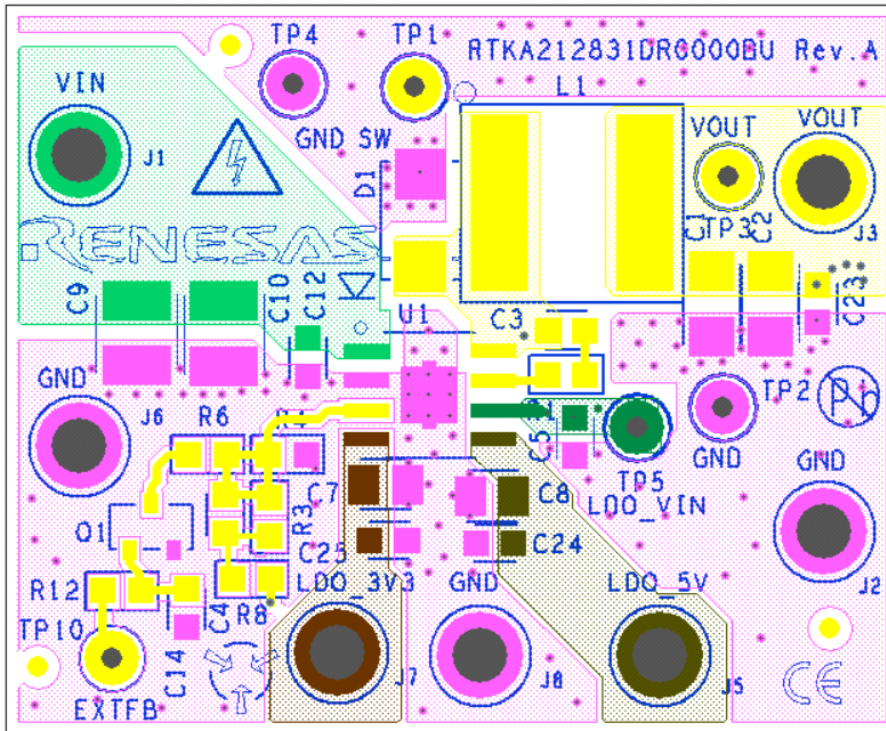


Figure 6. Top Layer

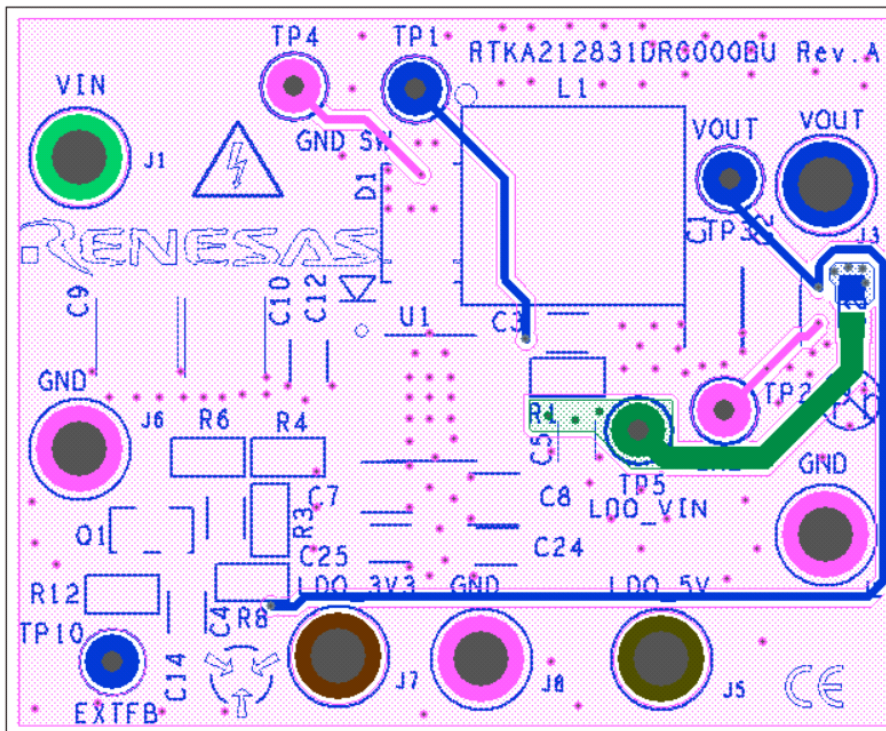


Figure 7. Bottom Layer

### 3. Typical Performance Graphs

$V_{IN} = 56V$ ,  $V_{OUT} = 6V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

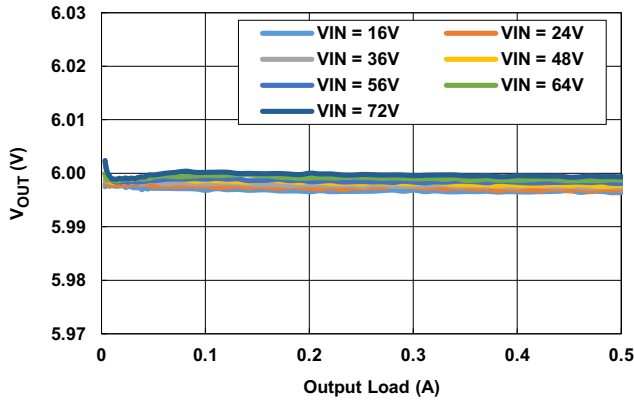


Figure 8. Load Regulation

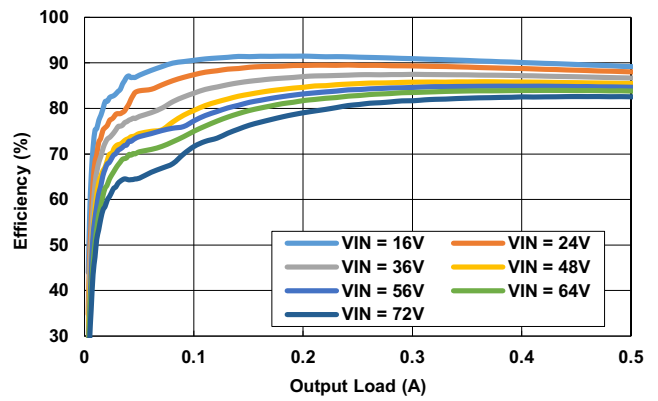


Figure 9. Efficiency

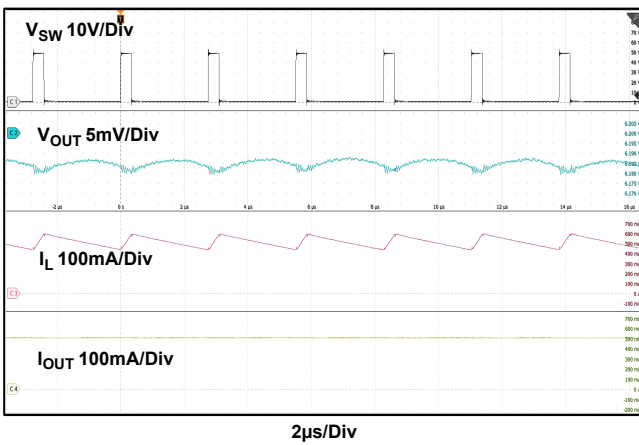


Figure 10. Buck Output Ripple at Full Load

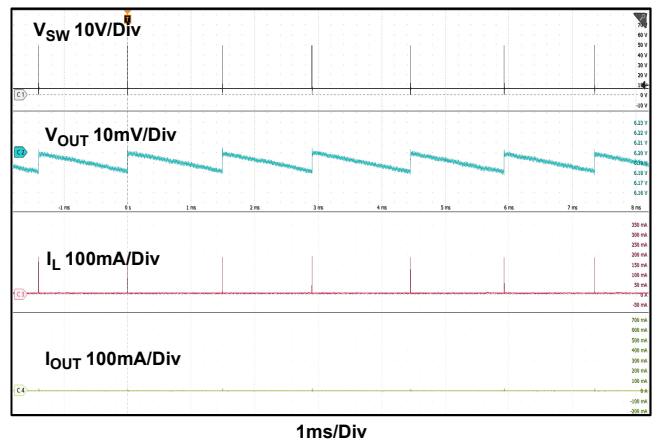


Figure 11. Buck Output Ripple at No Load

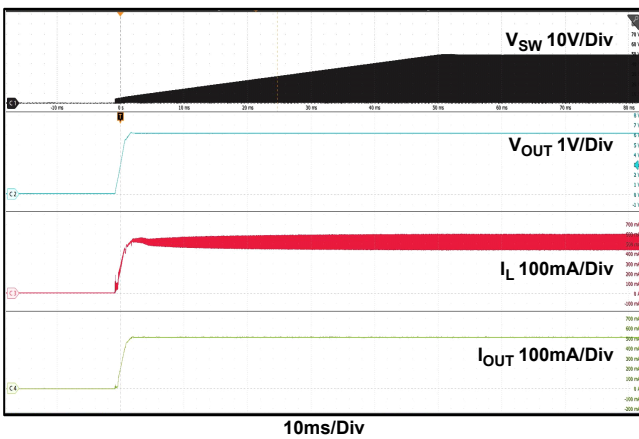


Figure 12. Power-On at Full Load

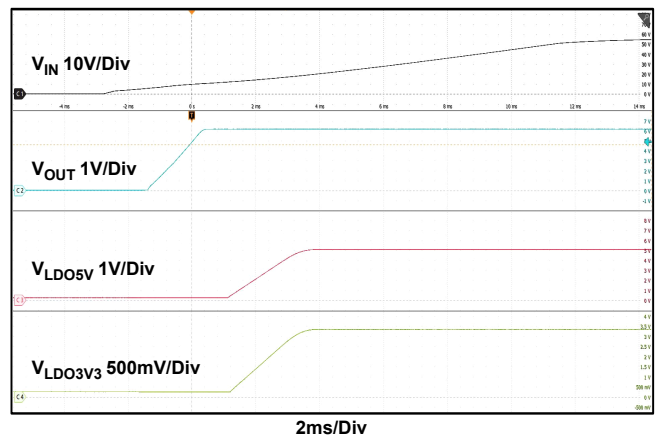


Figure 13. Power-On at Full Load with LDO Channels



$V_{IN} = 56V$ ,  $V_{OUT} = 6V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

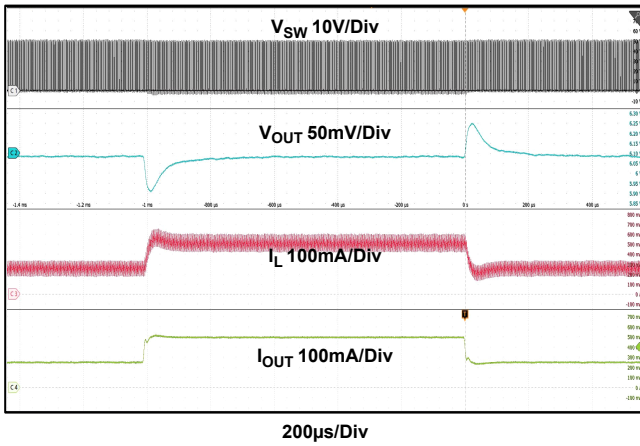


Figure 14. Load Transient between 0.25A to 0.5A

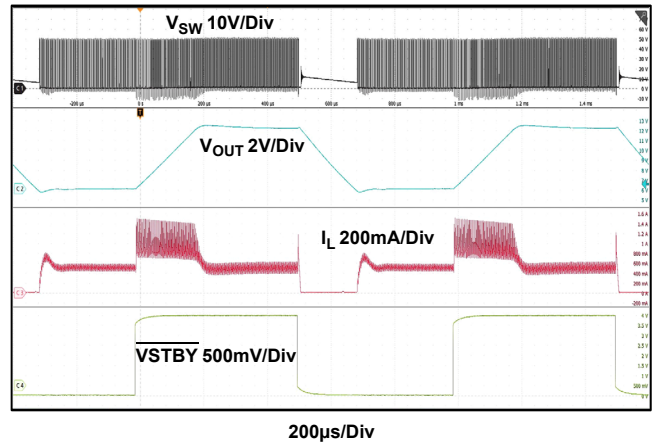


Figure 15. With External Standby Function at Full Load

$V_{IN} = 56V$ ,  $V_{OUT} = 12V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

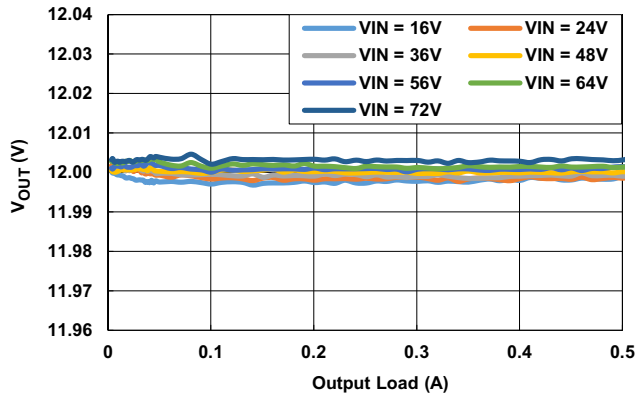


Figure 16. Load Regulation

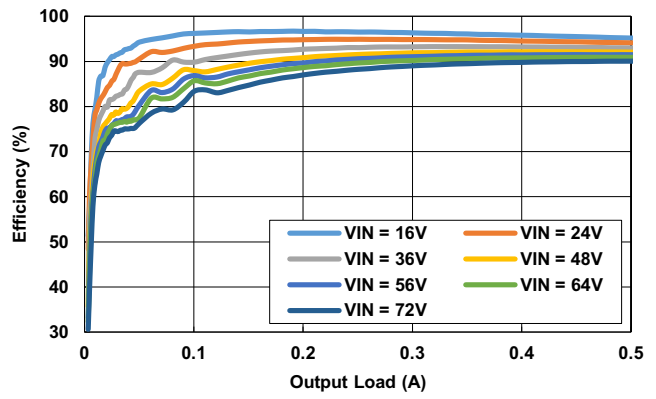


Figure 17. Efficiency

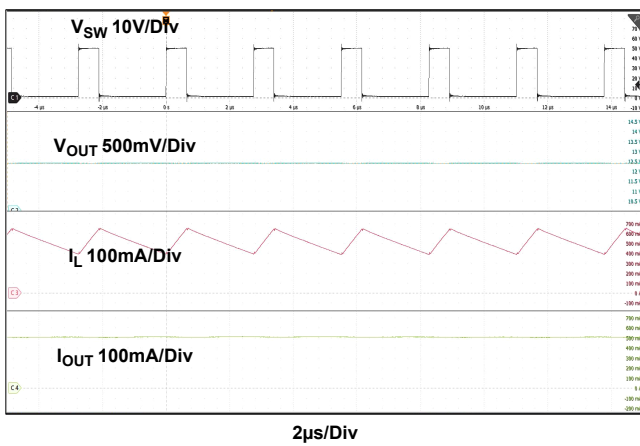


Figure 18. Buck Output Ripple at Full Load

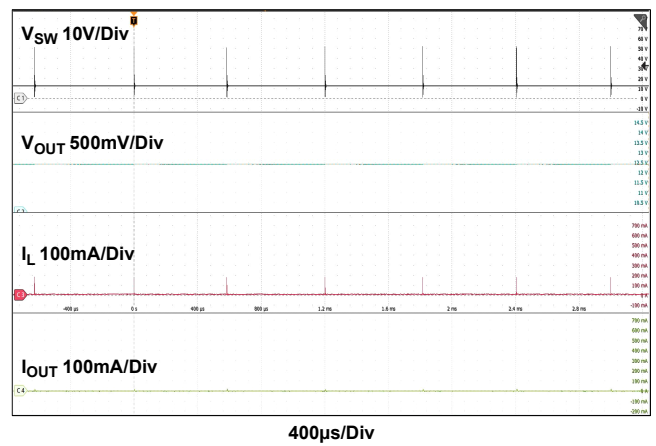


Figure 19. Buck Output Ripple at No Load

$V_{IN} = 56V$ ,  $V_{OUT} = 12V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

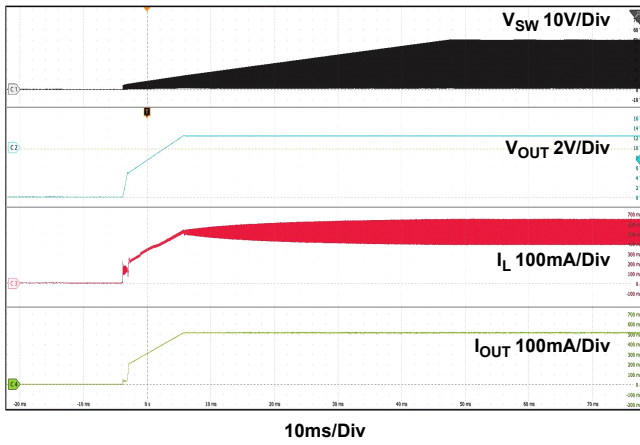


Figure 20. Power-On at Full Load

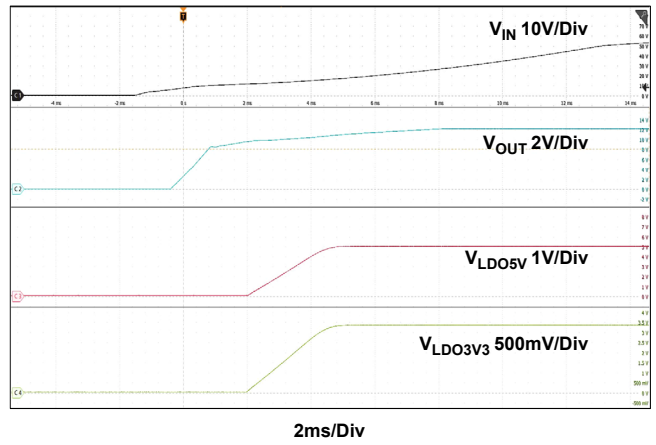


Figure 21. Power-On at Full Load with LDO Channels

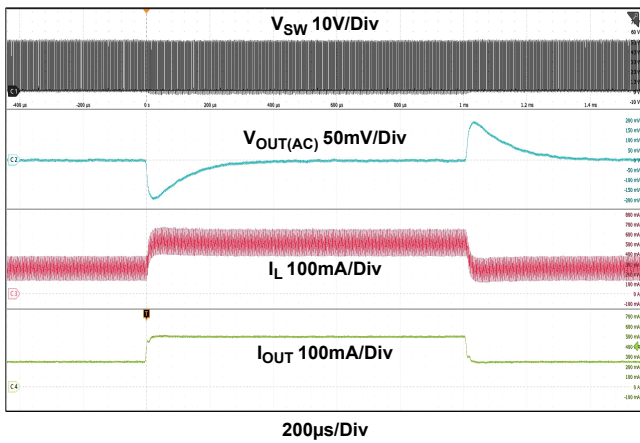


Figure 22. Load Transient between 0.25A to 0.5A

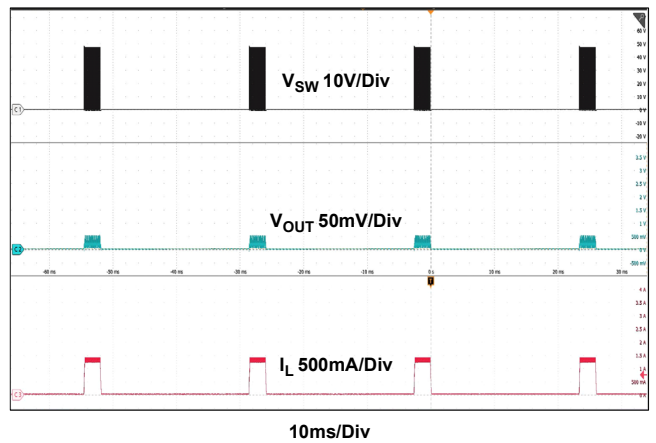


Figure 23. UVP Fault with Hiccup Operation

$V_{OUT} = V_{INLDO} = 6V$ ,  $V_{LDO5V} = 5V$ ,  $V_{LDO3V3} = 3.3V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

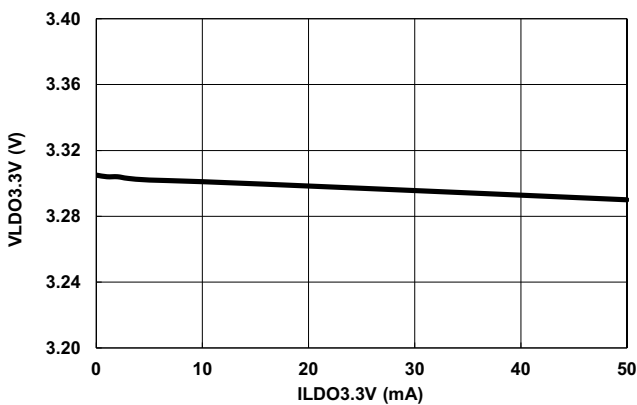


Figure 24. VLDO3V3 Load Regulation

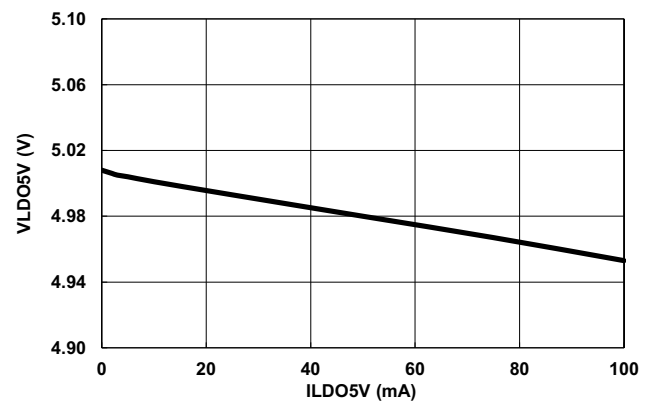


Figure 25. VLDO5V Load Regulation

$V_{OUT} = V_{INLDO} = 6V$ ,  $V_{LDO5V} = 5V$ ,  $V_{LDO3V3} = 3.3V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. (Cont.)

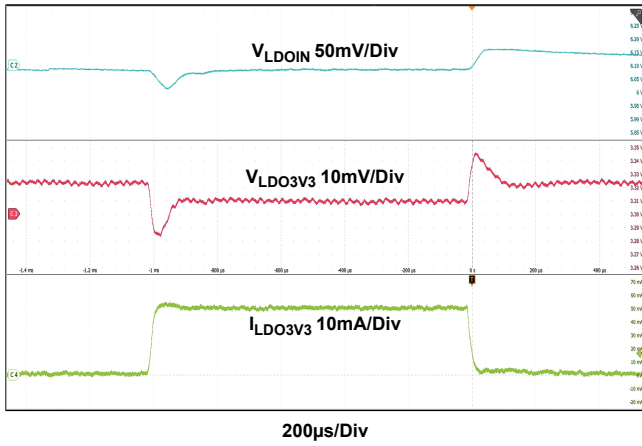


Figure 26. VLDO3V3 Load Transient between 0A to 0.05A

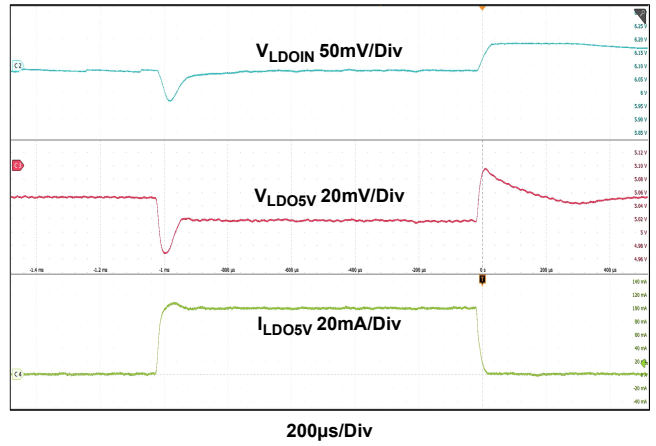


Figure 27. VLDO5V Load Transient between 0A to 0.1A

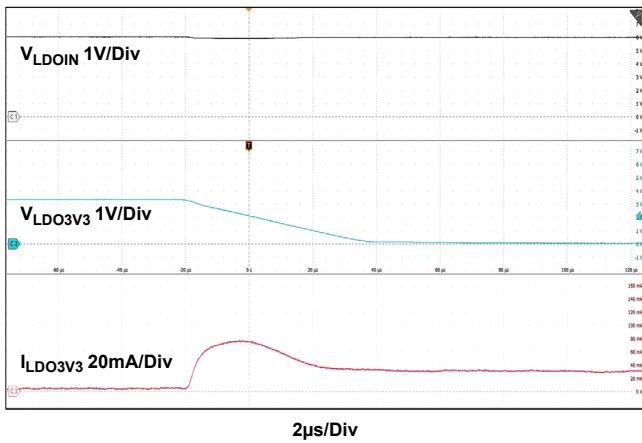


Figure 28. VLDO3V3 OCP Fault with Current Foldback

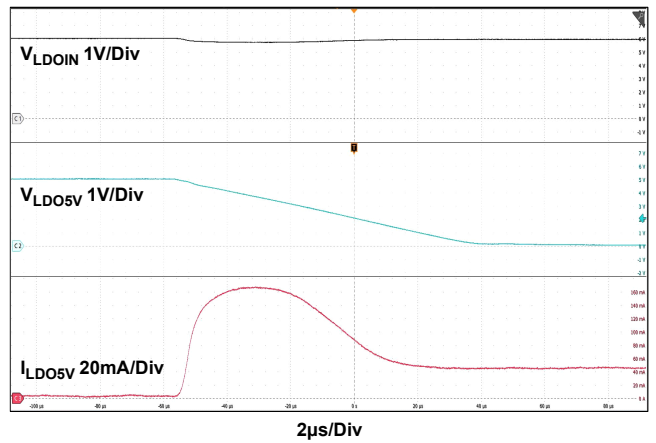


Figure 29. VLDO5V OCP Fault with Current Foldback

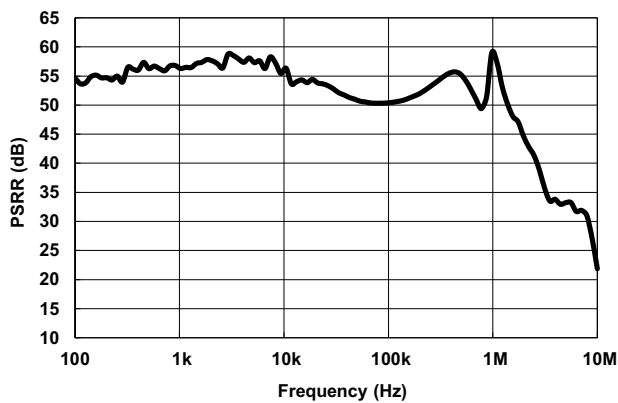


Figure 30. VLDO3V3 PSRR at Full Load

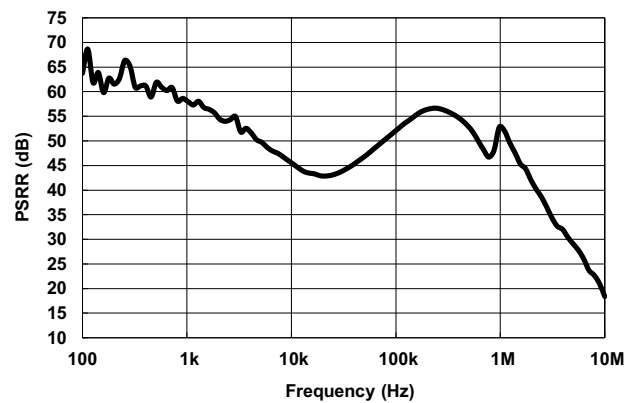


Figure 31. VLDO5V PSRR at Full Load

## 4. Ordering Information

| Part Number        | Description                   |
|--------------------|-------------------------------|
| RTKA212831DR0000BU | RAA212831 Demonstration Board |

## 5. Revision History

| Revision | Date         | Description                                 |
|----------|--------------|---|
| 1.02     | Mar 2, 2023  | Updated output voltage range maximum value. |
| 1.01     | Jun 15, 2022 | Updated Figures 3 and 4.                    |
| 1.00     | Sep 27, 2021 | Initial release                             |