RTKA214020DE0010BU

Evaluation Board

The RTKA214020DE0010BU evaluation board provides a simple platform to evaluate the RAA214020. It contains all the important circuitry needed to characterize critical performance parameters.

The RAA214020 is a low noise, high PSRR, low dropout voltage regulator. It accepts an input voltage range of 2.7V to 5.5V and the output voltage can be programmed from 0.9V to V_{IN}-$V_{DROPOUT}$ by means of a resistor divider feedback network. The device can source a load current of up to 2A and has an output voltage accuracy of ±1.25% over line, load, and temperature.

Key Features

- Input voltage range: 2.7V to 5.5V
- Output Voltage adjustable range: 0.9V to V_{IN} - $V_{DROPOUT}$
- Convenient shutdown mode function using jumper JP1
- Power-Good (PG) indication test point

Specifications

This board has been optimized for the following operating conditions:

- V_{IN} range from 2.7V to 5.5V
- V_{OUT} adjustable from 0.9V to V_{IN}-$V_{DROPOUT}$
- Low dropout: 540mV at 3.3V and 2A (maximum)
- High PSRR for $V_{HEADROOM}$ = 1.7V:
  - 100kHz: 56dB at 2A and 77dB at 500mA
  - 1MHz: 50dB at 2A and 57dB at 500mA

Ordering Information

Part Number	Description
RTKA214020DE0010BU	RAA214020 evaluation board

Content

1. Functional Description

The RTKA214020DE0010BU evaluation board provides a simple platform to demonstrate the features of the RAA214020 low-noise, high PSRR LDO and help characterize important critical performance parameters. The evaluation board is functionally optimized to allow efficient operation up to the maximum output current of 2A.

1.1 Adjusting the Output Voltage

The RAA214020 output voltage (V_{OUT}) can be programmed down to 0.9V and up to 5.5V-V_{DO} using the feedback (FB) resistors, R_F and R_G, as shown in Figure 1.

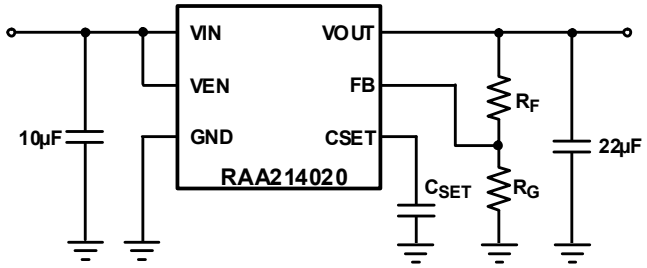

Figure 1. RAA214020 Simplified Application Schematic

V_{OUT} is calculated using Equation 1.

(EQ. 1) $$V_{OUT} = 0.9V \times \left(1 + \frac{R_F}{R_G}\right)$$

Similarly, the R_F and R_G resistors are calculated for any target output voltage by rearranging Equation 1 to get Equation 2 and solving for R_F.

(EQ. 2) $$R_F = R_G \times \left(\frac{V_{OUT(TARGET)}}{0.9V} - 1\right)$$

Table 1 suggests the FB resistor values to get some common voltage rails with 0.1% error. These resistors are commercially available in 0.1% tolerances. This table is not exhaustive and there may be other R_F and R_G resistor combinations that can provide better accuracy.

Table 1. Recommended R_F and R_G Feedback Resistor Values for Common Voltage Rails

$V_{OUT(TARGET)}$ (V)	R_F (kΩ)	R_G (kΩ)	V_{OUT} Error (%)
1	1.13	10.2	-0.03
1.2	3.4	10.2	0.0
1.5	6.8	10.2	0.0
1.8	10	10	0.0
1.9	1.11	10	-0.05
2.5	17.8	10	0.08
3	28.0	12.0	0.0
3.3	26.7	10.0	0.0
4.2	37.4	10.2	0.0
4.5	56.0	14.0	0.0
5	45.3	10.7	0.08

1.2 Setting Noise Performance

For low-noise applications, a 1µF C_{SET} capacitor is optimal. Larger capacitor values can be used with little benefit in lowering the internally generated output voltage noise for frequencies above 10Hz.

1.3 Quick Start Guide

1. Verify jumper J1 is not in the circuit. The 10kΩ pull-up resistor R_4 provides a logic HIGH that enables the LDO.
2. Connect the input supply to VIN and GND.
3. Connect the load to VOUT and GND.
4. Observe the output voltage.

2. Board Design

2.1 PCB Layout Guidelines

A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance, and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The trace for FB must be away from noisy planes and traces.

The large 1.6mmx2mm thermal pad under the RAA214020 is connected to a large ground copper plane on the bottom layer for effective thermal dissipation.

2.2 RTKA214020DE0010BU Evaluation Board

Figure 2. RTKA214020DE0010BU Evaluation Board

2.3 Schematic

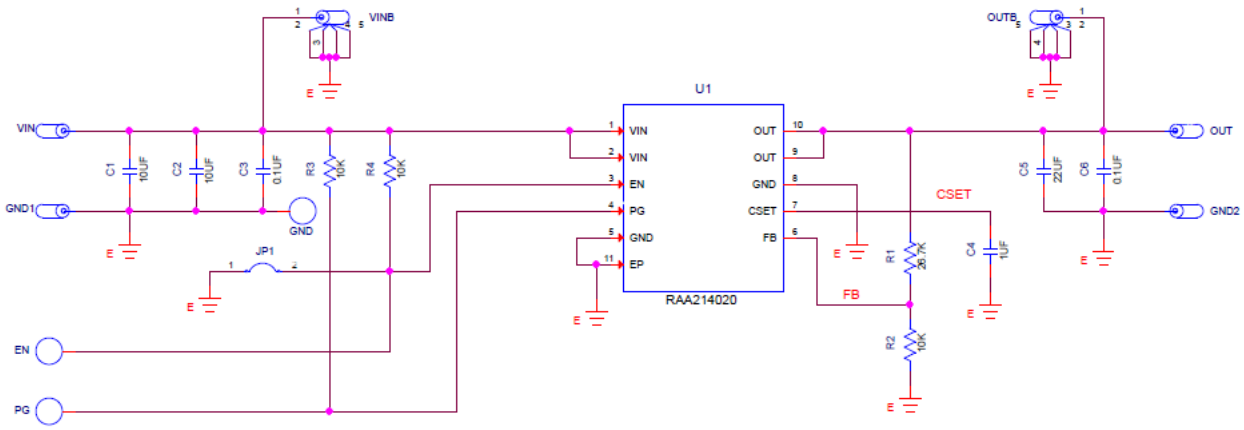

Figure 3. RTKA214020DE0010BU Schematic

2.4 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
2	TP1, TP2	Test Point Turret 0.150 Pad 0.100 Thole	Keystone	1514-2
2	BNC1, BNC2	Silver Plated 50Ω PCB Mount Receptacle	Amphenol	31-5329-51RFX
1	TP3	Miniature White Test Point 0.100 Pad 0.040 Thole	Keystone	5002
4	BAN1-BAN4	L = 0.218in Solder Mount Banana Plug	Keystone	575-4
2	C1, C2	10µF, 10%, 10V, 0805, Multilayer Cap (Automotive AEC-Q200)	Murata	GCJ21BR71A106KE01L
1	C5	22µF, 10%, 10V, 1206, Ceramic Cap	Murata	GRM31CR71A226KE15L
1	C4	1000pF, 10%, 100V, 1206, Multilayer Cap	Generic	Various
2	C3, C6	0.1µF, 10%, 16V, 0603, Multilayer Cap	Generic	Various
1	R5	0, 1%, 1/10W, 0603, Thick Film Chip Resistor	Generic	Various
2	R3, R4	010k, 1%, 1/16W, 0603, Thick Film Chip Resistor	Generic	Various
1	R2	100k, 1%, 1/16W, 0603, Thick Film Chip Resistor	Generic	Various
1	R1	267k, 1%, 1/16W, 0603, Thick Film Chip Resistor	Generic	Various
1	JP1	Two Pin Jumper	Generic	Various
1	U1	RAA214020 LDO, 10Ld DFN, Ultra Loise Noise High PSSR LDO	Renesas	RAA214020GNP

2.5 Board Layout

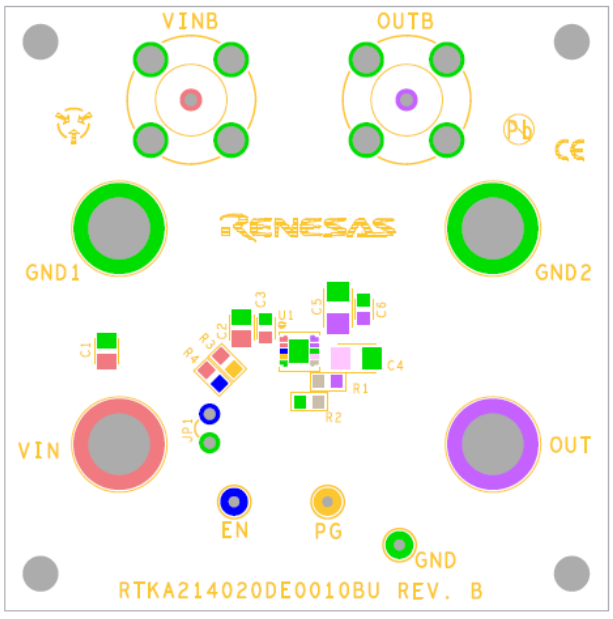

Figure 4. Top Layer Silk Screen

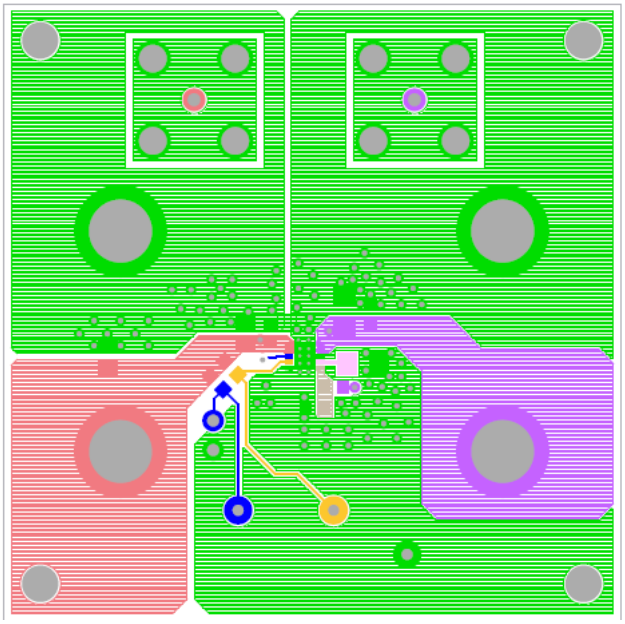

Figure 5. Top Layer

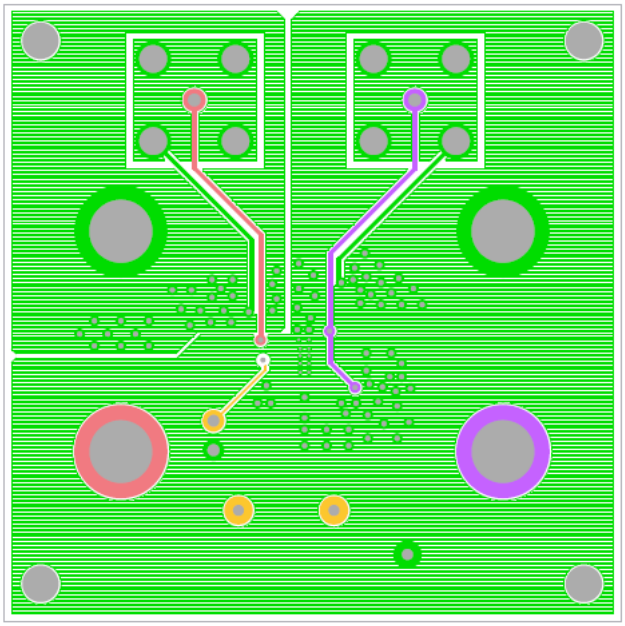

Figure 6. Bottom Layer

3. Typical Performance Curves

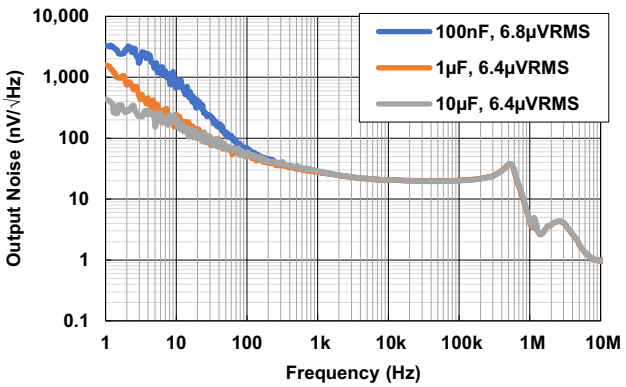

Figure 7. Output Noise vs Frequency for Various C_{SET}
(V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

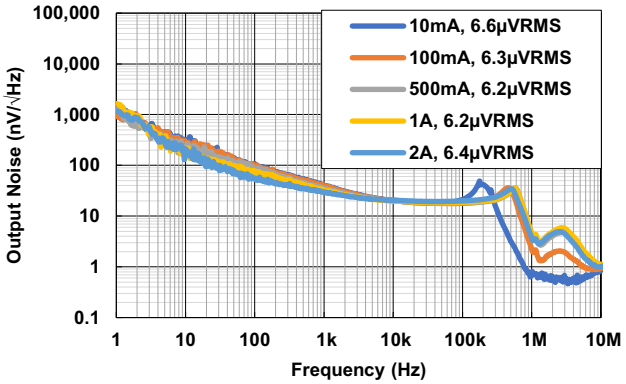

Figure 8. Output Noise vs Frequency for Various I_{OUT}
(V_{IN} = V_{OUT} + 1V, I_{OUT} = 2A)

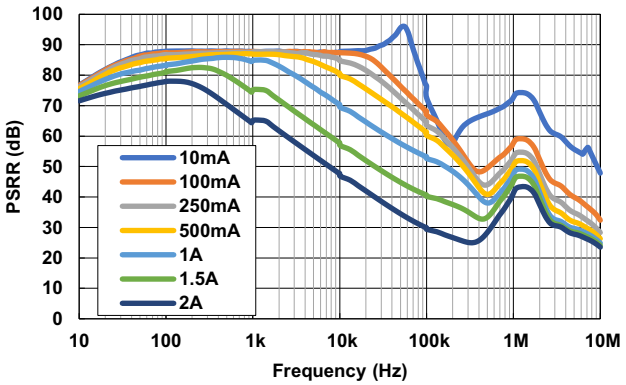

Figure 9. PSRR vs Frequency for Various I_{OUT}
(V_{IN} = 4V, V_{OUT} = 3.3V)

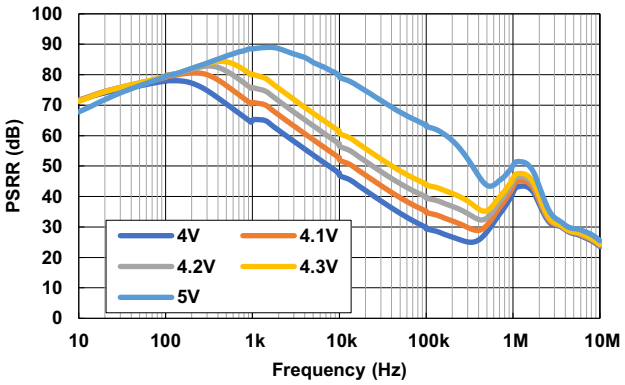

Figure 10. PSRR vs Frequency for Various V_{IN}
(V_{OUT} = 3.3V, I_{OUT} = 2A)

4. Revision History

Rev.	Date	Description
2.0	Jul 20, 2021	Removed Related literature and added link to description on page 1. Updated File number from X0115610 to R16UZ0014EU0200 (Renesas format). Added TOC. Updated last two specifications bullets (sub bullets) on page 1. Replaced the Setting the Output Voltage with the Adjusting the Output Voltage section on page 3. Replaced the Setting the Noise Performance and Start-Up Time with the Setting Noise Performance section on page 4. Updated Figures 7, 8, 9, 10 on page 8.
1.0	Nov 5, 2020	Initial release