REFLEX CES
Custom Embedded Systems

ALARIC

Instant-DevKit
Arria® 10 SoC FMC IDK

The Arria® 10 SoC FMC Instant-Development Kit provides to developers the best Out-Of-The box experience, combining the Best-In Class compact hardware platform and the most efficient intuitive software environment.

Dual-core ARM© Cortex™-A9 MPCore™ hard processor system (HPS).

DevKitInvasion

ACHILLES
Arria® 10 SoC SoM IDK

SARGON
Stratix® 10 FPGA FMC+ IDK

Target markets:

Medical

Industrial

Test & Measurement

Video capture and processing

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ALARIC Instant-DevKit
Arria® 10 SoC SoM IDK

Featured Device

Arria® 10 SoC 660 KLEs

- Board based on Intel® Arria® 10 SoC 660KLEs, speed grade -2 by default
- PCIe end point edge connector for Gen3 x4 (32Gb/s)
- PCIe root Complex edge connector for Gen3 x4 (32Gb/s)
- FMC High Pin Count fully compliant:
  - 168 LVCMOS (1.8V) or 84 LVDS (1.8V,2.5V)
  - 10 XCVR (Typical 10Gb/s)
- One serial over USB High speed link (through USB Hub)
- 2 x RJ45 copper connector 10/100/1000Base-T Ethernet connected to the FPGA core fabric part
- 1 x RJ45 copper connector 10/100/1000Base-T Ethernet connected to the HPS part of the FPGA
- On board DDR3 for HPS (2GB) speed up to 2133 MT/s*
- On board DDR3 for FPGA (2GB) speed up to 2133 MT/s*
- DisplayPort Rev1.2 (up to 5.4Gbit/s)
- One microSD 8 GB SDHC Class 10 (already insert into the support connector) with factory image boot
- Mini USB connector B-type to enable the USB2.0 PHY OTG high speed, ULPI interface connected to the HPS of the FPGA
- MAX 10 Power supplies monitoring with its ADCs solution
- Innovative clock tree (Silicon Labs)
- +12V on a JACK/Edge PCIe connector / ATX connector
- Active Heat sink
- PCIe Bracket, LED
- SATA connector to FPGA 1 x XCVR
- MCX connector for PPS interface
- Mictor connector for HPS debug trace

* Depends on FPGA speed grade

Board Programming

- JTAG : On-board USB-Blaster II MAX V (reachable by USB Hub)
- Fast passive parallel (FPP) configuration via MAX®10 device and flash memory
- AS configuration supported with NOR FLASH
- Boot selection for HPS throught user dipswitch

Clock Circuitry

- 3 x SMA connectors (1 main input clock + 1 diff. output programmable clock)
- 9 x FPGA XCVR programmable inputs Clocks (up to 800 MHz to reach different communication protocol)

Board Size

- Length : 240 mm (9.45 inches)
- Height : 111.15 mm (4.38 inches) / Standard Height PCIe
- Standard Thickness PCIe

Kit Content

- Alaric Arria® 10 SoC FMC PCIe DevKit
- Power adapter (US, UK, EU, JP) and Micro USB2.0 cable
- One microSD 8 GB SDHC Class 10
- PDF Documentation (Starter Guide, Hardware Reference Manual, Board Outline, Schematics)
- FMC Interface Control Excel sheet
- Board test design files available under FTP after the creation of a user account (Quartus Prime Pro software required)
- Software Board support packages for Hard Processing System Interface (HPS) available under FTP after the creation of a user account (Reserved for software engineers experimented with Linux)
- Under request on the online support **support.reflexces.com** :
  - Quartus Prime Pro DKE
  - Mechanical files (DWF/STEP models and 2D drawing)

Power & Environmental

- Power : 75W max/ 40W typical
- Environmental : 0°C/ +60°C

Kit Ordering information

- RXCA10S066PF34-IDK00A (Production version)

= Development Kit (FPGA Arria® 10 SX 660)