

## 1Gb/2Gb/4Gb, 3V, SPI SLC NAND Flash Memory for Embedded

### Distinctive Characteristics

#### ■ Density

- 1Gb / 2Gb / 4Gb

#### ■ Architecture

- Page size:
  - 1 Gb : (2048 + 64) bytes; 64-byte spare area (Default)
  - 1 Gb : (2048 + 128) bytes; 128-byte spare area (Contact sales for the 128-byte spare area option)
  - 2 Gb / 4 Gb: (2048 + 128) bytes; 128-byte spare area
- Block size: 64 Pages
  - 1 Gb : 128 KB + 4 KB
  - 1 Gb : 128 KB + 8 KB
  - 2 Gb / 4 Gb: 128 KB + 8 KB
- Plane size
  - 1 Gb: 1024 blocks per plane or (128 MB + 4 MB)
  - 1 Gb: 1024 blocks per plane or (128 MB + 8 MB)
  - 2 Gb: 1024 blocks per plane or (128 MB + 8 MB)
  - 4 Gb: 2048 blocks per plane or (256 MB + 16 MB)
- Device Size
  - 1 Gb: 1 plane per device or 128 Mbyte
  - 2 Gb: 2 planes per device or 256 Mbyte
  - 4 Gb: 2 planes per device or 512 Mbyte

### Performance

#### ■ Page Read / Program

- Read Page Time (tR): 45  $\mu$ s (Typ)
- Program time: 350  $\mu$ s (Typ)

#### ■ Block Erase

- Block Erase time: 4.0 ms (Typ)

#### ■ Reliability

- 80,000 Program / Erase cycles (Typ)
- 10 Year Data Retention (Typ)
- Blocks 0-7 are good at the time of shipment

#### ■ NAND Flash interface

- Supports Serial Peripheral Interface (SPI)

#### ■ Supply Voltage

- 3.3-V device:  $V_{CC} = 2.7 V \sim 3.6 V$

#### ■ Security

- One Time Programmable (OTP) area
- Serial number (unique ID) (Contact factory for support)
- Hardware program/erase disabled during power transition
- Volatile and Permanent Block Protection

#### ■ Additional features

- On- chip ECC correction Program and Erase
- Supports single I/O, Dual I/O, Quad I/O
- Support Frequency up to 104MHZ
- Supports Clock Polarity and phase modes 0 and 3

#### ■ Electronic signature

- Manufacturer ID:01h

#### ■ Operating temperature

- Industrial:  $-40^{\circ}C$  to  $85^{\circ}C$
- Industrial Plus:  $-40^{\circ}C$  to  $105^{\circ}C$

#### ■ Package options

- Pb-free and low halogen
- 8-Pin LGA 6 x 8 mm
- 16-Pin SOIC 300 mils
- 24-Ball FBGA 8 x 6 mm

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## 1. General Description

The S35ML01G3 / S35ML02G3 / S35ML04G3 SPI devices are offered with a 3.3-V VCC power supply, and with industry standard Serial Peripheral Interface (SPI). Its NAND cell provides the most cost-effective solution for the solid state mass storage market with low pin count and a modified SPI-NOR command set to address NAND specific functions and features.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The page size for the 1Gb/2Gb/4Gb SPI devices is (2048 + 128 spare) bytes and for the 1Gb device with 64 bytes spare option is (2048 + 64 spare) bytes. SkyHigh SPI NAND family is designed with powerful internal ECC engine. To protect the system bus from transmission errors, the implementation of a 1 bit ECC is recommended.

Like all other 2-kB page NAND flash devices, a program operation typically writes 2 KB (×8) in 350 μs and an erase operation can typically be performed in 4ms on a 128-kB block.

The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data.

SkyHigh's SPI device offers many useful features including first page auto-load on power-up. SkyHigh's SPI NAND Flash has six signal lines in addition to VCC and GND pins. The signal lines are: SCK, SI, SO, CS, HOLD#, WP#.

The devices are available in the LGA- 8 pins (6 x 8 mm), SOIC- 16 pins (300 mil), FBGA- 24 pins (8 x 6 mm) packages and come with the following security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely identified. Contact factory for support of this feature.
- Volatile and Permanent Block Protection.

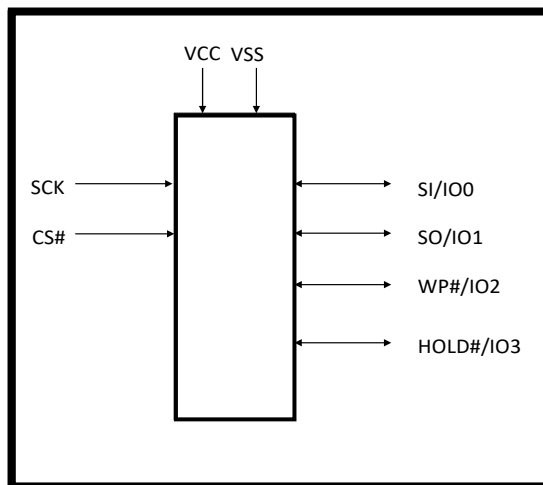
**Table 1. Product List**

| Device    | Density (bits) | Number of Planes | Number of Blocks per Plane |
|-----------|----------------|------------------|----------------------------|
| S35ML01G3 | 1 Gb           | 1                | 1024                       |
| S35ML02G3 | 2 Gb           | 2                | 1024                       |
| S35ML04G3 | 4 Gb           | 2                | 2048                       |

Note 1): Since Dual plane operation are not supported in SPI, therefore the whole array is described in number of blocks. The planes are reflected in this document to match the physical implementation.

## 1.1 Logic Diagram

**Figure 1. Logic Diagram**



**Table 2. Signal Names**

| Signal Name | Type   | Description  |
|-------------|--------|--|
| CS#         | Input  | Chip Select  |
| SI/IO0      | I/O    | Serial Input for single bit data commands or I/O0 for Dual or Quad commands. |
| SO/IO1      | I/O    | Serial Output for single bit data commands. I/O1 for Dual or Quad commands.  |
| WP#/IO2     | I/O    | Write Protect when not in Quad mode, I/O2 when in Quad                       |
| HOLD#/IO3   | I/O    | Hold Input / I/O3 when in Quad mode  |
| SCK         | Input  | Serial Clock Input   |
| VCC         | Supply | Power Supply   |
| VSS         | Supply | Ground   |
| NC          | Unuse  | No Connection  |
| DNU         | Reserv | Do not use   |

**Notes:**

1. A 0.1  $\mu$ F capacitor should be connected between the VCC Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.



## 1.2 Connection Diagram

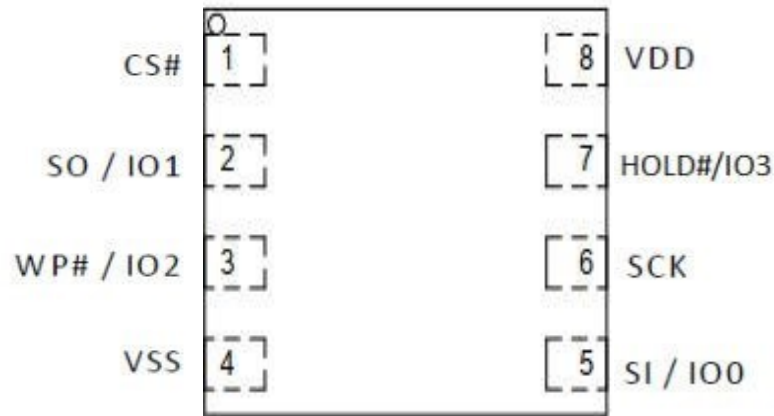


Figure 2. 8-pin LGA package (6 x 8 mm), Top View

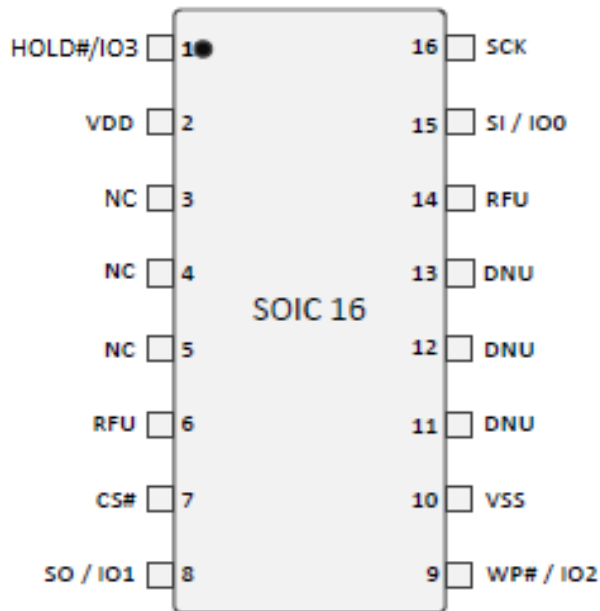


Figure 3. 16-pin SOIC (300 mils), Top View

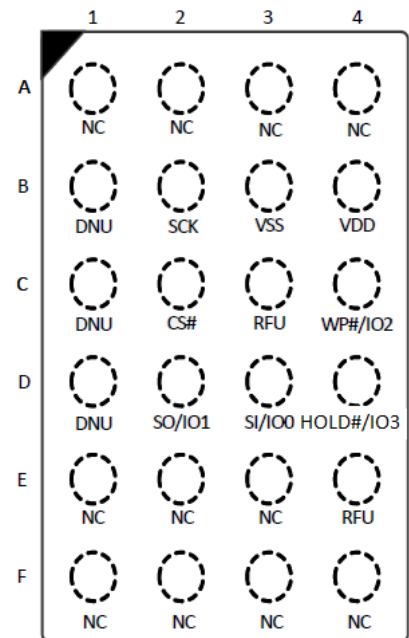


Figure 4. 24-Ball 6 x 4 Ball Array (6 x 8 mm), Top View

### 1.3 Pin Description

Table 3. Pin Description

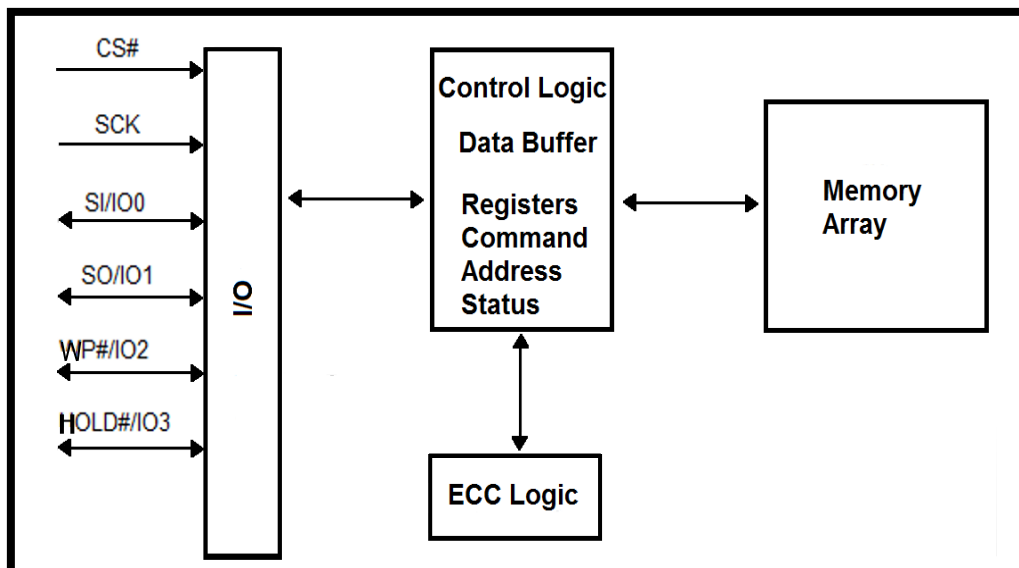
| Signal Name | Type     | Description  |
|-------------|----------|--|
| CS#         | Input    | Chip Select  |
| SI/IO0      | I/O      | Serial Input for single bit data commands or I/O0 for Dual or Quad commands. |
| SO/IO1      | I/O      | Serial Output for single bit data commands. I/O1 for Dual or Quad commands.  |
| WP#/IO2     | I/O      | Write Protect when not in Quad mode, I/O2 when in Quad mode                  |
| HOLD#/IO3   | I/O      | Hold Input / I/O3 when in Quad mode  |
| SCK         | Input    | Serial Clock Input   |
| VCC         | Supply   | Power Supply   |
| VSS         | Supply   | Ground   |
| NC          | Unused   | No Connection  |
| DNU         | Reserved | Do not use   |

**Notes:**

1. A 0.1  $\mu\text{F}$  capacitor should be connected between the VCC Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.

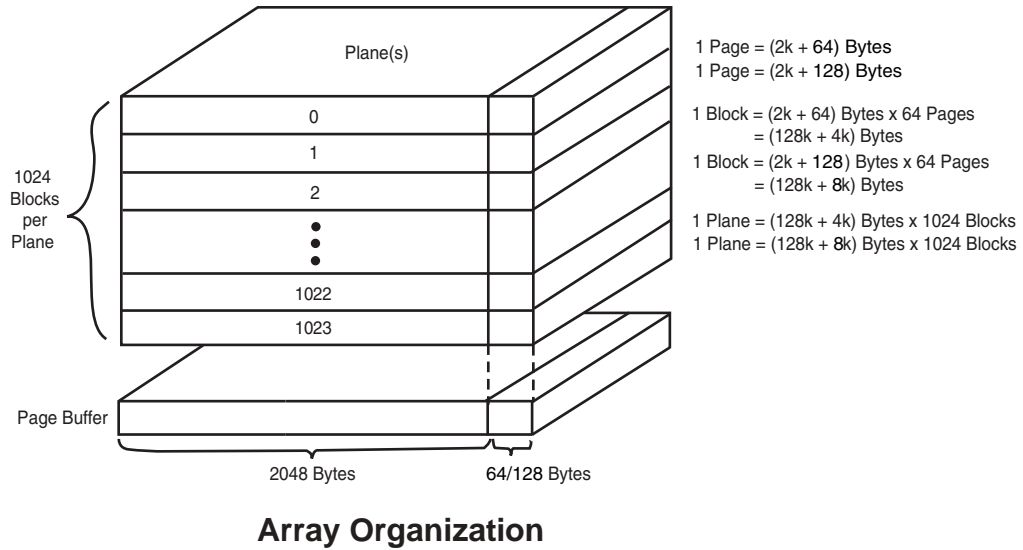
### 1.4 Block Diagram

Figure 5. Block Diagram



## 1.5 Array Organization

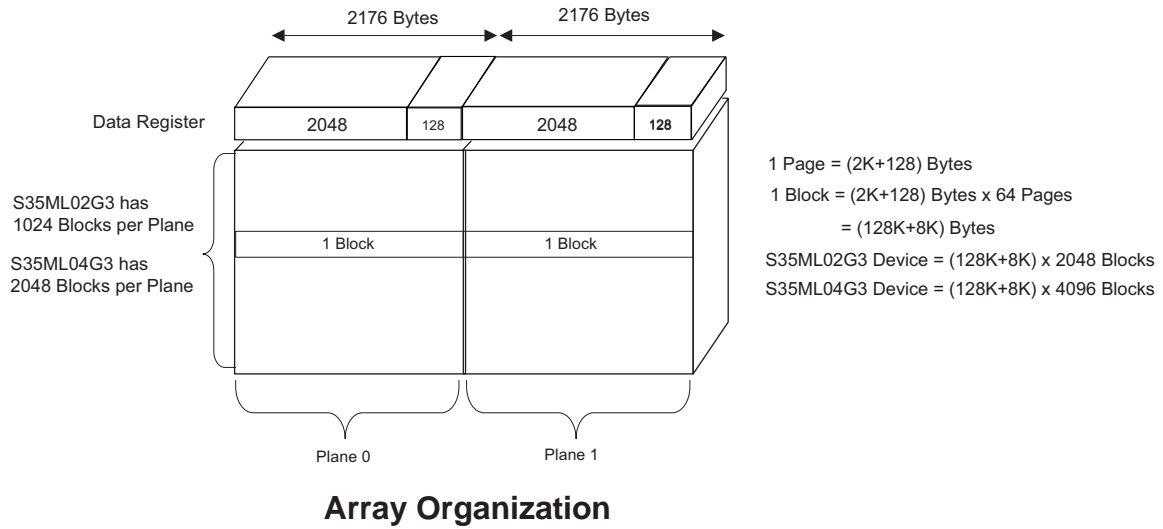
**Figure 6. Array Organization — S35ML01G3**



Note 1): S35ML01G3 is offered with 64 bytes spare are and 128 bytes spare area options.

## 1.5 Array Organization

**Figure 6.1 Array Organization— S35ML02G3 / S35ML04G3**



Note 1): Since Dual plane operation are not supported in SPI, therefore the whole array is described in number of blocks. The planes are reflected in this document to match the physical implementation.

## 1.6 Memory Addressing

**Table 4. Memory Array organization**

| Density_<br>Page Size | Device and Array organization |     |        |                     |                   |                        |                                   |     |                      | Address bits |            |            |
|-----------------------|-------------------------------|-----|--------|---------------------|-------------------|------------------------|-----------------------------------|-----|----------------------|--------------|------------|------------|
|                       | Page Size                     | Die | Planes | #block<br>per plane | Page<br>per block | Spare Byte<br>per page | Spare Byte<br>per partial<br>page | NOP | Partial<br>Word Size | CA<br>bits   | PA<br>bits | BA<br>bits |
| 01Gb_2KB              | 2KB                           | 1   | 1      | 1024                | 64                | 64                     | 16                                | 4   | 512B                 | 12           | 6          | 10         |
| 01Gb_2KB              | 2KB                           | 1   | 1      | 1024                | 64                | 128                    | 32                                | 4   | 512B                 | 12           | 6          | 10         |
| 02Gb_2KB              | 2KB                           | 1   | 2      | 1024                | 64                | 128                    | 32                                | 4   | 512B                 | 12           | 6          | 11         |
| 04Gb_2KB              | 2KB                           | 1   | 2      | 2048                | 64                | 128                    | 32                                | 4   | 512B                 | 12           | 6          | 12         |

Notes:

1. CA<sub>b</sub> = Column Address bit.
2. PA<sub>b</sub> = Page Address bit.
3. BA<sub>b</sub> = Block Address bit.

**Table 5 : Address phase cycles for buffer and array operations**

| Address Cycle Map  |           |             |        |        |        |         |         |         |             |
|--|-----------|-------------|--------|--------|--------|---------|---------|---------|-------------|
| Bus Cycle  | SI        | SI[7] (MSB) | SI[6]  | SI[5]  | SI[4]  | SI[3]   | SI[2]   | SI[1]   | SI[0] (LSB) |
| <b>Buffer Operation:</b> Load Pin inputs Data to Buffer or Data Buffer to Output Pins  |           |             |        |        |        |         |         |         |             |
| 1 <sup>st</sup>  | CA[15:8]  | Low         | Low    | Low    | Low    | CAX[11] | CAX[10] | CAX[9]  | CAX[8]      |
| 2 <sup>nd</sup>  | CA[7:0]   | CAX[7]      | CAX[6] | CAX[5] | CAX[4] | CAX[3]  | CAX[2]  | CAX[1]  | CAX[0]      |
| <b>Array Operation:</b> Load Data Array to buffer or Program Data from buffer to Array |           |             |        |        |        |         |         |         |             |
| Bus Cycle  | SI        | SI[7] (MSB) | SI[6]  | SI[5]  | SI[4]  | SI[3]   | SI[2]   | SI[1]   | SI[0] (LSB) |
| 1 <sup>st</sup>  | PA[23:16] | Low         | Low    | Low    | Low    | low     | Low     | BAX[11] | BAX[10]     |
| 2 <sup>nd</sup>  | PA[15:8]  | BAX[9]      | BAX[8] | BAX[7] | BAX[6] | BAX[5]  | BAX[4]  | BAX[3]  | BAX[2]      |
| 3 <sup>rd</sup>  | PA[7:0]   | BAX[1]      | BAX[0] | PAX[5] | PAX[4] | PAX[3]  | PAX[2]  | PAX[1]  | PAX[0]      |

Notes:

1. CA<sub>x</sub> = Column Address bit. If CA[11]=1 then CA[10:7] must Low
2. PA<sub>x</sub> = Page Address bit.
3. BA<sub>x</sub> = Block Address bit.

Since Dual plane operation are not supported in SPI, therefore the whole array is described in number of blocks.  
The planes are reflected in this document to match the physical implementation.

| Density_Page Size | #of<br>Dies | #<br>Planes | #Blocks<br>per plane | BA[13:0]              | Plane Selection |
|-------------------|-------------|-------------|----------------------|-----------------------|-----------------|
| 01Gb_2KB          | 1           | 1           | 1024                 | BA[13:10]=L, BA[9:0]  | N/A             |
| 02Gb_2KB          | 1           | 2           | 1024                 | BA[13:11]=L, BA[10:0] | BA[0]           |
| 04Gb_2KB          | 1           | 2           | 2048                 | BA[13:12]=L, BA[11:0] | BA[0]           |

## 2. Bus Operation

### 2.1 SPI Modes

The SPI NAND can be driven by a micro-controller with its SPI interface running in either of the two following clocking modes:

**Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0

**Mode 3** with CPOL = 1 and, CPHA = 1

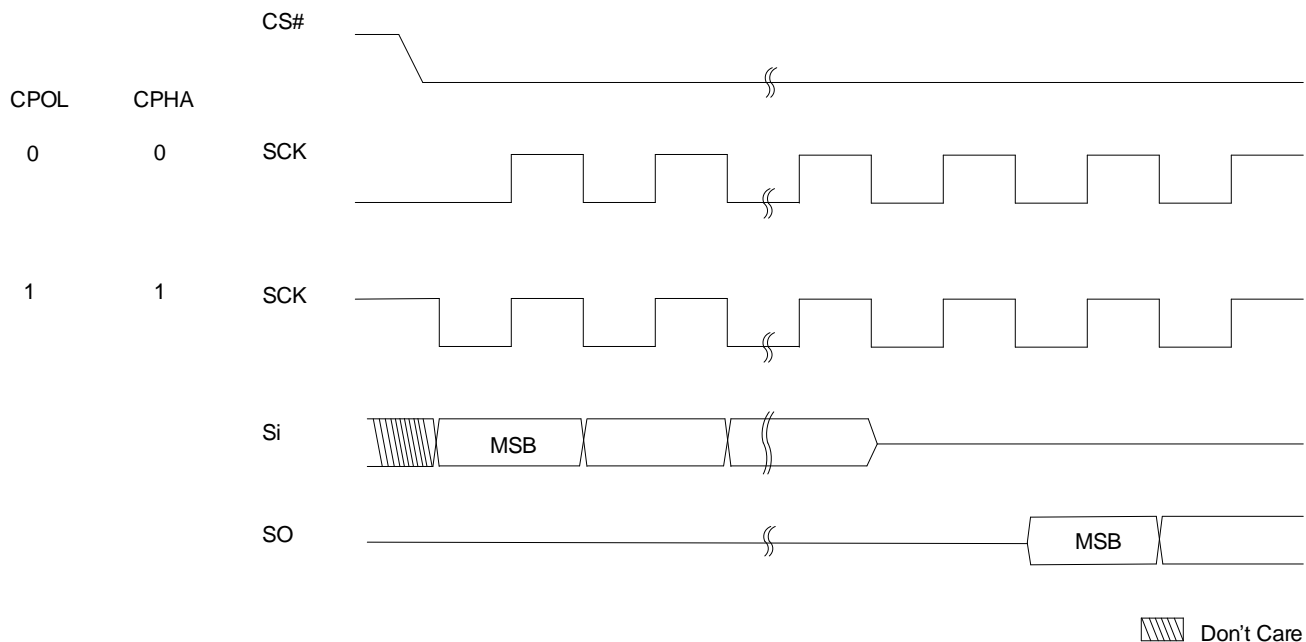
For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

SCK will stay at logic low state with CPOL = 0, CPHA = 0

SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 7. SPI Modes Timing Diagram



### 2.1 SPI Protocols

#### Standard (Traditional) SPI

Standard SPI NAND Flash supports a serial peripheral interface with 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) Serial Data Output (SO).

#### Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SI/IO0, SO/IO1

#### Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI, SO, WP#, HOLD# pins become bidirectional I/O pins: SI/IO0, SI/IO1, WP#/IO2, HOLD#/IO3

### 3. Command Set

Table 6 : Command Set

| Command                              | Op Code    | Byte 2                                 | Byte 3 | Byte 4                               | Byte 5   | Byte 6   | Byte 7 | Notes                                   |
|--------------------------------------|------------|--|--------|--------------------------------------|----------|----------|--------|---|
| Reset                                | FFh        |  |        |                                      |          |          |        |   |
| Write Enable                         | 06h        |  |        |                                      |          |          |        |   |
| Write Disable                        | 04h        |  |        |                                      |          |          |        |   |
| Get Feature                          | 0Fh        | CA7-0                                  | D7-0   |                                      |          |          |        |   |
| Set Feature                          | 1Fh        | CA7-0                                  | D7-0   |                                      |          |          |        |   |
| Read ID                              | 9Fh        | 8 Dummy clock cycles (So Output HighZ) | D7-0   | D7-0                                 |          |          |        |   |
| Block Erase                          | D8h        | PA23-16                                | PA15-8 | PA7-0                                |          |          |        |   |
| <b>Array operations</b>              |            |  |        |                                      |          |          |        |   |
| Program Execute                      | 10h        | PA23-16                                | PA15-8 | PA7-0                                |          |          |        |   |
| Page Read                            | 13h        | PA23-16                                | PA15-8 | PA7-0                                |          |          |        |   |
| <b>Buffer operations</b>             |            |  |        |                                      |          |          |        |   |
| Read Buffer 1X                       | 03h or 0Bh | CA15-8                                 | CA7-0  | 8 Dummy clock cycles (Outputs HighZ) | D7-0     | D7-0     |        |   |
| Dual Read Output 2X                  | 3Bh        | CA15-8                                 | CA7-0  | 8 Dummy cycles (HighZ)               | D7-0(2X) | D7-0(2X) |        | 4 clock cycles to output 1 Byte of Data |
| Quad Read Output 4X                  | 6Bh        | CA15-8                                 | CA7-0  | 8 Dummy clock cycles (outputs HighZ) | D7-0(4X) | D7-0(4X) |        | 2 clock cycles to output 1 Byte of Data |
| Program Load 1X                      | 02h        | CA15-8                                 | CA7-0  | D7-0                                 | D7-0     | D7-0     |        |   |
| Program Load Random Data 1X (Note 1) | 84h        | CA15-8                                 | CA7-0  | D7-0                                 | D7-0     | D7-0     |        |   |

## Command Set- cont'd

|   |     |            |           |  |                                      |          |  |  |
|---|-----|------------|-----------|--|--------------------------------------|----------|--|--|
| Fast Read Dual I/O                        | BBh | CA15-8(2X) | CA7-0(2X) | 8 Dummy clock cycles (outputs High Z) (Note 4) | D7-0(2X)                             | D7-0(2X) |  |  |
| Fast Read Quad I/O                        | EBh | CA15-8(4X) | CA7-0(4X) | 8 Dummy clock cycles (outputs High Z) (Note 4) | D7-0(4X)                             | D7-0(4X) |  |  |
| Quad Program Data Load 4X                 | 32h | CA15-8     | CA7-0     | D7-0(4X)                                       | D7-0(4X)                             | D7-0(4X) |  | 2 clock cycles to input 1 Byte Data    |
| Quad Program Data Load Random 4X (Note 2) | 34h | CA15-8     | CA7-0     | D7-0(4X)                                       | D7-0(4X)                             | D7-0(4X) |  | 2 clock cycles to input 1 Byte of Data |
| <b>Block Protection operations</b>        |     |            |           |  |                                      |          |  |  |
| Block Protection Status                   | 7Ah | PA23-16    | PA15-8    | PA7-0  | 8 Dummy clock cycles (Outputs HighZ) | D7-0     |  |  |
| Program PBP Setting (Note 3)              | 2Ch | PBPA23-16  | PBPA15-8  | PBPA7-0  |                                      |          |  |  |

### Notes:

1. The Program Load random data (84h) operation is similar to Program Load 02h. The 84h command does not clear the data buffer to an all FFh value and will only update the data bytes specified by the command input sequence while the rest of the input buffer remains unchanged. The host must always consider chunks of 32 bytes starting from address 0 to accommodate internal ECC requirements.
2. The Quad Program Load (32h) operation is similar to Quad Program Load random data (34h). The 34h command does not clear the data buffer to an all FFh value and will only update the data bytes specified by the command input sequence while the rest of the input buffer remains unchanged. The host must always consider chunks of 32 bytes starting from address 0 to accommodate internal ECC requirements.
3. PBPA 23-0 address cycle mapping is described in the Security Features section.
4. The number of dummy cycles is 8 cycles for 01Gb/02Gb/04Gb .



### 3.1 Power up and Reset Commands

Reset (FFh) command is required after power-on as a first command for S35ML02/04G3 and optional for S35ML01G3 .

(Call factory for S35ML02/04G3 no FFh option as a first command after power-on)

During Power on Reset, the first page data of page0 is auto-loaded to the buffer register.

The reset command FFh, does not clear the feature registers but does clear the configuration register bits CONFIG[2:0] placing the device in normal operation.

### 3.2 Write Enable and Write Disable Commands

A WRITE\_EN (06h) command needs to be issued before any OTP, Program Execute and Block Erase operation . A WRITE\_DIS (04h) command is also provided to clear the WSEL bit in the status register (see GET FEATURES and SET\_FEATURES section).

### 3.3 Hardware Write Protection

Hardware write protection prevents the block protection state from hardware modifications.

The following command sequence enables hardware write protection: The SET FEATURE command is issued on feature address A0h. Then, the Config\_Protect\_en bit-state is set to 0 as the default after power up.

The BRWD bit is operated in conjunction with Config\_Protect\_en bit. When BRWD is set to 1 and WP# is LOW, none of the other block protect register A0h bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked.

Also, when the WP#/Hold# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and Config\_Protect\_en bits = 0 after power up.

### 3.4 Read Operation

The PAGE READ (13h) command uses 24-bit address to transfers data from the NAND Flash array to the Data register. After the block/page address is registered, the device starts the transfer from the main array to the data register. During this data transfer busy time of t<sub>R</sub>, the 0Fh GET FEATURES command can be issued to monitor the operation.

Following successful completion of PAGE READ, one of the following READ commands must be issued to read data out of data buffer:

- 03h or 0Bh (READ buffer 1X)
- 3Bh (Dual Read Output 2X)
- 6Bh (Quad READ Output 4X)
- BBh (Fast READ Dual I/O)
- EBh (Fast READ Quad I/O)

### 3.5 Page Program Operation

A PAGE PROGRAM operation sequence enables the host to input 1 byte to 2176 bytes of data (Page size: 2048 + 128 spare bytes) or 1 byte to 2112 bytes (Page size: 2048 + 64 spare bytes) of data to the data register, and moves the data from the data register to the specified block and page address in the array. Four partial-page programs are allowed on a single page. If more than 2176 bytes are loaded, the additional bytes will be ignored by the data register.

Both main data and user spare shall be input at the same time for NOP operation; otherwise, data is not guaranteed.

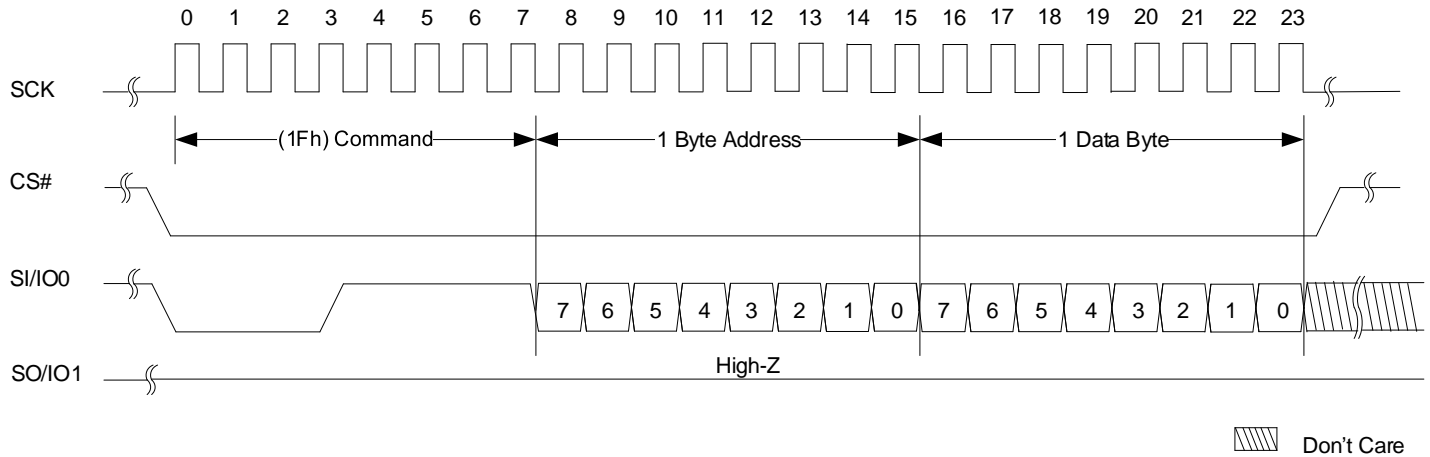
The page program sequence starts by issuing 06h (Write Enable Command) followed by 02h (Program Load Command) and 10h (ProgramExecute Command). the 0Fh GET FEATURES command can be issued to monitor the operation.

### 3.6 Feature Operations

#### 3.6.1 Set Features

The SET FEATURE command uses a 1-byte feature address to specify the feature to be modified.

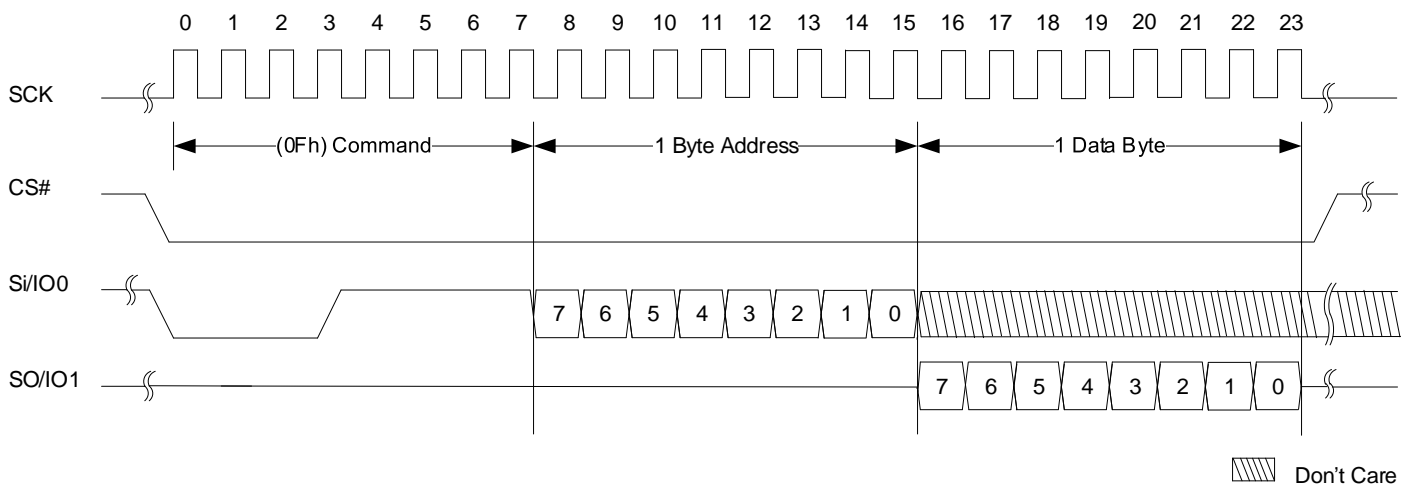
**Figure 8. SET FEATURE Timing Diagram**



#### 3.6.2 Get Features

The GET FEATURE command uses a 1-byte feature address to specify the feature to be read.

**Figure 9. GET FEATURE Timing Diagram**



### 3.7 Feature Registers

There are 3 registers with the following addresses: A0h, B0h and C0h. While the Set Feature commands may only writes in some of the registers, the Get Feature commands allows reading back the content of all these registers. During Get Feature operation, the same status register is continuously outputted until CS# goes high.

The feature registers are volatile. Each POR will reset these registers to the default value. The Reset (FFh) only clears the configuration bits (B0[7,1,0]) to zero.

**Table 7 : Feature Address A0h (Block Protect Register R/W, protected when WP# pin = 0)**

| Bit | Symbol                         | Parameter                    | Default | Description   |
|-----|--------------------------------|------------------------------|---------|---|
| 7   | BRWD <sup>1</sup>              | Block Register Write Disable | 0       | 1b: Disable update of the A0[7:0] when WP# Low<br>0b: Enable update of the A0[7:0] (Default)  |
| 6   | AVBP_BL[3] <sup>1</sup>        | AVBP Lock 3                  | 1       | Volatile Block protection based on addressable blocks in the device<br>0000b: All Blocks Unlocked<br>0001b: 1/1024 Blocks Locked<br>0010b: 1/512 Blocks Locked<br>0011b: 1/256 Blocks Locked<br>0100b: 1/128 Blocks Locked<br>0101b: 1/64 Blocks Locked<br>0110b: 1/32 Blocks Locked<br>0111b: 1/16 Blocks Locked<br>1000b: 1/8 Blocks Locked<br>1001b: 1/4 Blocks Locked<br>1010b: 1/2 Blocks Locked<br>1011b: All Blocks locked<br>11xx: All Blocks Locked<br><b>1111b: All Blocks Locked (default)</b> |
| 5   | AVBP_BL[2] <sup>1</sup>        | AVBP Lock 2                  | 1       |   |
| 4   | AVBP_BL[1] <sup>1</sup>        | AVBP Lock 1                  | 1       |   |
| 3   | AVBP_BL[0] <sup>1</sup>        | AVBP Lock 0                  | 1       |   |
| 2   | AVBP_BL_U <sup>1</sup>         | AVBP Lock Upper/Lower range  | 1       | 1: Protect Upper blocks<br>0: Protect Lower blocks  |
| 1   | Config_Protect_en <sup>1</sup> | WP#/Config_Protect enable    | 0       |   |
| 0   | Reserved                       | Reserved                     | 0       |   |

**Table 8 : Feature Address A0h protection**

|        |             |   |                                    |                |                                    |                                    |
|--------|-------------|---|------------------------------------|----------------|------------------------------------|------------------------------------|
| State  | WP# pin     | 0 | 1                                  | 1              | 1                                  | 1                                  |
|        | A0h[7]=BRWD | X | 0                                  | 0              | 1                                  | 1                                  |
|        | A0h[1]      | X | 0                                  | 1              | 1                                  | 0                                  |
| Effect | A0h[1]      | R | W/R                                | W/R            | W/R                                | W/R                                |
|        | A0h[7:2]    | R | A0h[7:2] = R Protected By A0h[1]=0 | A0h[7:2] = W/R | A0h[7:2] = R Protected By A0h[7]=1 | A0h[7:2] = R Protected By A0h[1]=0 |

1) A0h[1]= 0

A0h[7:2] R/W :Write operation depends on WP#, A0h[1], and A0h[7] values

2) For Data Security, bit (A0h[1]) must be enabled first before block unlock region is set

3) Feature address A0h command is allowed to be issued in OIP Ready status

**Table 9 : Feature Address B0h (Configuration Register R/W, protected when WP# pin = 0)**

| Bit | Symbol     | Parameter                | Default | Description  |
|-----|------------|--------------------------|---------|--|
| 7   | Config[2]  | Configuration bit 2      | 0       | Config[2:0]<br>000: (default) Normal Operation<br>010: Access OTP Area/parameter page / Unique ID (Note 1)<br>110: <b>Access to OTP data protection bit to lock OTP area</b><br>111: Access to PBP lock-down |
| 6   | Config[1]  | Configuration bit 1      | 0       |  |
| 5   | AVBP_LD_EN | Advance Lock down enable | 0       | 1: AVBP_Lock down is enabled A0[7:0] and B0[5] are locked until power down.<br>0: AVB_Lock_down is disabled  |
| 4   | ECC_Enable | ECC_Enable               | 1       | Must be always set to 1  |
| 3   | Reserved   | Reserved                 | 0       |  |
| 2   | Reserved   | Reserved                 | 0       |  |
| 1   | Config[0]  | Configuration bit 0      | 0       | See Config[2:1] description  |
| 0   | Reserved   | Reserved                 | 0       |  |

1) AVBP\_LD\_EN when set to 1, this bit along with the Block Protection register [6:0] can only be cleared during POR

2) Feature address B0h command is allowed to be issued in OIP Ready status

**Table 10 : Feature Address C0h (Status Register R Only)**

| Bit | Symbol   | Parameter                               | Default | Description  |
|-----|----------|---|---------|--|
| 7   | Reserved | Reserved                                | 0       |  |
| 6   | Reserved | Reserved                                | 0       |  |
| 5   | ECCS1    | ECC status register[1:0] <sup>1,2</sup> | 0       | 11 = 5-6 errors (Rewrite recommended)<br>10 = 3-4 errors corrected<br>01 = 1-2 errors corrected<br>00 = Normal     |
| 4   | ECCS0    |   | 0       |  |
| 3   | P_Fail   | Program fail                            | 0       | 1: Program failure occurred<br>0: Operation passed   |
| 2   | E_Fail   | Erase fail                              | 0       | 1: Erase Failure occurred<br>0: Operation passed   |
| 1   | WEL      | Write enable latch                      | 0       | 1: Write Enabled<br>0: Write Disabled  |
| 0   | OIP      | Operation in progress                   | 0       | 1: Device is busy with executing commands:<br>Reset, Program Execute, Page Read, Block Erase<br>0: Device is ready |

1: SR [5:4] defines the number of corrections.

2: 11 can be used as uncorrectable.

3: A Program and Erase fails include a block being protected (Array blocks + OTP) for 1Gb/2Gb densities

A Program fail does not include OTP block for 4Gb density

### 3.8 Read ID

| Byte | Description                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Value |
|------|------------------------------|---|---|---|---|---|---|---|---|-------|
| 0    | Manufacturer ID              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h   |
| 1    | Device ID : 01G (64B Spare)  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15h   |
| 1    | Device ID : 01G (128B spare) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14h   |
| 1    | Device ID : 02G              | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25h   |
| 1    | Device ID : 04G              | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35h   |

### 3.9 Read Unique ID

#### Read Unique ID located in OTP page 0

- Use SET FEATURES command (1Fh) with feature address B0h and data value of 50h for ECC enabled
- Page Read command (13h) with Block/Page address:
  - 0x180 for unique ID (OTP page 0)
  - GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready
- Read Buffer (03h) command to read the data out
- Use SET FEATURES command (1Fh) with feature address B0h and data value with Config[2:0] = 000b to exit.
- Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

### 3.10 One-Time Programmable (OTP)

The device contains a one-time programmable (OTP) area, that consists of (62 pages), accessed by SET/GET FEATURES commands

#### 3.10.1 OTP Read

##### OTP Read: 62 pages accessible for user data located in Block #6 from page 2 to page 63

- Use SET FEATURES command (1Fh) with feature address B0h and data value of 50h.
- Page Read command (13h) with Block/Page address (0x182h-0x19Fh)  
GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready
- Read Buffer (03h) command to read the data out
- Use SET FEATURES command (1Fh) with feature address B0h and data value with Config[2:0] = 000b to exit
- Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

#### 3.10.2 OTP Program

##### OTP Program: 62 pages accessible for user data located in Block 6 from page 2 to page 63

- Use SET FEATURES command (1Fh) with feature address B0h and data value of 50h for ECC enabled
- Use Write Enable command 06h
- Program using Load command x1 (02h), Quad Program Data Load (32h) or random program data load with data
- Program Execute command x1 (10h) with Block/Page address (0x182h-0x19Fh)
- Use GET FEATURE command (0Fh) with feature address C0h to check OIP bitready
- Use SET FEATURES command (1Fh) with feature address B0h and value with Config[2:0] = 000b to exit
- After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P\_Fail bit is not set.

### 3.10.3 OTP Data Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. The following sequence is used to protect and prevent further programming of the OTP area:

- Use SET FEATURES command (1Fh) with feature address B0h and Config [2:0] = 110b
- Use Write Enable command 06h
- Program execute command (10h) with row address 00h
- Verify until OIP bit not busy and P\_FAIL bit 0 using GET FEATURE command (0Fh) with status register address (C0h)

### 3.11 Internal Data Move (S35ML02G3, S35ML04G3)

The copy back feature is intended to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also needs to be copied to the newly assigned free block. For S35ML02G3/ S35ML04G3, the source and destination pages in the Copy Back Program sequence must belong to the same device plane (same BA[0]). If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h), (34h) command must be issued with the new column address.

The internal data move command sequence is as follows:

- Page Read command (13h)
- Write Enable command (06h)
- Program Load Random Data command (84h), (34h)
- Program Execute command (10h)
- Get Feature command (0Fh) - Read the Status

### 3.12 Read Parameter Page

- Use SET FEATURES command (1Fh) with feature address B0h and data value of 50h for ECC enabled
- Page Read command (13h) with Block/Page address:  
 - 0x181 for Parameter Page (located OTP page 1)
- GET FEATURE command (0Fh) with feature address C0h to check OIP bitready
- Read Buffer (03h) command to read the data out
- Use SET FEATURES command (1Fh) with feature address B0h and data value with Config[2:0] = 000b to exit
- Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

**Table 11: Parameter Page Description**

| Byte   | O/M | Description  | Values   |
|--|-----|--|--|
| <b>Revision Information and Features Block</b> |     |  |  |
| 0-3  | M   | Parameter page signature   | 4Fh, 4Eh, 46h, 49h   |
| 4-5  | M   | Revision number<br>2-15 Reserved (0)<br>1 1 = supports ONFI version 1.0<br>0 Reserved (0)  | 00h, 00h   |
| 6-7  | M   | Features supported<br>5-15 Reserved (0)<br>4 1 = supports odd to even page Copyback<br>3 1 = supports interleaved operations<br>2 1 = supports non-sequential page programming<br>1 1 = supports multiple LUN operations<br>0 1 = supports 16-bit data bus width   | 00h, 00h   |
| 8-9  | M   | Optional commands supported<br>6-15 Reserved (0)<br>5 1 = supports Read Unique ID (contact factory)<br>4 1 = supports Copyback<br>3 1 = supports Read Status Enhanced<br>2 1 = supports Get Features and Set Features<br>1 1 = supports Read Cache commands<br>0 1 = supports Page Cache Program command | ML01G3: 24h, 00h<br>ML02G3 / ML04G3: 34h, 00   |
| 10-31  |     | Reserved (0)   | 00h  |
| <b>Manufacturer Information Block</b>          |     |  |  |
| 32-43  | M   | Device manufacturer (12 ASCII characters)  | 53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h   |
| 44-63  | M   | Device model (20 ASCII characters)   | S35ML01G3: 53h, 33h, 35h, 4Dh, 4Ch, 30h, 31h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h<br>S35ML02G3: 53h, 33h, 35h, 4Dh, 4Ch, 30h, 32h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h<br>S35ML04G3: 53h, 33h, 35h, 4Dh, 4Ch, 30h, 34h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| 64   | M   | JEDEC manufacturer ID  | 01h  |
| 65-66  | O   | Date code  | 00h  |
| 67-79  |     | Reserved (0)   | 00h  |
| <b>Memory Organization Block</b>               |     |  |  |
| 80-83  | M   | Number of data bytes per page  | 00h, 08h, 00h, 00h   |



**Table 11. Parameter Page Description (Continued)**

| Byte                               | O/M | Description  | Values  |
|------------------------------------|-----|--|---|
| 84-85                              | M   | Number of spare bytes per page   | S35ML01G3 (64B spare): 40h, 00h<br>S35ML01G3 (128B spare): 80h, 00h<br>S35ML02G3/ S35ML04G3 :80h, 00h |
| 86-89                              | M   | Number of data bytes per partial page  | 00h, 02h, 00h, 00h  |
| 90-91                              | M   | Number of spare bytes per partial page   | S35ML01G3 (64B spare): 10h, 00h<br>S35ML01G3 (128B spare): 20h, 00h<br>S35ML02G3/ S35ML04G3: 20h, 00h |
| 92-95                              | M   | Number of pages per block  | 40h, 00h, 00h, 00h  |
| 96-99                              | M   | Number of blocks per logical unit (LUN)  | S35ML01G3: 00h, 04h, 00h, 00h<br>S35ML02G3: 00h, 08h, 00h, 00h<br>S35ML04G3: 00h, 10h, 00h, 00h       |
| 100                                | M   | Number of logical units (LUNs)   | 01h   |
| 101                                | M   | Number of address cycles<br>4-7 Column address cycles<br>0-3 Row address cycles  | 00h   |
| 102                                | M   | Number of bits per cell  | 01h   |
| 103-104                            | M   | Bad blocks maximum per LUN   | S35ML01G3: 14h, 00h<br>S35ML02G3: 28h, 00h<br>S35ML04G3: 50h, 00h                                     |
| 105-106                            | M   | Block endurance  | 08h, 04h (-40°C to 85°C)<br>06h, 04h (-40°C to 105°C)   |
| 107                                | M   | Guaranteed valid blocks at beginning of target   | 08h   |
| 108-109                            | M   | Block endurance for guaranteed valid blocks  | 00h, 00h  |
| 110                                | M   | Number of programs per page  | 04h   |
| 111                                | M   | Partial programming attributes<br>5-7 Reserved<br>4 1 = partial page layout is partial page data followed by partial page spare<br>1-3 Reserved<br>0 1 = partial page programming has constraints  | 00h   |
| 112                                | M   | Number of bits ECC correctability  | 00h   |
| 113                                | M   | Number of interleaved address bits<br>4-7 Reserved (0)<br>0-3 Number of interleaved address bits   | 00h, 00h  |
| 114                                | O   | Interleaved operation attributes<br>4-7 Reserved (0)<br>3 Address restrictions for program cache<br>2 1 = program cache supported<br>1 1 = no block address restrictions<br>0 Overlapped / concurrent interleaving support                             | 00h, 00h  |
| 115-127                            |     | Reserved (0)   | 00h   |
| <b>Electrical Parameters Block</b> |     |  |   |
| 128                                | M   | I/O pin capacitance  | 0Ah   |
| 129-130                            | M   | Timing mode support<br>6-15 Reserved (0)<br>5 1 = supports timing mode 5<br>4 1 = supports timing mode 4<br>3 1 = supports timing mode 3<br>2 1 = supports timing mode 2<br>1 1 = supports timing mode 1<br>0 1 = supports timing mode 0, shall be 1   | 00h, 00h  |
| 131-132                            | O   | Program cache timing mode support<br>6-15 Reserved (0)<br>5 1 = supports timing mode 5<br>4 1 = supports timing mode 4<br>3 1 = supports timing mode 3<br>2 1 = supports timing mode 2<br>1 1 = supports timing mode 1<br>0 1 = supports timing mode 0 | 00h, 00h  |
| 133-134                            | M   | t <sub>PROG</sub> Maximum page program time (μs)   | 58h, 02h  |

**Table 11. Parameter Page Description (Continued)**

| Byte                             | O/M | Description  | Values   |
|----------------------------------|-----|--|--|
| 135-136                          | M   | t <sub>BERS</sub> Maximum block erase time (μs)        | 10h, 27h   |
| 137-138                          | M   | t <sub>R</sub> Maximum page read time (μs)             | FAh, 00h   |
| 139-140                          | M   | t <sub>CCS</sub> Minimum Change Column setup time (ns) | 00h, 00h   |
| 141-163                          |     | Reserved (0)   | 00h  |
| <b>Vendor Block</b>              |     |  |  |
| 164-165                          | M   | Vendor specific Revision number                        | 00h  |
| 166-253                          |     | Vendor specific  | 00h  |
| 254-255                          | M   | Integrity CRC  | 01G3/64B spare (-40°C to 85°C):1Eh, 94h<br>01G3/64B spare (-40°C to 105°C):94h,BCh<br>01G3/128B spare(-40°C to 85°C):B0h, D2h<br>01G3/128B spare(-40°C to 105°C):3Ah,FAh<br>02G3 (-40°C to 85°C): 7Bh, 66h<br>02G3 (-40°C to 105°C): F1h, 4Eh<br>04G3 (-40°C to 85°C) : 05h, 2Dh<br>04G3 (-40°C to 105°C) : 8Fh, 05h |
| <b>Redundant Parameter Pages</b> |     |  |  |
| 256-511                          | M   | Value of bytes 0-255                                   | Repeat Value of bytes 0-255  |
| 512-767                          | M   | Value of bytes 0-255                                   | Repeat Value of bytes 0-255  |
| 768+                             | O   | Additional redundant parameter pages                   | FFh  |

**Note:**

1. O" Stands for Optional, "M" for Mandatory, "N/A" for Not Applicable.

## 4. Electrical Characteristics

### 4.1 Valid Blocks

Table 12. Valid Blocks

| Device    | Symbol   | Min  | Typ | Max  | Unit   |
|-----------|----------|------|-----|------|--------|
| S35ML01G3 | $N_{VB}$ | 1004 | —   | 1024 | Blocks |
| S35ML02G3 | $N_{VB}$ | 2008 | —   | 2048 | Blocks |
| S35ML04G3 | $N_{VB}$ | 4016 | —   | 4096 | Blocks |

### 4.2 Absolute Maximum Ratings

Table 13: Absolute Maximum Ratings

| Parameter                      | Symbol | Test conditions | Min  | Typ | Max | Units | Comments |
|--------------------------------|--------|-----------------|------|-----|-----|-------|----------|
| Temperature under Bias         | TBIAS  |                 | -50  |     | 125 | °C    |          |
| Storage Temperature            | TSTG   |                 | -65  |     | 150 | °C    |          |
| Input or Output Voltage (3.3V) | VIO    |                 | -0.6 |     | 4.6 | V     |          |
| Supply Voltage (3.3V)          | VCC    |                 | -0.6 |     | 4.6 | V     |          |

**Notes:**

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the table [Absolute Maximum Ratings](#) “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.
3. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions.

### 4.3 Recommended Operating Conditions

Table 14: Recommended Operating Conditions

| Parameter             | Symbol | Min | Typ | Max | Units |
|-----------------------|--------|-----|-----|-----|-------|
| Vcc Supply Voltage    | Vcc    | 2.7 | 3.3 | 3.6 | V     |
| Ground Supply Voltage | Vss    | 0   | 0   | 0   | V     |

### 4.4 AC Test Conditions

Table 15: AC Test Conditions

| Parameter                      | Value                       |
|--------------------------------|-----------------------------|
| Input Pulse Levels             | 0.0 V to $V_{CC}$           |
| Input Rise and Fall Times      | 5 ns                        |
| Input and Output Timing Levels | $V_{CC} / 2$                |
| Output Load (2.7V - 3.6V)      | 1 TTL Gate and $CL = 30$ pF |

## 4.5 AC Characteristics

**Table 16:** AC Characteristics

| Symbol      | SPI-NOR Symbol | Parameter                 | Min   | Typ | Max | Unit |
|-------------|----------------|---------------------------|-------|-----|-----|------|
| fC          |                | Serial Clock Frequency    |       |     | 104 | MHz  |
| tCH         | tWH            | Serial Clock High Time    | 4.316 |     |     | ns   |
| tCL         | tWL            | Serial Clock Low Time     | 4.316 |     |     | ns   |
| tCLCH       | tCRT           | Serial Clock Rise Time    | 1.3   |     |     | V/ns |
| tCHCL       | tCFT           | Serial Clock Fall Time    | 1.3   |     |     | V/ns |
| tSLCH       |                | CS# Active Setup Time     | 4.316 |     |     | ns   |
| tCHSH       |                | CS# Active Hold Time      | 4.316 |     |     | ns   |
| tSHCH       |                | CS# Not Active Setup Time | 2.877 |     |     | ns   |
| tCHSL       |                | CS# Not Active Hold Time  | 2.877 |     |     | ns   |
| tSHSL / tCS |                | CS# High Time             | 30    |     |     | ns   |
| tSHQZ       | tDIS           | Output Disable Time       |       |     | 10  | ns   |

## AC Characteristics- cont'd

|       |        |  |      |    |               |    |
|-------|--------|--|------|----|---------------|----|
| tCLQX | tHO    | Output Hold Time   | 2    |    |               | ns |
| tDVCH | tSUDAT | Data In Setup Time   | 2.5  |    |               | ns |
| tCHDX | tHD    | Data In Hold Time  | 1.75 |    |               | ns |
| tHLCH |        | Hold# Low Setup Time relative to Clock                         | 5    |    |               | ns |
| tHHCH |        | Hold# High Setup Time relative to Clock                        | 5    |    |               | ns |
| tCHHL |        | Hold# High Hold Time relative to Clock                         | 5    |    |               | ns |
| tCHHH |        | Hold# Low Hold Time relative to Clock                          | 5    |    |               | ns |
| tHLQZ |        | Hold# Low To High-Z Output                                     |      |    | 12            | ns |
| tHHQX |        | Hold# High To Output   |      |    | 9             | ns |
| tCLQV | tV     | Clock Low To Output Valid                                      |      |    | 7<br>(Note 2) | ns |
| tWHSL | tWPS   | WP# Setup Time Before CS# Low                                  | 20   |    |               | ns |
| tSHWL | tWPH   | WP# Hold Time After CS# High                                   | 100  |    |               | ns |
| tRST  |        | Device Reset Time<br>(Ready/Read/Program/Erase)                |      |    | 5/6/10/500    | μs |
| tR    |        | Data transfer from cell to register<br>tR with internal ECC on |      | 45 | 250           | μs |

Note 1: VCC = 2.7V - 3.6V

Note 2: The maximum value for tCLQV at 105°C = 7.5ns

## 4.6 DC Characteristics

**Table 17:** DC Characteristics and Operating Conditions

| Parameter                         | Symbol | Test Conditions              | Min       | Typ | Max       | Units |
|-----------------------------------|--------|------------------------------|-----------|-----|-----------|-------|
| Standby current                   | ICC1   | CS# = VIH,<br>Vin= 0V or VCC |           | 20  | 100       | uA    |
| Read Current                      | ICC2   |                              |           | 25  | 35        | mA    |
| Array program current             | ICC3   |                              |           | 20  | 25        | mA    |
| Array erase current               | ICC4   |                              |           | 20  | 25        | mA    |
| Input leakage current             | ILI    |                              |           |     | ±10       | uA    |
| Output leakage current ILO        | ILO    |                              |           |     | ±10       | uA    |
| DC Input high voltage             | VIH    |                              | VCC * 0.8 |     | VCC + 0.3 | V     |
| DC Input low voltage              | VIL    |                              | -0.3      |     | VCC * 0.2 | V     |
| Output high voltage               | VOH    | IOH=-400 µA                  | 2.4       |     |           | V     |
| Output low voltage                | VOL    | IOL=2.1mA                    |           |     | 0.4       | V     |
| Erase and program lockout voltage | VLKO   |                              |           | 1.8 |           | V     |

## 4.7 Pin Capacitance

**Table 18:** Pin Capacitance (TA = 25°C, f = 1.0 MHz)

| Parameter      | Symbol          | Test Condition       | Min | Max | Unit |
|----------------|-----------------|----------------------|-----|-----|------|
| Input          | C <sub>IN</sub> | V <sub>IN</sub> = 0V | —   | 10  | pF   |
| Input / Output | C <sub>IO</sub> | V <sub>IL</sub> = 0V | —   | 10  | pF   |

## 4.8 Program / Erase Characteristics

**Table 19:** Program / Erase Characteristics

| Parameter  | Description       | Min | Typ | Max | Unit   |
|--|-------------------|-----|-----|-----|--------|
| Program Time   | t <sub>PROG</sub> |     | 350 | 600 | uS     |
| Block Erase Time   | t <sub>BERS</sub> |     | 4   | 10  | ms     |
| Number of partial Program Cycles in the same page (Main + Spare) | NOP               |     |     | 4   | Cycles |
| Power on Reset Time  | t <sub>POR</sub>  |     |     | 2   | ms     |

## 5. Security Features

The security features below provide block protection from program and erase operations. Two security methods are described below:

- Advanced Volatile Block Protection (AVBP)

The AVBP parameter settings are stored in registers that can be accessed through Set and Get feature commands. Power cycling will reset the settings to the default status (all blocks protected on power up). This AVBP method can protect one range of contiguous blocks. The Set Feature command must be issued to alter the state of the AVBP. After power-up, the device is in the locked state by default.

- Permanent Block Protection (PBP)

The PBP parameter settings will be maintained after a power cycle. The PBP method can protect up to 64 blocks (blocks 0 to 63) organized in groups of 4 contiguous blocks. Each group can be protected individually and are permanently protected.

### 5.1 Volatile Block Protection (VBP) Overview

The AVBP feature can protect all blocks, or one selected range of contiguous blocks, from erase and program operations. After a power-cycle, all blocks are protected as the AVBP\_BL[3:0] bits are high (see Block protection feature register (A0h).) The SET FEATURE command must be issued to alter the state of block protection. A Reset command will not reset the A0h register and therefore will not modify the block protection state. When a PROGRAM/ERASE command is issued to a locked block, a status register P\_Fail bit or E\_Fail bit will be set to indicate the operation failure.



The following tables provides block protection range addresses for each device densities and page size.

**Table 20** : AVBP block protection range (Address Min and Max)

1Gb, 2KB page devices

| AVB Block Selection | Description                | 01Gb_2KB |      |
|---------------------|----------------------------|----------|------|
|                     |                            | MIN      | MAX  |
| 10000               | All Blocks unlocked        | -        | -    |
| 10001               | Upper 1/1024 Blocks locked | 1023     | 1023 |
| 10010               | Upper 1/512 Blocks locked  | 1022     | 1023 |
| 10011               | Upper 1/256 Blocks locked  | 1020     | 1023 |
| 10100               | Upper 1/128 Blocks locked  | 1016     | 1023 |
| 10101               | Upper 1/64 Blocks locked   | 1008     | 1023 |
| 10110               | Upper 1/32 Blocks locked   | 992      | 1023 |
| 10111               | Upper 1/16 Blocks locked   | 960      | 1023 |
| 11000               | Upper 1/8 Blocks locked    | 896      | 1023 |
| 11001               | Upper 1/4 Blocks locked    | 768      | 1023 |
| 11010               | Upper 1/2 Blocks locked    | 512      | 1023 |
| all others          | All Blocks locked          | 0        | 1023 |
| 00000               | All Blocks unlocked        | -        | -    |
| 00001               | Lower 1/1024 Blocks locked | 0        | 0    |
| 00010               | Lower 1/512 Blocks locked  | 0        | 1    |
| 00011               | Lower 1/256 Blocks locked  | 0        | 3    |
| 00100               | Lower 1/128 Blocks locked  | 0        | 7    |

AVBP block protection range (Address Min and Max) for for 1Gb, 2KB page devices - cont'd

|                 |                             |   |      |
|-----------------|-----------------------------|---|------|
| 00101           | Lower 1/64<br>Blocks locked | 0 | 15   |
| 00110           | Lower 1/32<br>Blocks locked | 0 | 31   |
| 00111           | Lower 1/16<br>Blocks locked | 0 | 63   |
| 01000           | Lower 1/8<br>Blocks locked  | 0 | 127  |
| 01001           | Lower 1/4<br>Blocks locked  | 0 | 255  |
| 01010           | Lower 1/2<br>Blocks locked  | 0 | 511  |
| all others      | All Blocks locked           | 0 | 1023 |
| 11111 (default) |                             | 0 | 1023 |

**Table 20 :** AVBP block protection range (Address Min and Max)

| 2Gb, 2KB page devices   |                            |          |      | 4Gb, 2KB page devices   |                            |          |      |
|-------------------------|----------------------------|----------|------|-------------------------|----------------------------|----------|------|
| AVB Block Selection     | Description                | 02Gb_2KB |      | AVB Block Selection     | Description                | 04Gb_2KB |      |
| AVBP_BL_U, AVBP_BL[3:0] |                            | MIN      | MAX  | AVBP_BL_U, AVBP_BL[3:0] |                            | MIN      | MAX  |
| 10000                   | All Blocks unlocked        | -        | -    | 10000                   | All Blocks unlocked        | -        | -    |
| 10001                   | Upper 1/1024 Blocks locked | 2046     | 2047 | 10001                   | Upper 1/1024 Blocks locked | 4092     | 4095 |
| 10010                   | Upper 1/512 Blocks locked  | 2044     | 2047 | 10010                   | Upper 1/512 Blocks locked  | 4088     | 4095 |
| 10011                   | Upper 1/256 Blocks locked  | 2040     | 2047 | 10011                   | Upper 1/256 Blocks locked  | 4080     | 4095 |
| 10100                   | Upper 1/128 Blocks locked  | 2032     | 2047 | 10100                   | Upper 1/128 Blocks locked  | 4064     | 4095 |
| 10101                   | Upper 1/64 Blocks locked   | 2016     | 2047 | 10101                   | Upper 1/64 Blocks locked   | 4032     | 4095 |
| 10110                   | Upper 1/32 Blocks locked   | 1984     | 2047 | 10110                   | Upper 1/32 Blocks locked   | 3968     | 4095 |
| 10111                   | Upper 1/16 Blocks locked   | 1920     | 2047 | 10111                   | Upper 1/16 Blocks locked   | 3840     | 4095 |
| 11000                   | Upper 1/8 Blocks locked    | 1792     | 2047 | 11000                   | Upper 1/8 Blocks locked    | 3584     | 4095 |
| 11001                   | Upper 1/4 Blocks locked    | 1536     | 2047 | 11001                   | Upper 1/4 Blocks locked    | 3072     | 4095 |
| 11010                   | Upper 1/2 Blocks locked    | 1024     | 2047 | 11010                   | Upper 1/2 Blocks locked    | 2048     | 4095 |
| all others              | All Blocks locked          | 0        | 2047 | all others              | All Blocks locked          | 0        | 4095 |
| 00000                   | All Blocks unlocked        | -        | -    | 00000                   | All Blocks unlocked        | -        | -    |
| 00001                   | Lower 1/1024 Blocks locked | 0        | 1    | 00001                   | Lower 1/1024 Blocks locked | 0        | 3    |
| 00010                   | Lower 1/512 Blocks locked  | 0        | 3    | 00010                   | Lower 1/512 Blocks locked  | 0        | 7    |
| 00011                   | Lower 1/256 Blocks locked  | 0        | 7    | 00011                   | Lower 1/256 Blocks locked  | 0        | 15   |
| 00100                   | Lower 1/128 Blocks locked  | 0        | 15   | 00100                   | Lower 1/128 Blocks locked  | 0        | 31   |

|                 |                             |   |      |
|-----------------|-----------------------------|---|------|
| 00101           | Lower 1/64<br>Blocks locked | 0 | 31   |
| 00110           | Lower 1/32<br>Blocks locked | 0 | 63   |
| 00111           | Lower 1/16<br>Blocks locked | 0 | 127  |
| 01000           | Lower 1/8<br>Blocks locked  | 0 | 255  |
| 01001           | Lower 1/4<br>Blocks locked  | 0 | 511  |
| 01010           | Lower 1/2<br>Blocks locked  | 0 | 1023 |
| all others      | All Blocks locked           | 0 | 2047 |
| 11111 (default) |                             | 0 | 2047 |

|                 |                             |   |      |
|-----------------|-----------------------------|---|------|
| 00101           | Lower 1/64<br>Blocks locked | 0 | 63   |
| 00110           | Lower 1/32<br>Blocks locked | 0 | 127  |
| 00111           | Lower 1/16<br>Blocks locked | 0 | 255  |
| 01000           | Lower 1/8<br>Blocks locked  | 0 | 511  |
| 01001           | Lower 1/4<br>Blocks locked  | 0 | 1023 |
| 01010           | Lower 1/2<br>Blocks locked  | 0 | 2047 |
| all others      | All Blocks locked           | 0 | 4095 |
| 11111 (default) |                             | 0 | 4095 |

## 5.2 Permanent Block Protection (PBP) Overview

The device contains 16 protection parameter setting entries. Each entry enables protection from program and erase of a group of 4 contiguous blocks (64 blocks total) in the main array.

The device ships from the factory with no blocks protected by the PBP method.

Because this block protection is permanent, a power-on to power-off sequence does not affect the block status after the Permanent block protection command is issued.

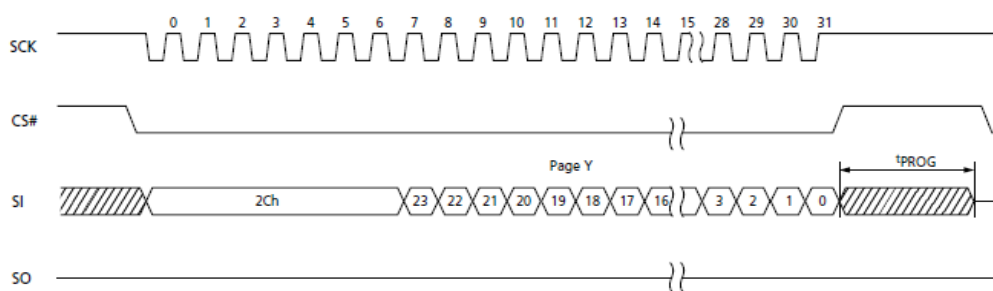
The PBP method is used to select a group of blocks in the main array to be protected from program and erase operation. Multiple groups of blocks can be protected at the same time. Once a group of blocks is protected, the group of blocks can no longer be unprotected.

Additional unprotected groups can still be protected using the PBP sequence. However, the user must not re-issue a PBP command with a group that has been previously protected.

The following PBP sequence is used:

- 06h (WRITE ENABLE)
  - 2Ch (PBP Command) followed by 24-bit address (X=0 and Y= block select: see table below)
  - After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P\_Fail bit is not set.
- If the host attempts to program data to a protected block, this operation will fail and the status register (with feature address C0h) reads the following values: P\_FAIL = 1 and WEL = 1. The timing diagram and address phase cycle of the PBP sequence is provided below:

**Figure 10. Timing Diagram and Address Phase Cycle of the PBP Sequence**



**Table 21 : PBPA[23:0] Address Cycle Map**

| PBPA[23:0] Address Cycle Map |       |                |       |       |       |       |       |       |                |
|------------------------------|-------|----------------|-------|-------|-------|-------|-------|-------|----------------|
| Bus Cycle                    | SI    | SI[7]<br>(MSB) | SI[6] | SI[5] | SI[4] | SI[3] | SI[2] | SI[1] | SI[0]<br>(LSB) |
| 1 <sup>st</sup>              | 23-16 | L              | L     | L     | L     | L     | L     | L     | L              |
| 2 <sup>nd</sup>              | 15-8  | L              | L     | L     | L     | Y[3]  | Y[2]  | Y[1]  | Y[0]           |
| 3 <sup>rd</sup>              | 7-0   | L              | L     | L     | L     | L     | L     | L     | L              |

The group of blocks being protected is determined by the value of Y (see Table 7) on the second address cycle

**Table 22 : Second Address Cycle protection Scheme Table**

| Y Value | Protection Group | Group Block addresses |
|---------|------------------|-----------------------|
| 0000    | 0                | 0,1,2,3               |
| 0001    | 1                | 4,5,6,7               |
| 0010    | 2                | 8,9,10,11             |
| 0011    | 3                | 12,13,14,15           |
| 0100    | 4                | 16,17,18,19           |
| 0101    | 5                | 20,21,22,23           |
| 0110    | 6                | 24,25,26,27           |
| 0111    | 7                | 28,29,30,31           |
| 1000    | 8                | 32,33,34,35           |
| 1001    | 9                | 36,37,38,39           |
| 1010    | 10               | 40,41,42,43           |
| 1011    | 11               | 44,45,46,47           |
| 1100    | 12               | 48,49,50,51           |
| 1101    | 13               | 52,53,54,55           |
| 1110    | 14               | 56,57,58,59           |
| 1111    | 15               | 60,61,62,63           |

### 5.3 Permanent Block protection lock down sequence

The Permanent Block Protection (PBP) lock down can be set through the SET feature. This operation is irreversible and once the permanent lock down protection has been issued, the current protection settings are permanent. All group of blocks protected by PBP are permanently protected from program and erase operations. The PBP operations can no longer be used to protect additional groups.

The following command sequence to lock down the Permanent Block Protection is as follow:

- Use SET FEATURES command (1Fh) with feature address B0h and Config[2:0] = 111b
- Use Write Enable command (06h)
- Program Execute command (10h) with block/page address (00)
- Use GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready
- Use SET FEATURES command (1Fh) with feature address B0h and data value with Config[2:0] = 000b to exit
- After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P\_Fail bit is not set

### 5.4 Block Protection Status Command

The Block Protection Status Read command (7Ah) is followed by 3 address cycles (see address mapping section), eight dummy cycles and one data cycle.

This register indicates whether a given block (addressed in the Block protection read address command field: BA[13:0]) is locked-down, locked or unlocked using the AVBP or PBP).

### 5.5 Block Lock Status Register

The Block Lock Status (BLS) register indicates whether a block is locked-down, locked or unlocked using the VBP or PBP protection methods.

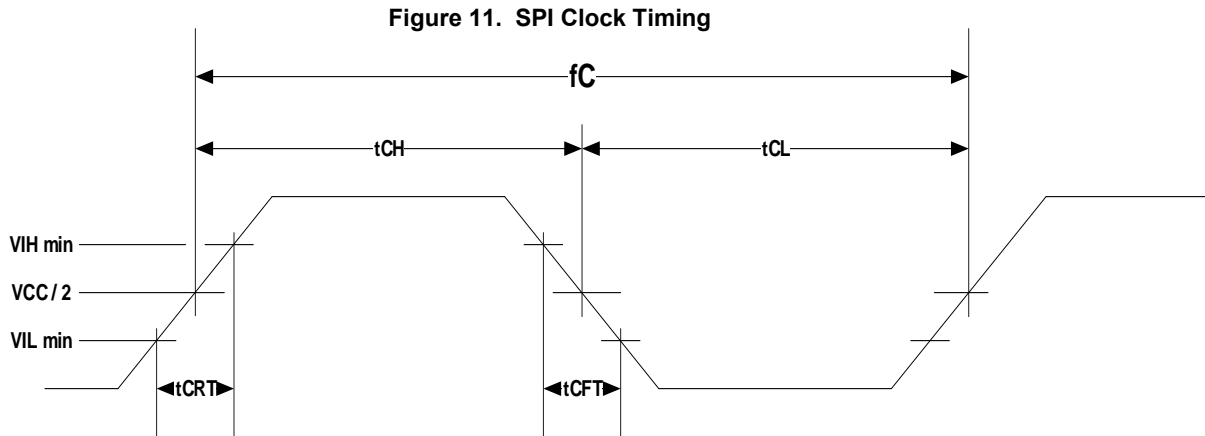
The following table provides the BLS register definition:

**Table 23** : Block Lock Status Register

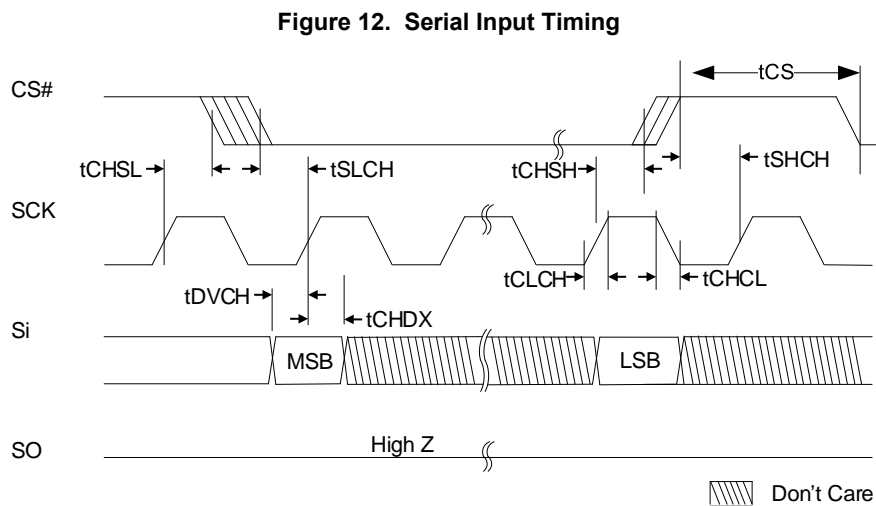
| Bits | Field Name             | Function                               | Default State | Description  |
|------|------------------------|--|---------------|--|
| 7    | RSVD                   | Reserved                               | 0             |  |
| 6    | RSVD                   | Reserved                               | 0             |  |
| 5    | RSVD                   | Reserved                               | 0             |  |
| 4    | RSVD                   | Reserved                               | 0             |  |
| 3    | PBP Lock/Unlock Status | Permanent Block Protection Lock Status | 1             | 0: The address selected block is locked by PBP<br>1: The address selected block is not locked by PBP |
| 2    | VBP Lock/Unlock Status | Volatile Block Protection Status       | 0             | 001: Block is locked down by AVBP<br>010: Block is locked by AVBP ( <b>Default</b> )                 |
| 1    |                        |  | 1             | 101: Block is unlocked, Device is locked-down by AVBP  |
| 0    |                        |  | 0             | 110: Block is unlocked, Device is not locked-down by AVBP (Register B0h BIT[5])                      |

## 6. Timing Diagrams

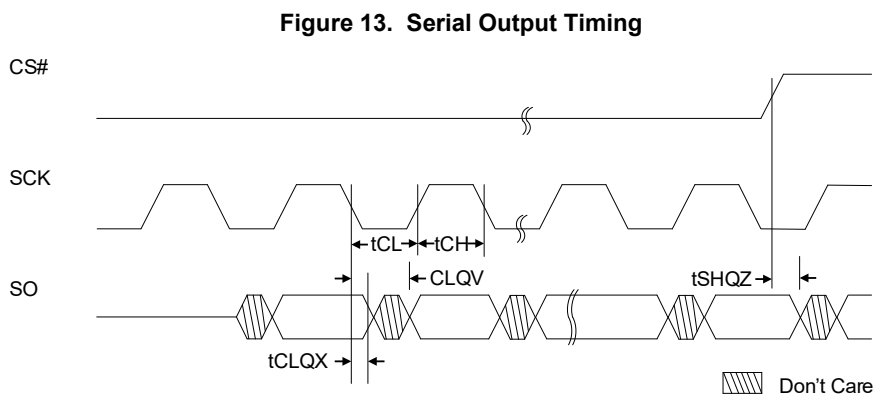
### 6.1 SPI Clock Timing



### 6.2 Serial Input Timing

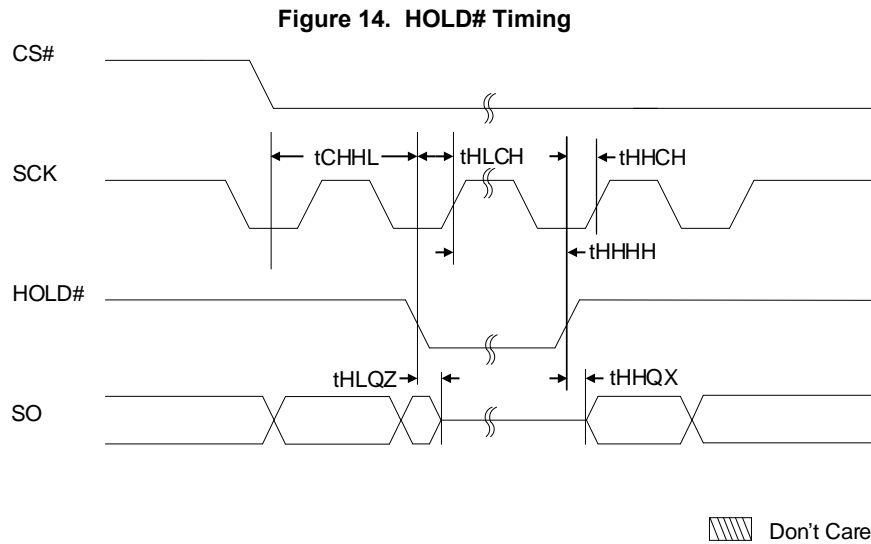


### 6.3 Serial Output Timing

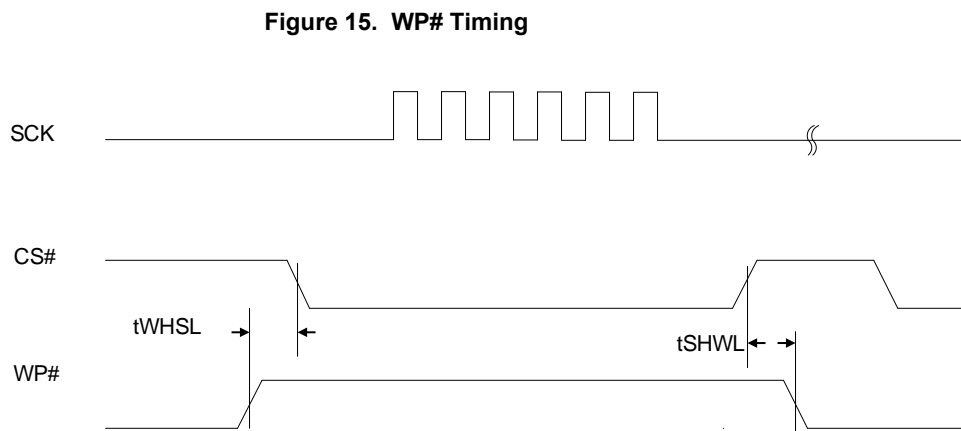




## 6.4 Hold# Timing



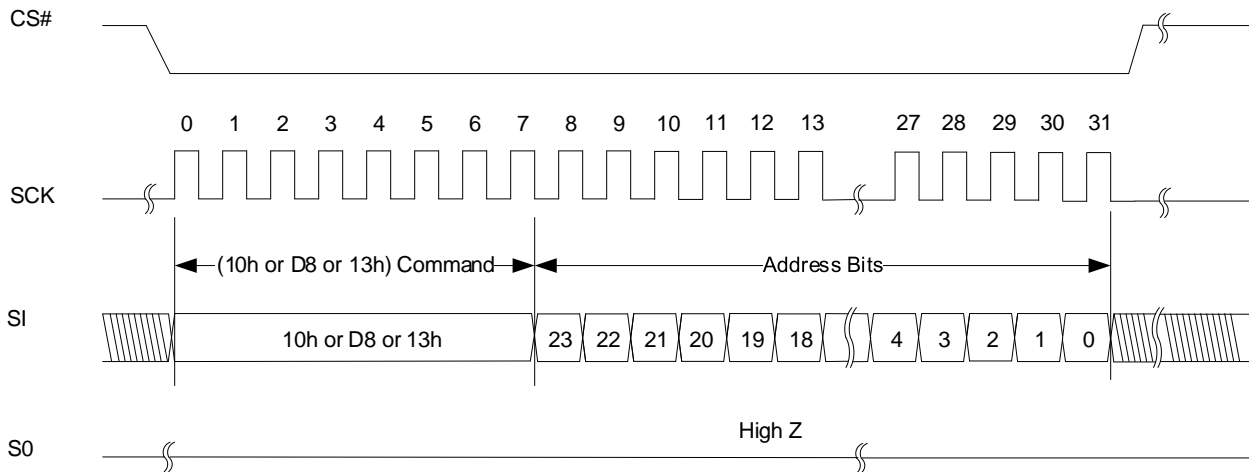
## 6.5 WP# Timing



## 6.6 Block Erase (D8h), Program Execute (10h), Page Read (13h) Timing Diagram

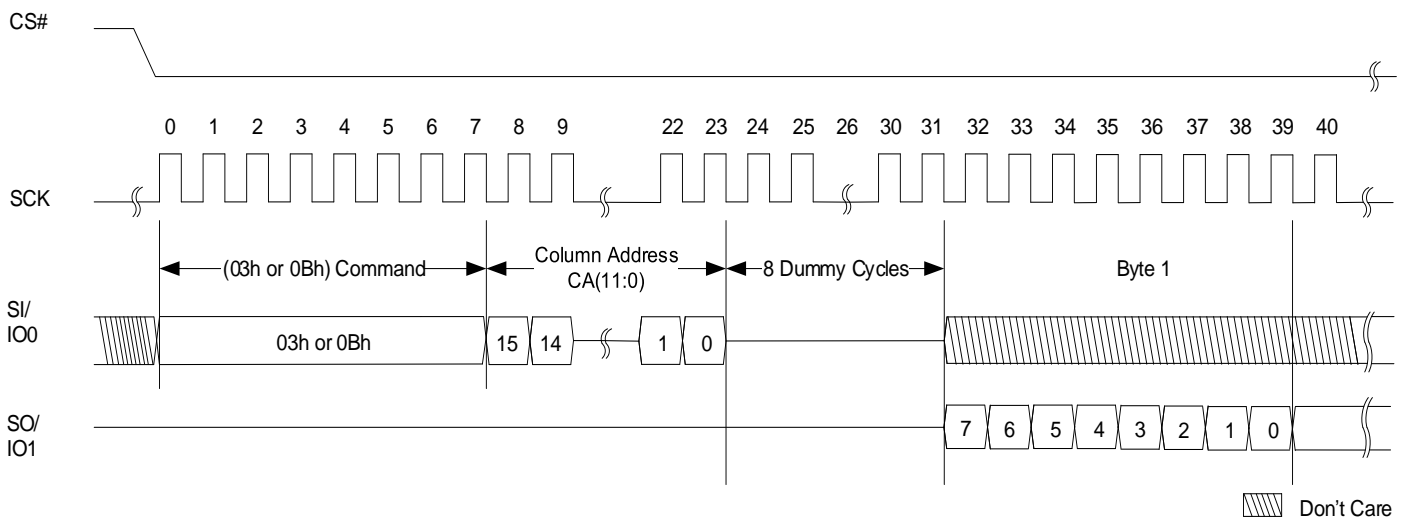
Timing diagrams Figure 16 covers Block Erase, Program Execute and Page Read. The address field consists of 3 bytes for block address.

**Figure 16. Block Erase, Program Execute, Page Read Timing**



## 6.7 Read Buffer 1X (03h or 0Bh) Timing Diagram

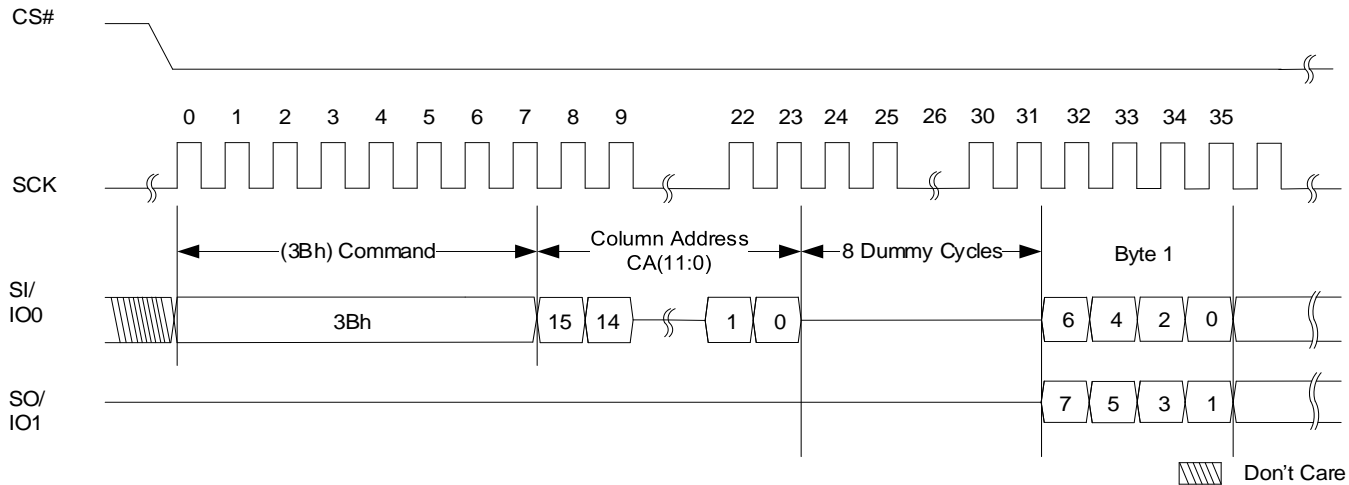
**Figure 17: Read Buffer (03h or 0Bh) Timing**



## 6.8 Dual Read Output Buffer 2X (3Bh) Timing Diagram

For the Dual I/O Read command, data bits are output through two pins: IO0, and IO1. there is a latency required after the mode bits before data begins shifting out of IO0-IO1. This latency period (i.e., dummy cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0-IO1 are "don't care" while the master stops driving the IO and the slave begins driving the IO. Following the latency period, the memory contents at the address given, is shifted out two bits at a time through IO0-IO1.

Figure 18. Dual Read Output Buffer 2x (3Bh) Timing

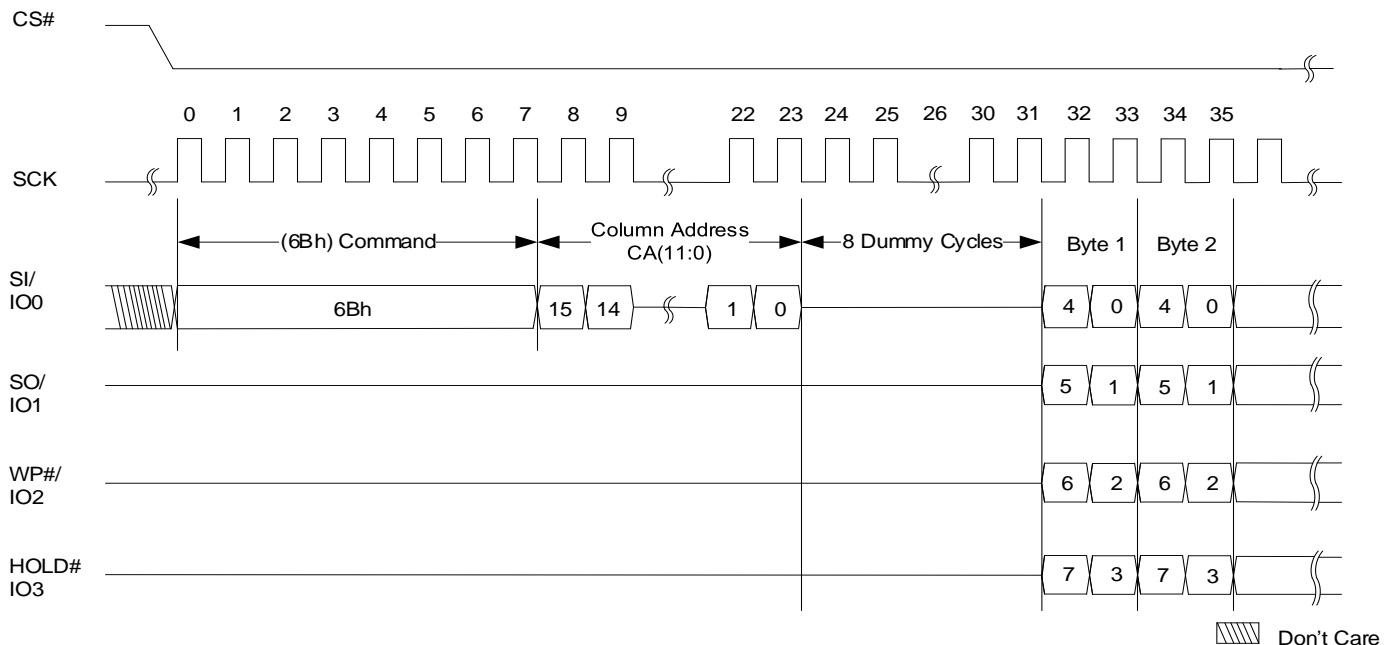


## 6.9 Quad Read Output Buffer 4X(6Bh)Timing Diagram

For the Quad I/O Read output command, data bits are input and output through four pins: IO0, IO1, IO2, and IO3. The quad data read command improves throughput per serial SCK clock.

For the Quad I/O Read command, there is a latency required after the mode bits before data begins shifting out of IO0-IO3. This latency period (i.e., dummy cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0-IO3 are "don't care". Following the latency period, the memory contents at the address given, is shifted out four bits at a time through IO0-IO3.

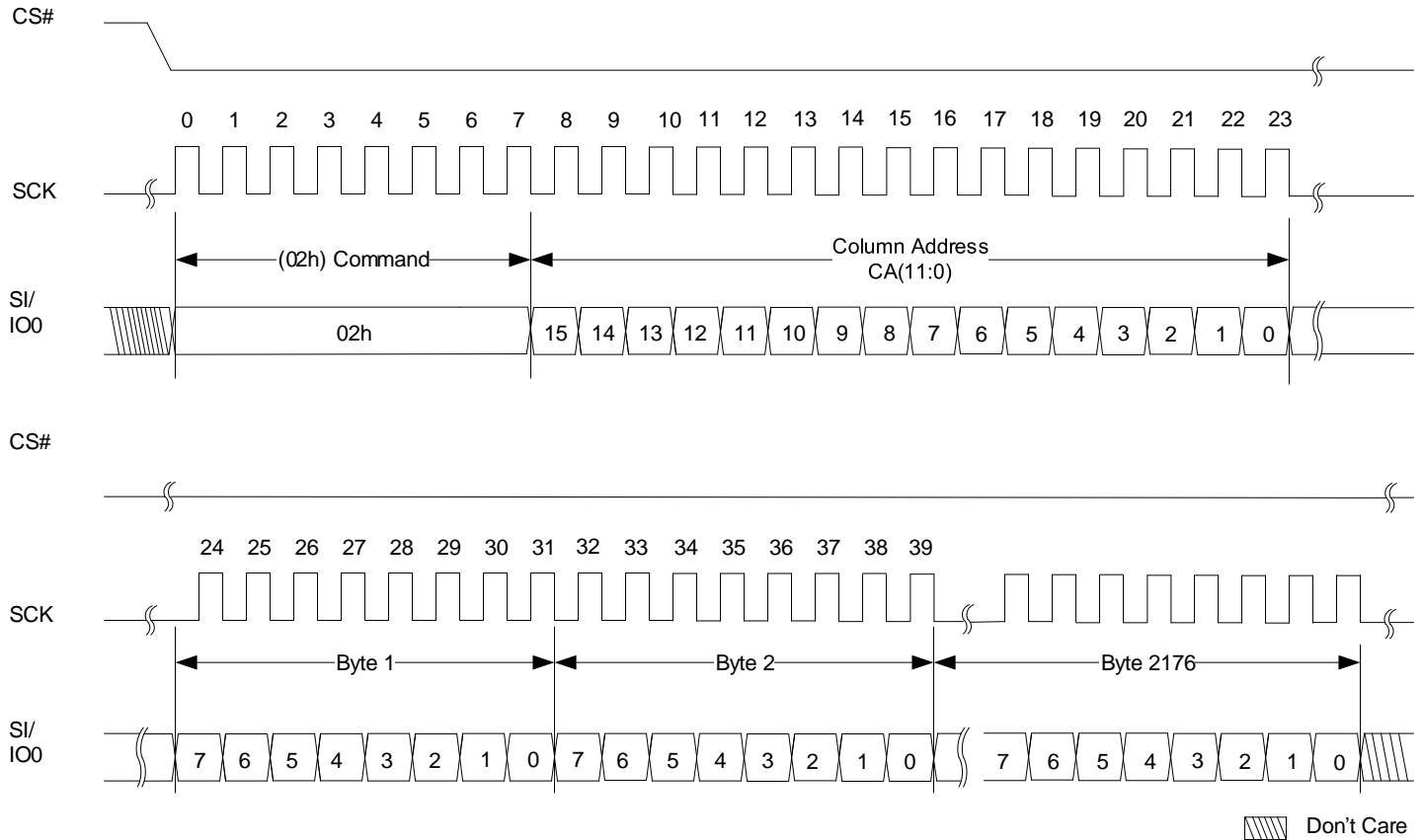
Figure 19. Quad Read Output Buffer 4X (6Bh) Timing



## 6.10 Program Load 1X(02h) and Program Load Random Data 1X(84h) Buffer Timing Diagram

Figure 20 shows the timing diagram for Program Load 1X (command 02h).

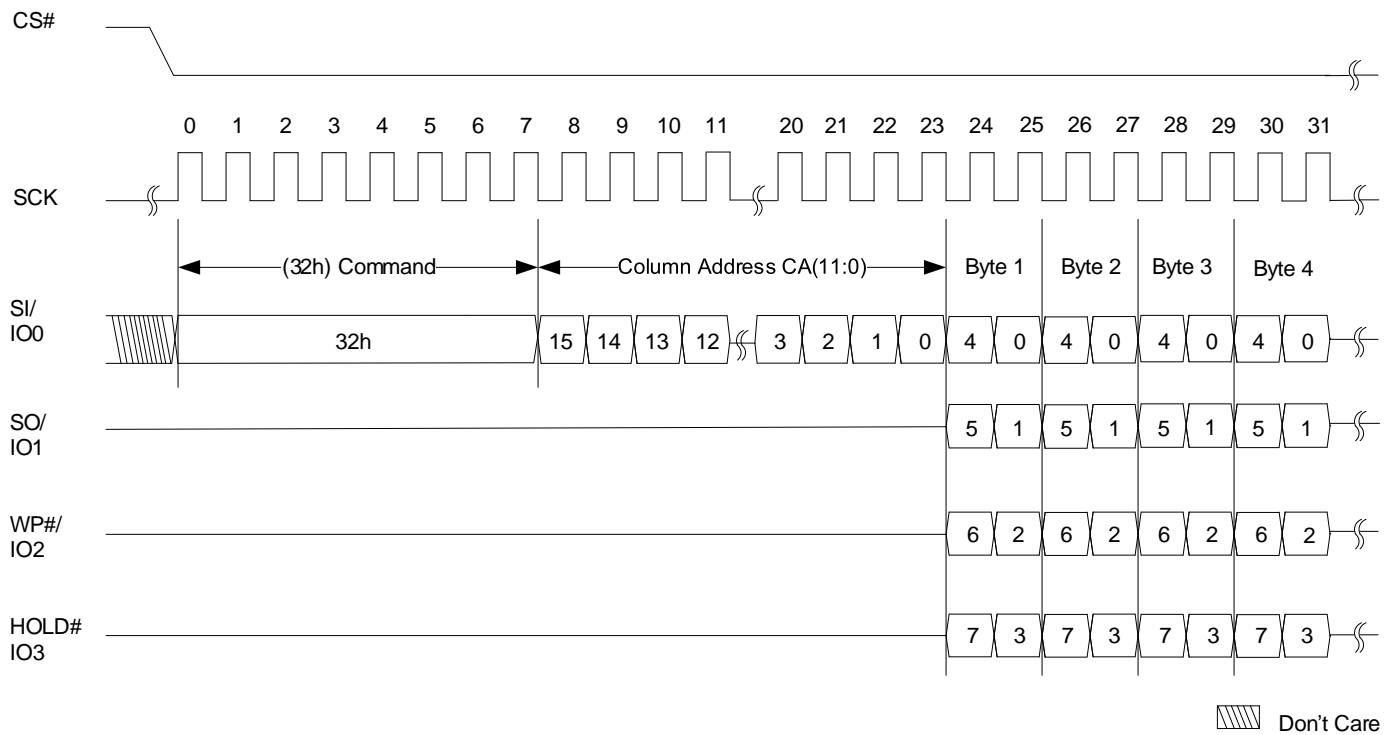
**Figure 20. Program Load 1X (02h) and Program Load Random Data 1X Buffer Timing**



## 6.11 Quad Program Data Load 4X(32h) and Quad Program Load Random Data 1X(34h) Buffer

The Quad load program command allows bytes to be programmed in the memory using four signals: IO0- IO3 for improved performance.

**Figure 21. Quad Program Data Load 4X (32h) and Quad Program Load Random Data 1X (34h) Buffer Timing**



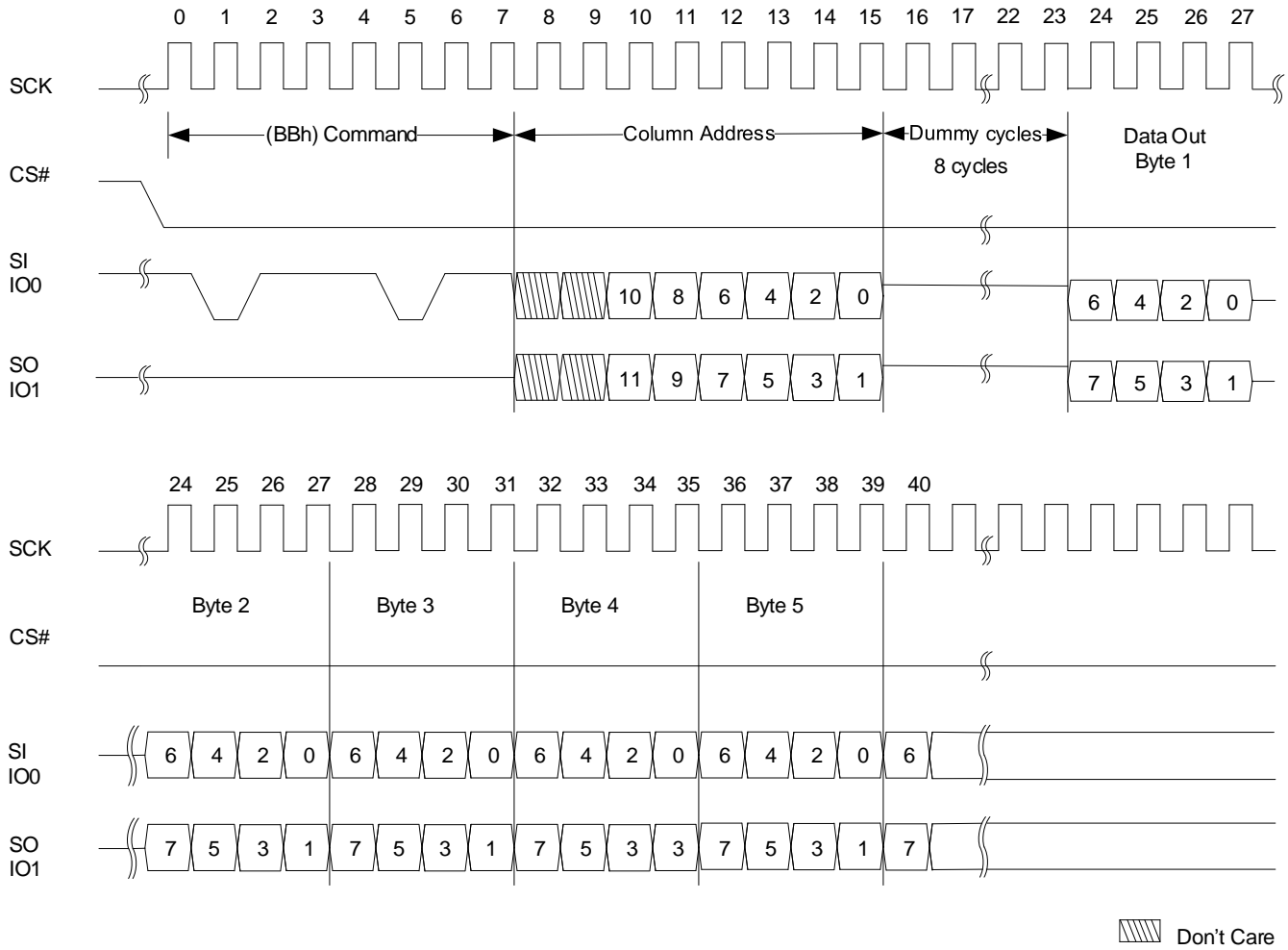
## 6.12 Small Data Input Guidelines

Small data input is allowed within an NOP provided that it meets the following conditions:

- Data size must be a minimum of 4 bytes or greater within single NOP.
- Data input column address must start from xxxx0h, xxx4h, xxx8h, and xxxCh.

### 6.13 Fast Read Dual IO 2X(BBh)

Figure 22. Fast Read Dual IO 2X(BBh) Timing Diagram

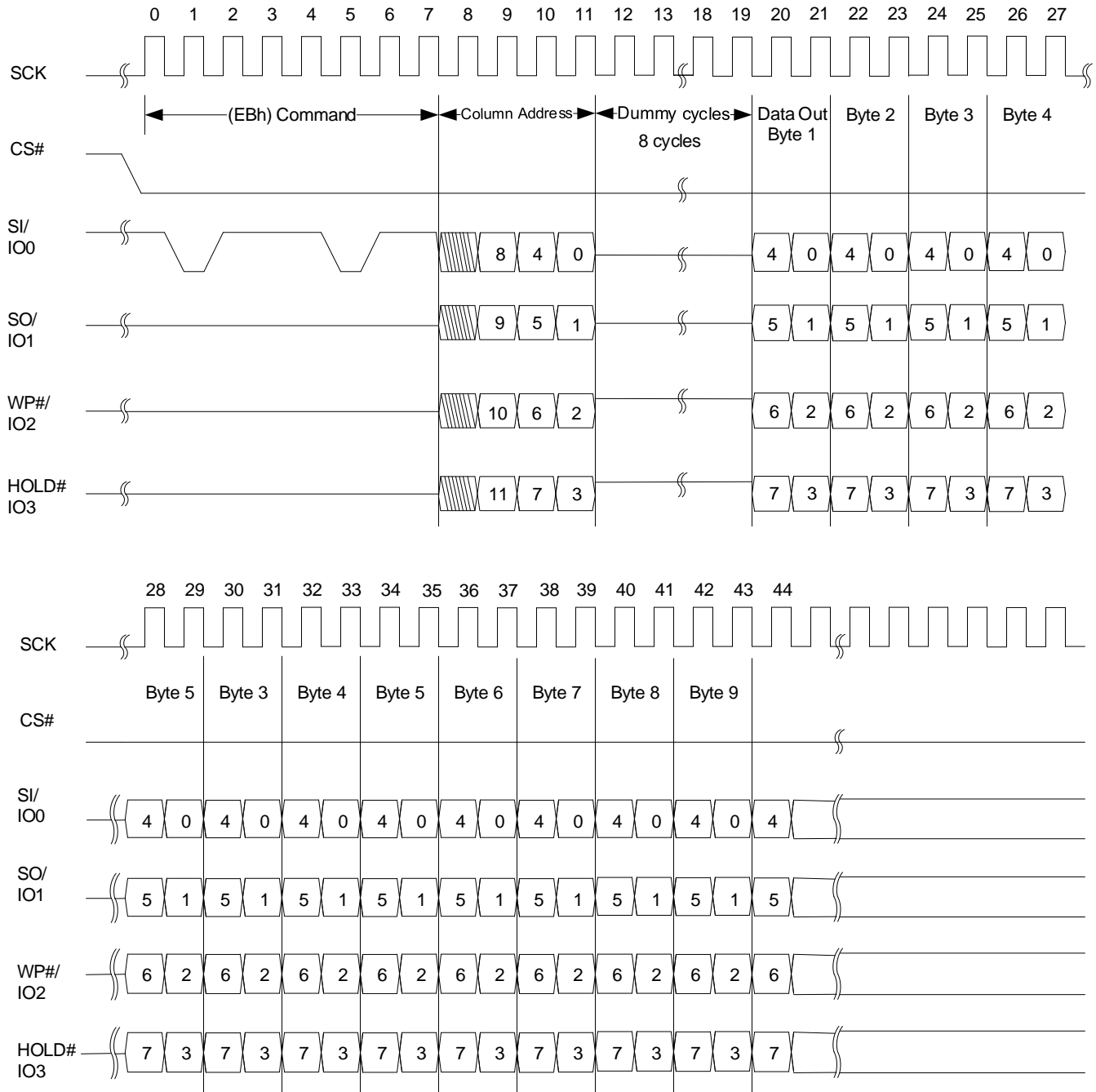


**Note:**

1. The number of dummy cycles is 8 cycles .

## 6.14 Fast Read Quad IO 4X(EBh)

Figure 23. Fast Read Quad IO 4X(EBh) Timing Diagram



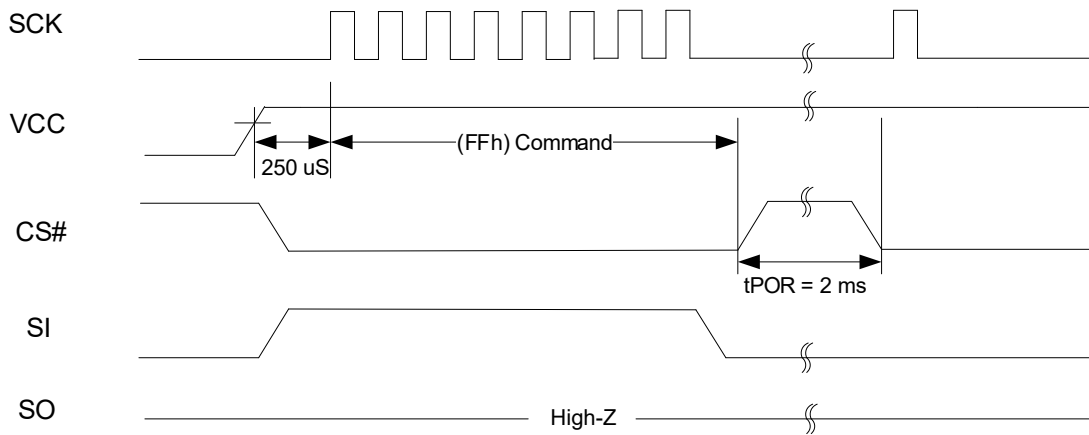
 Don't Care

**Note:**

1. The number of dummy cycles is 8 cycles .

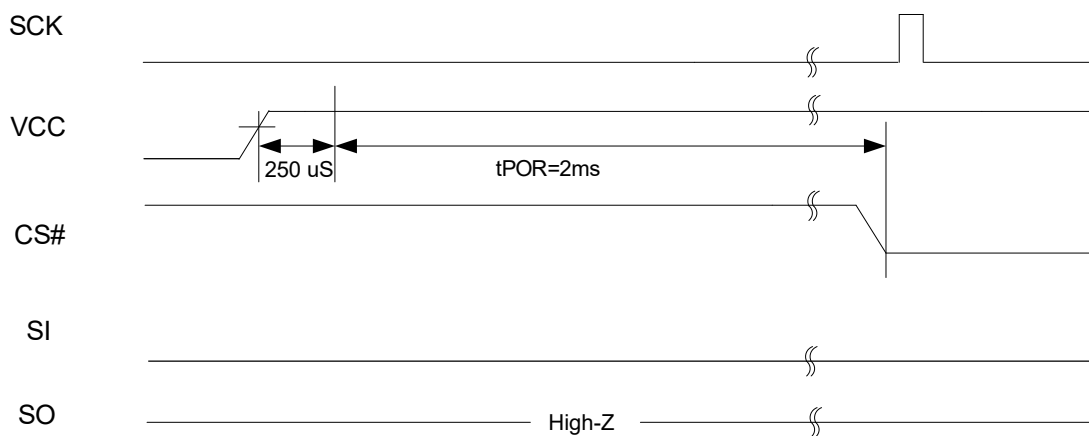
## 6.15 Power Up Timing

Figure 24. Power Up Timing Diagram (with FFh)



Note: Reset (FFh) command is required after power-on as a first command for S35ML02/04G3 and optional for S35ML01G3 .

Figure 25. Power up Timing (without FFh)



Note: Call factory for S35ML02/04G3 devices without FFh power-on option .

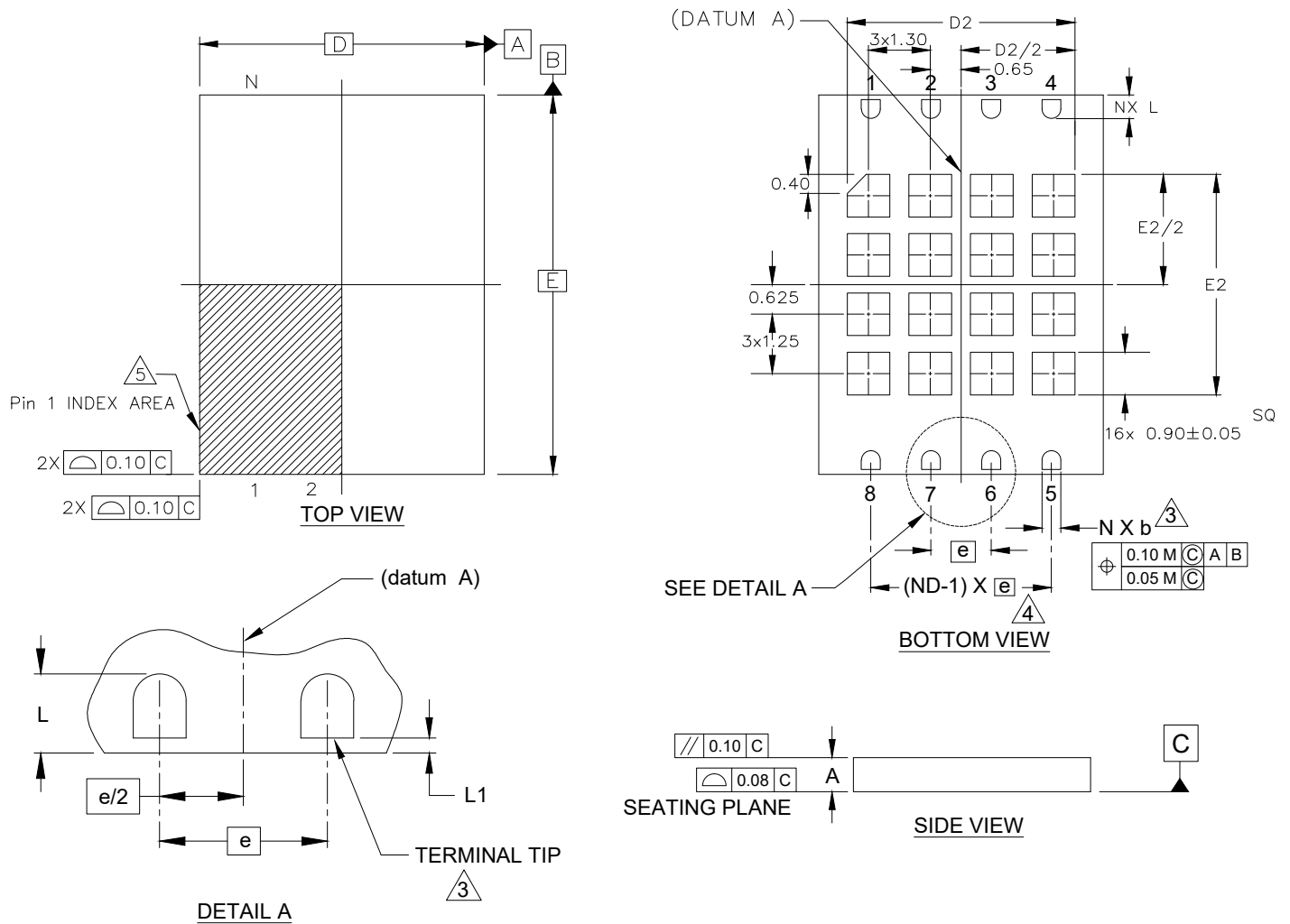


## 7.0 : Physical Interface

### 7.1 : Physical Diagram

#### 7.1.1 : 8-pin LGA Package (6 x 8 mm body width)

Figure 26. 8-pin LGA Package (6 x 8 mm)



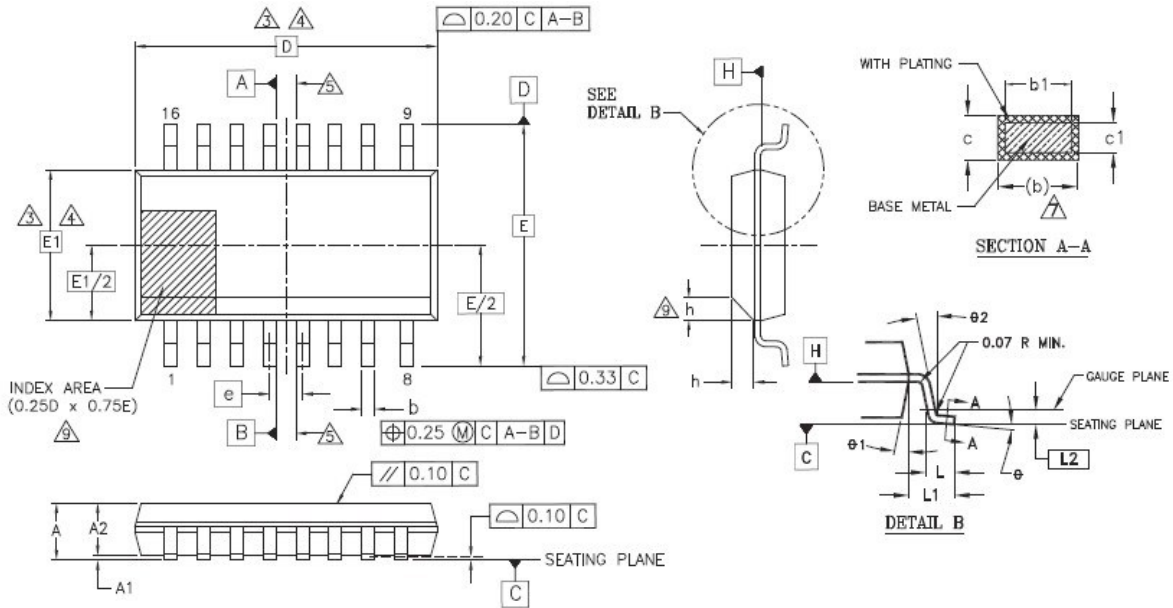
| SYMBOL | DIMENSIONS |          |      |
|--------|------------|----------|------|
|        | MIN.       | NOM.     | MAX. |
| e      |            | 1.27 BSC |      |
| N      |            | 8        |      |
| ND     |            | 4        |      |
| L      | 0.45       | 0.50     | 0.55 |
| b      | 0.35       | 0.40     | 0.45 |
| D2     | 4.70       | 4.80     | 4.90 |
| E2     | 4.55       | 4.65     | 4.75 |
| D      |            | 6.00 BSC |      |
| E      |            | 8.00 BSC |      |
| A      | 0.70       | 0.75     | 0.80 |
| L1     | 0.00       | -        | 0.15 |

**NOTES:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF LANDS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM LAND WIDTH IN A PLANE PARALLEL TO DATUM C.
4. ND REFERS TO THE NUMBER OF LANDS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.

## 7.1.2 : 16-pin SOIC Package (300 mils body width)

Figure 27. 16-pin SOIC Package (300 mil)



| PACKAGE | SO3 016 (Inches) |       | SO3 016 (mm) |      |
|---------|------------------|-------|--------------|------|
| JEDEC   | MS-013(D)AA      |       | MS-013(D)AA  |      |
| SYMBOL  | MIN              | MAX   | MIN          | MAX  |
| A       | 0.093            | 0.104 | 2.35         | 2.65 |
| A1      | 0.004            | 0.012 | 0.10         | 0.30 |
| A2      | 0.081            | 0.104 | 2.05         | 2.55 |
| b       | 0.012            | 0.020 | 0.31         | 0.51 |
| b1      | 0.011            | 0.019 | 0.27         | 0.48 |
| c       | 0.008            | 0.013 | 0.20         | 0.33 |
| c1      | 0.008            | 0.012 | 0.20         | 0.30 |
| D       | 0.406 BSC        |       | 10.30 BSC    |      |
| E       | 0.406 BSC        |       | 10.30 BSC    |      |
| E1      | 0.295 BSC        |       | 7.50 BSC     |      |
| e       | .050 BSC         |       | 1.27 BSC     |      |
| L       | 0.016            | 0.050 | 0.40         | 1.27 |
| L1      | .055 REF         |       | 1.40 REF     |      |
| L2      | .010 BSC         |       | 0.25 BSC     |      |
| N       | 16               |       | 16           |      |
| h       | 0.10             | 0.30  | 0.25         | 0.75 |
| theta   | 0°               | 8°    | 0°           | 8°   |
| theta1  | 5°               | 15°   | 5°           | 15°  |
| theta2  | 0°               |       | 0°           |      |

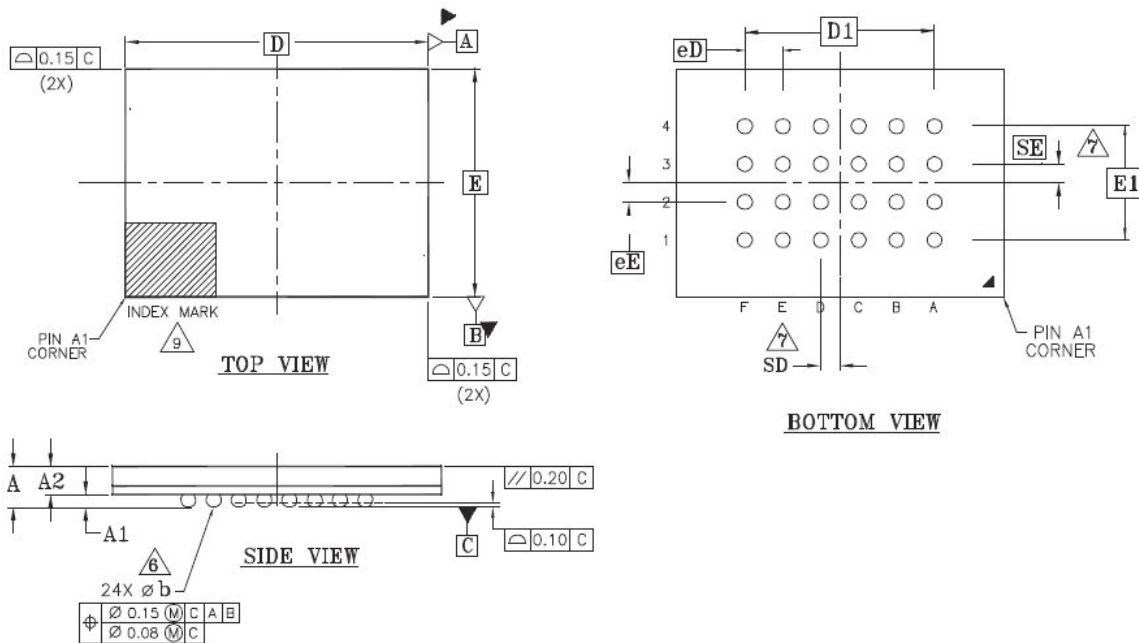
NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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### 7.1.4 : 24-pin BGA, 6 x 4 Ball Array (8 x 6 mm body width)

Figure 28. 24-pin BGA Ball Array (6 x 4 mm)



| PACKAGE | FAC024                        |      |      | NOTE                     |
|---------|-------------------------------|------|------|--------------------------|
| JEDEC   | N/A                           |      |      |                          |
| D x E   | 8.00 mm x 6.00 mm NOM PACKAGE |      |      |                          |
| SYMBOL  | MIN                           | NOM  | MAX  |                          |
| A       | ---                           | ---  | 1.20 | PROFILE                  |
| A1      | 0.25                          | ---  | ---  | BALL HEIGHT              |
| A2      | 0.70                          | ---  | 0.90 | BODY THICKNESS           |
| D       | 8.00 BSC.                     |      |      | BODY SIZE                |
| E       | 6.00 BSC.                     |      |      | BODY SIZE                |
| D1      | 5.00 BSC.                     |      |      | MATRIX FOOTPRINT         |
| E1      | 3.00 BSC.                     |      |      | MATRIX FOOTPRINT         |
| MD      | 6                             |      |      | MATRIX SIZE D DIRECTION  |
| ME      | 4                             |      |      | MATRIX SIZE E DIRECTION  |
| N       | 24                            |      |      | BALL COUNT               |
| øb      | 0.35                          | 0.40 | 0.45 | BALL DIAMETER            |
| e       | 1.00 BSC.                     |      |      | BALL PITCHL              |
| SD/ SE  | 0.5/0.5                       |      |      | SOLDER BALL PLACEMENT    |
|         |                               |      |      | DEPOPULATED SOLDER BALLS |
|         | J                             |      |      | PACKAGE OUTLINE TYPE     |

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- e REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- 6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.  
DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
- 7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- 9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- 10 OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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## 8. Error Management

### 8.1 System Bad Block Replacement

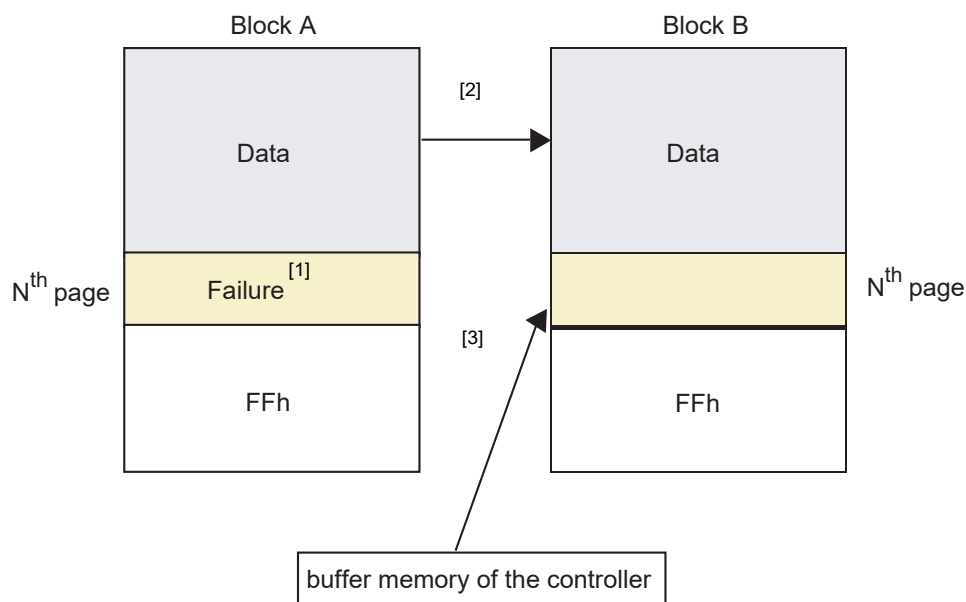
Over the lifetime of the device, additional Bad Blocks may develop. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional Bad Blocks can be identified whenever a program or erase operation reports “Fail” in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 24 and Figure 29 for the recommended procedure to follow if an error occurs during an operation.

**Table 24. Block Failure**

| Operation | Recommended Procedure      |
|-----------|----------------------------|
| Erase     | Block Replacement          |
| Program   | Block Replacement          |
| Read      | Check Read Status Register |

**Figure 29. Bad Block Replacement**



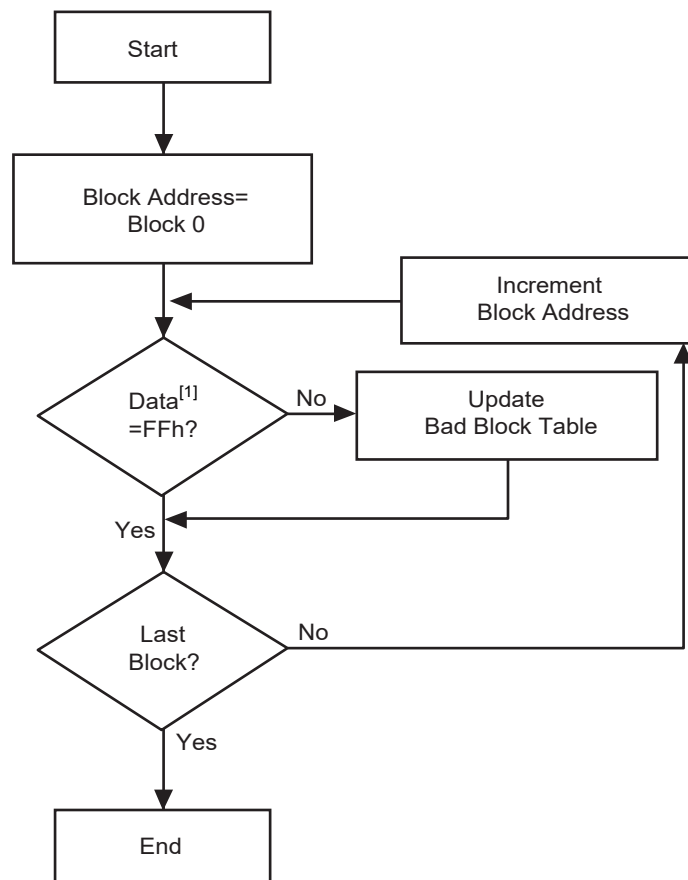
**Notes**

1. An error occurs on the Nth page of Block A During a program operation.
2. Data in Block A is copied to the same location in Block B, which is a valid block.
3. The Nth page of block A, which is in controller buffer memory is copied into the Nth page of Block B.
4. Bad block table should be updated to prevent from erasing or programming Block A.

## 8.2 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written before shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block. The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure 30. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. Blocks 0-7 are guaranteed good at the time of shipment.

Figure 30. Bad Block Management Flowchart<sup>[1]</sup>

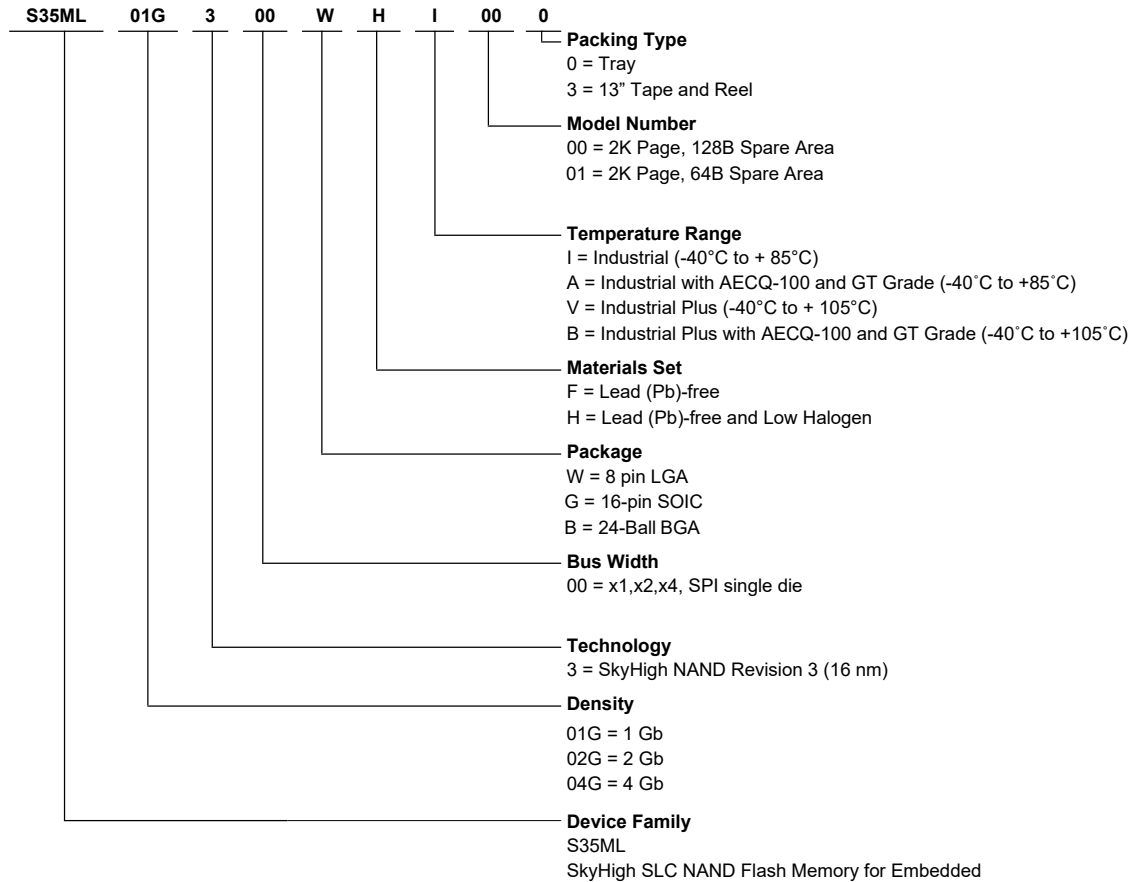


**Note**

1. Check for FFh at the 1st byte in the spare area of the 1st, 2nd, and last pages.

## 9. Ordering Information

The ordering part number is formed by a valid combination of the following:



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Device Family | Density | Technology | Bus Width | Package Type | Temperature Range | Additional Ordering Options | Packing Type | Package Description |
|---------------|---------|------------|-----------|--------------|-------------------|-----------------------------|--------------|---------------------|
| S35ML         | 01G     | 3          | 00        | WH           | I , V             | 01                          | 0, 3         | LGA <sup>[1]</sup>  |
| S35ML         | 02G/04G | 3          | 00        | WH           | I , V             | 00                          | 0, 3         | LGA                 |

**Note**

1. 64 bytes is the default value for the spare area. Contact sales for the 128 Bytes option.