

2 Gbit (256 MB) GL-T MIRRORBIT™ Flash

Parallel, 3.0 V

General description

The S70GL02GS 2-Gb MIRRORBIT™ flash memory device is fabricated on 65-nm MIRRORBIT™ process technology. This device offers a fast page access time of 25 ns with a corresponding random access time of 110 ns. It features a write buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard single byte/word programming algorithms. This makes the device an ideal product for today's embedded applications that require higher density, better performance and lower power consumption.

This document contains information for the S70GL02GS device, which is a dual die stack of two S29GL01GS die. For detailed specifications, please refer to the discrete die datasheet.

| Document | Document number |
|---------------------|-----------------|
| S29GL01GS datasheet | 001-98285 |

Distinctive characteristics

- CMOS 3.0 V core with Versatile I/O™
- Two 1024 Megabit (S29GL01GS) in a single 64-ball Fortified-BGA package (see [S29GL01GS datasheet](#) for full specifications)
- 65-nm MIRRORBIT™ process technology
- Single supply (V_{CC}) for read / program / erase (2.7 V to 3.6 V)
- Versatile I/O feature
 - Wide I/O voltage (V_{IO}): 1.65 V to V_{CC}
- ×16 data bus
- 16-word/32-byte page read buffer
- 512-byte programming buffer
 - Programming in page multiples, up to a maximum of 512 bytes
- Sector erase
 - Uniform 128-KB sectors
 - S70GL02GS: two thousand forty-eight sectors
- Suspend and Resume commands for Program and Erase operations
- Status Register, data polling, and Ready/Busy pin methods to determine device status
- Advanced sector protection (ASP)
 - Volatile and non-volatile protection methods for each sector
- Separate 1024-byte one time program (OTP) array with two lockable regions
 - Available in each device Support for common flash interface (CFI)
- WP# input
 - Protects first or last sector, or first and last sectors of each device, regardless of sector protection settings

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Performance characteristics

- Temperature range:
 - Industrial temperature range (-40°C to +85°C)
 - Automotive AEC-Q100 grade 3 (-40°C to +85°C)
 - Automotive AEC-Q100 grade 2 (-40°C to +105°C)
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Packaging options
 - 64-ball LSH Fortified BGA, 13 mm × 11 mm

Performance characteristics

Maximum read access times (ns) ^[1]

| Parameter | 2 Gb | |
|----------------------------------|------|-----|
| Random access time (t_{ACC}) | 110 | 120 |
| Page access time (t_{PACC}) | 20 | 30 |
| CE# access time (t_{CE}) | 110 | 120 |
| OE# access time (t_{OE}) | 25 | 35 |

Typical program and erase rates

| Operation | Rate |
|--------------------------------|----------|
| Buffer Programming (512 bytes) | 1.5 MBps |
| Sector Erase (128 kbytes) | 477 KBps |

Maximum current consumption

| Operation | Current |
|-----------------------------|-------------|
| Active read at 5 MHz, 30 pF | 60 mA |
| Program | 100 mA |
| Erase | 100 mA |
| Standby | 200 μ A |

Notes

1. Access times are dependent on V_{IO} operating ranges. See [“Ordering information”](#) on page 21 for further details.
2. Contact Infineon sales representative for availability.

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1 Input/output description and logic symbol

Table 1 identifies the input and output package connections provided on the device.

Table 1 Input/output description

| Symbol | Type | Description |
|-----------------|------------|---|
| A26–A0 | Input | Address lines for GL02GS. |
| DQ15–DQ0 | I/O | Data input/output. |
| CE# | Input | Chip Enable. |
| OE# | Input | Output Enable. |
| WE# | Input | Write Enable. |
| V _{CC} | Supply | Device power supply. |
| V _{IO} | Supply | Versatile IO input. |
| V _{SS} | Supply | Ground. |
| RY/BY# | Output | Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V _{IL} , the device is actively erasing or programming. At High Z, the device is in ready. |
| RESET# | Input | Hardware Reset. LOW = device resets and returns to reading array data. |
| WP# | Input | Write Protect/Acceleration Input. At V _{IL} , disables program and erase functions in the outermost sectors. At V _{HH} , accelerates programming; automatically places device in unlock bypass mode. Should be at V _{IH} for all other conditions. |
| NC | No Connect | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a printed circuit board (PCB). |
| DNU | Reserved | Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V _{IL} . The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V _{SS} . Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections. |
| RFU | No Connect | Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices. |

2 Block diagrams

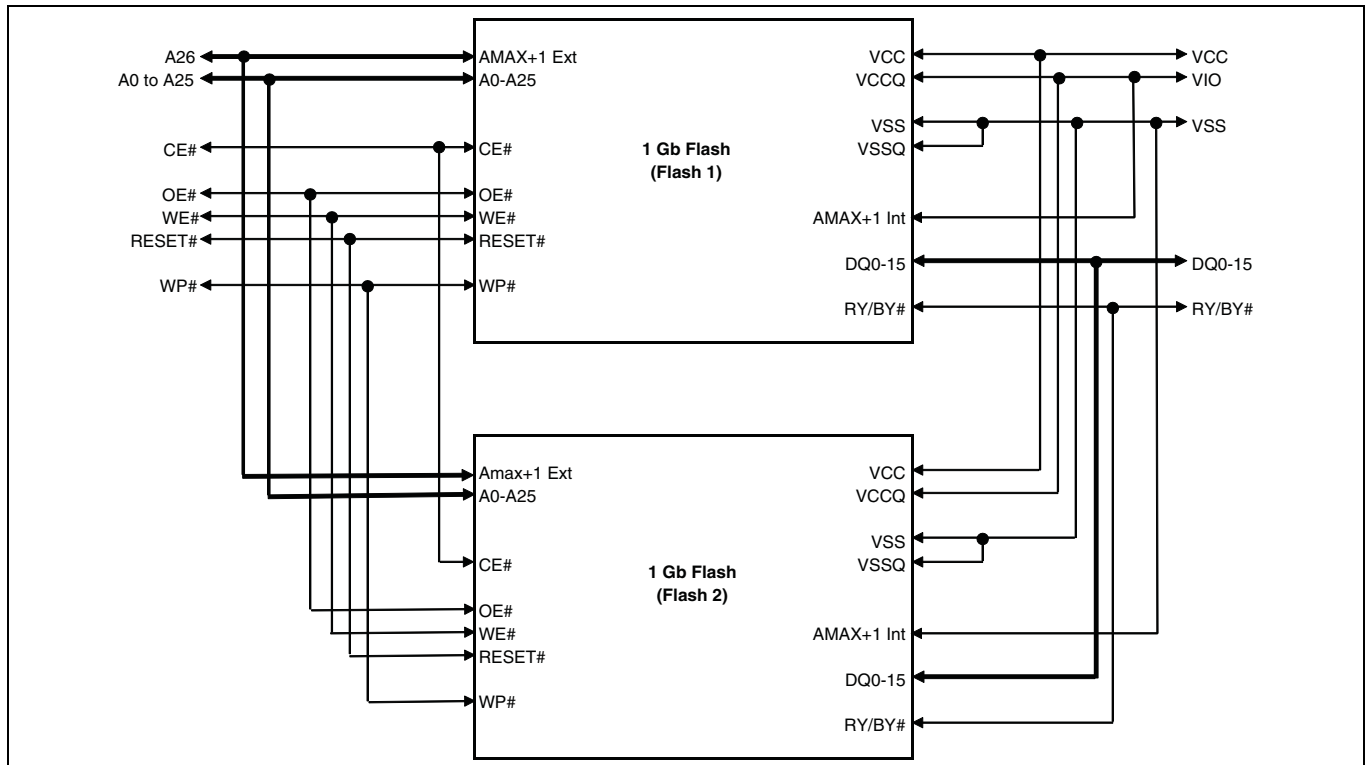


Figure 1 2 x GL01GS (Highest and lowest address sectors protected) block diagram

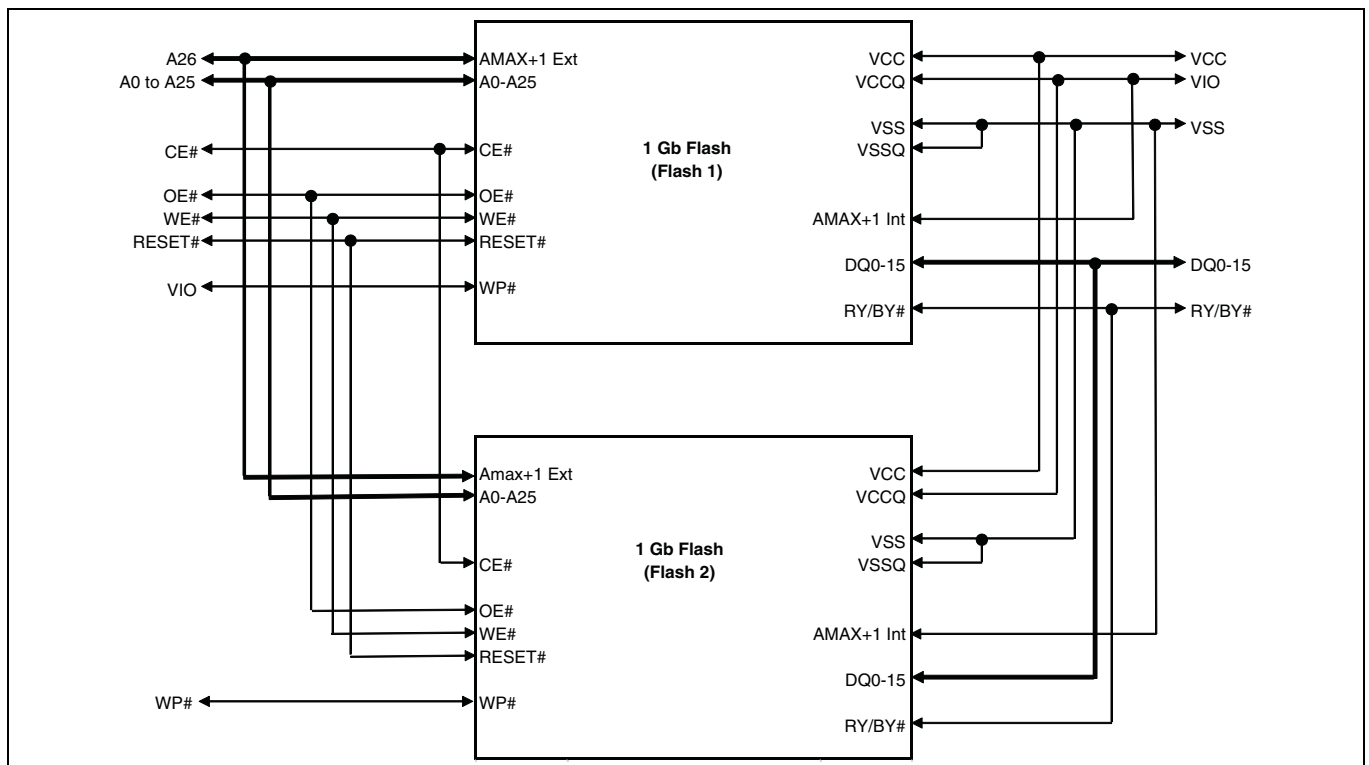


Figure 2 2 x GL01GS (Lowest address sector protected) block diagram

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Block diagrams

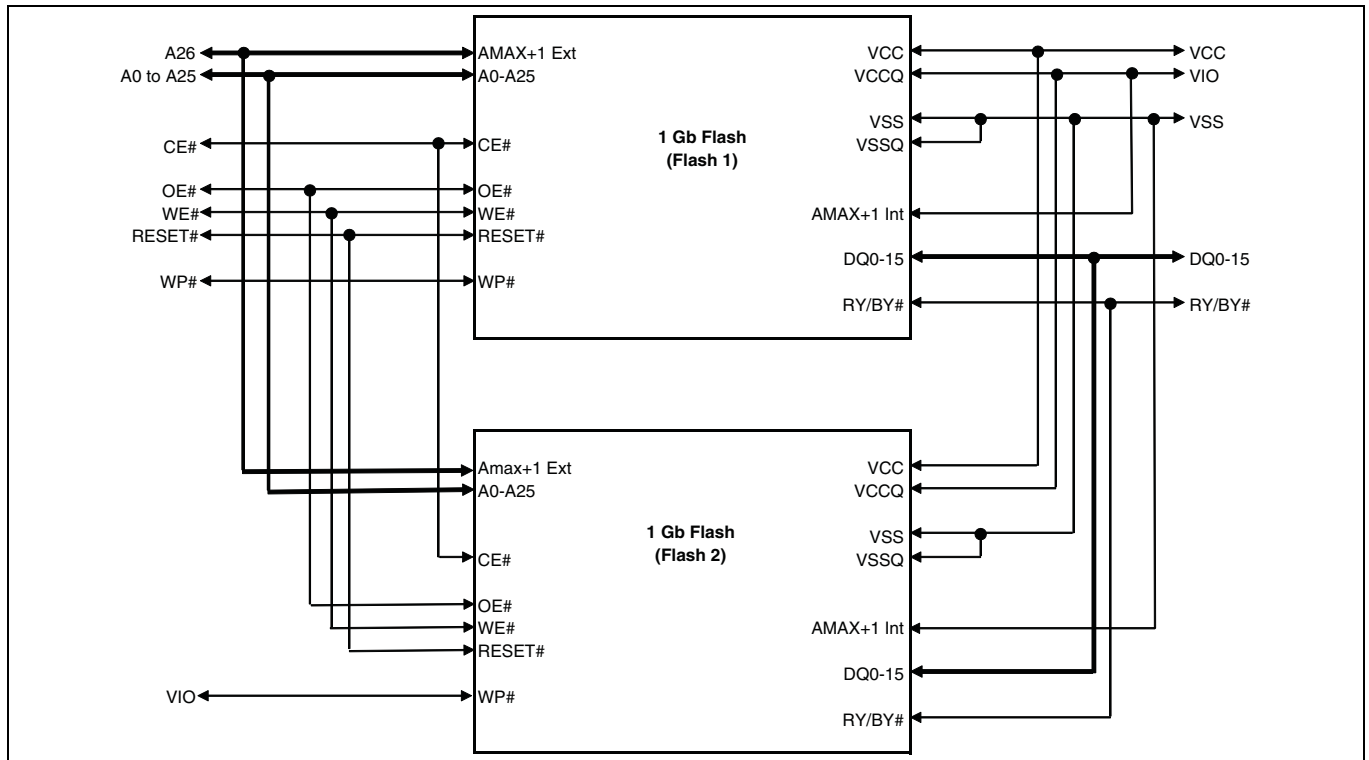


Figure 3 2 x GL01GS (Highest address sector protected) block diagram

3 Connection diagrams

3.1 Special handling instructions for BGA package

Special handling is required for flash memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

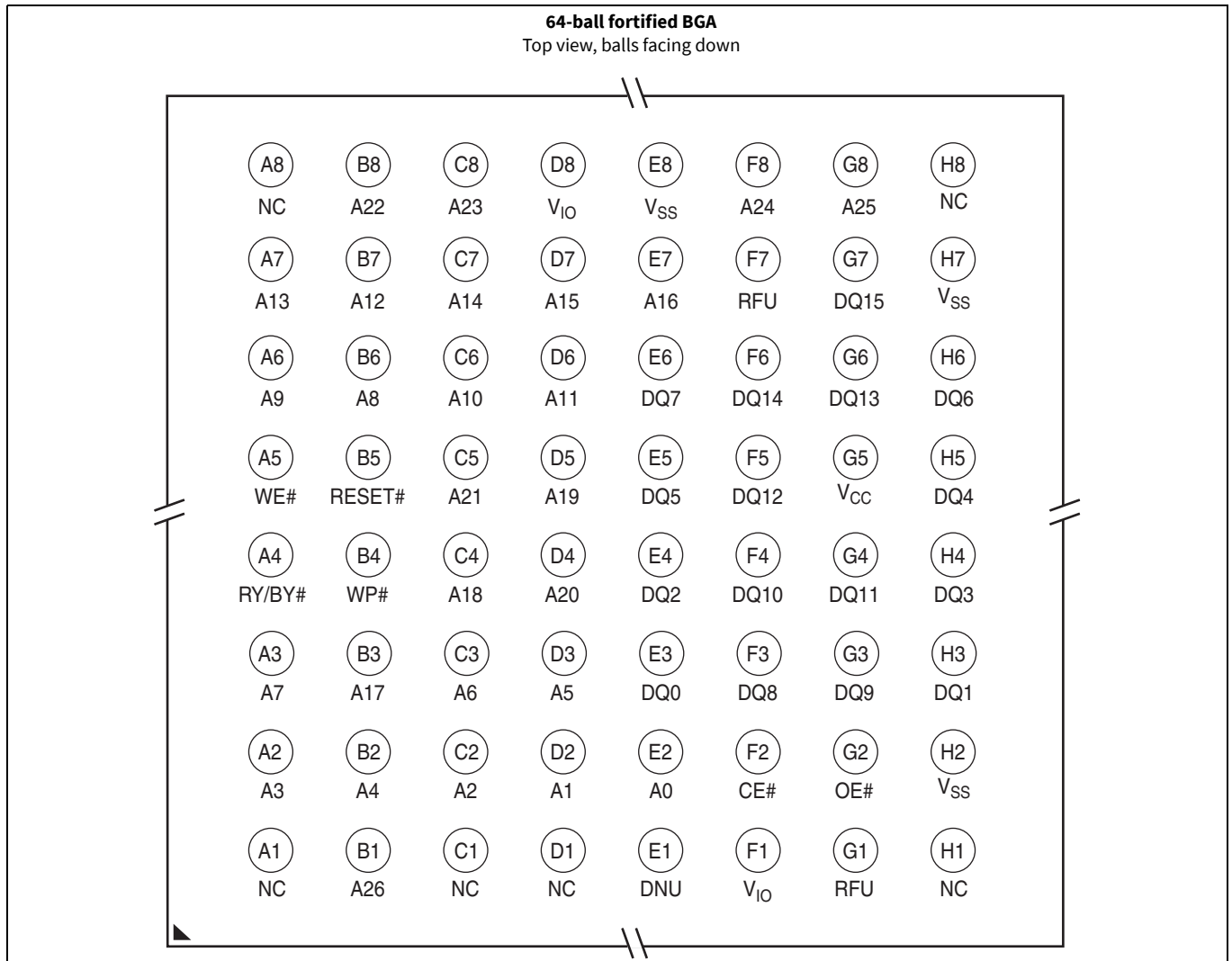


Figure 4 64-ball fortified ball grid array

Notes

- Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
- Balls F7 and G1, Reserved for Future Use (RFU).
- Balls A1, A8, C1, D1, H1, and H8, No Connect (NC).

4 Memory map

The S70GL02GS consist of uniform 64 Kword (128-KB) sectors organized as shown in [Table 2](#).

Table 2 S70GL02GS sector and memory address map

| Uniform sector size | Sector count | Sector range | Address range (16-bit) | Notes |
|---------------------|--------------|--------------|------------------------|-------------------------|
| 64 Kword/128 KB | 2048 | SA00 | 0000000h-000FFFFh | Sector starting address |
| | | : | : | |
| | | SA2047 | 7FF0000H-7FFFFFFh | Sector ending address |

Note

6. This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001–SA2046) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the pattern xxx0000h–xxxFFFFh.

5 Second die access

The S70GL02GS device is a dual die stack comprising two S29GL01GS dies connected in parallel, but with only one chip select (CS#) signal. This means that each die receives commands in parallel. The low-address die accepts commands with A26 = 0, while the high-address die accepts commands with A26 = 1. So, it is necessary to set the address bit A26 to '1' while sending commands to access the second die of S70GL02GS. You can manage this by adding the base address for each die to each address argument for each command; the base address for first die is 0x0 and for the second die is 0x4000000. The following table provides an example.

Table 3 Second die access example

| | Command sequence to erase first sector in die 1 | Command sequence to erase first sector in die 2 |
|---------------------------------------|--|--|
| 1st unlock cycle | Address 0x555 / Data 0xAA | Address 0x4000555 / Data 0xAA |
| 2nd unlock cycle | Address 0x2AA / Data 0x55 | Address 0x40002AA / Data 0x55 |
| 1st command cycle | Address 0x555 / Data 0x80 | Address 0x4000555 / Data 0x80 |
| 2nd command cycle | Address 0x555 / Data 0xAA | Address 0x4000555 / Data 0xAA |
| 3rd command cycle | Address 0x2AA / Data 0x55 | Address 0x40002AA / Data 0x55 |
| Sector Address / Sector Erase command | Address 0x0000000 / Data 0x30 | Address 0x4000000 / Data 0x30 |

No special address manipulation is required for reading the main flash array. While reading you cannot tell that there are two flash die - only that there is a continuous address space that spans both flash chips.

The special address manipulation is required for writing commands and receiving command response. Many commands have “unlock cycles” consisting of the 555h/AAh and 2AAh/55h address/data pattern. For these cycles A26 must be set correctly, so the unlock cycles are accepted by the intended flash die. Some commands also have address arguments that must be directed to the correct die via A26. These arguments are: Read Address (RA), Program Address (PA), Sector Address (SA), Write Buffer Location (WBL), PassWord Address (PWA), Don't Care (XXX - for single die only)

Autoselect

6 Autoselect

Table 4 provides the device identification codes for the S70GL02GS. For more information on the autoselect function, refer to the S29GL-S datasheet.

Table 4 Autoselect addresses in system

| Description | Address | Read data (word/byte mode) |
|-----------------------|--------------|---|
| Manufacturer ID | (Base) + 00h | 0001h |
| Device ID, Word 1 | (Base) + 01h | 227Eh |
| Device ID, Word 2 | (Base) + 0Eh | 2248h |
| Device ID, Word 3 | (Base) + 0Fh | 2201h |
| Secure Device Verify | (Base) + 03h | For S70GL02GS highest address sector protect: XX3Fh = Not factory locked XXBFh = Factory locked For S70GL02GS lowest address sector protect: XX2Fh = Not factory locked XXAFh = Factory locked |
| Sector Protect Verify | (SA) + 02h | xx01h/01h = Locked, xx00h/00h = Unlocked |

7 Electrical specifications

7.1 Thermal resistance

Table 5 Thermal resistance

| Parameter | Description | Test condition | LSH064 | Unit |
|------------------|--|--|---------------|-------------|
| Theta JA | Thermal resistance (Junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51, with Still Air (0 m/s). | 29.2 | °C/W |
| Theta JB | Thermal resistance (Junction to board) | | 11.3 | °C/W |
| Theta JC | Thermal resistance (Junction to case) | | 8.4 | °C/W |

8 DC characteristics

Table 6 DC characteristics

| Parameter | Description | Test conditions | Min | Typ ^[8] | Max | Unit |
|-----------|---|--|-----|--------------------|------|------|
| I_{LI} | Input load current | $V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ max | - | +0.04 | ±2.0 | μA |
| I_{LO} | Output leakage current | $V_{OUT} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC}$ max | - | +0.04 | ±2.0 | μA |
| I_{CC4} | V_{CC} standby current | CE#, RESET#, OE# = V_{IH} , $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max | - | 140 | 200 | μA |
| I_{CC5} | V_{CC} reset current ^[8, 9] | CE# = V_{IH} , RESET# = V_{IL} , $V_{CC} = V_{CC}$ max | - | 20 | 40 | mA |
| I_{CC6} | Automatic Sleep mode ^[10] | $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, $t_{ACC} + 30$ ns | - | 6 | 12 | mA |
| | | $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ASSB} | - | 200 | 300 | μA |
| I_{CC7} | V_{CC} current during power-up ^[8, 13] | RESET# = V_{IO} , CE# = V_{IO} , OE# = V_{IO} , $V_{CC} = V_{CC}$ max | - | 106 | 160 | mA |

Notes

7. I_{CC} active while Embedded Algorithm is in progress.
8. Not 100% tested.
9. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH} . After the end of t_{RPH} the device will go to standby mode until the next read or write.
10. Automatic sleep mode enables the lower power mode when addresses remain stable for a designated time.
11. $V_{IO} = 1.65$ V to V_{CC} or 2.7 V to V_{CC} depending on the model.
12. $V_{CC} = 3$ V and $V_{IO} = 3$ V or 1.8 V. When V_{IO} is at 1.8 V, I/O pins cannot operate at >1.8 V.
13. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
14. The recommended pull-up resistor for RY/BY# output is 5 kΩ to 10 kΩ.
15. For all other DC current values, refer to the [S29GL-128S_01GS_00](#) datasheet.

BGA package capacitance

9 BGA package capacitance

Table 7 BGA package capacitance

| Parameter | Description | Typ | Max | Unit |
|------------------|-----------------------|-----|-----|------|
| C _{IN} | Input capacitance | 15 | 16 | pF |
| C _{OUT} | Output capacitance | 10 | 11 | pF |
| A26 | Highest order address | 6 | 7 | pF |
| CE# | Separated control pin | 12 | 13 | pF |
| OE# | Separated control pin | 7 | 8 | pF |
| WE# | Separated control pin | 11 | 12 | pF |
| WP# | Separated control pin | 11 | 12 | pF |
| RESET# | Separated control pin | 8 | 9 | pF |
| RY/BY# | Separated control pin | 5 | 6 | pF |

Notes

- 16. Sampled, not 100% tested.
- 17. Test conditions TA = 25°C, f = 1.0 MHz.

Device ID and common flash interface (ID-CFI)
 ASO map

10 Device ID and common flash interface (ID-CFI) ASO map

The device ID portion of the ASO (word locations 0h to 0Fh) provides manufacturer ID, device ID, sector protection state, and basic feature set information for the device.

ID-CFI location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go HIGH before the read and return LOW to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

Table 8 ID (Autoselect) address map

| Description | Address | Read data |
|-------------------------|--------------|---|
| Manufacture ID | (SA) + 0000h | 0001h |
| Device ID | (SA) + 0001h | 227Eh |
| Protection verification | (SA) + 0002h | Sector protection state (1 = Sector protected, 0 = Sector unprotected). This protection state is shown only for the SA selected when entering ID-CFI ASO. Reading other SA provides undefined data. To read a different SA protection state ASO exit command must be used and then enter ID-CFI ASO again with the new SA. |
| Indicator bits | (SA) + 0003h | For S70GL02GS highest address sector protect: XX3Fh = Not factory locked XXBFh = Factory locked For S70GL02GS lowest address sector protect: XX2Fh = Not factory locked XXAFh = Factory locked DQ15–DQ08 = 1 (Reserved) DQ7 - Factory locked secure silicon region 1 = Locked 0 = Not locked DQ6 - Customer locked secure silicon region 1 = Locked 0 = Not locked DQ5 = 1 (Reserved) DQ4 - WP# Protects 0 = lowest address Sector 1 = highest address Sector DQ3–DQ0 = 1 (Reserved) |
| RFU | (SA) + 0004h | Reserved |
| | (SA) + 0005h | Reserved |
| | (SA) + 0006h | Reserved |
| | (SA) + 0007h | Reserved |
| | (SA) + 0008h | Reserved |
| | (SA) + 0009h | Reserved |
| | (SA) + 000Ah | Reserved |
| | (SA) + 000Bh | Reserved |

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Device ID and common flash interface (ID-CFI)
ASO map

Table 8 ID (Autoselect) address map (Continued)

| Description | Address | Read data |
|---------------------|--------------|--|
| Lower software bits | (SA) + 000Ch | Bit 0 - Status Register support 1 = Status Register supported 0 = Status Register not supported Bit 1 - DQ polling Support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3-2 - Command set support 11 = reserved 10 = reserved 01 = Reduced Command set 00 = Classic Command set Bits 4-15 - Reserved = 0 |
| Upper software bits | (SA) + 000Dh | Reserved |
| Device ID | (SA) + 000Eh | 2248h = 2 Gb |
| Device ID | (SA) + 000Fh | 2201h |

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Device ID and common flash interface (ID-CFI)
ASO map

Table 9 CFI query identification string

| Word address | Data | Description |
|--|-------------------------|---|
| (SA) + 0010h (SA) + 0011h (SA) + 0012h | 0051h 0052h 0059h | Query Unique ASCII string "QRY" |
| (SA) + 0013h (SA) + 0014h | 0002h 0000h | Primary OEM Command set |
| (SA) + 0015h (SA) + 0016h | 0040h 0000h | Address for primary extended table |
| (SA) + 0017h (SA) + 0018h | 0000h 0000h | Alternate OEM command set (00h = none exists) |
| (SA) + 0019h (SA) + 001Ah | 0000h 0000h | Address for alternate OEM extended table (00h = none exists) |

Table 10 CFI system interface string

| Word address | Data | Description |
|--------------|--------------|--|
| (SA) + 001Bh | 0027h | V _{CC} Min. (erase/program) (D7–D4: volts, D3–D0: 100 mV) |
| (SA) + 001Ch | 0036h | V _{CC} Max. (erase/program) (D7–D4: volts, D3–D0: 100 mV) |
| (SA) + 001Dh | 0000h | V _{PP} Min. voltage (00h = no V _{PP} pin present) |
| (SA) + 001Eh | 0000h | V _{PP} Max. voltage (00h = no V _{PP} pin present) |
| (SA) + 001Fh | 0008h | Typical timeout per single word write 2 ^N μs |
| (SA) + 0020h | 0009h | Typical timeout for max multi-byte program, 2 ^N μs (00h = not supported) |
| (SA) + 0021h | 0008h | Typical timeout per individual block erase 2 ^N ms |
| (SA) + 0022h | 0013h (2 Gb) | Typical timeout for full chip erase 2 ^N ms (00h = not supported) |
| (SA) + 0023h | 0001h | Max. timeout for single word write 2 ^N times typical |
| (SA) + 0024h | 0002h | Max. timeout for buffer write 2 ^N times typical |
| (SA) + 0025h | 0003h | Max. timeout per individual block erase 2 ^N times typical |
| (SA) + 0026h | 0003h | Max. timeout for full chip erase 2 ^N times typical (00h = not supported) |

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Device ID and common flash interface (ID-CFI)
 ASO map

Table 11 CFI device geometry definition

| Word address | Data | Description |
|--------------|--------------|---|
| (SA) + 0027h | 001Ch (2 Gb) | Device Size = 2 ^N byte |
| (SA) + 0028h | 0001h | Flash Device Interface Description 0 = x8-only, 1 = x16-only, 2 = x8/x16 capable |
| (SA) + 0029h | 0000h | |
| (SA) + 002Ah | 0009h | Max. number of byte in multi-byte write = 2 ^N (00 = not supported) |
| (SA) + 002Bh | 0000h | |
| (SA) + 002Ch | 0001h | Number of erase block regions within device 1 = Uniform device, 2 = Boot device |
| (SA) + 002Dh | 00XXh | Erase block region 1 information (refer to JEDEC JESD68-01 or JEP137 specifications) 00FFh, 0007h, 0000h, 0002h = 2 Gb |
| (SA) + 002Eh | 000Xh | |
| (SA) + 002Fh | 0000h | |
| (SA) + 0030h | 000Xh | |
| (SA) + 0031h | 0000h | Erase block region 2 information (refer to CFI publication 100) |
| (SA) + 0032h | 0000h | |
| (SA) + 0033h | 0000h | |
| (SA) + 0034h | 0000h | |
| (SA) + 0035h | 0000h | Erase block region 3 information (refer to CFI publication 100) |
| (SA) + 0036h | 0000h | |
| (SA) + 0037h | 0000h | |
| (SA) + 0038h | 0000h | |
| (SA) + 0039h | 0000h | Erase block region 4 information (refer to CFI publication 100) |
| (SA) + 003Ah | 0000h | |
| (SA) + 003Bh | 0000h | |
| (SA) + 003Ch | 0000h | |

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Device ID and common flash interface (ID-CFI)
ASO map

Table 12 CFI primary vendor-specific extended query

| Word address | Data | Description |
|--------------|-------|---|
| (SA) + 0040h | 0050h | Query-unique ASCII string "PRI" |
| (SA) + 0041h | 0052h | |
| (SA) + 0042h | 0049h | |
| (SA) + 0043h | 0031h | Major version number, ASCII |
| (SA) + 0044h | 0035h | Minor version number, ASCII |
| (SA) + 0045h | 001Ch | Address sensitive unlock (Bits 1–0) 00b = Required 01b = Not required Process technology (Bits 5–2) 0000b = 0.23 μm floating gate 0001b = 0.17 μm floating gate 0010b = 0.23 μm MIRRORBIT™ 0011b = 0.13 μm floating gate 0100b = 0.11 μm MIRRORBIT™ 0101b = 0.09 μm floating gate 0110b = 0.09 μm MIRRORBIT™ 0111b = 0.065 μm MIRRORBIT™ Eclipse 1000b = 0.065 μm MIRRORBIT™ 1001b = 0.045 μm MIRRORBIT™ |
| (SA) + 0046h | 0002h | Erase Suspend 0 = Not supported 1 = Read only 2 = Read and write |
| (SA) + 0047h | 0001h | Sector protect 00 = Not supported X = Number of sectors in smallest group |
| (SA) + 0048h | 0000h | Temporary sector unprotect 00 = Not supported 01 = Supported |
| (SA) + 0049h | 0008h | Sector protect/unprotect scheme 04 = High voltage method 05 = Software command locking method 08 = Advanced sector protection method |
| (SA) + 004Ah | 0000h | Simultaneous operation 00 = Not supported X = Number of banks |
| (SA) + 004Bh | 0000h | Burst mode type 00 = Not supported 01 = Supported |
| (SA) + 004Ch | 0003h | Page mode type 00 = Not supported 01 = 4 word page 02 = 8 word page 03 = 16 word page |
| (SA) + 004Dh | 0000h | ACC (Acceleration) supply minimum 00 = Not supported D7–D4: Volt D3–D0: 100 mV |

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Device ID and common flash interface (ID-CFI)
ASO map

Table 12 CFI primary vendor-specific extended query (Continued)

| Word address | Data | Description |
|--------------|-------------------------------|---|
| (SA) + 004Eh | 0000h | ACC (Acceleration) supply maximum 00 = Not supported D7-D4: Volt D3-D0: 100 mV |
| (SA) + 004Fh | 0004h (Bottom) 0005h (Top) | WP# Protection 00h = Flash device without WP Protect (No boot) 01h = Eight 8 KB sectors at top and bottom with WP (Dual boot) 02h = Bottom boot device with WP protect (Bottom boot) 03h = Top boot device with WP protect (Top boot) 04h = Uniform, bottom WP protect (Uniform bottom boot) 05h = Uniform, top WP protect (Uniform top boot) 06h = WP Protect for all sectors 07h = Uniform, top or bottom WP protect |
| (SA) + 0050h | 0001h | Program Suspend 00 = Not supported 01 = Supported |
| (SA) + 0051h | 0000h | Unlock Bypass 00 = Not supported 01 = Supported |
| (SA) + 0052h | 0009h | Secured silicon sector (Customer OTP area) size 2^N (bytes) |
| (SA) + 0053h | 008Fh | Software features bit 0: Status Register polling (1 = Supported, 0 = Not supported) bit 1: DQ polling (1 = Supported, 0 = Not supported) bit 2: New Program Suspend/Resume commands (1 = Supported, 0 = Not supported) bit 3: Word programming (1 = Supported, 0 = Not supported) bit 4: Bit-field programming (1 = Supported, 0 = Not supported) bit 5: Autodetect programming (1 = Supported, 0 = Not supported) bit 6: RFU bit 7: Multiple writes per line (1 = Supported, 0 = Not supported) |
| (SA) + 0054h | 0005h | Page Size = 2^N bytes |
| (SA) + 0055h | 0006h | Erase Suspend timeout maximum < 2^N (μ s) |
| (SA) + 0056h | 0006h | Program Suspend timeout maximum < 2^N (μ s) |
| (SA) + 0078h | 0006h | Embedded hardware reset timeout maximum < 2^N (μ s) Reset with reset pin |
| (SA) + 0079h | 0009h | Non-embedded hardware reset timeout maximum < 2^N (μ s) Power-on reset |

11 Package diagram

11.1 LSH064 – 64-ball fortified ball grid array, 13 x 11 mm

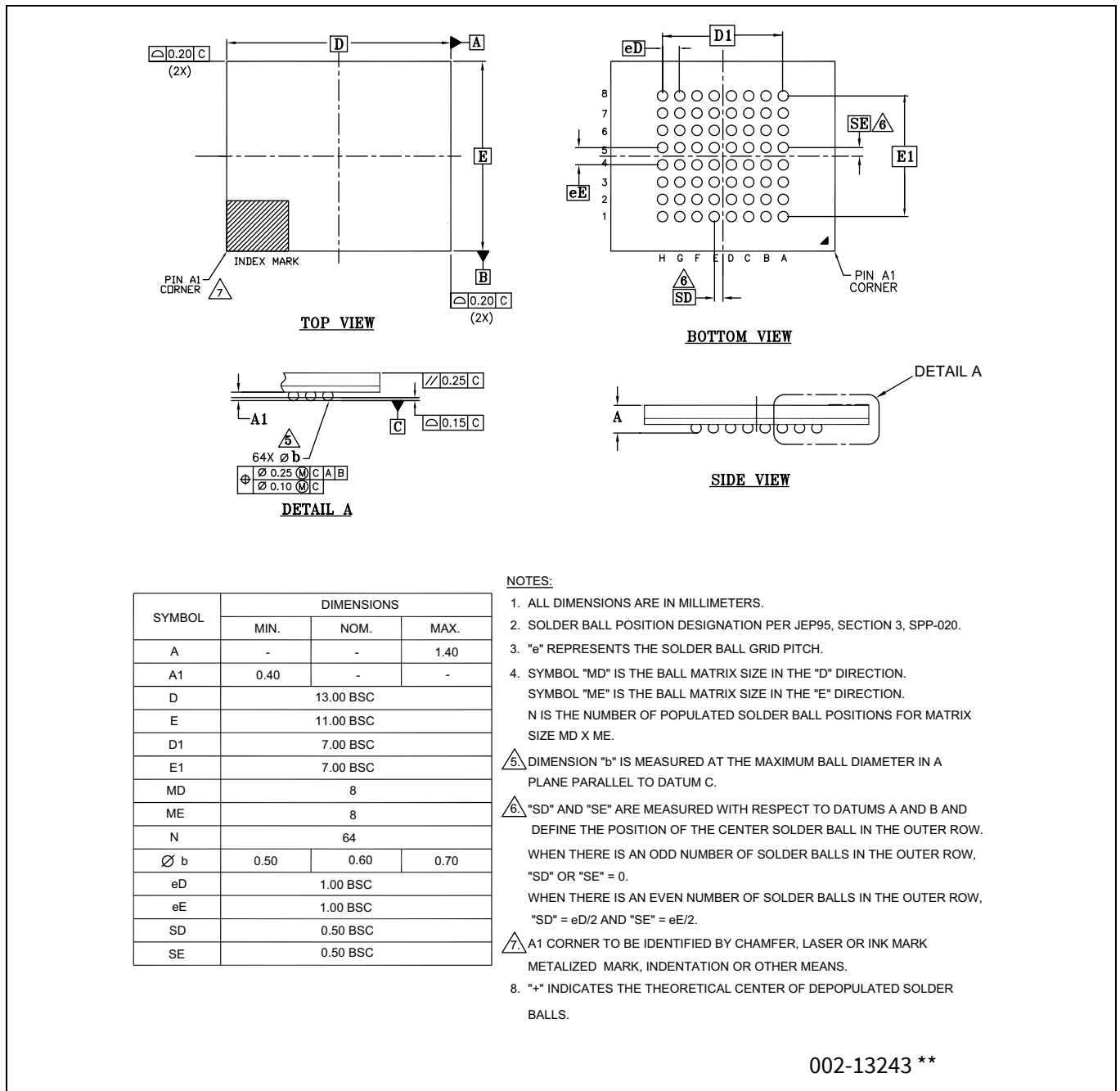


Figure 5 64-ball FBGA (13.0 × 11.0 × 1.4 mm) package outline, 002-13243

Ordering information

12 Ordering information

12.1 Recommended combinations

Recommended combinations table below list various configurations planned to be available in volume. **Table 13** will be updated as new combinations are released. Contact your local Infineon sales representative to confirm availability of specific configuration not listed or to check on newly released combinations.

Table 13 S29GL-S valid combinations

| Base OPN | Speed (ns) | Package and temperature | Model number | Packing type | Ordering part number (yy = Model number, x = Packing type) |
|-----------|------------|--------------------------|--------------|----------------------|--|
| S70GL02GS | 110 | FHI, FHV ^[18] | 01, 02 | 0, 3 ^[19] | S70GL02GS11FHI01x S70GL02GS11FHI02x S70GL02GS11FHV01x S70GL02GS11FHV02x |
| | 120 | | V1, V2 | | S70GL02GS12FHIV1x S70GL02GS12FHIV2x S70GL02GS12FHV1x S70GL02GS12FHV2x |

Table 14 lists configurations that are automotive grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production part approval process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non-AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 14 Valid combinations – automotive grade / AEC-Q100

| Base OPN | Speed (ns) | Package and temperature | Model number | Packing type | Ordering part number (yy = Model Number, x = Packing Type) |
|-----------|------------|--------------------------|--------------|----------------------|--|
| S70GL02GS | 110 | FHA, FHB ^[18] | 01, 02 | 0, 3 ^[19] | S70GL02GS11FHA01x S70GL02GS11FHA02x S70GL02GS11FHB01x S70GL02GS11FHB02x |
| | 120 | | V1, V2 | | S70GL02GS12FHAV1x S70GL02GS12FHAV2x S70GL02GS12FHBV1x S70GL02GS12FHBV2x |

Notes

18. BGA package marking omits leading “S70” and packing type designator from ordering part number.

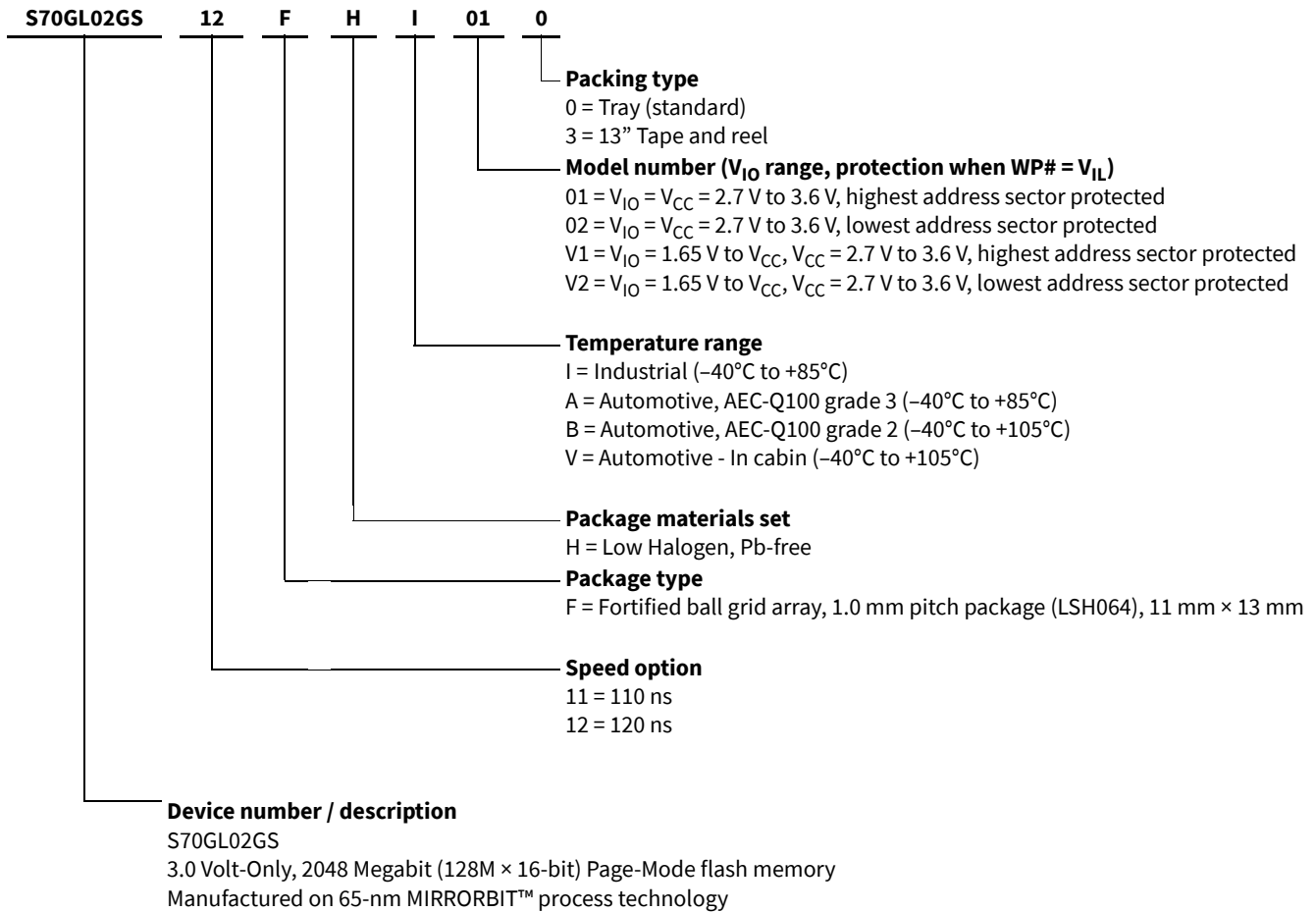
19. Packing Type “0” is standard option.

2 Gbit (256 MB) GL-T MIRRORBIT™ Flash Parallel, 3.0 V



Ordering information

The ordering part number is formed by a valid combination of the following:



Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|---|
| ** | 2011-05-19 | Spansion Publication Number: S70GL-S_00 Initial release. |
| *A | 2011-07-08 | Performance Characteristics: Updated Typical Program and Erase Rates Ordering Information: Updated model number description of V1 and V2 DC Characteristics: Modified Note 3 |
| *B | 2011-09-23 | Distinctive Characteristics: Cosmetic changes Ordering Information: Updated CFI Device Geometry Definition: Data at (SA) + 002Eh modified |
| *C | 2011-12-15 | Global: Data sheet status changed from Preliminary to Full Production Performance Characteristics: Updated Sector Erase time Figure: 64-ball Fortified Ball Grid Array: Added notes BGA Package Capacitance: Updated |
| *D | 2014-06-27 | Global: Added –40°C to +105°C temperature range |
| *E | 2015-08-13 | Updated to Cypress template. |
| *F | 2016-03-04 | General Description: Updated Cypress Document Number as “001-98285” in the table. Distinctive Characteristics: Updated link to S29GL01GS datasheet. Updated to new template. |
| *G | 2016-07-08 | Updated Document Title to read as “S70GL02GS 2 Gbit (256 MB) GL-T MIRRORBIT™ Flash”. Updated to new template. |
| *H | 2017-05-31 | Updated Cypress Logo and Copyright. |
| *I | 2017-06-15 | Updated Ordering information: Updated description. Added Table 14 . Updated details under “Temperature range” in valid combination. |
| *J | 2017-08-09 | Updated Ordering information: Updated details under “Device number/description” in valid combination. Added Second die access . |
| *K | 2022-09-09 | Updated Document Title to read as “S70GL02GS, 2 Gbit (256 MB) GL-T MIRRORBIT™ Flash Parallel, 3.0 V”. Updated Distinctive characteristics: Updated hyperlinks. Updated Electrical specifications: Added Thermal resistance . Updated Package diagram: Updated LSH064 – 64-ball fortified ball grid array, 13 x 11 mm: Replaced existing spec with 002-13243 **. Migrated to Infineon template. |