2 Gb (256 MB) GL-T MIRRORBIT™ Flash

Parallel, 3.0 V

General description

The S70GL02GT 2-Gb MIRRORBIT™ flash memory device is fabricated on 45-nm MIRRORBIT™ process technology. This device offers a fast page access time of 20 ns with a corresponding random access time of 110 ns. It features a write buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard single byte/word programming algorithms. This makes the device an ideal product for today's embedded applications that require higher density, better performance and lower power consumption.

This document contains information for the S70GL02GT device, which is a dual-die stack of two S29GL01GT dies.

For detailed specifications, refer to the discrete die datasheet provided in the below table.

Table 1 Reference documents

Document	Infineon document number
S29GL01GT, S29GL512T datasheet	002-00247

Features

- CMOS 3.0 V core with versatile I/O
- Two 1024 Mb (S29GL01GT) in a single 64-ball fortified-BGA package (see the **S29GL01GT datasheet** for full specifications)
- 45 nm MIRRORBIT™ process technology
- Single supply (V_{CC}) for read/program/erase (2.7 V to 3.6 V)
- Versatile I/O feature
  - Wide I/O voltage (V_{IO}): 1.65 V to V_{CC}
- ×8 and ×16 data bus
- 16-word/32-byte page read buffer
- 512-byte programming buffer
  - Programming in page multiples, up to a maximum of 512 bytes
- Sector erase
  - Uniform 128-KB sectors
  - S70GL02GT: 2048 sectors
- Suspend and Resume commands for program and erase operations
- Status Register, data polling, and ready/busy pin methods to determine device status
- Advanced sector protection (ASP)
  - Volatile and non-volatile protection methods for each sector
- Separate 1024-bye one time program (OTP) array with two lockable regions
  - Each device supports common flash interface (CFI)
- WP# input
  - Protects the last sector of the device, regardless of sector protection settings

- Temperature range/grade
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Automotive, AEC-Q100 grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 grade 2 (–40°C to +105°C)
- 100,000 program-erase cycles
- 20-year data retention
- Packaging options
  - 64-ball LSH fortified BGA, 13 mm × 11 mm

Performance characteristics

Max read access times (ns)

Parameter	2 Gb	
Random access time (t_{ACC})	110	120
Page access time (t_{PACC})	20	30
CE# access time (t_{CE})	110	120
OE# access time (t_{OE})	25	35

Typical program and erase rates

Operation	–40°C to +85°C	–40°C to +105°C
Buffer programming (512 bytes)	1.114 MBps	1.14 MBps
Sector erase (128 KB)	245 KBps	245 KBps

Maximum current consumption

Operation	–40°C to +85°C	–40°C to +105°C
Active read at 5 MHz, 30 pF	60 mA	60 mA
Program	100 mA	100 mA
Erase	100 mA	100 mA
Standby	200 µA	400 µA

Note
1. Access times are dependent on V_{IO} operating ranges. See **"Ordering information"** on page 20 for further details.

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1 Block diagram

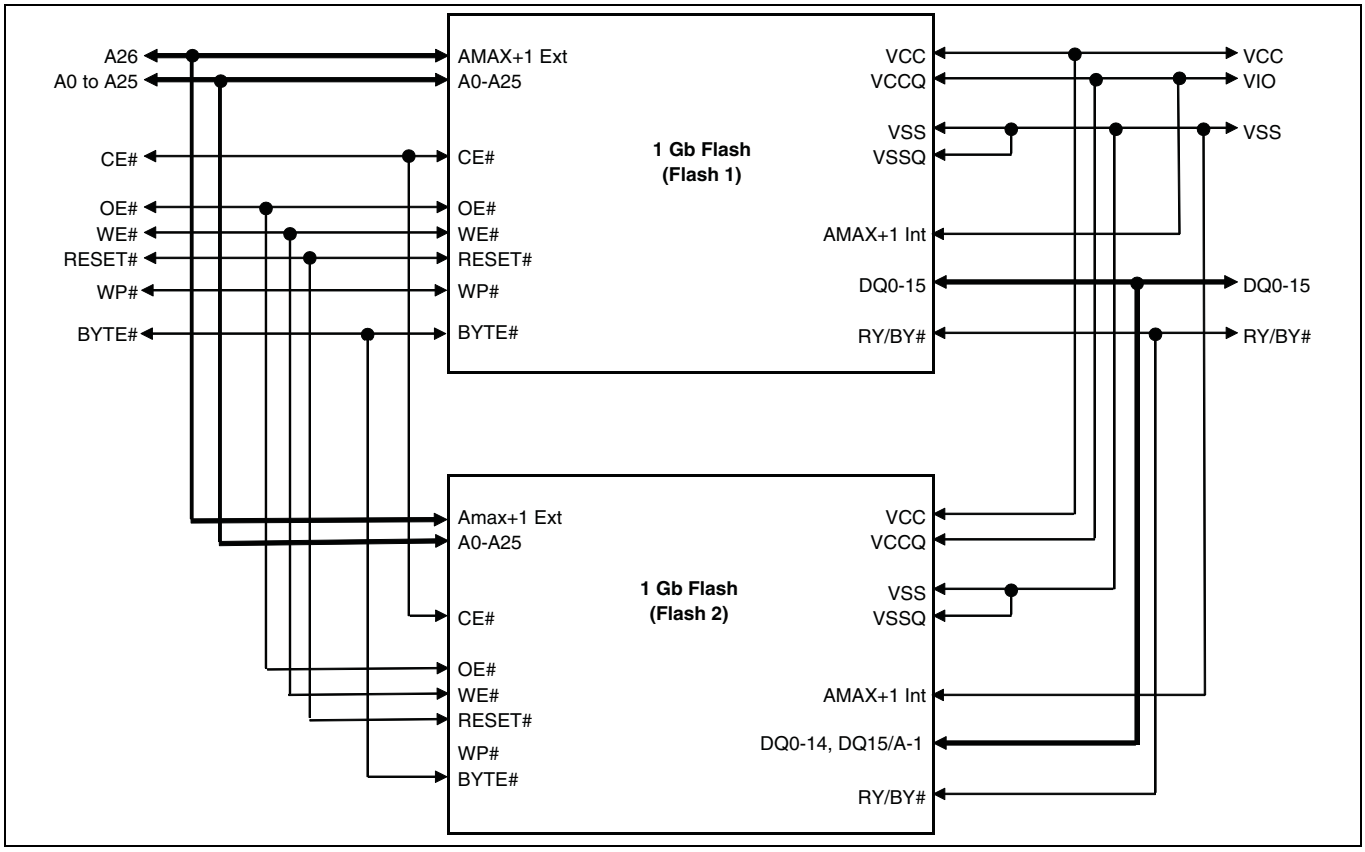


Figure 1 2 x GL01GT (Highest address sector protected) block diagram

2 Connection diagrams

2.1 Special handling instructions for BGA package

Special handling is required for flash memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

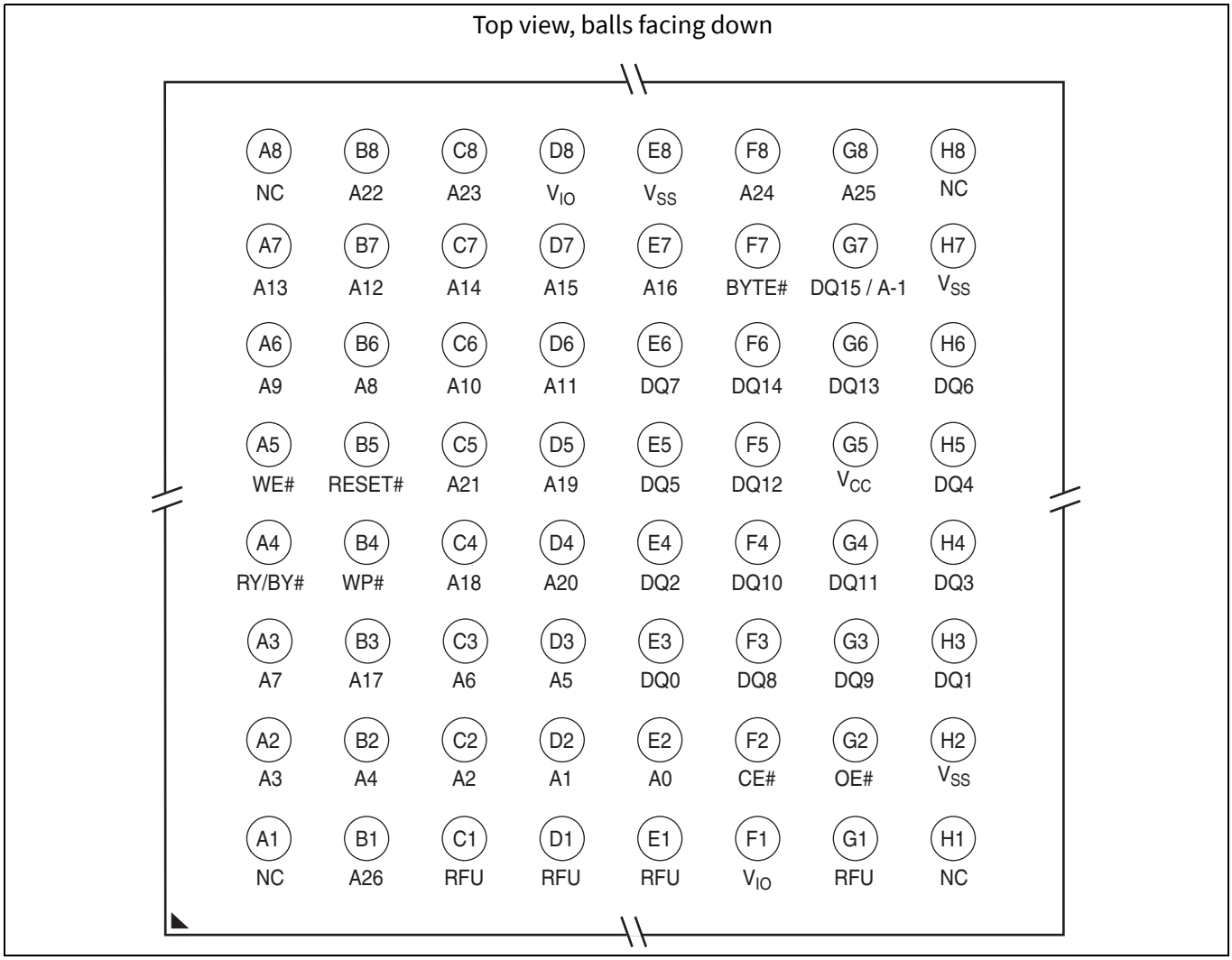


Figure 2 64-ball fortified ball grid array

Notes

2. Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
3. Balls C1, D1, E1, G1: Reserved for Future Use (RFU).
4. Balls A1, A8, H1, H8: No Connect (NC).

3 Input/output description and logic symbol

Table 2 identifies the input and output package connections provided on the device.

Table 2 Input/output description

Symbol	Type	Description
DQ14–DQ0	I/O	Data inputs and outputs.
DQ15/A1	Input/Output	DQ15: Data inputs and outputs. A1: LSB address input in byte mode.
CE#	Input	Chip Enable. At V_{IL}, selects the device for data transfer with the host memory controller.
OE#	Input	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH}, causes outputs to be high impedance (High-Z).
WE#	Input	Write Enable. At V_{IL}, indicates data transfer from the host to device. At V_{IH}, indicates data transfer is from the device to host.
A26-A0	Input	Address lines for S29GL02GT.
V_{CC}	Supply	Core power supply.
V_{IO}	Supply	Versatile I/O power supply.
V_{SS}	Supply	Power supplies ground.
RY/BY#	Output — open drain	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively engaged in an embedded algorithm such as erasing or programming. At High-Z, the device is ready for read or a new command write — requires an external pull-up resistor to detect the High-Z state. Multiple devices may have their RY/BY# outputs tied together to detect when all devices are ready.
BYTE#	Input	Selects data bus width. At V_{IL}, the device is in byte configuration and data I/O pins DQ7–DQ0 are active and DQ15/A1 becomes the LSB address input. At V_{IH}, the device is in word configuration and data I/O pins DQ15–DQ0 are active.
RESET#	Input	Hardware Reset. At V_{IL}, causes the device to reset control logic to its standby state, ready for reading array data.
WP#	Input	Write Protect. At V_{IL}, disables program and erase functions in the highest address 64-kword (128-KB) sector of the device. At V_{IH}, the sector is not protected. WP# has an internal pull-up; When unconnected WP# is at V_{IH}.
NC	No Connect	Not Connected internally. The pin/ball location may be used in the printed circuit board (PCB) as part of a routing channel.
DNU	Reserved	Do Not Use. Reserved for use by Infineon. The pin/ball is connected internally. The input has an internal pull-down resistance to V_{SS}. The pin/ball can be left open or tied to V_{SS} on the PCB.
RFU	No Connect	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by the PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.

4 Memory map

The S70GL02GT consist of uniform 64 kword (128-KB) sectors organized as shown in **Table 3**.

Table 3 S70GL02GT sector and memory address map

Uniform sector size	Sector count	Sector range	Address range (16-bit)	Notes
64 Kword/128 KB	2048	SA00	0000000h–000FFFFh	Sector starting address
		:	:	
		SA2047	7FF0000H–7FFFFFFh	Sector ending address

Note
5. This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001–SA2046) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the pattern xxx0000h–xxxFFFFh.

5 Autoselect

Table 4 provides the device identification codes for S70GL02GT. For more information on the autoselect function, refer to the S29GL-S datasheet (Infineon publication number 002-00247).

Table 4 Autoselect addresses in system

Description	Address	Read data (word/byte mode)
Manufacturer ID	(Base) + 00h	0001h
Device ID, Word 1	(Base) + 01h	227Eh
Device ID, Word 2	(Base) + 0Eh	2248h
Device ID, Word 3	(Base) + 0Fh	2201h
Secure Device Verify	(Base) + 03h	For S70GL02GT highest address sector protect: XX3Fh = Not Factory Locked XXBFh = Factory Locked
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

6 Electrical specifications

6.1 DC characteristics

Table 5 DC characteristics (–40°C to +85°C)

Parameter	Description	Test conditions		Min	Typ[7]	Max	Unit
I_{LI}	Input load current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	All others	–	±0.04	±2.0	µA
			WP#, BYTE#	–	±1.0	±4.0	
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±0.04	±2.0	µA
I_{CC4}	V_{CC} standby current	CE#, RESET#, OE# = V_{IH}, $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max	–	–	140	200	µA
I_{CC5}	V_{CC} reset current[7, 8]	CE# = V_{IH}, RESET# = V_{IL}, $V_{CC} = V_{CC}$ max	–	–	20	40	mA
I_{CC6}	Automatic sleep mode[9]	$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ACC} + 30 ns	–	–	6	12	mA
		$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ASSB}	–	–	200	300	µA
I_{CC7}	V_{CC} current during power-up[7, 12]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$ max,	–	–	106	160	mA

Notes

6. I_{CC} active while Embedded Algorithm is in progress.
7. Not 100% tested.
8. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
9. Automatic sleep mode enables the lower power mode when addresses remain stable for a designated time.
10. V_{IO} = 1.65 V to V_{CC} or 2.7 V to V_{CC} depending on the model.
11. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/O pins cannot operate at >1.8 V.
12. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
13. For all other DC current values, refer to the **S29GL01GT/S29GL512T** datasheet.

Table 6 DC characteristics (–40°C to +105°C)

Parameter	Description	Test conditions		Min	Typ[15]	Max	Unit
I_{LI}	Input load current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	All others	–	±0.04	±2.0 / ±20.0[22]	µA
			WP#, BYTE#	–	±1.0	±4.0 / ±20.0[22]	
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±0.04	±2.0	µA
I_{CC4}	VCC standby current	CE#, RESET#, OE# = V_{IH}, $V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max	–	–	140	400	µA
I_{CC5}	V_{CC} reset current[15, 16]	CE# = V_{IH}, RESET# = V_{IL}, $V_{CC} = V_{CC}$ max	–	–	20	40	mA
I_{CC6}	Automatic sleep mode[17]	$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ACC} + 30 ns	–	–	6	12	mA
		$V_{IH} = V_{IO}$, $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max, t_{ASSB}	–	–	200	400	µA
I_{CC7}	V_{CC} current during power-up[15, 20]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$ max	–	–	106	160	mA

Notes

14. I_{CC} active while Embedded Algorithm is in progress.
15. Not 100% tested.
16. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
17. Automatic sleep mode enables the lower power mode when addresses remain stable for a designated time.
18. V_{IO} = 1.65 V to V_{CC} or 2.7 V to V_{CC} depending on the model.
19. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/O pins cannot operate at >1.8 V.
20. During power-up there are spikes of current demand, the system needs to be able to supply this current to ensure that the part initializes correctly.
21. For all other DC current values, refer to the **S29GL01GT/S29GL512T** datasheet.
22. For S70GL02GT11FHB02x, S70GL02GT12FHBV1x, and S70GL02GT12FHBV2x devices.

6.2 BGA package capacitance

Table 7 BGA package capacitance

Symbol	Description	Typ	Max	Unit
C_{IN}	Input capacitance	9	11	pF
C_{OUT}	Output capacitance	7	9	pF
A26	Highest order address	5	6	pF
CE#	Separated control pin	4	5	pF
OE#	Separated control pin	4	5	pF
WE#	Separated control pin	7	8	pF
WP#	Separated control pin	5	6	pF
RESET#	Separated control pin	39	41	pF
RY/BY#	Separated control pin	4	5	pF

6.3 Thermal resistance

Table 8 Thermal resistance

Parameter	Description	Test condition	LSH064	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. with Still Air (0 m/s).	29	°C/W
Theta JB	Thermal resistance (Junction to board)		11.3	°C/W
Theta JC	Thermal Resistance (Junction to case)		8.4	°C/W

Notes
23.Sampled, not 100% tested.
24.Test conditions T_A = 25°C, f = 1.0 MHz.

7 Data integrity

7.1 Erase endurance

Table 9 Erase endurance

Parameter	Minimum	Unit
Program/erase cycles per main flash array sectors	100K	P/E cycle
Program/erase cycles per PPB array or non-volatile register array[25]	100K	P/E cycle

7.2 Data retention

Table 10 Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	1K program/erase cycles	20	Years
	10K program/erase cycles	2	Years
	100K program/erase cycles	0.2	Years

Contact Infineon sales or an FAE representative for additional information regarding data integrity.

Note
25. Each write command to a non-volatile register causes a P/E cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not P/E cycled.

8 Device ID and Common Flash Interface (ID-CFI) ASO map

The device ID portion of the ASO (word locations 0h to 0Fh) provides manufacturer ID, device ID, sector protection state, and basic feature set information for the device.

ID-CFI location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go HIGH before the read and return LOW to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

Table 11 ID (autoselect) address map

Description	Address (×16)	Address (×8)	Read data
Manufacture ID	(SA) + 0000h	(SA) + 0000h	0001h
Device ID	(SA) + 0001h	(SA) + 0002h	227Eh
Protection verification	(SA) + 0002h	(SA) + 0004h	Sector protection state (1 = Sector protected, 0 = Sector unprotected). To read a different SA protection state only a new SA needs to be given.
Indicator bits	(SA) + 0003h	(SA) + 0006h	For S70GL02Gt highest address sector protect: XX3Fh = Not Factory Locked XXBFh = Factory Locked For S70GL02GT lowest address sector protect: XX2Fh = Not Factory Locked XXAFh = Factory Locked DQ15–DQ08 = 1 (Reserved) DQ7 - Factory Locked Secure Silicon Region 1 = Locked 0 = Not Locked DQ6 - Customer Locked Secure Silicon Region 1 = Locked 0 = Not Locked DQ5 = 1 (Reserved) DQ4 - WP# Protects 0 = lowest address Sector 1 = highest address Sector DQ3–DQ0 = 1 (Reserved)
RFU	(SA) + 0004h	(SA) + 0008h	Reserved
	(SA) + 0005h	(SA) + 000Ah	Reserved
	(SA) + 0006h	(SA) + 000Ch	Reserved
	(SA) + 0007h	(SA) + 000Eh	Reserved
	(SA) + 0008h	(SA) + 0010h	Reserved
	(SA) + 0009h	(SA) + 0012h	Reserved
	(SA) + 000Ah	(SA) + 0014h	Reserved
	(SA) + 000Bh	(SA) + 0016h	Reserved

Device ID and Common Flash Interface (ID-CFI)
ASO map

Table 11 ID (autoselect) address map (Continued)

Description	Address (×16)	Address (×8)	Read data
Lower software bits	(SA) + 000Ch	(SA) + 0018h	Bit 0 - Status Register support 1 = Status Register supported 0 = Status Register not supported Bit 1 - DQ polling support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3–2 - Command Set support 11 = Reserved 10 = Reserved 01 = Reduced Command Set 00 = Classic Command set Bits 4–15 - Reserved = 0
Upper software bits	(SA) + 000Dh	(SA) + 001Ah	Reserved
Device ID	(SA) + 000Eh	(SA) + 001Ch	2248h = 2 Gb
Device ID	(SA) + 000Fh	(SA) + 000Eh	2201h

Table 12 CFI query identification string

Word address	Data	Description
(SA) + 0010h (SA) + 0011h (SA) + 0012h	0051h 0052h 0059h	Query unique ASCII string “QRY”
(SA) + 0013h (SA) + 0014h	0002h 0000h	Primary OEM command set
(SA) + 0015h (SA) + 0016h	0040h 0000h	Address for primary extended table
(SA) + 0017h (SA) + 0018h	0000h 0000h	Alternate OEM command set (00h = none exists)
(SA) + 0019h (SA) + 001Ah	0000h 0000h	Address for alternate OEM extended table (00h = none exists)

Table 13 CFI system interface string

Word address	Data	Description
(SA) + 001Bh	0027h	V_{CC} Min (erase/program) (D7–D4: volts, D3–D0: 100 mV)
(SA) + 001Ch	0036h	V_{CC} Max (erase/program) (D7–D4: volts, D3–D0: 100 mV)
(SA) + 001Dh	0000h	V_{PP} Min voltage (00h = No V_{PP} pin present)
(SA) + 001Eh	0000h	V_{PP} Max voltage (00h = No V_{PP} pin present)
(SA) + 001Fh	0008h	Typical timeout per single word write 2^N µs
(SA) + 0020h	0009h	Typical timeout for max multi-byte program, 2^N µs (00h = Not supported)
(SA) + 0021h	000Ah	Typical timeout per individual block erase 2^N ms
(SA) + 0022h	0015h (2 Gb)	Typical timeout for full chip erase 2^N ms (00h = Not supported)
(SA) + 0023h	0002h (85°C) 0003h (105°C)	Max timeout for single word write 2^N times typical
(SA) + 0024h	0001h (85°C) 0002h (105°C)	Max timeout for buffer write 2^N times typical
(SA) + 0025h	0002h	Max timeout per individual block erase 2^N times typical
(SA) + 0026h	0002h	Max timeout for full chip erase 2^N times typical (00h = Not supported)

Table 14 CFI device geometry definition

Word address	Data	Description
(SA) + 0027h	001Ch (2 Gb)	Device size = 2^N byte
(SA) + 0028h	0002h	Flash device interface description 0 = ×8-only, 1 = ×16-only, 2 = ×8/×16 capable
(SA) + 0029h	0000h	
(SA) + 002Ah	0009h	Max. number of byte in multi-byte write = 2^N (00 = Not supported)
(SA) + 002Bh	0000h	
(SA) + 002Ch	0001h	Number of erase block regions within device 1 = Uniform device, 2 = Boot device
(SA) + 002Dh	00FFh	Erase block region 1 information (Refer to JEDEC JESD68-01 or JEP137 specifications)
(SA) + 002Eh	0007h	
(SA) + 002Fh	0000h	
(SA) + 0030h	0002h	
(SA) + 0031h	0000h	Erase block region 2 information (Refer to CFI publication 100)
(SA) + 0032h	0000h	
(SA) + 0033h	0000h	
(SA) + 0034h	0000h	
(SA) + 0035h	0000h	Erase block region 3 information (Refer to CFI publication 100)
(SA) + 0036h	0000h	
(SA) + 0037h	0000h	
(SA) + 0038h	0000h	
(SA) + 0039h	0000h	Erase block region 4 information (Refer to CFI publication 100)
(SA) + 003Ah	0000h	
(SA) + 003Bh	0000h	
(SA) + 003Ch	0000h	
(SA) + 003Dh	FFFFh	Reserved
(SA) + 003Eh	FFFFh	
(SA) + 003Fh	FFFFh	

Table 15 CFI primary vendor-specific extended query

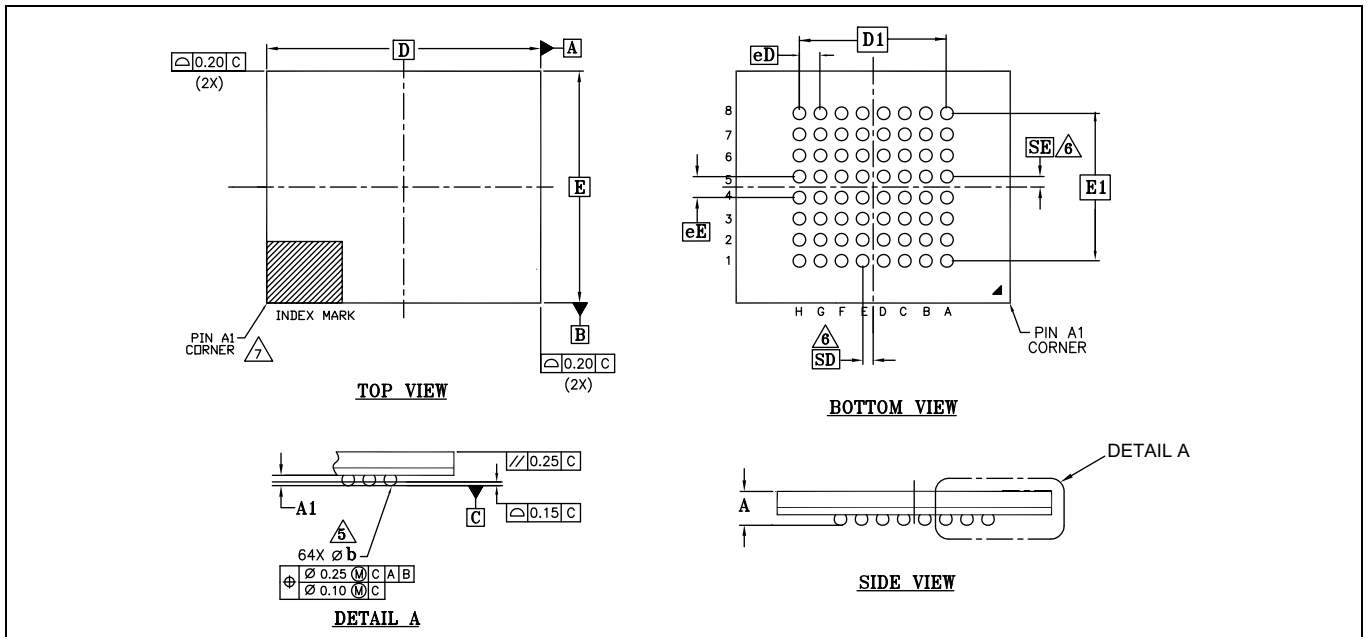
Word address	Data	Description
(SA) + 0040h	0050h	Query-unique ASCII string “PRI”
(SA) + 0041h	0052h	
(SA) + 0042h	0049h	
(SA) + 0043h	0031h	Major version number, ASCII
(SA) + 0044h	0035h	Minor version number, ASCII
(SA) + 0045h	0024h	Address sensitive unlock (Bits 1–0) 00b = Required 01b = Not required Process technology (Bits 5–2) 0000b = 0.23 µm Floating Gate 0001b = 0.17 µm Floating Gate 0010b = 0.23 µm MIRRORBIT™ 0011b = 0.13 µm Floating Gate 0100b = 0.11 µm MIRRORBIT™ 0101b = 0.09 µm Floating Gate 0110b = 0.09 µm MIRRORBIT™ 0111b = 0.065 µm MIRRORBIT™ 1000b = 0.065 µm MIRRORBIT™ 1001b = 0.045 µm MIRRORBIT™
(SA) + 0046h	0002h	Erase Suspend 0 = Not supported 1 = Read only 2 = Read and write
(SA) + 0047h	0001h	Sector protect 00 = Not supported X = Number of sectors in smallest group
(SA) + 0048h	0000h	Temporary sector unprotect 00 = Not supported 01 = Supported
(SA) + 0049h	0008h	Sector protect/unprotect scheme 04 = High voltage method 05 = Software command locking method 08 = Advanced sector protection method
(SA) + 004Ah	0000h	Simultaneous operation 00 = Not supported X = Number of banks
(SA) + 004Bh	0000h	Burst mode type 00 = Not supported 01 = Supported
(SA) + 004Ch	0003h	Page mode type 00 = Not supported 01 = 4 word page 02 = 8 word page 03 = 16 word page
(SA) + 004Dh	00B5h	ACC (Acceleration) supply minimum 00 = Not supported D7–D4: Volt D3–D0: 100 mV

Table 15 CFI primary vendor-specific extended query (Continued)

Word address	Data	Description
(SA) + 004Eh	00C5h	ACC (Acceleration) supply maximum 00 = Not supported D7–D4: Volt D3–D0: 100 mV
(SA) + 004Fh	0005h (Top)	WP# protection 00h = Flash device without WP protect (No boot) 01h = Eight 8 KB sectors at top and bottom with WP (Dual boot) 02h = Bottom boot device with WP protect (Bottom boot) 03h = Top boot device with WP protect (Top boot) 04h = Uniform, bottom WP protect (Uniform bottom boot) 05h = Uniform, top WP protect (Uniform top boot) 06h = WP protect for all sectors 07h = Uniform, top or bottom WP protect
(SA) + 0050h	0001h	Program Suspend 00 = Not supported 01 = Supported
(SA) +0051h	0002h	Unlock Bypass 00 = Not supported 01 =Supported
(SA) + 0052h	0009h	Secured silicon sector (Customer OTP Area) size 2^N (bytes)
(SA) + 0053h	008Fh	Software features bit 0: status register polling (1 = Supported, 0 = Not supported) bit 1: DQ polling (1 = Supported, 0 = Not supported) bit 2: new program suspend/resume commands (1 = Supported, 0 = Not supported) bit 3: word programming (1 = Supported, 0 = Not supported) bit 4: bit-field programming (1 = Supported, 0 = Not supported) bit 5: autodetect programming (1 = Supported, 0 = Not supported) bit 6: RFU bit 7: multiple writes per Line (1 = Supported, 0 = Not supported)
(SA) + 0054h	0005h	Page size = 2^N bytes
(SA) + 0055h	0006h	Erase suspend timeout maximum < 2^N (µs)
(SA) + 0056h	0006h	Program suspend timeout maximum < 2^N (µs)
(SA) + 0057h to (SA) + 0077h	FFFFh	Reserved
(SA) + 0078h	0006h	Embedded hardware reset timeout maximum < 2^N (µs) Reset with reset pin
(SA) + 0079h	0009h	Non-embedded hardware reset timeout maximum < 2^N (µs) Power-on-reset

9 Physical dimensions

9.1 LSH064 — 64-ball fortified ball grid array, 13 x 11 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.40
A1	0.40	-	-
D	13.00 BSC		
E	11.00 BSC		
D1	7.00 BSC		
E1	7.00 BSC		
MD	8		
ME	8		
N	64		
⌀ b	0.50	0.60	0.70
eD	1.00 BSC		
eE	1.00 BSC		
SD	0.50 BSC		
SE	0.50 BSC		

NOTES:

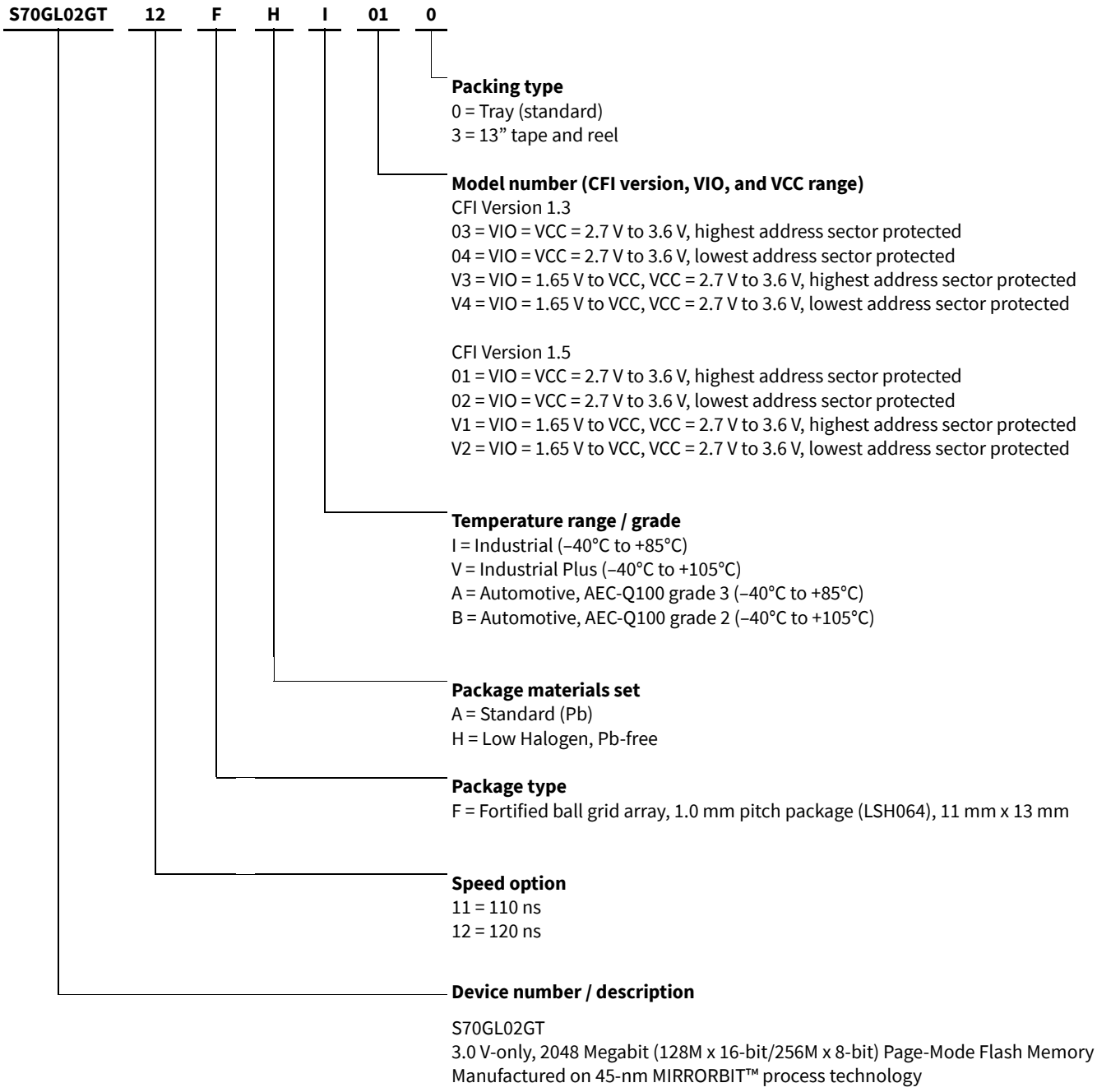
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13243 **

Figure 3 64-ball FBGA (13.0 × 11.0 × 1.4 mm) package outline, 002-13243

10 Ordering information

The ordering part number is formed by a valid combination of the following:



10.1 Recommended combinations

Table 16 lists various configurations planned to be available in volume. This table will be updated when new combinations are released. Check with your local Infineon sales representative to confirm availability of specific configurations not listed here or to check on newly released combinations.

10.1.1 Valid combinations – standard grade

Table 16 S29GL-T valid combinations

Base OPN	Speed (ns)	Package and temperature	Model number	Packing type	Ordering part number (x = Packing type)
S70GL02GT	110	FHI, FHV, FAI[26]	01	0, 3[27]	S70GL02GT11FHI01x S70GL02GT11FHV01x S70GL02GT11FAI01x
			02		S70GL02GT11FHI02x
					S70GL02GT11FAI02x
					S70GL02GT11FHV02x
			03		S70GL02GT11FAI03x
			04		S70GL02GT11FAI04x
	120		V1		S70GL02GT12FHIV1x S70GL02GT12FHVV1x
			V2		S70GL02GT12FHIV2x
					S70GL02GT12FHVV2x

Note
26.BGA package marking omits leading “S70” and packing type designator from ordering part number.
27.Packing type “0” is standard option.

10.1.2 Valid combinations – automotive grade / AEC-Q100

Table 17 lists configurations that are automotive grade/AEC-Q100 qualified and are planned to be available in volume. This table will be updated when new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production part approval process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements. AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 17 S29GL-T valid combinations

Base OPN	Speed (ns)	Package and temperature	Model number	Packing type	Ordering part number (x = Packing type)
S70GL02GT	110	FHA, FHB[28]	01	0, 3[29]	S70GL02GT11FHA01x S70GL02GT11FHB01x
			02		S70GL02GT11FHA02x
					S70GL02GT11FHB02x
	120		V1		S70GL02GT12FHAV1x S70GL02GT12FHBV1x
			V2		S70GL02GT12FHAV2x
					S70GL02GT12FHBV2x

Note
28.BGA package marking omits leading “S70” and packing type designator from ordering part number.
29.Packing type “0” is standard option.

Revision history

Document revision	Date	Description of changes
**	2016-08-26	Initial release.
*A	2016-10-21	Updated **Electrical specifications**: Updated **BGA package capacitance**: Updated **Table 7**. Added **Thermal resistance**. Added **Data integrity**. Added “Other resources”.
*B	2017-03-16	Updated **Ordering information**: Updated **Recommended combinations**: Updated description. Added 02, V2 model number combinations related information. Added **Valid combinations – standard grade**. Added **Valid combinations – automotive grade / AEC-Q100**. Updated to new template.
*C	2017-04-05	Updated **Ordering information**: Updated **Recommended combinations**: Updated **Valid combinations – standard grade**: Updated **Table 16**. Updated **Valid combinations – automotive grade / AEC-Q100**: Updated **Table 17**. Updated to new template.
*D	2017-11-02	Updated **Ordering information**: Updated **Recommended combinations**: Updated **Valid combinations – standard grade**: Added 03, 04 model number combinations related information. Updated **Table 16**.
*E	2018-02-13	Updated **Electrical specifications**: Updated **DC characteristics**: Updated **Table 6**. Updated to new template.
*F	2022-08-22	Updated Document Title to read as “S70GL02T, 2 Gb (256 MB) GL-T MIRRORBIT™ Flash Parallel, 3.0 V”. Replaced “MirrorBit® Eclipse” with “MIRRORBIT™” in all instances across the document. Updated **General description**: Replaced “fast page access time of 25 ns” with “fast page access time of 20 ns”. Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 8**. Removed “Other resources”. Migrated to Infineon template.