1 Gbit, 1.8 V Dual-Quad Serial Peripheral Interface with Multi-I/O Flash

Features

- Density
  - 1 Gb (128 MB)

- SPI with multi-I/O
  - SPI clock polarity and phase modes 0 and 3
  - DDR option
  - Extended addressing – 24 or 32-bit address options

- Read
  - Commands: Normal, Fast Quad I/O, DDR Quad I/O
  - Modes: Burst Wrap, Continuous (XIP), QPI
  - Serial flash discoverable parameters (SFDP) and common flash interface (CFI), for configuration information

- Program
  - 256 or 512 bytes page programming buffer per die
  - Program suspend and resume
  - Automatic error correction code (ECC) – internal hardware ECC with single bit error correction

- Erase
  - Hybrid sector option
    - Physical set of eight 8 KB sectors and one 448 KB sector at the top or bottom of address space with all remaining sectors of 512 KB per die
  - Uniform sector option
    - Uniform 512-KB blocks
  - Erase suspend and resume
  - Erase status evaluation

- Cycling endurance
  - 100,000 program-erase cycles, minimum

- Data retention
  - 20 year data retention, minimum

- Security features
  - OTP array of 2048 bytes
  - Block protection:
    - Status Register bits to control protection against program or erase of a contiguous range of sectors.
    - Hardware and software control options
  - Advanced sector protection (ASP)
    - Individual sector protection controlled by boot code or password
    - Option for password control of read access

- Technology
  - 65-nm MIRRORBIT™ technology with Eclipse architecture

- Supply voltage
  - 1.7 V to 2.0 V

Logic block diagram

- Temperature range / grade
  - Automotive, AEC-Q100 Grade 2 (−40°C to +105°C)
- Packages (all Pb-free)
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (ZSA024) footprint

Logic block diagram
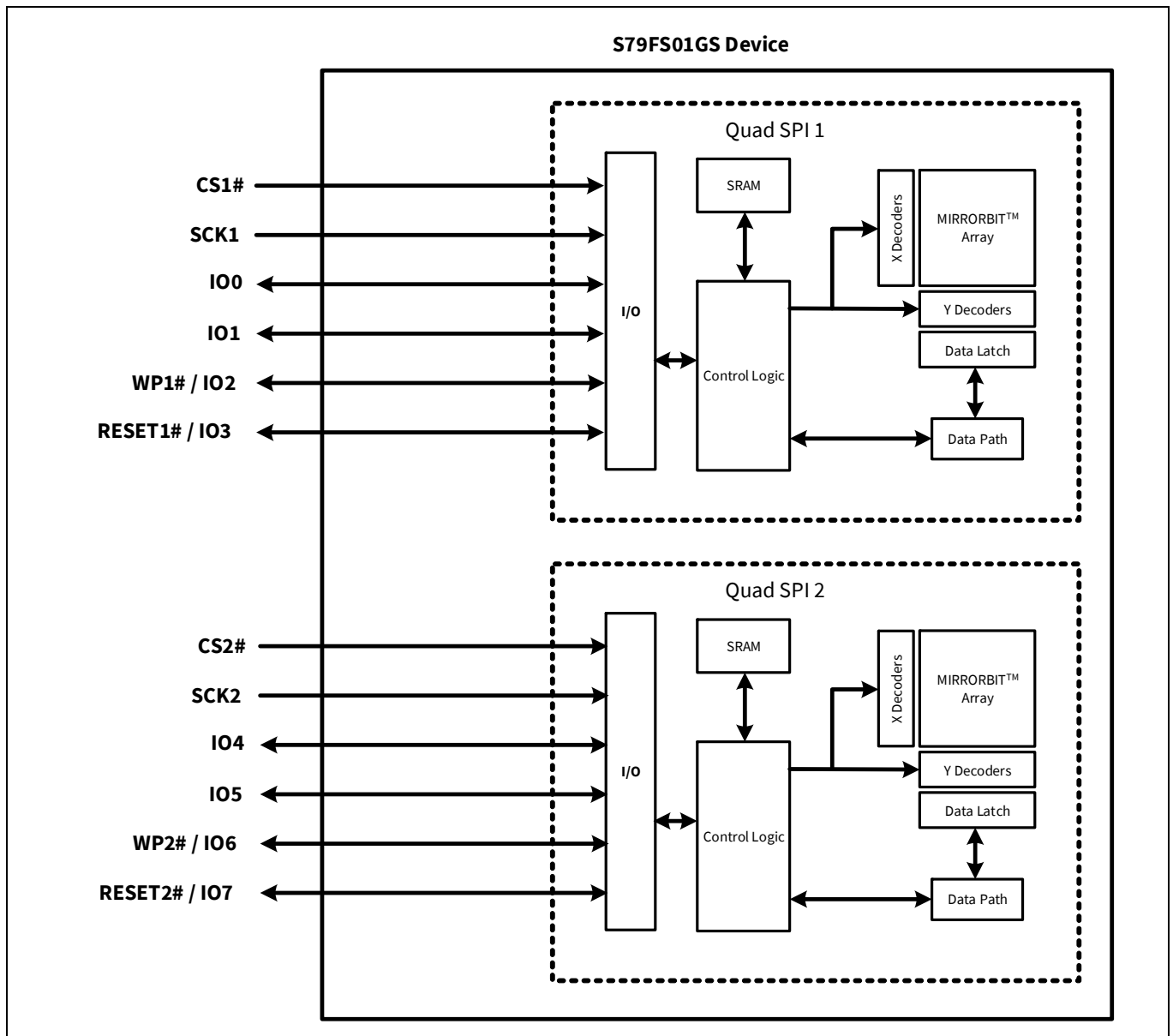
Performance summary

Maximum read rates

Command	Clock rate (MHz)	MBps
Read	50	12.5
Fast read	133	33
Quad read	133	133
DDR quad I/O read	102	204

Typical program and erase rates

Operation	KBps
Page programming (512 bytes page buffer)	1424
Page programming (1024 bytes page buffer)	2160
8 KB physical sector erase (hybrid sector)	56
512 KB sector erase (uniform logical sector)	500

Typical current consumption

Operation	Current (mA)
Serial read 50 MHz	20
Serial read 133 MHz	50
Quad read 133 MHz	120
Quad DDR read 102 MHz	140
Program	120
Erase	120
Standby	0.050
Deep power down (DPD)	0.016

Table of contents

1 Overview

1.1 General description

This document contains information for the S79FS01GS flash memory device constructed from two S25FS512S devices. Specifications contained in this datasheet supersede those in the S25FS512S datasheet. The maximum DDR clock rate was increased from 80 MHz to 102 MHz.

The S79FS01GS Dual-Quad SPI device uses the industry standard single bit SPI using two Quad SPI devices in each package (Quad SPI-1 and Quad SPI-2). This interface is called Dual-Quad and enables support of byte wide (8 bit) serial transfers.

2 SPI with multiple input / output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S79FS01GS uses the industry standard single bit SPI and also supports optional extension commands for two-bit (Dual) and four-bit (Quad) wide serial transfers. This multiple width interface is called SPI multi-I/O or SPI-MIO.

3 Signal description

3.1 Input/Output summary

Table 1   Dual-Quad SPI input/output description

Signal name	Type	Description
SCK1	Input	**Serial Clock for Quad SPI-1**
SCK2	Input	**Serial Clock for Quad SPI-2**
CS1#	Input	**Chip Select for Quad SPI-1**
CS2#	Input	**Chip Select for Quad SPI-2**
IO0	I/O	**I/O 0 for Quad SPI-1**
IO1	I/O	**I/O 1 for Quad SPI-1**
WP1# / IO2	I/O	**I/O 2 for Quad SPI-1 / Write Protect for Quad SPI-1**
RESET1# / IO3	I/O	**I/O 3 for Quad SPI-1 / RESET# for Quad SPI-1**
IO4	I/O	**I/O 0 for Quad SPI-2**
IO5	I/O	**I/O 1 for Quad SPI-2**
WP2# / IO6	I/O	**I/O 2 for Quad SPI-2 / Write Protect for Quad SPI-2**
RESET2# / IO7	I/O	**I/O 3 for Quad SPI-2 / RESET# for Quad SPI-2**
V_{CC}	Supply	**Core Power Supply**
V_{SS}	Supply	**Ground**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a PCB. However, any signal connected to a NC pin must not have voltage levels higher than the V_{CC} absolute maximum on page 1 (Supply Voltage).
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

3.2 Multiple Input / Output (Dual-Quad)

Quad Input / Output (I/O) commands send instructions to the memory only on the IO0 (Quad SPI-1) and IO4 (Quad SPI-2) signals. Address is sent from the host to the memory as four bit (nibble) on IO0, IO1, IO2, IO3 (Quad SPI-1)and repeated on IO4, IO5, IO6, IO7 (Quad SPI-2). Data is sent and returned to the host as bytes on IO0–IO7.

3.3 Serial Clock (SCK1, SCK2)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands, and after every edge in DDR commands.

3.4 Chip Select (CS1#, CS2#)

The Chip Select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic HIGH state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Write-In-Progress bit (SR1V[1]) set to '1', until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic LOW state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

3.5 Serial Input (IO0, IO4)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

Input and output during Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.6 Serial Output (IO1, IO5)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

Input and output during Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.7 Write Protect (WP1#, WP2#) / (IO2, IO6)

When WP# is driven LOW (V_{IL}), during a WRR or WRAR command and while the Status Register Write Disable (SRWD_NV) bit of Status Register 1 (SR1NV[7]) is set to '1', it is not possible to write to Status Register 1 or Configuration Register 1 related registers. In this situation, a WRR command is ignored, a WRAR command selecting SR1NV, SR1V, CR1NV, or CR1V is ignored, and no error is set.

This prevents any alteration of the Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Block Protection feature are also hardware protected against data modification if WP# is LOW during a WRR or WRAR command with SRWD_NV set to '1'.

The WP# function is not available when the Quad mode is enabled (CR1V[1] = 1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode or protection.

3.8   IO3, IO7 / RESET1#, RESET2#

(IO3, IO7) is used for input and output during Quad mode (CR1V[1] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The (IO3, IO7 / RESET1#, RESET2#) signal may also be used to initiate the hardware reset function when the reset feature is enabled by writing Configuration Register 2 non-volatile bit 5 (CR2V[5] = 1). The input is only treated as RESET# when the device is not in Quad-I/O mode, CR1V[1] = 0, or when CS# is HIGH. When Quad I/O mode is in use, CR1V[1] = 1, and the device is selected with CS# LOW, the (IO3, IO7 / RESET1#, RESET2#) is used only as (IO3, IO7) for information transfer. When CS# is HIGH, the (IO3, IO7 / RESET1#, RESET2#) is not in use for information transfer and is used as the RESET# input. By conditioning the reset operation on CS# HIGH during Quad mode, the reset function remains available during Quad mode.

When the system enters a reset condition, the CS# signal must be driven HIGH as part of the reset process and the (IO3, IO7 / RESET1#, RESET2#) signal is driven LOW. When CS# goes HIGH the (IO3, IO7 / RESET1#, RESET2#) input transitions from being (IO3, IO7) to being the RESET# input. The reset condition is then detected when CS# remains HIGH and the (IO3, IO7 / RESET1#, RESET2#) signal remains LOW for t_{RP}. If a reset is not intended, the system is required to actively drive IO3 / Reset# to HIGH along with CS# being driven HIGH at the end of a transfer of data to the memory. Following transfers of data to the host system, the memory will drive (IO3, IO7) high during t_{CS}. This will ensure that IO3 / Reset is not left floating or being pulled slowly to HIGH by the internal or an external passive pull-up. Thus, an unintended reset is not triggered by the (IO3, IO7 / RESET1#, RESET2#) not being recognized as HIGH before the end of t_{RP}.

The (IO3, IO7 / RESET1#, RESET2#) signal is unused when the reset feature is disabled (CR2V[5] = 0).

The (IO3, IO7 / RESET1#, RESET2#) signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode or the reset function. The internal pull-up will hold (IO3, IO7 / RESET1#, RESET2#) HIGH after the host system has actively driven the signal HIGH and then stops driving the signal.

Note that (IO3, IO7 / RESET1#, RESET2#) cannot be shared by more than one SPI-MIO memory if any of them are operating in Quad I/O mode as (IO3, IO7) being driven to or from one selected memory may look like a reset signal to a second non-selected memory sharing the same (IO3, IO7 / RESET1#, RESET2#) signal.

3.9   Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

3.10   Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.11   Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a PCB.

3.12   Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.13   Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

3.14 Block diagrams
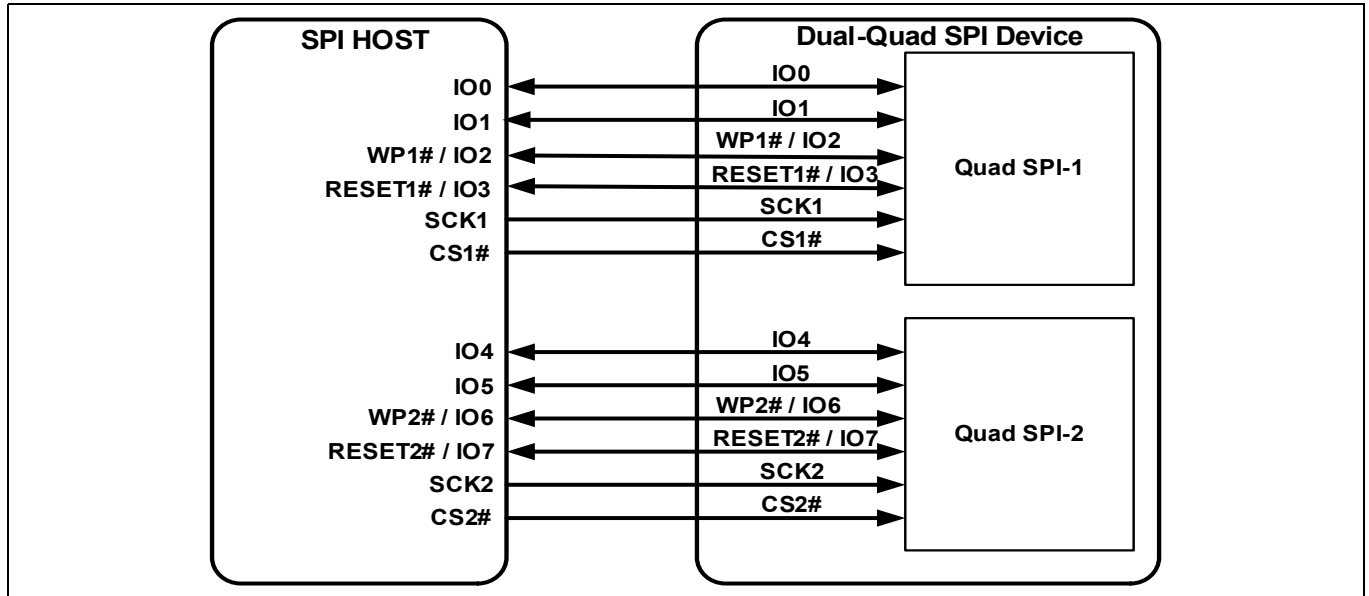
Figure 1 SPI host and Dual-Quad SPI device example 1
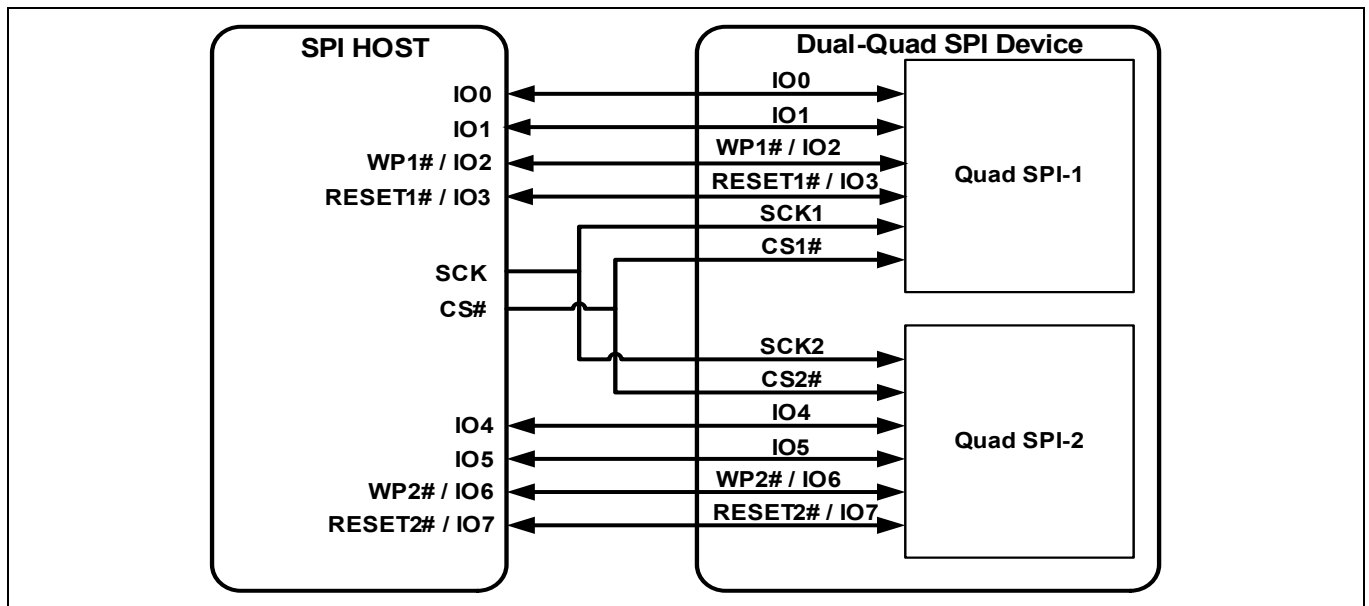
Figure 2 SPI host and Dual-Quad SPI device example 2

4 Signal protocols

4.1 SPI clock modes

4.1.1 Single data rate (SDR)

The S79FS01GS can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0

- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic LOW state with CPOL = 0, CPHA = 0

- SCK will stay at logic HIGH state with CPOL = 1, CPHA = 1
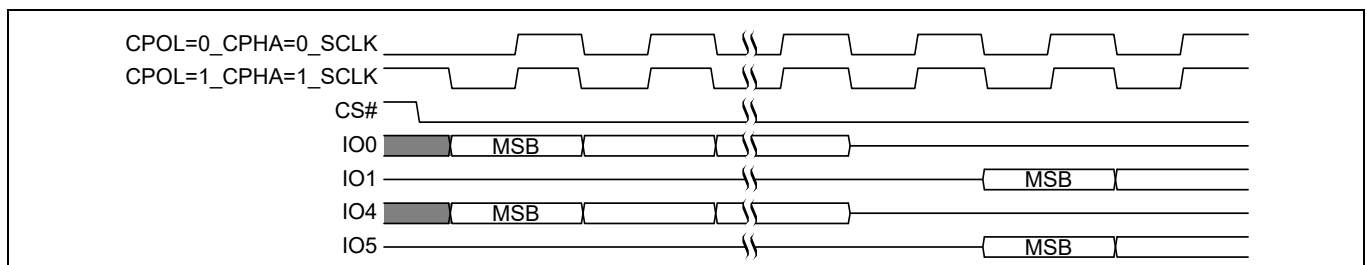
Figure 3   **SPI SDR Modes supported**

Timing diagrams throughout the remainder of the document are generally shown as both Mode 0 and 3 by showing SCK as both HIGH and LOW at the fall of CS#. In some cases, a timing diagram may show only Mode 0 with SCK LOW at the fall of CS#. In such a case, Mode 3 timing simply means clock is HIGH at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for Mode 3.

SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

4.1.2 Double data rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already LOW at the beginning of a command.
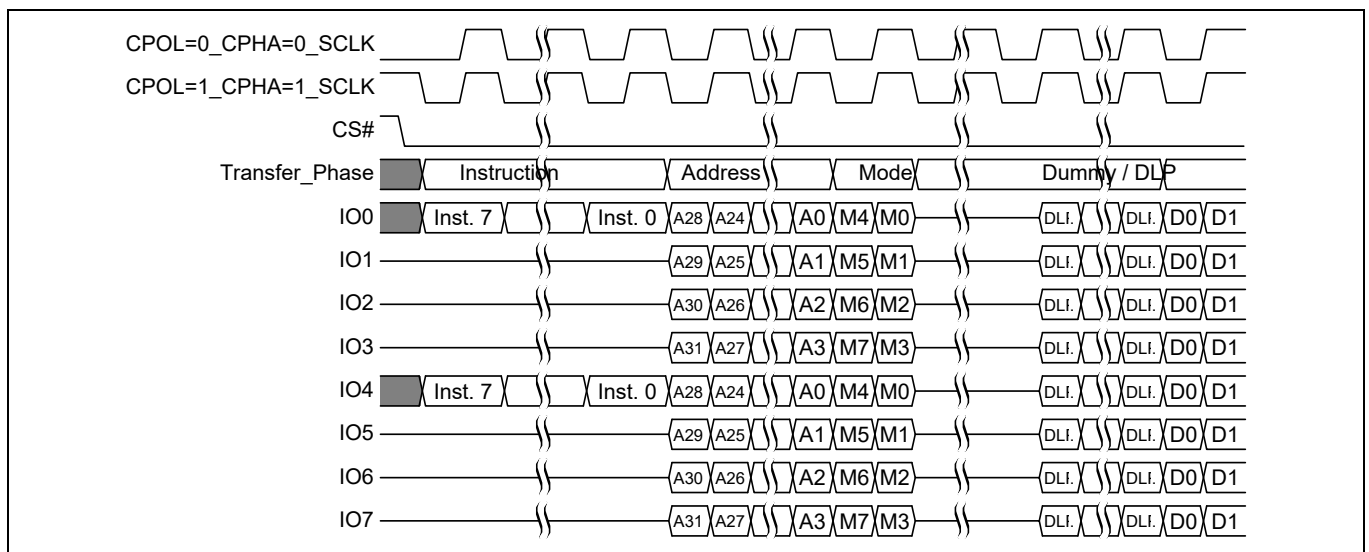
Figure 4   SPI DDR Modes supported

4.2 Command protocol

All communication between the host system and S79FS01GS devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

Quad Input / Output (I/O) commands provide an address sent from the host as four bit (nibble) groups on IO0, IO1, IO2, IO3 and repeated on IO4, IO5, IO6, IO7, then followed by dummy cycles. Data is returned to the host as byte on IO0–IO7. This is referenced as 2-8-8 for Quad I/O command protocols.

QPI commands transfers all instructions and address from the host to the memory as four bit (nibble) groups on IO0, IO1, IO2, IO3 and repeated on IO4, IO5, IO6, IO7. Data is sent and returned to the host as bytes on IO0–IO7. This is referenced as a 8-8-8 command protocol.

Commands are structured as follows:

- Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal LOW throughout a command.

- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.

- Each command begins with an 8-bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (IO0 and IO4) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.

Signal protocols

- The instruction may be standalone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- In QPI mode, the width of all transfers is a 8-bit wide (byte) transfer on the IO0–IO7 signals.

- Quad I/O read instructions send an instruction modifier called Continuous Read mode bits, following the address, to indicate whether the next command will be of the same type with an implied, rather than an explicit, instruction. These mode bits initiate or end the continuous read mode. In Continuous Read mode, the next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the IO0 and IO4 or Serial Output (IO1 and IO5) signals, they may be done in 4-bit groups per (quad) transfer on the IO0–IO3 signals. Within the quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.

- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.

- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal HIGH. The CS# signal can be driven HIGH after any transfer in the read data sequence. This will terminate the command.

- At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a standalone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of clock cycles after CS# signal was driven LOW is an exact multiple of eight cycles. If the CS# signal does not go HIGH exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.

- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.

- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.

- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

4.2.1 Command sequence examples
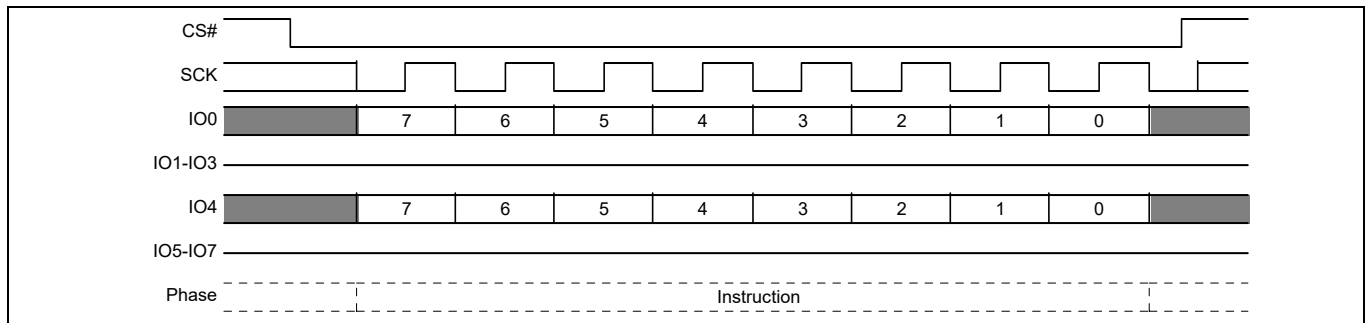
Figure 5   **Dual-Quad Standalone Instruction command**[1]
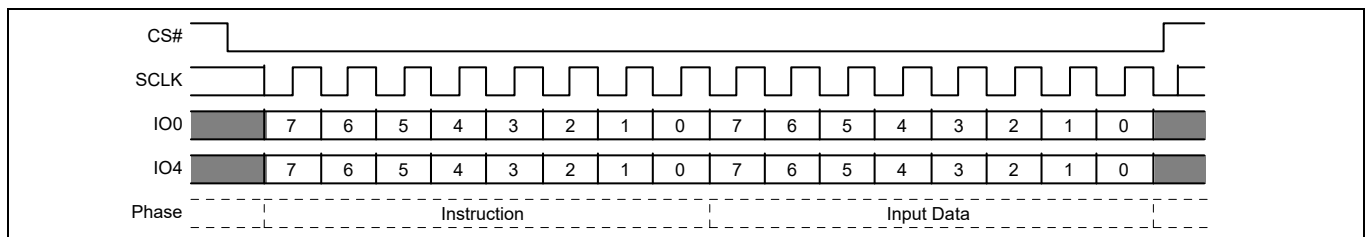
Figure 6   **Dual-Quad Single Bit Wide Input command**[1]
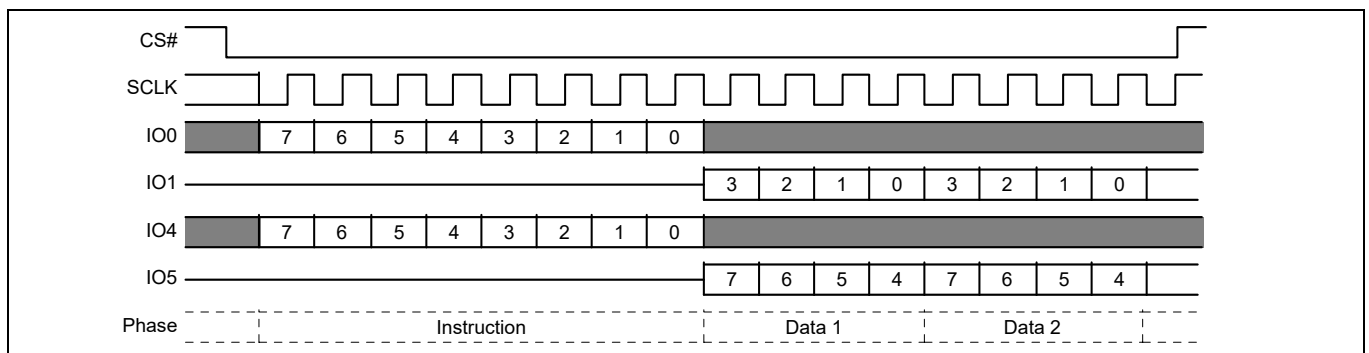
Figure 7   **Dual-Quad Single Bit Wide I/O command without latency**[1]

Note
1. Instruction needs to be the same for both IO0 (Quad SPI-1) and IO4 (Quad SPI-2).

Signal protocols
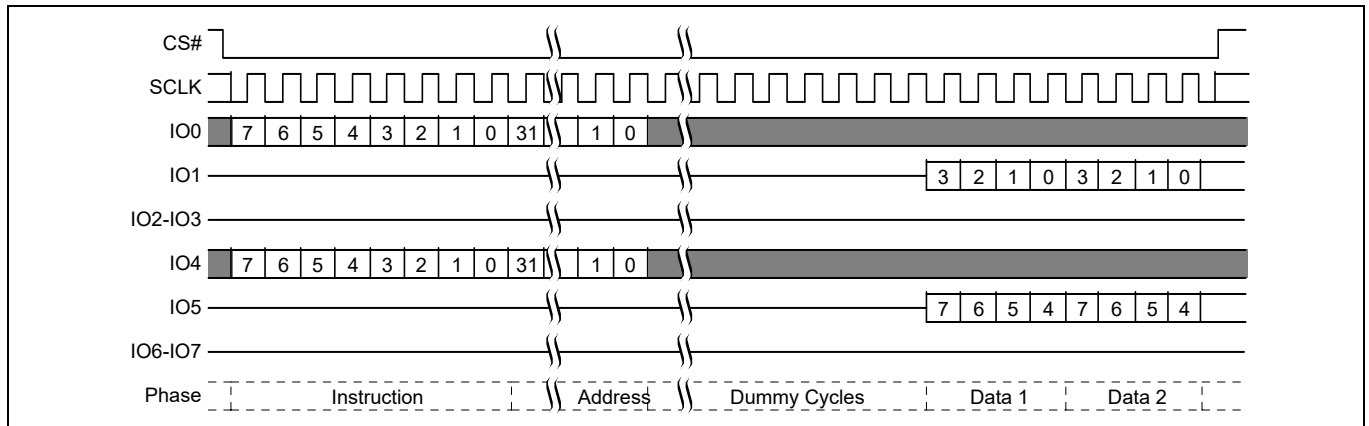
Figure 8   **Dual-Quad Single Bit Wide I/O command with latency**[2]
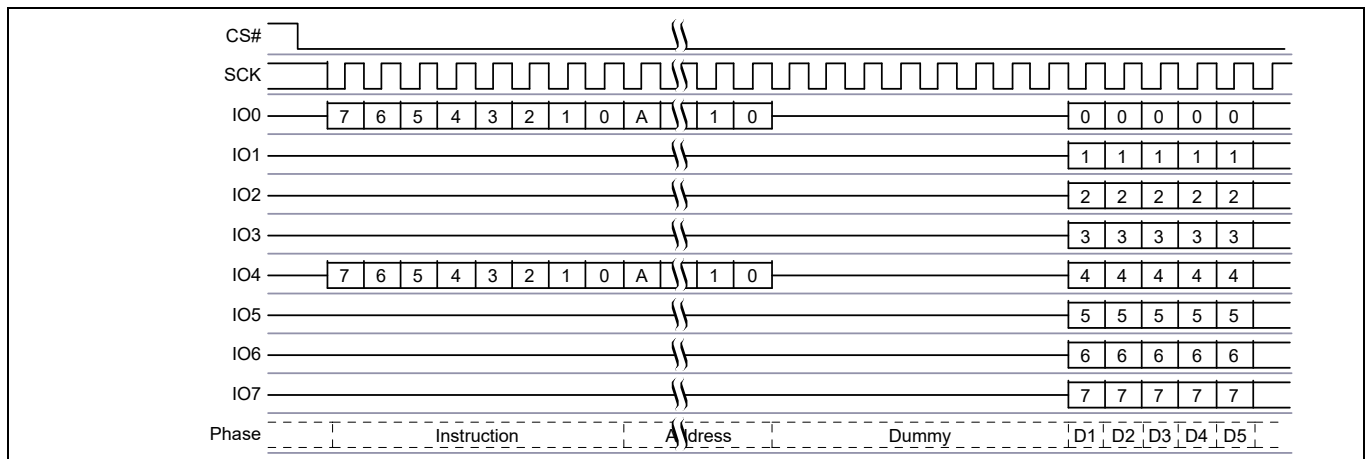
Figure 9   **Dual-Quad, Quad Output Read command**[3]

Notes
2. Instruction needs to be the same for both IO0 (Quad SPI-1) and IO4 (Quad SPI-2).
3. A = MSB of address = 23 for 3-byte address, or 31 for 4-byte address.

Signal protocols
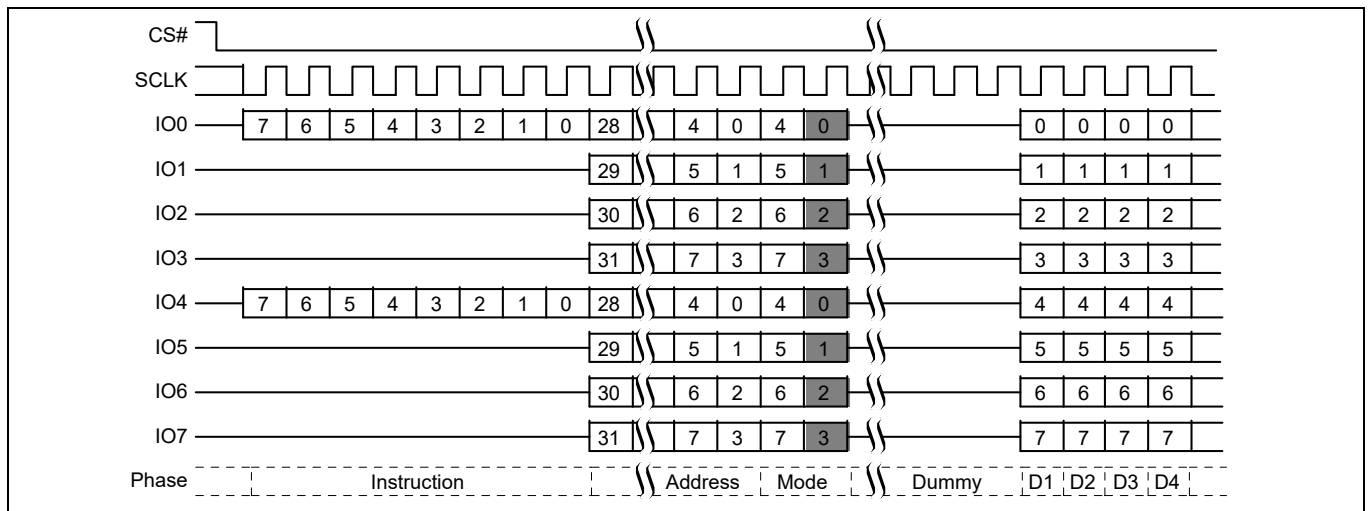
Figure 10   Dual-Quad, Quad I/O command[4, 5]
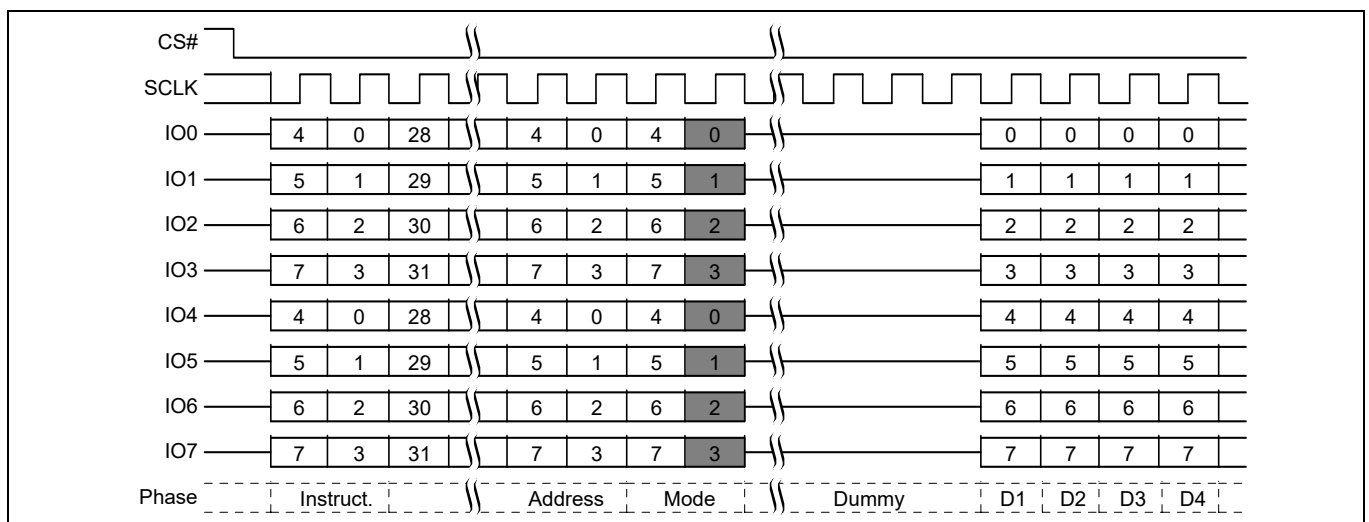
Figure 11   Dual-Quad SPI, Quad I/O Read command in QPI Mode[4, 5]

Notes
4. Instruction, Address, and Mode bits needs to be the same for both IO0–IO3 (Quad SPI-1) and IO4–IO7 (Quad SPI-2).
5. The gray bits are optional, the host does not have to drive bits during that cycle.

Signal protocols
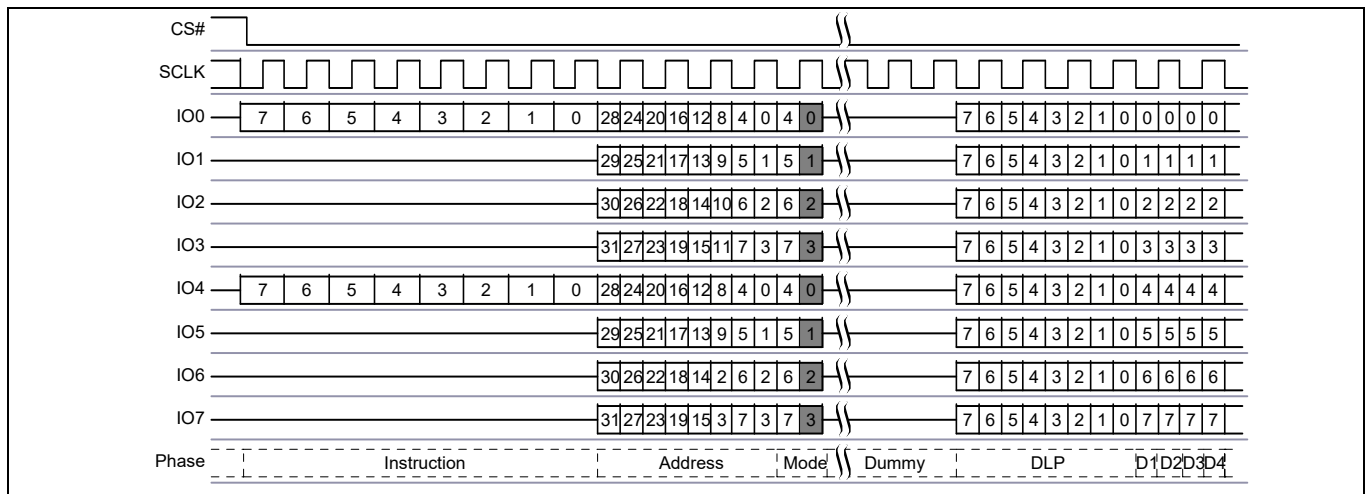
Figure 12   Dual-Quad DDR Quad I/O Read command[6, 7]
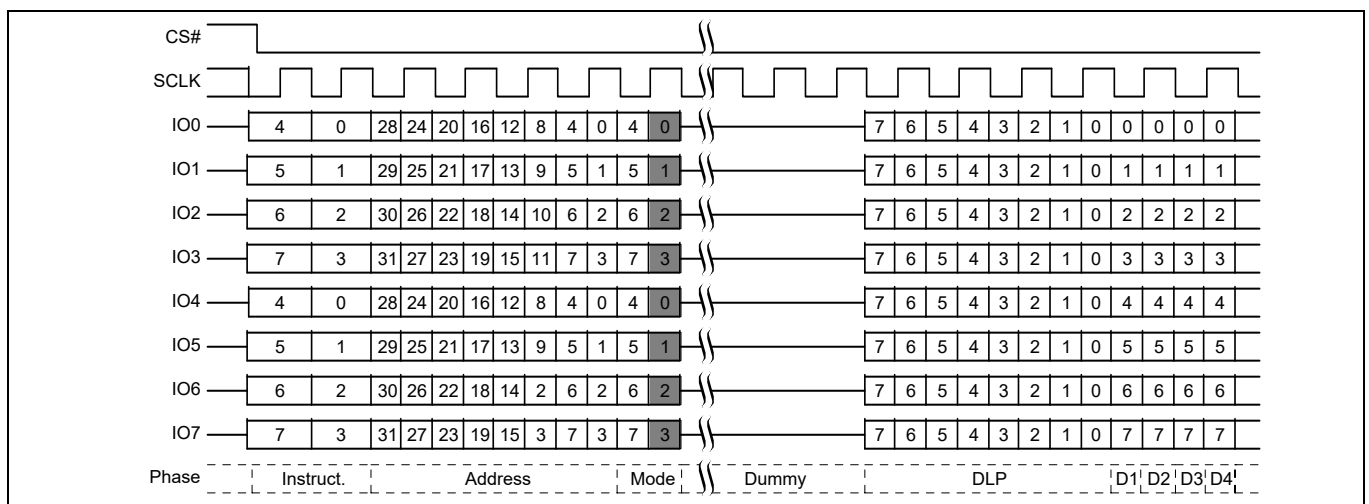
Figure 13   Dual-Quad SPI DDR Quad I/O Read command QPI Mode[6, 7]

Additional sequence diagrams, specific to each command, are provided in **"Commands"** on page 80.

Notes

6. Instruction, Address, and Mode bits needs to be the same for both IO0–IO3 (Quad SPI-1) and IO4–IO7 (Quad SPI-2).
7. The gray bits are optional, the host does not have to drive bits during that cycle.

Signal protocols

4.3 Interface states

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 2 **Interface states summary**

Interface state	V_{CC}	SCK1 SCK2	CS1# CS2#	RESET1# / IO3 RESET2# / IO7	WP# / IO2 WP2# / IO6	IO1, IO5	IO0, IO4
Power-Off	<V_{CC}(low)	X	X	X	X	Z	X
Low Power Hardware Data Protection	<V_{CC}(cut-off)	X	X	X	X	Z	X
Power-On (Cold) Reset	≥V_{CC}(min)	X	HH	X	X	Z	X
Hardware (Warm) Reset Non-Quad Mode	≥V_{CC}(min)	X	X	HL	X	Z	X
Hardware (Warm) Reset Quad Mode	≥V_{CC}(min)	X	HH	HL	X	Z	X
Interface Standby	≥V_{CC}(min)	X	HH	X	X	Z	X
Instruction Cycle (Legacy SPI)	≥V_{CC}(min)	HT	HL	HH	HV	Z	HV
Single Input Cycle Host to Memory Transfer	≥V_{CC}(min)	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥V_{CC}(min)	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥V_{CC}(min)	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥V_{CC}(min)	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥V_{CC}(min)	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥V_{CC}(min)	HT	HL	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥V_{CC}(min)	HT	HL	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥V_{CC}(min)	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥V_{CC}(min)	HT	HL	MV	MV	MV	MV
DDR Quad Input Cycle Host to Memory Transfer	≥V_{CC}(min)	HT	HL	HV	HV	HV	HV
DDR Latency (Dummy) Cycle	≥V_{CC}(min)	HT	HL	MV or Z	MV or Z	MV or Z	MV or Z
DDR Quad Output Cycle Memory to Host Transfer	≥V_{CC}(min)	HT	HL	MV	MV	MV	MV

Legend

Z = No driver – floating signal

HL = Host driving V_{IL}

HH = Host driving V_{IH}

HV = Either HL or HH

X = HL or HH or Z

HT = Toggling between HL and HH

ML = Memory driving V_{IL}

MH = Memory driving V_{IH}

MV = Either ML or MH

4.3.1 Power-off

When the core supply voltage is at or below the $V_{CC (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

4.3.2 Low power hardware data protection

When V_{CC} is less than $V_{CC (cut-off)}$, the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.3.3 Power-on (cold) reset

When the core voltage supply remains at or below the $V_{CC (low)}$ voltage for ≥ t_{PD} time, then rises to ≥ $V_{CC (minimum)}$ the device will begin its power-on reset (POR) process. POR continues until the end of t_{PU}. During t_{PU}, the device does not react to external input signals nor drive any outputs. Following the end of t_{PU} the device transitions to the Interface Standby state and can accept commands. For additional information on POR, see

4.3.4 Hardware (warm) reset

A configuration option is provided to allow IO3 to be used as a hardware reset input when the device is not in Quad mode or when it is in Quad mode and CS# is HIGH. When IO3 / RESET# is driven LOW for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands.

4.3.5 Interface Standby

When CS# is HIGH, the SPI interface is in Standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes LOW to begin a new command.

While in interface Standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

A DPD mode is supported by the S79FS01GS devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being cleared to '0' (SR1V[0] = 0). While in DPD mode the device ignores all commands except the Release from DPD (RES ABh) command, that will return the device to the Interface Standby state after a delay of t_{RES}.

4.3.6 Instruction cycle (legacy SPI mode)

When the host drives the MSb of an instruction and CS# goes LOW, on the next rising edge of SCK the device captures the MSb of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# LOW, and drives the Write Protect (WP#) and IO3/RESET signals as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR or WRAR command and is otherwise ignored. IO3 / RESET# is driven HIGH when the device is not in Quad Mode (CR1V[1] = 0) or QPI Mode (CR2V[6] = 0) and hardware reset is not required.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual I/O, Quad I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are standalone, needing no address or data transfer to or from the memory. The host returns CS# HIGH after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

4.3.7   Instruction cycle (QPI mode)

In QPI mode, when CR2V[6] = 1, instructions are transferred 4 bits per cycle. In this mode instruction cycles are the same as a Quad Input Cycle (See **"Quad input cycle — Host to Memory transfer"** on page 21).

4.3.8   Single input cycle — Host to Memory transfer

Several commands transfer information after the instruction on the single serial input (IO0 and IO5) signal from host to the memory device. The host keeps RESET# HIGH, CS# LOW, and drives IO0 and IO4 as needed for the command. The memory does not drive the Serial Output (IO1 and IO5) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output cycle states.

4.3.9   Single latency (dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the latency code in the Configuration Register (CR2V[3:0]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The host may drive the IO0 and IO4 signal during these cycles or the host may leave IO0 and IO4 floating. The memory does not use any data driven on IO0 and IO4 or other I/O signals during the latency cycles. The memory does not drive the Serial Output (IO1 and IO5) or I/O signals during the latency cycles.

The next interface state depends on the command structure, i.e., the number of latency cycles, and whether the read is single, dual, or quad width.

4.3.10   Single output cycle — Memory to Host transfer

Several commands transfer information back to the host on the single Serial Output (IO1 and IO5) signal. The host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (IO0 and IO4) signal. The memory drives IO1 and IO5 with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to HIGH ending the command.

4.3.11   Quad input cycle — Host to Memory transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. In QPI mode, the Quad I/O Read and Page Program commands transfer four data bits to the memory in each cycle, including the instruction cycles. The host keeps CS# LOW, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For QPI mode Page Program, the host returns CS# HIGH following the delivery of data to be programmed and the interface returns to standby state.

4.3.12   Quad latency (dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the latency code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps CS# LOW. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

4.3.13   Quad output cycle — Memory to Host transfer

The Quad I/O Read returns data to the host four bits in each cycle. The host keeps CS# LOW. The memory drives data on IO0–IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to HIGH ending the command.

4.3.14   DDR Quad input cycle — Host to Memory transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state following the delivery of address and mode bits is a DDR latency cycle.

4.3.15   DDR latency cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the latency code in the Configuration Register (CR2V[3:0]). During the latency cycles, the host keeps CS# LOW. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last four latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than four cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Single, or Quad Output Cycle, depending on the instruction.

4.3.16   DDR Quad output cycle — Memory to Host transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to HIGH ending the command.

4.4 Configuration Register effects on the interface

The Configuration Register 2 volatile bits 3 to 0 (CR2V[3:0]) select the variable latency for all array read commands except Read and Read SDFP (RSFDP). Read always has zero latency cycles. RSFDP always has eight latency cycles. The variable latency is also used in the OTPR and RDAR commands.

The Configuration Register bit 1 (CR1V[1]) selects whether Quad mode is enabled to switch WP# to IO2 function, RESET# to IO3 function, and thus allow Quad I/O Read and QPI mode commands. Quad mode must also be selected to allow DDR Quad I/O Read commands.

4.5 Data protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

4.5.1 Power-up

When the core supply voltage is at or below the $V_{CC\,(low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. Program and erase operations continue to be prevented during the POR because no command is accepted until the exit from POR to the Interface Standby state.

4.5.2 Low power

When V_{CC} is less than $V_{CC\,(cut-off)}$, the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.5.3 Clock pulse count

The device verifies that all non-volatile memory and register data modifying commands consist of a clock pulse count that is a multiple of eight bit transfers (byte boundary) before executing them. A command not ending on an 8-bit (byte) boundary is ignored and no error status is set for the command.

4.5.4 DPD

In DPD mode, the device responds only to the Release from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3   Absolute maximum ratings

Storage temperature plastic packages	−65°C to +150°C
Ambient temperature with power applied	−65°C to +150°C
V_{CC}	−0.5 V to +2.5 V
Input voltage with respect to ground (V_{SS})[8]	−0.5 V to V_{CC} + 0.5 V
Output short circuit current[9]	100 mA

5.2 Thermal resistance

Table 4   Thermal resistance

Parameter	Description	Test conditions	ZSA024	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51 with still air (0 m/s).	33	°C/W
Theta JB	Thermal resistance (Junction to board)		12.3	°C/W
Theta JC	Thermal resistance (Junction to case)		11.5	°C/W

5.3 Latchup characteristics

Table 5   Latchup specification[11]

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	−1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	−1.0	V_{CC} + 1.0	V
V_{CC} current	−100	+100	mA

Notes
8. See **"Input signal overshoot"** on page 25 for allowed maximums during signal transition.
9. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
10. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
11. Excludes power supply V_{CC}. Test conditions: V_{CC} = 1.8 V, one connection at a time tested, connections not being tested are at V_{SS}.

5.4 Operating ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

5.4.1 Power supply voltages

Table 6   Power supply voltages

V_{CC}	1.7 V to 2.0 V

5.4.2 Temperature ranges[12]

Table 7   Temperature ranges

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial (I)	−40	+85	°C
		Industrial Plus devices (V)	−40	+105	
		Automotive, AEC-Q100 grade 3 (A)	−40	+85	
		Automotive, AEC-Q100 grade 2 (B)	−40	+105	
		Automotive, AEC-Q100 grade 1 (M)	−40	+125	

5.4.3 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –1.0 V or overshoot to V_{CC} + 1.0 V, for periods up to 20 ns.
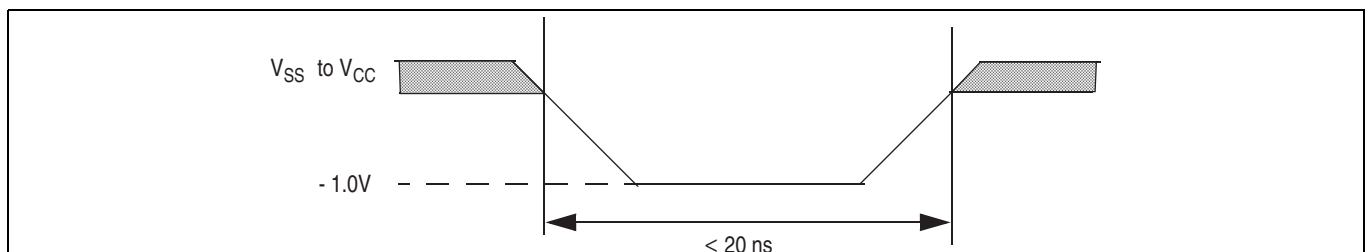
Figure 14   Maximum negative overshoot waveform
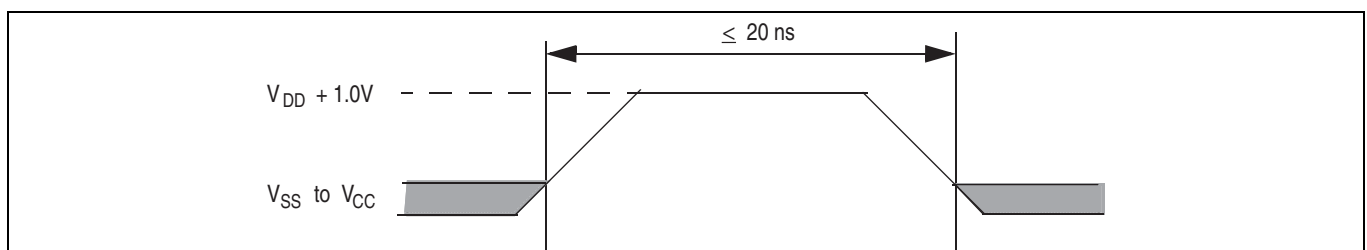
Figure 15   Maximum positive overshoot waveform

Note

12.Industrial Plus operating and performance parameters will be determined by device characterization and may vary from standard industrial temperature range devices as currently shown in this specification.

5.5 Power-up and power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

• V_{CC} (min) at power-up, and then for a further delay of t_{PU}

• V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 16**). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

The device draws I_{POR} during t_{PU}. After power-up (t_{PU}), the device is in Standby mode, draws CMOS standby current (I_{SB}), and the WEL bit is reset.

During power-down or voltage drops below V_{CC}(cut-off), the voltage must drop below V_{CC}(low) for a period of t_{PD} for the part to initialize correctly on power-up (see **Figure 17**). If during a voltage drop the V_{CC} stays above V_{CC}(cut-off) the part will stay initialized and will work correctly when V_{CC} is again above V_{CC}(min). In the event POR did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} supply at the device. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µF).

Table 8   FS-S power-up / power-down voltage and timing

Symbol	Parameter	Min	Max	Unit
V_{CC} (min)	V_{CC} (minimum operation voltage)	1.7	–	V
V_{CC} (cut-off)	V_{CC} (cut 0ff where re-initialization is needed)	1.5	–	V
V_{CC} (low)	V_{CC} (low voltage for initialization to occur)	0.7	–	V
t_{PU}	V_{CC}(min) to Read operation	–	300	µs
t_{PD}	V_{CC}(low) time	10.0	–	µs
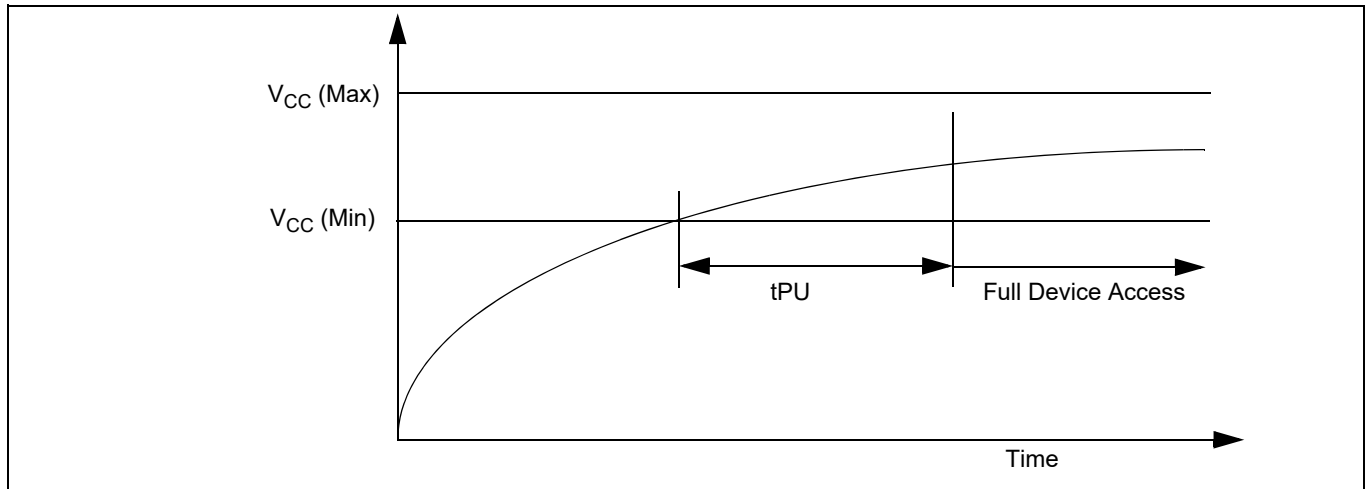
Figure 16   Power-up
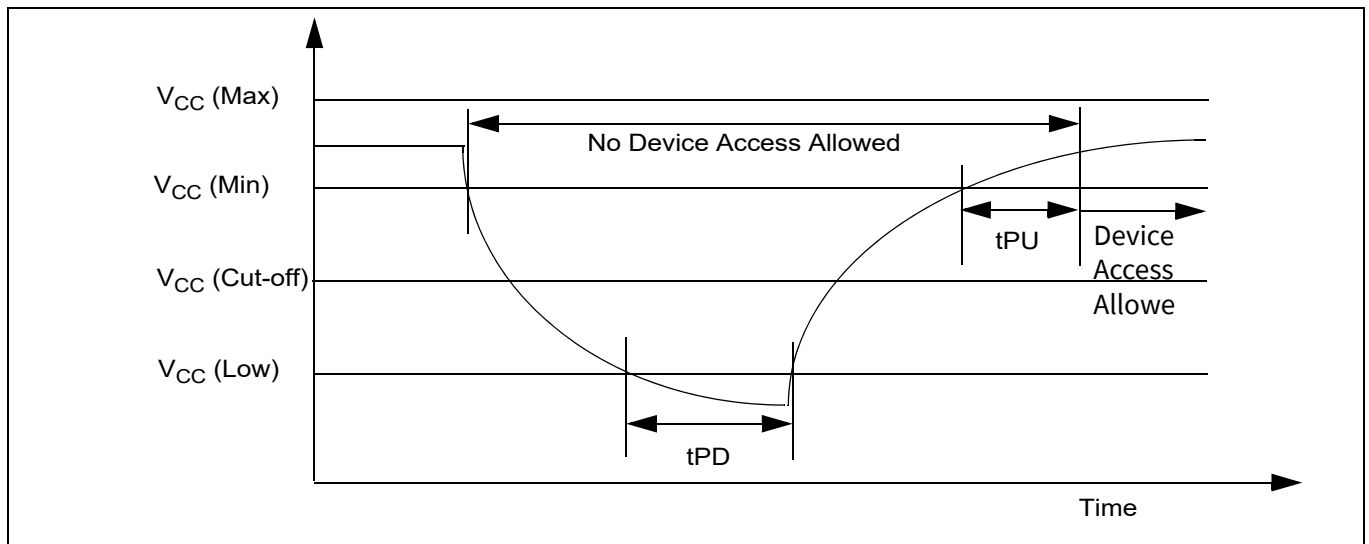
Figure 17   Power-down and voltage drop

6 DC characteristics

Table 9   DC characteristics — operating temperature range −40°C to +105°C

Symbol	Parameter	Test conditions	Min	Typ[13]	Max	Unit
V_{IL}	Input low voltage	–	−0.5	–	$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage	–	$0.7 \times V_{CC}$	–	$V_{CC} + 0.4$	V
V_{OL}	Output low voltage	$I_{OL} = 0.1$ mA	–	–	0.2	V
V_{OH}	Output high voltage	$I_{OH} = -0.1$ mA	$V_{CC} - 0.2$	–	–	V
I_{LI}	Input leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}	–	–	±8	µA
I_{LO}	Output leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}	–	–	±8	µA
I_{CC1}	Active power supply current (READ)[14]	Serial SDR @ 54 MHz Serial SDR @ 133 MHz Quad SDR @ 133 MHz Quad DDR @ 102 MHz	–	20 50 120 140	34 60 130 180	mA
I_{CC2}	Active power supply current (Page program)	CS# = V_{CC}	–	120	200	mA
I_{CC3}	Active power supply current (WRR or WRAR)	CS# = V_{CC}	–	120	200	mA
I_{CC4}	Active power supply current (SE)	CS# = V_{CC}	–	120	200	mA
I_{CC5}	Active power supply current (BE)	CS# = V_{CC}	–	120	200	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}	–	50	600	µA
I_{DPD}	Deep power-down current	IO3 / RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}	–	16	300	µA
I_{POR}	Power on reset current	IO3 / RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}	–	–	160	mA

Notes
13. Typical values are at $T_{AI} = 25°C$ and $V_{CC} = 1.8$ V.
14. Outputs unconnected during read data return. Output switching current is not included.

6.1 Active Power and Standby Power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

6.2 Deep Power Down (DPD) mode

DPD mode is supported by the S79FS01GS devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 Volatile Write In Progress (WIP) bit being cleared to '0' (SR1V[0] = 0). While in DPD mode, the device ignores all commands except the Release from DPD (RES ABh) command, which will return the device to the Interface Standby state after a delay of t_{RES}.

Table 10   Valid Enter DPD mode and Release from DPD mode sequence

Current mode	CS#	SCK	Command	Next mode	Comments
Active	LOW to HIGH	N/A	N/A	Standby	–
Standby	HIGH to LOW	Toggling	B9h Enter DPD	DPD	DPD entered after CS# goes HIGH and after the t_{DPD} duration (see **Table 14**).
DPD	HIGH to LOW	Not Toggling	N/A	DPD	If SCK is toggling and Command is not ABh, device remains in DPD.
		Toggling	Command not ABh		
DPD	HIGH to LOW	Toggling	ABh Release from DPD	Standby	Release from DPD after CS# goes HIGH and after the t_{RES} duration (see **Table 14**). After CS# goes HIGH to start the release from DPD, it is an invalid sequence to have a CS# transition when the SCK is not toggling.

7 Timing specifications

7.1 Key to switching waveforms
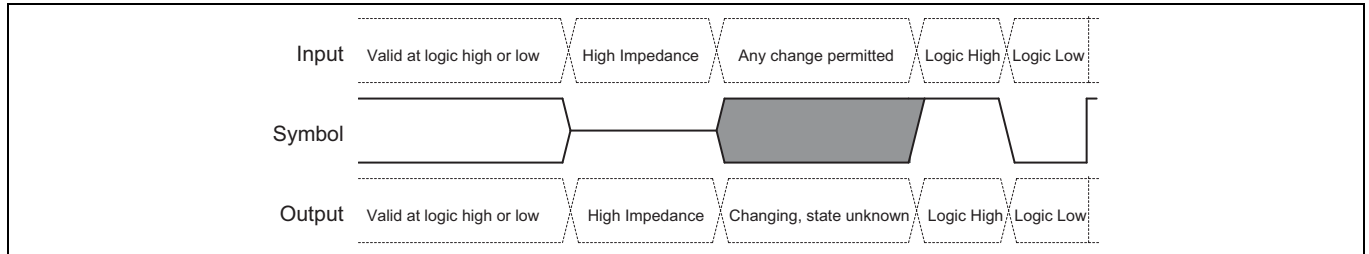
Figure 18   Waveform element meanings

7.2 AC test conditions
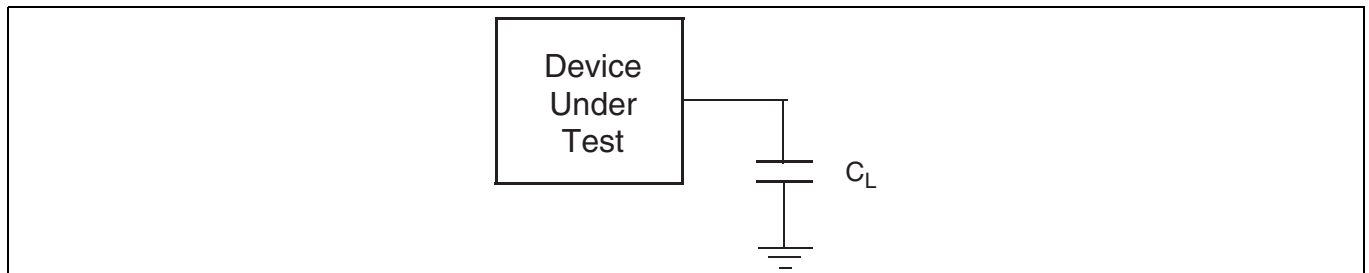
Figure 19   Test setup

Table 11   AC measurement conditions[15, 16]

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	–	30	pF
	Input pulse voltage	$0.2 \times V_{CC}$	$0.8 \times V_{CC}$	V
	Input slew rate	0.23	1.25	V/ns
	Input rise and fall times	0.9	5	ns
	Input timing ref voltage	$0.5 \times V_{CC}$		V
	Output timing ref voltage	$0.5 \times V_{CC}$		V

Notes

15. Input slew rate measured from input pulse min to max at V_{CC} max.
    Example: (1.9 V × 0.8) – (1.9 V × 0.2) = 1.14 V; 1.14 V/1.25 V/ns = 0.9 ns rise or fall time.
16. AC characteristics tables assume clock and data signals have the same slew rate (slope).

Timing specifications

Input Levels   Output Levels

V_{CC} + 0.4V
0.7 x V_{CC} V_{CC} - 0.2V

0.5 x V_{CC} Timing Reference Level

0.3 x V_{CC}
- 0.5V   0.2V
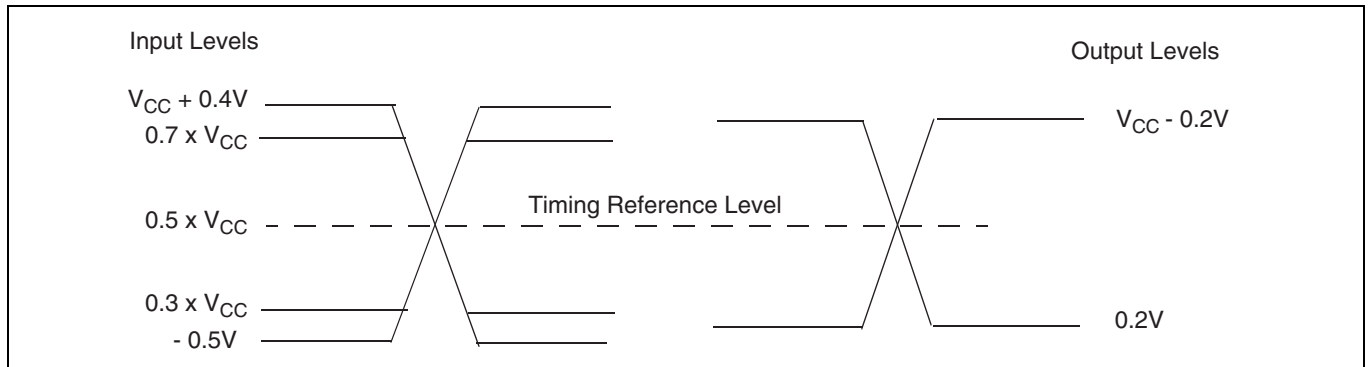
Figure 20   **Input, output, and timing reference levels**

7.2.1   Capacitance characteristics

Table 12   FS512S capacitance[17]

Symbol	Parameter	Test conditions	Min	Max	Unit
C_{IN}	Input capacitance (applies to SCK, CS#, IO3 / RESET#)	1 MHz	–	16	pF
C_{OUT}	Output capacitance (applies to All I/O)	1 MHz	–	16	pF

Note
17. Parameter values are not 100% tested. For more details, please refer to the IBIS models.

7.3 Reset

7.3.1 Power-on (cold) reset

The device executes a POR process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See **Figure 16** and **Table 8**. The device must not be selected (CS# to go HIGH with V_{CC}) during power-up (t_{PU}), i.e. no commands may be sent to the device until the end of t_{PU}.

The IO3 / RESET# signal functions as the RESET# input when CS# is HIGH for more than t_{CS} time or when Quad Mode is not enabled CR1V[1] = 0.

RESET# is ignored during POR. If RESET# is LOW during POR and remains LOW through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RH} after RESET# returns HIGH. RESET# must return HIGH for greater than t_{RS} before returning low to initiate a hardware reset.
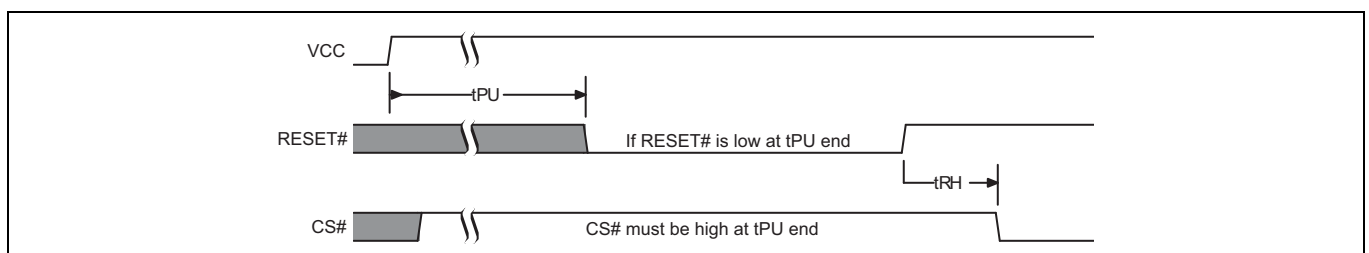
Figure 21   **Reset LOW at the end of POR**
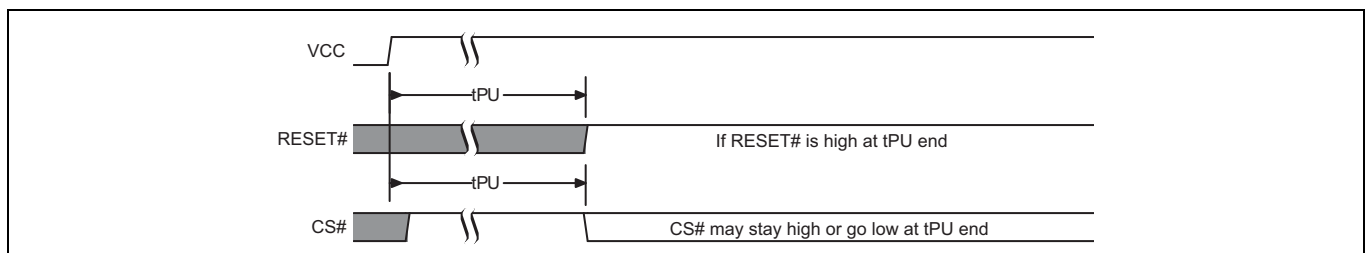
Figure 22   **Reset HIGH at the end of POR**
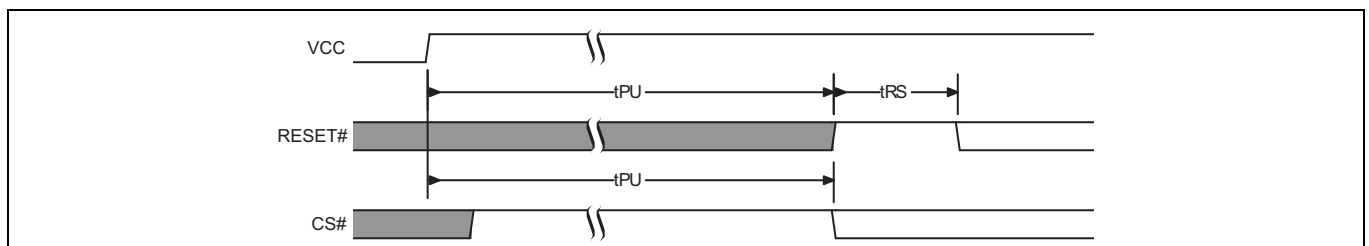
Figure 23   **POR followed by hardware reset**

7.3.2 IO3, IO7 / RESET1#, RESET2# input initiated hardware (warm) reset

The IO3, IO7 / RESET1#, RESET2# signal functions as the RESET# input when CS# is HIGH for more than t_{CS} time or when Quad Mode is not enabled CR1V[1] = 0. The IO3, IO7 / RESET1#, RESET2# input has an internal pull-up to V_{CC} and may be left unconnected if Quad mode is not used. The t_{CS} delay after CS# goes HIGH gives the memory or host system time to drive IO3 high after its use as a Quad mode I/O signal while CS# was LOW. The internal pull-up to V_{CC} will then hold IO3, IO7 / RESET1#, RESET2# HIGH until the host system begins driving IO3, IO7 / RESET1#, RESET2#. The IO3, IO7 / RESET1#, RESET2# input is ignored while CS# remains HIGH during t_{CS}, to avoid an unintended Reset operation. If CS# is driven LOW to start a new command, IO3, IO4 / RESET1#, RESET2# is used as IO3, IO7.

When the device is not in Quad mode or, when CS# is HIGH, and IO3, IO7 / RESET1#, RESET2# transitions from V_{IH} to V_{IL} for > t_{RP}, following t_{CS}, the device will reset register states in the same manner as POR but, does not go through the full reset process that is performed during POR. The hardware reset process requires a period of t_{RPH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

The RESET command is independent of the state of IO3, IO7 / RESET1#, RESET2#. If IO3, IO7 / RESET1#, RESET2# is HIGH or unconnected, and the RESET instruction is issued, the device will perform software reset.

Additional IO3, IO7 / RESET1#, RESET2# Notes:

- IO3, IO7 / RESET1#, RESET2# must be HIGH for t_{RS} following t_{PU} or t_{RPH}, before going LOW again to initiate a hardware reset.

- When IO3, IO7 / RESET1#, RESET2# is driven LOW for at least a minimum period of time (t_{RP}), following t_{CS}, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write commands for the duration of t_{RPH}. The device resets the interface to standby state.

- If Quad mode and the IO3, IO7 / RESET1#, RESET2# feature are enabled, the host system should not drive IO3 LOW during t_{CS}, to avoid driver contention on IO3, IO4. Immediately following commands that transfer data to the host in Quad mode, e.g. Quad I/O Read, the memory drives IO3 / Reset HIGH during t_{CS}, to avoid an unintended Reset operation. Immediately following commands that transfer data to the memory in Quad mode, e.g. Page Program, the host system should drive IO3 / Reset HIGH during t_{CS}, to avoid an unintended Reset operation.

- If Quad mode is not enabled, and if CS# is LOW at the time IO3, IO7 / RESET1#, RESET2# is asserted LOW, CS# must return HIGH during t_{RPH} before it can be asserted LOW again after t_{RH}.

Table 13   Hardware reset parameters[18, 19, 20]

Parameter	Description	Limit	Time	Unit
t_{RS}	Reset setup – prior reset end and RESET# HIGH before RESET# LOW	Min	50	ns
t_{RPH}	Reset pulse hold – RESET# LOW to CS# LOW	Min	35	µs
t_{RP}	RESET# pulse width	Min	200	ns
t_{RH}	Reset hold – RESET# HIGH before CS# LOW	Min	50	ns

Notes
18. IO3, IO7 / RESET1#, RESET2# LOW is ignored during power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the Reset state and t_{RH} will determine when CS# may go LOW.
19. If Quad mode is enabled, IO3 / RESET# LOW is ignored during t_{CS}.
20. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

Timing specifications
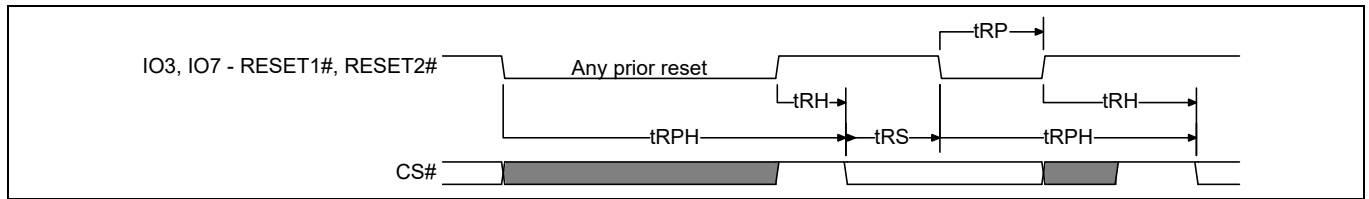
Figure 24   **Hardware reset when quad mode is not enabled and IO3, IO7 / RESET1#, RESET2# is enabled**
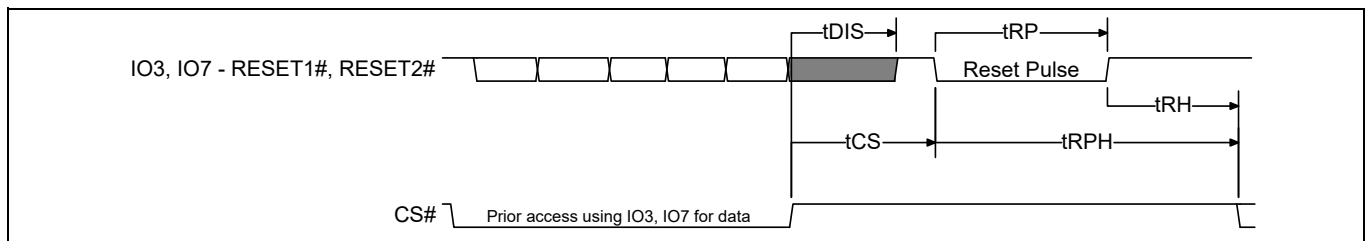
Figure 25   **Hardware reset when quad mode and IO3, IO7 / RESET1, RESET2# are enabled**

7.4 SDR AC characteristics

Table 14   AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for READ and 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK clock frequency for the following Dual and Quad commands: QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	DC	–	133	MHz
P_{SCK}	SCK clock period	$1/ F_{SCK}$	–	∞	
t_{WH}, t_{CH}	Clock HIGH time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	ns
t_{WL}, t_{CL}	Clock LOW time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	ns
t_{CRT}, t_{CLCH}	Clock Rise time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall time (slew rate)	0.1	–	–	V/ns
t_{CS}	CS# HIGH time (read instructions) CS# HIGH time (read instructions when Reset feature and Quad mode are both enabled) CS# HIGH time (program / erase Instructions)	10 20[25] 50	–	–	ns
t_{CSS}	CS# active setup time (relative to SCK)	2	–	–	ns
t_{CSH}	CS# active hold time (relative to SCK)	3	–	–	ns
t_{SU}	Data in setup time	2	–	–	ns
t_{HD}	Data in hold time	3	–	–	ns
t_V	Clock LOW to output valid	–	–	8[22] 6[23]	ns
t_{HO}	Output hold time	1	–	–	ns
t_{DIS}	Output disable time[24] Output disable time (when Reset feature and Quad mode are both enabled)	–	–	8 20[25]	ns
t_{WPS}	WP# setup time[21]	20	–	–	ns
t_{WPH}	WP# hold time[21]	100	–	–	ns
t_{DPD}	CS# HIGH to Power-down mode	–	–	3	µs
t_{RES}	CS# HIGH to Standby mode without electronic signature read	–	–	30	µs

Notes
21. Only applicable as a constraint for WRR or WRAR instruction when SRWD is set to '1'.
22. Full V_{CC} range and CL = 30 pF.
23. Full V_{CC} range and CL = 15 pF.
24. Output Hi-Z is defined as the point where data is no longer driven.
25. t_{CS} and t_{DIS} require additional time when the Reset feature and Quad mode are enabled (CR2V[5] = 1 and CR1V[1] = 1).
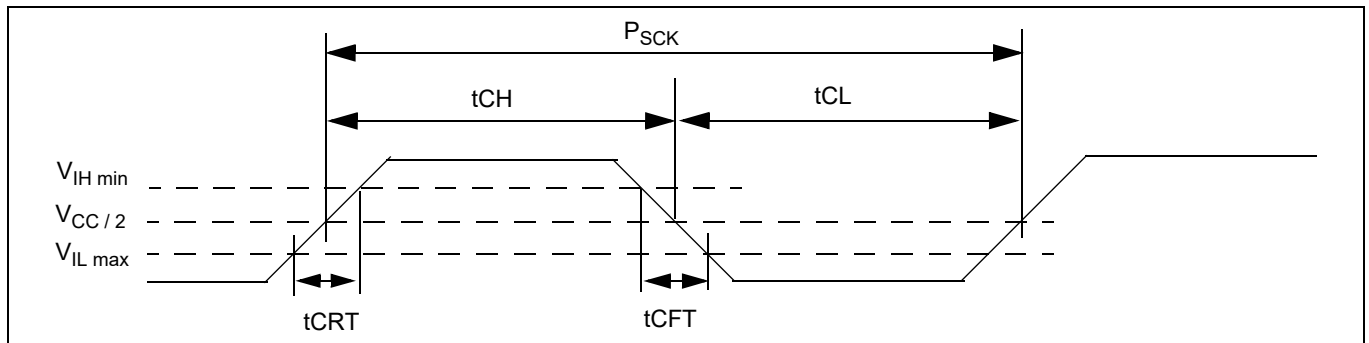
7.4.1 Clock timing

Figure 26   Clock timing

7.4.2 Input / output timing
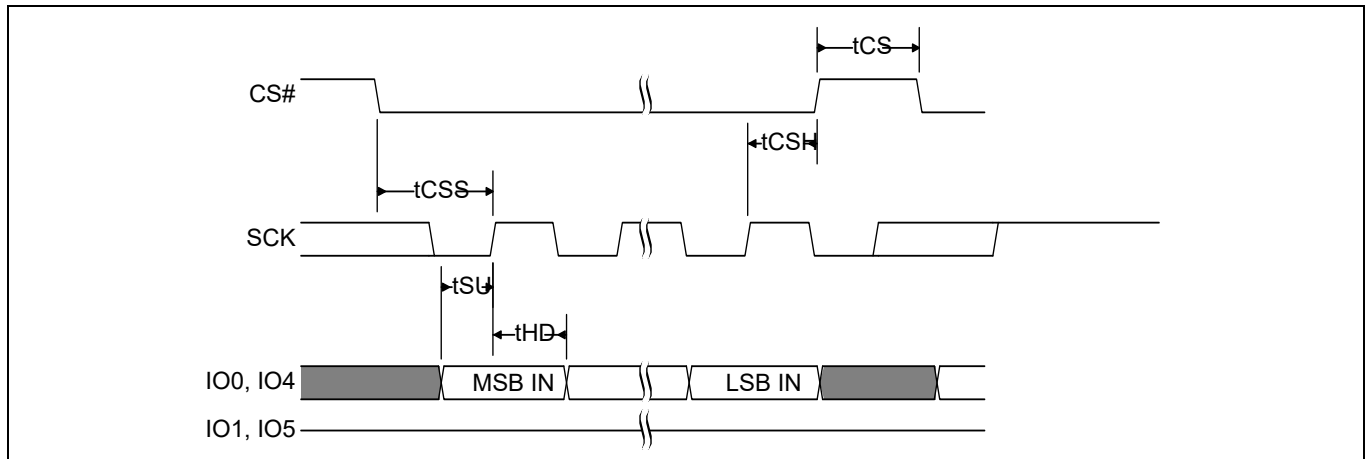
Figure 27   SPI single bit input timing
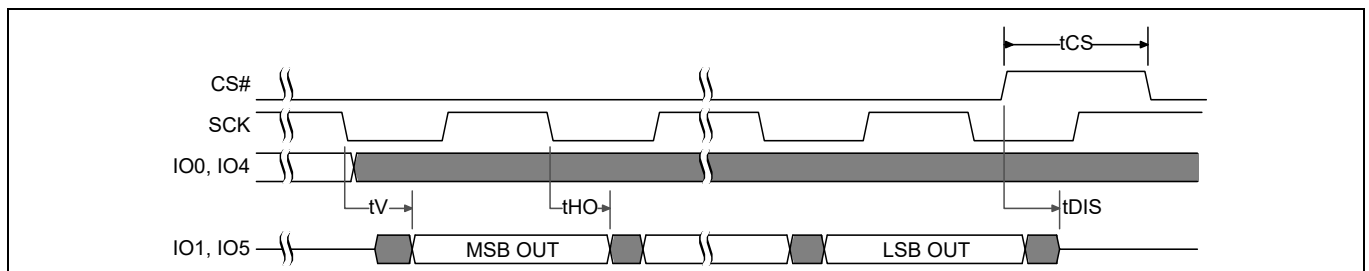
Figure 28   SPI single bit output timing

Figure 29   Dual-Quad SPI timing
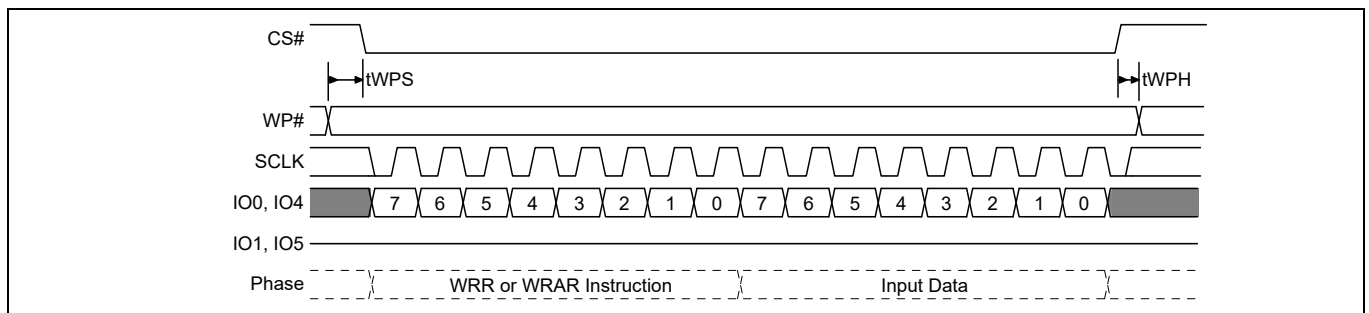
Figure 30   WP# SPI input timing

Timing specifications

7.5   DDR AC characteristics

Table 15   DDR 102 MHz AC characteristics operation[26]

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	–	102	MHz
$P_{SCK, R}$	SCK clock period for DDR READ instruction	$1/F_{SCK}$	–	∞	ns
t_{WH}, t_{CH}	Clock HIGH time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	ns
t_{WL}, t_{CL}	Clock LOW time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	ns
t_{CS}	CS# HIGH time (read instructions) CS# HIGH time (read instructions when Reset feature is enabled)	10 20	–	–	ns
t_{CSS}	CS# active setup time (relative to SCK)	2	–	–	ns
t_{CSH}	CS# active hold time (relative to SCK)	3	–	–	ns
t_{SU}	IO in setup time	1.5	–	–	ns
t_{HD}	IO in hold time	1.5	–	–	ns
t_V	Clock LOW to output valid	1.5	–	6.0[26]	ns
t_{HO}	Output Hold time	1	–		ns
t_{DIS}	Output disable time Output disable time (when Reset feature is enabled)	– 	–	8 20	ns
t_{IO_skew}	First IO to last IO data valid time	–	–	400	ps
t_{DPD}	CS# HIGH to Power-down mode	–	–	3	µs
t_{RES}	CS# HIGH to Standby mode without electronic signature read	–	–	30	µs

Note
26. CL = 15 pF.

7.5.1 DDR input timing
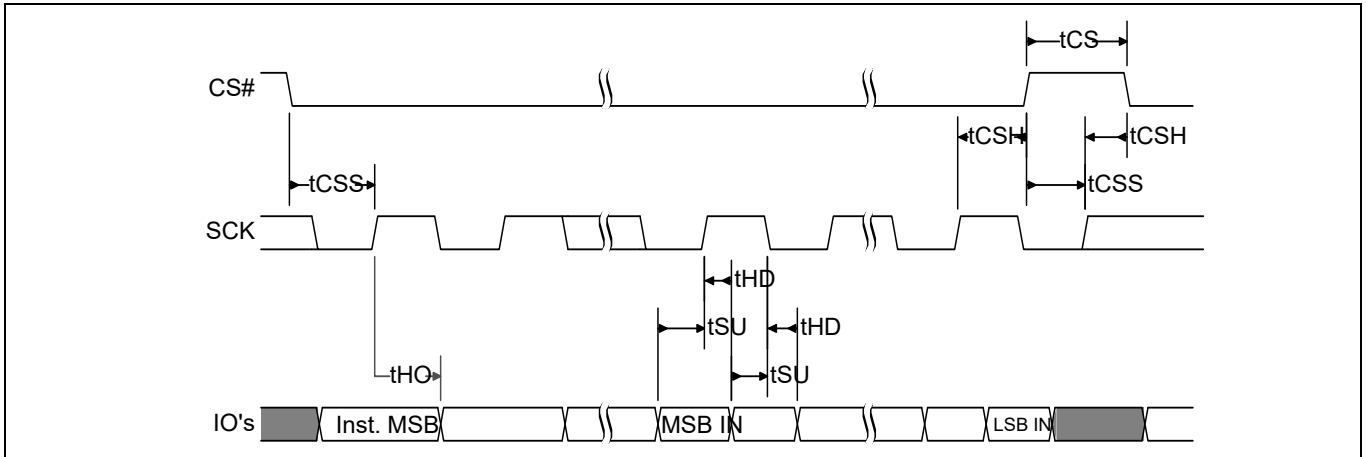
Figure 31   SPI DDR input timing

7.5.2 DDR output timing
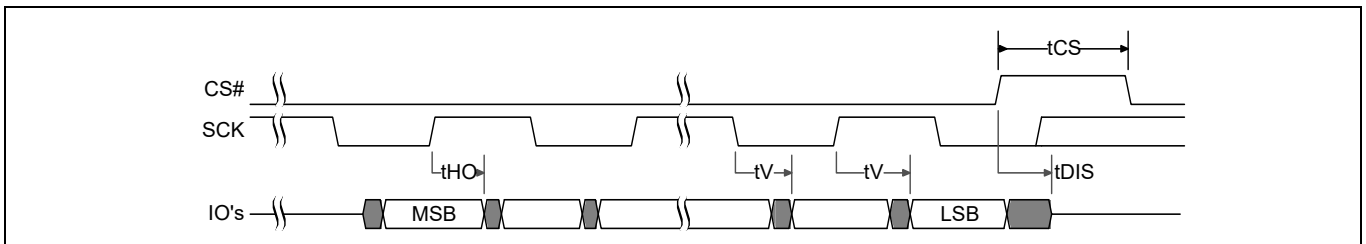
Figure 32   SPI DDR output timing

7.5.3   DDR data valid timing using DLP
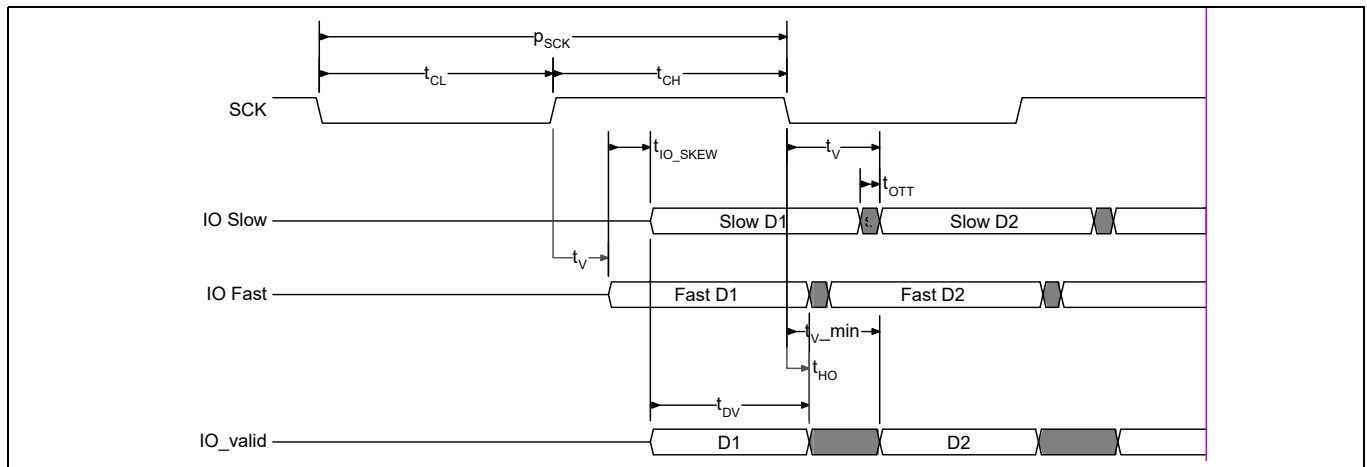
Figure 33   SPI DDR data valid window

The minimum data valid window (t_{DV}) and t_V minimum can be calculated as follows:

t_{DV} = minimum half clock cycle time (t_{CLH})[27] – t_{OTT}[28] – t_{IO_SKEW}[29]

$t_V\_min = t_{HO} + t_{IO\_SKEW} + t_{OTT}$

Example:

102 MHz clock frequency = 9.8 ns clock period, DDR operations and duty cycle of 45% or higher

$t_{CLH} = 0.45 \times PSCK = 0.45 \times 9.8\ ns = 4.41\ ns$

Bus impedance of 30 ohm and capacitance of 15 pf, with timing reference of 0.75 × V_{CC}, the rise time from 0 to 1 or fall time 1 to 0 is 1.4[31] × RC time constant (Tau)[32] = 1.4 × 0.45 ns = 0.63 ns

t_{OTT} = rise time or fall time = 0.63 ns.

Data Valid Window

$t_{DV} = t_{CLH} - t_{IO\_SKEW} - t_{OTT} = 4.41\ ns - 400\ ps - 0.63\ ns = 3.947\ ns$

t_V Minimum

$t_V\_min = t_{HO} + t_{IO\_SKEW} + t_{OTT} = 1.0\ ns + 400\ ps + 0.63\ ns = 2.03\ ns$

Notes

27. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
28. t_{OTT} is the maximum output transition time from one valid data value to the next valid data value on each IO.
    t_{OTT} is dependent on system level considerations including:
    a. Memory device output impedance (drive strength).
    b. System level parasitics on the IOs (primarily bus capacitance).
    c. Host memory controller input V_{IH} and V_{IL} levels at which '0' to '1' and '1' to '0' transitions are recognized.
    d. t_{OTT} is not a specification tested by Infineon, it is system dependent and must be derived by the system designer based on the above considerations.
29. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
30. t_{DV} is the data valid window.
31. Multiplier of Tau time for voltage to rise to 75% of V_{CC}.
32. Tau = R (Output Impedance) × C (Load capacitance).

8 Package diagrams

8.1 BGA 24-ball, 5 × 5 ball footprint (ZSA024)

8.1.1 BGA connection diagram
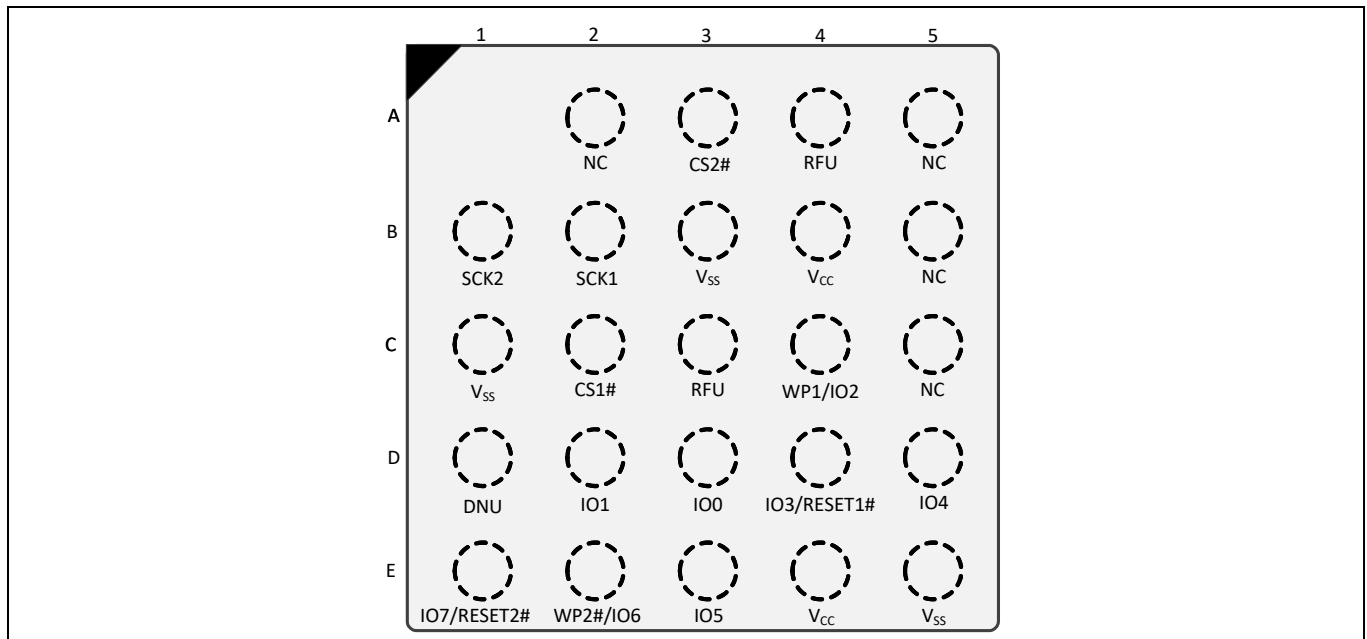
Figure 34 **24-ball BGA, 5 × 5 ball footprint (ZSA024), top view**[33, 34]

8.1.2 Special handling instructions for FBGA packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Notes
33. Signal connections are in the same relative positions as FAC024 BGA, allowing a single PCB footprint to use either package.
34. The RESET# input has an internal pull-up and may be left unconnected in the system if Quad Mode and hardware reset are not in use.

Package diagrams

8.1.3 BGA physical diagram

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	4.00 BSC		
E1	4.00 BSC		
MD	5		
ME	5		
n	24		
Ø b	0.35	0.40	0.45
eD	1.00 BSC		
eE	1.00 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE
   MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE
   PARALLEL TO DATUM C.

7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE
   THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW,
   "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW,
   "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK,
   METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15078 **

Figure 35   24-ball FBGA (8.0 × 6.0 × 1.2 mm) package outline, 002-15078

9 Address space maps

9.1 Overview

9.1.1 Extended address

The S79FS01GS supports 32-bit (4-byte) addresses to enable higher density devices than allowed by previous generation (legacy) SPI devices that supported only 24-bit (3-byte) addresses. A 24-bit, byte resolution, address can access only 16 MB (128 Mb) maximum density. A 32-bit, byte resolution, address allows direct addressing of up to a 4 GBytes (32 Gb) address space.

Legacy commands continue to support 24-bit addresses for backward software compatibility. Extended 32-bit addresses are enabled in two ways:

- Extended Address mode — a volatile configuration register bit that changes all legacy commands to expect 32 bits of address supplied from the host system.

- 4-byte address commands — that perform both legacy and new functions, which always expect 32-bit address.

The default condition for extended address mode, after power-up or reset, is controlled by a non-volatile configuration bit. The default extended address mode may be set for 24 or 32-bit addresses. This enables legacy software compatible access to the first 128 Mb of a device or for the device to start directly in 32-bit address mode.

9.1.2 Multiple address spaces

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main flash array. Each separate address space uses the full 24- or 32-bit address but may only define a small portion of the available address space.

9.2 Flash memory array

The main flash array is divided into erase units called physical sectors.

The FS-S family physical sectors may be configured as a hybrid combination of eight 8 KB parameter sectors at the top or bottom of the address space with all but one of the remaining sectors being uniform size. Because the group of eight 8 KB parameter sectors is in total smaller than a uniform sector, the group of 8 KB physical sectors respectively overlay (replace) the top or bottom 64 KB of the highest or lowest address uniform sector.

The parameter sector erase commands (20h or 21h) must be used to erase the 8 KB sectors individually. The sector (uniform block) erase commands (D8h or DCh) must be used to erase any of the remaining sectors, including the portion of highest or lowest address sector that is not overlaid by the parameter sectors. The uniform block erase command has no effect on parameter sectors.
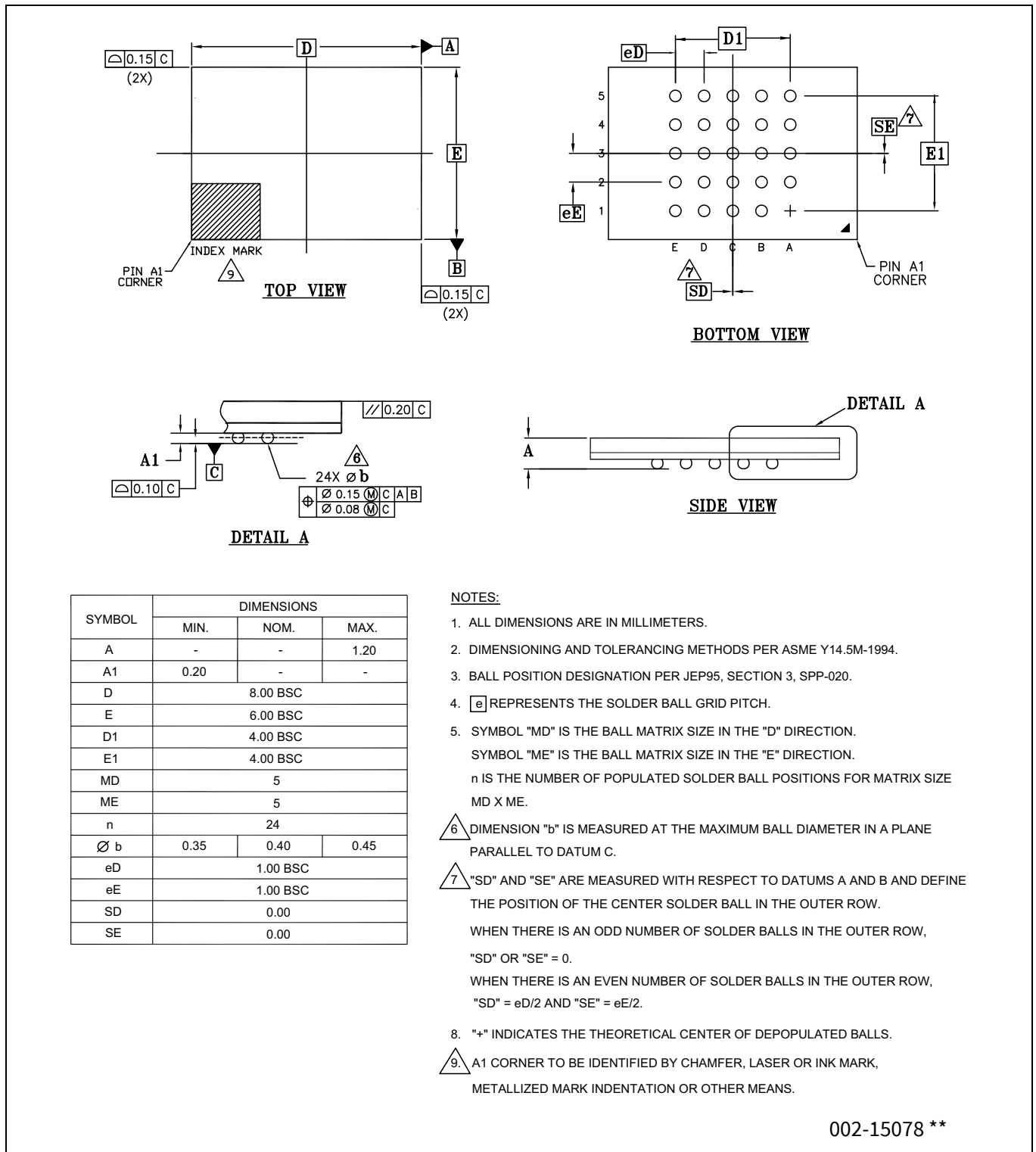
Configuration Register 1 non-volatile bit 2 (CR1NV[2]) equal to 0 overlays the parameter sectors at the bottom of the lowest address uniform sector. CR1NV[2] = 1 overlays the parameter sectors at the top of the highest address uniform sector.

See **"Registers"** on page 47 for more information.

There is also a configuration option to remove the 8 KB parameter sectors from the address map so that all sectors are uniform size. Configuration Register 3 volatile bit 3 (CR3V[3]) equal to '0' selects the hybrid sector architecture with 8 KB parameter sectors. CR3V[3] = 1 selects the uniform sector architecture without parameter sectors. Uniform physical sectors are:

- 512 KB in S79FS01GS

The sector erase (SE) commands erase the physical 512 KB sectors of the 1 Gb device.

Table 16   S79FS01GS sector address map, bottom 8 KB sectors

Sector size (KB)	Sector count	Sector range	Address range (byte address)	Notes
8	8	SA00	00000000h–00000FFFh	Sector starting address
		:	:	
		SA7	00007000h–00007FFFh	
448	1	SA8	00008000h–0003FFFFh	—
512	255	SA9	00040000h–0007FFFFh	
		:	:	
		SA263	03FC0000h–03FFFFFFh	Sector ending address

Table 17   S79FS01GS sector address map, top 8 KB sectors

Sector size (KB)	Sector count	Sector range	Address range (byte address)	Notes
512	255	SA00	0000000h–003FFFFh	Sector starting address
		:	:	
		SA254	03F80000h–03FBFFFFh	
448	1	SA255	03FC0000h–03FF7FFFh	—
8	8	SA256	03FF8000h–03FF8FFFh	
		:	:	
		SA263	03FFF000h–03FFFFFFh	Sector ending address

Table 18   S79FS01GS sector address map (uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (byte address)	Notes
512	256	SA00	00000000h–0003FFFFh	Sector starting address
		:	:	—
		SA255	03FC0000h–03FFFFFFh	Sector ending address

Note These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 8 KB sectors have the pattern XXXX000h–XXXXFFFh. All 512 KB sectors have the pattern XX00000h–XX3FFFFh, XX40000h–XX7FFFFh, XX80000h–XXCFFFFh, or XXD0000h–XXFFFFFh.

9.3 ID-CFI address space

The RDID command (9Fh) reads information from a separate flash memory address space for device identification (ID) and common flash interface (CFI) information. See **"Device ID and common flash interface (ID-CFI) address map"** on page 144 for the tables defining the contents of the ID-CFI address space. The ID-CFI address space is programmed by Infineon and read-only for the host system.

9.4 JEDEC JESD216 serial flash discoverable parameters (SFDP) space

The RSFDP command (5Ah) reads information from a separate flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216 standard for Serial Flash Discoverable Parameters. The ID-CFI address space is incorporated as one of the SFDP parameters. See **"Serial flash discoverable parameters (SFDP) address map"** on page 141 for the tables defining the contents of the SFDP address space. The SFDP address space is programmed by Infineon and read-only for the host system. For the Dual-Quad device only read SFDP on Quad SPI-1.

9.5 OTP address space

Each S79FS01GS memory device has a 2048-byte OTP address space that is separate from the main flash array. The OTP area is divided into 64, individually lockable, 32-byte aligned and length regions.

In the 64-byte region starting at address zero:

- The 16 lowest address bytes are programmed by Infineon with a 128-bit random number. Only Infineon is able to program these bytes.

- The next 4 higher address bytes (OTP Lock Bytes) are used to provide one bit per OTP region to permanently protect each region from programming. The bytes are erased when shipped from Infineon. After an OTP region is programmed, it can be locked to prevent further programming, by programming the related protection bit in the OTP Lock Bytes.

- The next higher 12 bytes of the lowest address region are Reserved for Future Use (RFU). The bits in these RFU bytes may be programmed by the host system but it must be understood that a future device may use those bits for protection of a larger OTP space. The bytes are erased when shipped from Infineon.

The remaining regions are erased when shipped from Infineon, and are available for programming of additional permanent data.

Figure 36 shows a pictorial representation of the OTP memory space.

The OTP memory space is intended for increased system security. OTP values, such as the random number programmed by Infineon, can be used to "mate" a flash component with the system CPU/ASIC to prevent device substitution.

The configuration register FREEZE (CR1V[0]) bit protects the entire OTP memory space from programming when set to '1'. This allows trusted boot code to control programming of OTP regions then set the FREEZE bit to prevent further OTP memory space programming during the remainder of normal power-on system operation.

During the programming of each OTP region, bits 0–3 are programmed on Quad SPI-1 via IO0–IO3, and bits 4–7 are programmed on Quad SPI-2 via IO4–IO7.

Address space maps
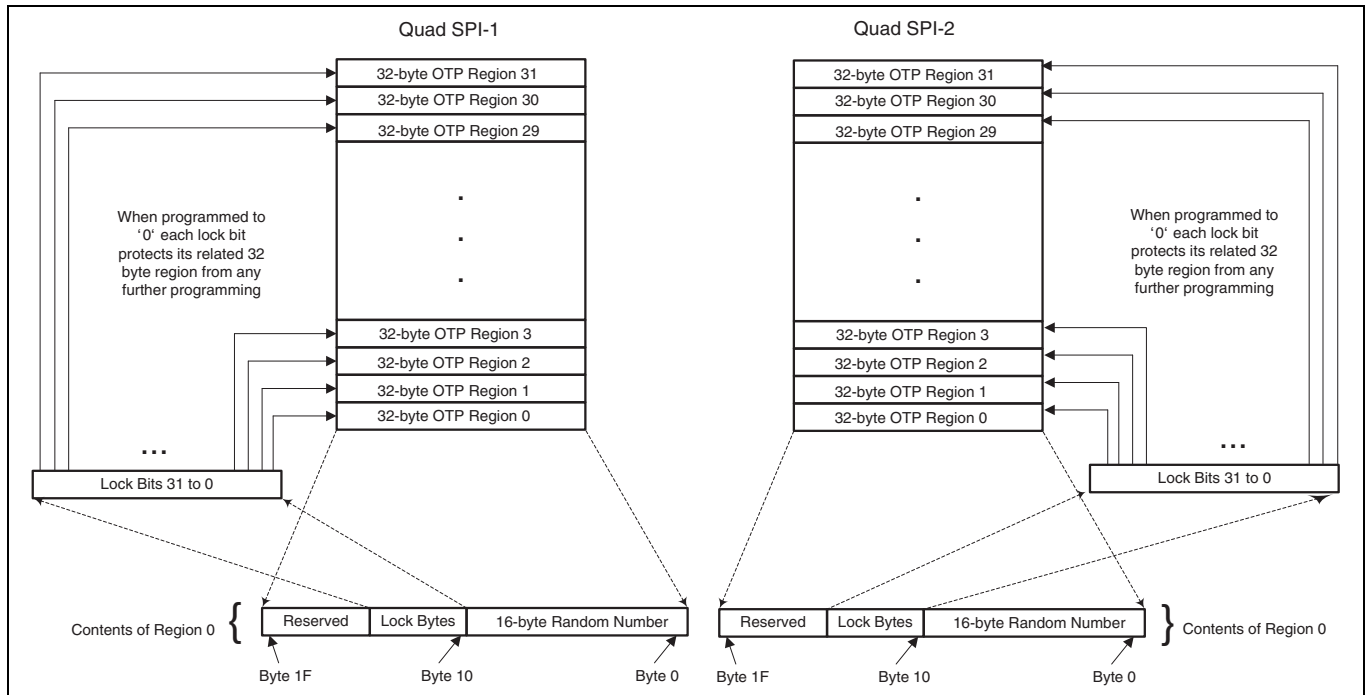
Figure 36   **OTP address space — Quad SPI-1 and Quad SPI-2**

Table 19   **OTP address map for Quad SPI-1 and Quad SPI-2**

Region	Byte address range (Hex)	Contents	Initial delivery state (Hex)
Region 0	000	Least Significant Byte of Infineon programmed random number	Infineon programmed random number
	...	...	
	00F	Most Significant Byte of Infineon programmed random number	
	010 to 013	Region Locking Bits Byte 10 [bit 0] locks region 0 from programming when = 0 ... Byte 13 [bit 7] locks region 31 from programming when = 0	All Bytes = FF
	014 to 01F	Reserved for Future Use (RFU)	All Bytes = FF
Region 1	020 to 03F	Available for user programming	All Bytes = FF
Region 2	040 to 05F	Available for user programming	All Bytes = FF
...	...	Available for user programming	All Bytes = FF
Region 31	3E0 to 3FF	Available for user programming	All Bytes = FF

9.6 Registers

Registers are small groups of memory cells used to configure how the S79FS01GS memory device operates or to report the status of device operations. The registers are accessed by specific commands. The commands (and hexadecimal instruction codes) used for each register are noted in each register description.

In legacy SPI memory devices the individual register bits could be a mixture of volatile, non-volatile, or OTP bits within the same register. In some configuration options the type of a register bit could change e.g. from non-volatile to volatile.

The S79FS01GS uses separate non-volatile or volatile memory cell groups (areas) to implement the different register bit types. However, the legacy registers and commands continue to appear and behave as they always have for legacy software compatibility. There is a non-volatile and a volatile version of each legacy register when that legacy register has volatile bits or when the command to read the legacy register has zero read latency. When such a register is read the volatile version of the register is delivered. During POR, hardware reset, or software reset, the non-volatile version of a register is copied to the volatile version to provide the default state of the volatile register. When non-volatile register bits are written the non-volatile version of the register is erased and programmed with the new bit values and the volatile version of the register is updated with the new contents of the non-volatile version. When OTP bits are programmed the non-volatile version of the register is programmed and the appropriate bits are updated in the volatile version of the register. When volatile register bits are written, only the volatile version of the register has the appropriate bits updated.

The S79FL01GS Dual-Quad SPI device has a register of each type, one for each individual die. Each register must be accessed by a command given in parallel to IO0–IO3 (Quad SPI-1) and for IO4–IO7 (Quad SPI-2). Reading and writing to each of these registers must also be done in parallel for IO0–IO3 (Quad SPI-1) and for IO4–IO7 (Quad SPI-2).

The type for each bit is noted in each register description. The default state shown for each bit refers to the state after POR, hardware reset, or software reset if the bit is volatile. If the bit is non-volatile or OTP, the default state is the value of the bit when the device is shipped from Infineon. Non-volatile bits have the same cycling (erase and program) endurance as the main flash array.

Table 20   Register description

Register	Abbreviation	Type	Bit location
Status Register 1	SR1NV[7:0]	Non-volatile	7:0
Status Register 1	SR1V[7:0]	Volatile	7:0
Status Register 2	SR2V[7:0]	Volatile	7:0
Configuration Register 1	CR1NV[7:0]	Non-volatile	7:0
Configuration Register 1	CR1V[7:0]	Volatile	7:0
Configuration Register 2	CR2NV[7:0]	Non-volatile	7:0
Configuration Register 2	CR2V[7:0]	Volatile	7:0
Configuration Register 3	CR3NV[7:0]	Non-volatile	7:0
Configuration Register 3	CR3V[7:0]	Volatile	7:0
Configuration Register 4	CR4NV[7:0]	Non-volatile	7:0
Configuration Register 4	CR4V[7:0]	Volatile	7:0
ECC Status Register	ECCSR [7:0]	Volatile	7:0
ASP Register	ASPR[15:1]	OTP	15:1
ASP Register	ASPR[0]	RFU	0
Password Register	PASS[63:0]	Non-volatile OTP	63:0
PPB Lock Register	PPBL[7:1]	Volatile	7:1
PPB Lock Register	PPBL[0]	Volatile Read Only	0
PPB Access Register	PPBAR[7:0]	Non-volatile	7:0
DYB Access Register	DYBAR[7:0]	Volatile	7:0

Table 20   Register description (Continued)

Register	Abbreviation	Type	Bit location
SPI DDR Data Learning Registers	NVDLR[7:0]	Non-volatile	7:0
SPI DDR Data Learning Registers	VDLR[7:0]	Volatile	7:0

9.6.1   Status Register 1

9.6.1.1   Status Register 1 Non-volatile (SR1NV)

Related Commands: Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 21   Status Register 1 Non-volatile (SR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SRWD_NV	Status Register Write Disable Default	Non-volatile	0	1 = Locks state of SRWD, BP, and Configuration Register-1 bits when WP# is LOW by not executing WRR or WRAR commands that would affect SR1NV, SR1V, CR1NV, or CR1V. 0 = No protection, even when WP# is LOW.
6	P_ERR_D	Programming Error Default	Non-volatile Read Only	0	Provides the default state for the Programming Error Status. Not user programmable.
5	E_ERR_D	Erase Error Default	Non-volatile Read Only	0	Provides the default state for the Erase Error Status. Not user programmable.
4	BP_NV2	Block Protection non-volatile	Non-volatile	000b	Protects the selected range of sectors (Block) from Program or Erase when the BP bits are configured as non-volatile (CR1NV[3] = 0). Programmed to 111b when BP bits are configured to volatile (CR1NV[3] = 1) after which these bits are no longer user programmable.
3	BP_NV1				
2	BP_NV0				
1	WEL_D	WEL Default	Non-volatile Read Only	0	Provides the default state for the WEL Status. Not user programmable.
0	WIP_D	WIP Default	Non-volatile Read Only	0	Provides the default state for the WIP Status. Not user programmable.

Status Register Write Non-volatile (SRWD_NV) SR1NV[7]: Places the device in the Hardware Protected mode when this bit is set to '1' and the WP# input is driven LOW. In this mode, the Write Registers (WRR) and Write Any Register (WRAR) commands (that select Status Register 1 or Configuration Register 1) are ignored and not accepted for execution, effectively locking the state of the Status Register 1 and Configuration Register 1 (SR1NV, SR1V, CR1NV, or CR1V) bits, by making the registers read-only. If WP# is HIGH, Status Register 1 and Configuration Register 1 may be changed by the WRR or WRAR commands. If SRWD_NV is '0', WP# has no effect and Status Register 1 and Configuration Register 1 may be changed by the WRR or WRAR commands. WP# has no effect on the writing of any other registers. The SRWD_NV bit has the same non-volatile endurance as the main flash array. The SRWD (SR1V[7]) bit serves only as a copy of the SRWD_NV bit to provide zero read latency.

Program Error Default (P_ERR_D) SR1NV[6]: Provides the default state for the Programming Error Status in SR1V[6]. This bit is not user programmable.

Erase Error (E_ERR) SR1V[5]: Provides the default state for the Erase Error Status in SR1V[5]. This bit is not user programmable.

Block Protection (BP_NV2, BP_NV1, BP_NV0) SR1NV[4:2]: These bits define the main flash array area to be software-protected against program and erase commands. The BP bits are selected as either volatile or non-volatile, depending on the state of the BP non-volatile bit (BPNV_O) in the configuration register CR1NV[3]. When CR1NV[3] = 0 the non-volatile version of the BP bits (SR1NV[4:2]) are used to control Block Protection and the WRR command writes SR1NV[4:2] and updates SR1V[4:2] to the same value. When CR1NV[3] = 1 the volatile version of the BP bits (SR1V[4:2]) are used to control Block Protection and the WRR command writes SR1V[4:2] and does not affect SR1NV[4:2]. When one or more of the BP bits is set to '1', the relevant memory area is protected against program and erase. The Bulk Erase (BE) command can be executed only when the BP bits are cleared to 0's. See **"Block Protection"** on page 72 for a description of how the BP bit values select the memory array area protected. The non-volatile version of the BP bits have the same non-volatile endurance as the main flash array.

Write Enable Latch Default (WEL_D) SR1NV[1]: Provides the default state for the WEL Status in SR1V[1]. This bit is programmed by Infineon and is not user programmable.

Write In Progress Default (WIP_D) SR1NV[0]: Provides the default state for the WIP Status in SR1V[0]. This bit is programmed by Infineon and is not user programmable.

9.6.1.2   Status Register 1 Volatile (SR1V)

Related Commands: Read Status Register (RDSR1 05h), Write Registers (WRR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Clear Status Register (CLSR 30h or 82h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDSR1 command.

Table 22   Status Register 1 Volatile (SR1V)

Bits	Field name	Function	Type	Default state	Description
7	SRWD	Status Register Write Disable	Volatile Read Only	SR1NV	Volatile copy of SR1NV[7]
6	P_ERR	Programming Error Occurred	Volatile Read Only		1 = Error occurred 0 = No error
5	E_ERR	Erase Error Occurred	Volatile Read Only		1 = Error occurred 0 = No error
4	BP2	Block Protection Volatile	Volatile		Protects selected range of sectors (Block) from Program or Erase when the BP bits are configured as volatile (CR1NV[3] = 1). Volatile copy of SR1NV[4:2] when BP bits are configured as non-volatile. User writable when BP bits are configured as volatile.
3	BP1				
2	BP0				
1	WEL	Write Enable Latch	Volatile		1 = Device accepts Write Registers (WRR and WRAR), program, or erase commands. 0 = Device ignores Write Registers (WRR and WRAR), program, or erase commands. This bit is not affected by WRR or WRAR, only WREN and WRDI commands affect this bit.
0	WIP	Write in Progress	Volatile Read Only		1 = Device Busy, an embedded operation is in progress such as program or erase. 0 = Ready Device is in standby mode and can accept commands. This bit is not affected by WRR or WRAR, it only provides WIP status.

Status Register Write (SRWD) SR1V[7]: SRWD is a volatile copy of SR1NV[7]. This bit tracks any changes to the non-volatile version of this bit.

Program Error (P_ERR) SR1V[6]: The Program Error Bit is used as a program operation success or failure indication. When the Program Error bit is set to '1', it indicates that there was an error in the last program operation. This bit will also be set when the user attempts to program within a protected main memory sector, or program within a locked OTP region. When the Program Error bit is set to '1', this bit can be cleared to '0' with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Erase Error (E_ERR) SR1V[5]: The Erase Error Bit is used as an Erase operation success or failure indication. When the Erase Error bit is set to '1', it indicates that there was an error in the last erase operation. This bit will also be set when the user attempts to erase an individual protected main memory sector. The Bulk Erase command will not set E_ERR if a protected sector is found during the command execution. When the Erase Error bit is set to '1', this bit can be cleared to '0' with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Block Protection (BP2, BP1, BP0) SR1V[4:2]: These bits define the main flash array area to be software-protected against program and erase commands. The BP bits are selected as either volatile or non-volatile, depending on the state of the BP non-volatile bit (BPNV_O) in the configuration register CR1NV[3]. When CR1NV[3] = 0 the non-volatile version of the BP bits (SR1NV[4:2]) are used to control Block Protection and the WRR command writes SR1NV[4:2] and updates SR1V[4:2] to the same value. When CR1NV[3] = 1 the volatile version of the BP bits (SR1V[4:2]) are used to control Block Protection and the WRR command writes SR1V[4:2] and does not affect SR1NV[4:2]. When one or more of the BP bits is set to '1', the relevant memory area is protected against program and erase. The Bulk Erase (BE) command can be executed only when the BP bits are cleared to 0's. See **"Block Protection"** on page 72 for a description of how the BP bit values select the memory array area protected.

Write Enable Latch (WEL) SR1V[1]: The WEL bit must be set to '1' to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to '1' to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to '0' to prevent all program, erase, and write commands from execution. The WEL bit is cleared to '0' at the end of any successful program, write, or erase operation. Following a failed operation the WEL bit may remain set and should be cleared with a WRDI command following a CLSR command. After a power down / power up sequence, hardware reset, or software reset, the Write Enable Latch is set to '0'. The WRR or WRAR command does not affect this bit.

Write In Progress (WIP) SR1V[0]: Indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the bit is set to '1', the device is busy performing an operation. While WIP is '1', only Read Status (RDSR1 or RDSR2), Read Any Register (RDAR), Erase Suspend (ERSP), Program Suspend (PGSP), Clear Status Register (CLSR), and Software Reset (RESET) commands are accepted. ERSP and PGSP will only be accepted if memory array erase or program operations are in progress. The status register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to '1', the WIP bit will remain set to one indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to standby mode. When the WIP bit is cleared to '0', no operation is in progress. This is a read-only bit.

9.6.2 Status Register 2 Volatile (SR2V)

Related Commands: Read Status Register 2 (RDSR2 07h), Read Any Register (RDAR 65h). Status Register-2 does not have user programmable non-volatile bits, all defined bits are volatile read only status. The default state of these bits are set by hardware.

Table 23   Status Register 2 Volatile (SR2V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	–	0	Reserved for Future Use.
6	RFU	Reserved	–	0	Reserved for Future Use.
5	RFU	Reserved	–	0	Reserved for Future Use.
4	RFU	Reserved	–	0	Reserved for Future Use.
3	RFU	Reserved	–	0	Reserved for Future Use.
2	ESTAT	Erase Status	Volatile Read Only	0	1 = Sector Erase Status command result = Erase completed. 0 = Sector Erase Status command result = Erase not completed.
1	ES	Erase Suspend	Volatile Read Only	0	1 = In erase suspend mode. 0 = Not in erase suspend mode.
0	PS	Program Suspend	Volatile Read Only	0	1 = In program suspend mode. 0 = Not in program suspend mode.

Erase Status (ESTAT) SR2V[2]: The Erase Status bit indicates whether the sector, selected by an immediately preceding Erase status command, completed the last erase command on that sector. The Erase Status command must be issued immediately before reading SR2V to get valid erase status. Reading SR2V during a program or erase suspend does not provide valid erase status. The erase status bit can be used by system software to detect any sector that failed its last erase operation. This can be used to detect erase operations failed due to loss of power during the erase operation.

Erase Suspend (ES) SR2V[1]: The Erase Suspend bit is used to determine when the device is in Erase Suspend mode. This is a status bit that cannot be written by the user. When Erase Suspend bit is set to '1', the device is in erase suspend mode. When Erase Suspend bit is cleared to '0', the device is not in erase suspend mode. Refer to **"Erase or Program Suspend (EPS 85h, 75h, B0h)"** on page 121 for details about the Erase Suspend / Resume commands.

Program Suspend (PS) SR2V[0]: The Program Suspend bit is used to determine when the device is in Program Suspend mode. This is a status bit that cannot be written by the user. When Program Suspend bit is set to '1', the device is in program suspend mode. When the Program Suspend bit is cleared to '0', the device is not in program suspend mode. Refer to **"Erase or Program Suspend (EPS 85h, 75h, B0h)"** on page 121 for details.

9.6.3 Configuration Register 1

Configuration Register 1 controls certain interface and data protection functions. The register bits can be changed using the WRR command with sixteen input cycles or with the WRAR command.

9.6.3.1 Configuration Register 1 Non-volatile (CR1NV)

Related Commands: Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 24   Configuration Register 1 non-volatile (CR1NV)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved for Future Use	Non-volatile	0	Reserved
6	RFU			0	
5	TBPROT_O	Configures Start of Block Protection	OTP	0	1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
4	RFU	Reserved for Future Use	RFU	0	Reserved
3	BPNV_O	Configures BP2-0 in Status Register	OTP	0	1 = Volatile 0 = Non-volatile
2	TBPARM_O	Configures Parameter Sectors location	OTP	0	1 = 8 KB physical sectors at top, (High address) 0 = 8 KB physical sectors at top, (Low address) RFU in uniform sector configuration.
1	QUAD_NV	Quad Non-volatile	Non-volatile	0	Provides the default state for the QUAD bit.
0	FREEZE_D	FREEZE Default	Non-volatile Read Only	0	Provides the default state for the Freeze bit. Not user programmable.

Top or Bottom Protection (TBPROT_O) CR1NV[5]: This bit defines the operation of the Block Protection bits BP2, BP1, and BP0 in the Status Register. As described in the status register section, the BP2–0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, ¼, ½, and so on, up to the entire array. When TBPROT_O is set to '0', the Block Protection is defined to start from the top (maximum address) of the array. When TBPROT_O is set to '1', the Block Protection is defined to start from the bottom (zero address) of the array. The TBPROT_O bit is OTP and set to '0', when shipped from Infineon. If TBPROT_O is programmed to '1', writing the bit with a '0' does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

The desired state of TBPROT_O must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPROT_O must not be programmed after programming or erasing is done in the main flash array.

CR1NV[4]: Reserved for Future Use.

Address space maps

Block Protection Non-volatile (BPNV_O) CR1NV[3]: The BPNV_O bit defines whether the BP_NV 2–0 bits or the BP 2–0 bits in the Status Register are selected to control the Block Protection feature. The BPNV_O bit is OTP and cleared to '0' with the BP_NV bits cleared to '000' when shipped from Infineon. When BPNV_O is set to '0', the BP_NV 2–0 bits in the Status Register are selected to control the block protection and are written by the WRR command. The time required to write the BP_NV bits is t_W. When BPNV is set to '1', the BP2–0 bits in the Status Register are selected to control the block protection and the BP_NV 2–0 bits will be programmed to binary '111'. This will cause the BP 2–0 bits to be set to binary 111 after POR, hardware reset, or command reset. When BPNV is set to '1', the WRR command writes only the volatile version of the BP bits (SR1V[4:2]). The non-volatile version of the BP bits (SR1NV[4:2]) are no longer affected by the WRR command. This allows the BP bits to be written an unlimited number of times because they are volatile and the time to write the volatile BP bits is the much faster t_{CS} volatile register write time. If BPNV_O is programmed to '1', writing the bit with a '0' does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

TBPARM_O CR1NV[2]: TBPARM_O defines the logical location of the parameter block. The parameter block consists of eight 8 KB parameter sectors, which replace a 64 KB portion of the highest or lowest address sector. When TBPARM_O is set to '1', the parameter block is in the top of the memory array address space. When TBPARM_O is set to '0', the parameter block is at the Bottom of the array. TBPARM_O is OTP and set to '0', when it ships from Infineon. If TBPARM_O is programmed to '1', writing the bit with '0' does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

The desired state of TBPARM_O must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPARM_O must not be programmed after programming or erasing is done in the main flash array.

TBPROT_O can be set or cleared independent of the TBPARM_O bit. Therefore, the user can elect to store parameter information from the bottom of the array and protect boot code starting at the top of the array, or vice versa. Or, the user can elect to store and protect the parameter information starting from the top or bottom together.

When the memory array is configured as uniform sectors, the TBPARM_O bit is Reserved for Future Use (RFU) and has no effect because all sectors are uniform size.

Quad Data Width Non-volatile (QUAD_NV) CR1NV[1]: Provides the default state for the QUAD bit in CR1V[1]. The WRR or WRAR command affects this bit. Non-volatile selection of QPI mode, by programming CR2NV[6] = 1, will also program QUAD_NV = 1 to change the non-volatile default to Quad data width mode. While QPI mode is selected by CR2V[6] = 1, the Quad_NV bit cannot be cleared to '0'.

Freeze Protection Default (FREEZE) CR1NV[0]: Provides the default state for the FREEZE bit in CR1V[0]. This bit is not user programmable.

9.6.3.2 Configuration Register 1 Volatile (CR1V)

Related Commands: Read Configuration Register (RDCR 35h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDCR command.

Table 25   Configuration Register 1 Volatile (CR1V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved for Future Use	Volatile		Reserved
6	RFU				
5	TBPROT	Volatile copy of TBPROT_O	Volatile Read Only		Not user writable. See CR1NV[5] TBPROT_O.
4	RFU	Reserved for Future Use	RFU		Reserved
3	BPNV	Volatile copy of BPNV_O	Volatile Read Only		Not user writable. See CR1NV[3] BPNV_O.
2	TBPARM	Volatile copy of TBPARM_O	Volatile Read Only	CR1NV	Not user writable. See CR1NV[2] TBPARM_O.
1	QUAD	Quad I/O Mode	Volatile		1 = Quad 0 = Serial The WRR command writes the Non-Volatile Quad bit (CR1NV[1]). See full description below.
0	FREEZE	Lock-Down Block Protection until next power cycle	Volatile		Lock current state of Block Protection control bits, and OTP regions. 1 = Block Protection and OTP locked 0 = Block Protection and OTP unlocked

TBPROT, BPNV, and TBPARM CR1V[5,3,2]: These bits are volatile copies of the related non-volatile bits of CR1NV. These bits track any changes to the related non-volatile version of these bits.

Quad Data Width (QUAD) CR1V[1]: When set to '1', this bit switches the data width of the device to 4-bit Quad mode. That is, WP# becomes IO2 and IO3 / RESET# becomes an active I/O signal when CS# is LOW or the RESET# input when CS# is HIGH. The WP# input is not monitored for its normal function and is internally set to HIGH (inactive). The commands for Serial, and Dual I/O Read still function normally but, there is no need to drive the WP# input for those commands when switching between commands using different data path widths. Similarly, there is no requirement to drive the IO3 / RESET# during those commands (while CS# is LOW).

The QUAD bit must be set to one when using the Quad I/O Read, DDR Quad I/O Read, QPI mode (CR2V[6] = 1), and Read Quad ID commands. While QPI mode is selected by CR2V[6] = 1, the Quad bit cannot be cleared to '0'. The WRR command writes the non-volatile version of the Quad bit (CR1NV[1]), which also causes an update to the volatile version CR1V[1]. The WRR command can not write the volatile version CR1V[1] without first affecting the non-volatile version CR1NV[1]. The WRAR command must be used when it is desired to write the volatile Quad bit CR1V[1] without affecting the non-volatile version CR1NV[1].

Freeze Protection (FREEZE) CR1V[0]: The Freeze Bit, when set to '1', locks the current state of the Block Protection control bits and OTP area:

- BPNV_2–0 bits in the non-volatile Status Register 1 (SR1NV[4:2])

- BP 2–0 bits in the volatile Status Register 1 (SR1V[4:2])

- TBPROT_O, TBPARM_O, and BPNV_O bits in the non-volatile Configuration Register (CR1NV[5,3, 2])

- TBPROT, TBPARM, and BPNV bits in the volatile Configuration Register (CR1V[5, 3, 2]) are indirectly protected in that they are shadows of the related CR1NV OTP bits and are read only

- the entire OTP memory space

- Any attempt to change the above listed bits while FREEZE = 1 is prevented:

- The WRR command does not affect the listed bits and no error status is set.

- The WRAR command does not affect the listed bits and no error status is set.

- The OTPP command, with an address within the OTP area, fails and the P-ERR status is set.

As long as the FREEZE bit remains cleared to logic 0 the Block Protection control bits and FREEZE are writable, and the OTP address space is programmable.

Once the FREEZE bit has been written to a logic 1 it can only be cleared to a logic 0 by a power-off to power-on cycle or a hardware reset. Software reset will not affect the state of the FREEZE bit.

The CR1V[0] FREEZE bit is volatile and the default state of FREEZE after power-on comes from FREEZE_D in CR1NV[0]. The FREEZE bit can be set in parallel with updating other values in CR1V by a single WRR or WRAR command.

The FREEZE bit does not prevent the WRR or WRAR commands from changing the SRWD_NV (SR1NV[7]), Quad_NV (CR1NV[1]), or QUAD (CR1V[1]) bits.

9.6.4 Configuration Register 2

Configuration Register 2 controls certain interface functions. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile version of the register provides the ability to set the POR, hardware reset, or software reset state of the controls. These configuration bits are OTP and may only have their default state changed to the opposite value one time during system configuration. The volatile version of the register controls the feature behavior during normal operation.

9.6.4.1 Configuration Register 2 Non-volatile (CR2NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 26   Configuration Register 2 Non-volatile (CR2NV)

Bits	Field name	Function	Type	Default state	Description
7	AL_NV	Address Length	OTP	0	1 = 4-byte address 0 = 3-byte address
6	QA_NV	QPI		0	1 = Enabled – QPI (4-4-4) protocol in use 0 = Disabled – Legacy SPI protocols in use, instruction is always serial on SI
5	IO3R_NV	IO3, IO7 Reset		0	1 = Enabled – IO3, IO7 is used as RESET# input when CS# is HIGH or Quad Mode is disabled CR1V[1] = 1 0 = Disabled – IO3, IO7 has no alternate function, hardware reset is disabled
4	RFU	Reserved		0	Reserved For Future Use.
3				1	0 to 15 latency (dummy) cycles following read address or continuous mode bits. Note that bit 3 has a default value of '1' and may be programmed one time to '0' but cannot be returned to '1'.
2	RL_NV	Read Latency		0	
1				0	
0				0	

Address Length Non-volatile CR2NV[7]: This bit controls the POR, hardware reset, or software reset state of the expected address length for all commands that require address and are not fixed 3-byte only or 4-byte (32 bit) only address. Most commands that need an address are legacy SPI commands that traditionally used 3-byte (24 bit) address. For device densities greater than 128 Mbit, a 4-byte address is required to access the entire memory array. The address length configuration bit is used to change most 3-byte address commands to expect 4-byte address. See **Table 47** for command address length. This non-volatile Address Length configuration bit enables the device to start immediately (boot) in 4-byte address mode rather than the legacy 3-byte address mode.

QPI Non-volatile CR2NV[6]: This bit controls the POR, hardware reset, or software reset state of the expected instruction width for all commands. Legacy SPI commands always send the instruction one bit wide (serial I/O) on the IO0 and IO4 signal. The S79FS01GS also supports the QPI mode in which all transfers between the host system and memory are 4 bits wide on IO0 to IO3, including all instructions. This non-volatile QPI configuration bit enables the device to start immediately (boot) in QQPIPI mode rather than the legacy serial instruction mode. When this bit is programmed to QPI mode, the QUAD_NV bit is also programmed to Quad mode (CR1NV[1] = 1). The recommended procedure for moving to QPI mode is to first use the WRAR command to set CR2V[6] = 1, QPI mode. The volatile register write for QPI mode has a short and well defined time (t_{CS}) to switch the device interface into QPI mode. Following commands can then be immediately sent in QPI protocol. The WRAR command can be used to program CR2NV[6] = 1, followed by polling of SR1V[0] to know when the programming operation is completed. Similarly, to exit QPI mode, the WRAR command is used to clear CR2V[6] = 0. CR2NV[6] cannot be erased to '0' because it is OTP.

IO3 Reset Non-volatile CR2NV[5]: This bit controls the POR, hardware reset, or software reset state of the IO3, IO7 signal behavior. Most legacy SPI devices do not have a hardware reset input signal due to the limited signal count and connections available in traditional SPI device packages. The S79FS01GS provides the option to use the IO3, IO7 signal as a hardware reset input when the IO3, IO7 signal is not in use for transferring information between the host system and the memory. This non-volatile IO3 Reset configuration bit enables the device to start immediately (boot) with IO3, IO7 enabled for use as a RESET# signal.

Read Latency Non-volatile CR2NV[3:0]: This bit controls the POR, hardware reset, or software reset state of the read latency (dummy cycle) delay in all variable latency read commands. The following read commands have a variable latency period between the end of address or mode and the beginning of read data returning to the host:

- Fast Read

- Dual I/O Read

- Quad I/O Read

- DDR Quad I/O Read

- OTPR

- RDAR

This non-volatile read latency configuration bit sets the number of read latency (dummy cycles) in use so the device can start immediately (boot) with an appropriate read latency for the host system.

Table 27   Latency Code (Cycles) versus Frequency

Latency Code	Read Command Maximum Frequency (MHz)		
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	Quad I/O (1-4-4) Quad I/O (4-4-4)	DDR Quad I/O (1-4-4) DDR Quad I/O (4-4-4)[38]
	Mode Cycles = 0	Mode Cycles = 2	Mode Cycles = 1
0	50	40	N/A
1	66	53	22
2	80	66	34
3	92	80	45
4	104	92	57
5	116	104	68
6	129	116	80
7	133	129	97
8	133	133	102
9	133	133	102
10	133	133	102
11	133	133	102
12	133	133	102
13	133	133	102
14	133	133	102
15	133	133	102

Notes

35. SCK frequency > 133 MHz SDR, or 102 MHz DDR is not supported by this family of devices.
36. The Quad I/O, QPI, DDR Quad I/O, and DDR QPI, command protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read Mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency.
37. Other read commands have fixed latency, e.g. Read always has zero read latency. RSFDP always has eight cycles of latency.
38. DDR QPI is only supported for Latency Cycles 1 through 7 and for clock frequency of up to 92 MHz.

9.6.4.2 Configuration Register 2 Volatile (CR2V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h), 4BAM.

Table 28 **Configuration Register 2 Volatile (CR2V)**

Bits	Field name	Function	Type	Default state	Description
7	AL	Address Length			1 = 4-byte address 0 = 3-byte address
6	QA	QPI			1 = Enabled – QPI (4-4-4) protocol in use 0 = Disabled – Legacy SPI protocols in use, instruction is always serial on SI
5	IO3R_S	IO3 Reset	Volatile	CR2NV	1 = Enabled – IO3 is used as RESET# input when CS# is HIGH or Quad Mode is disabled CR1V[1] = 1 0 = Disabled – IO3 has no alternate function, hardware reset is disabled
4	RFU	Reserved			Reserved for Future Use
3					
2	RL	Read Latency			0 to 15 latency (dummy) cycles following read address or continuous mode bits.
1					
0					

Address Length CR2V[7]: This bit controls the expected address length for all commands that require address and are not fixed 3-byte only or 4-byte (32 bit) only address. See **Table 47** for command address length. This volatile Address Length configuration bit enables the address length to be changed during normal operation. The 4-byte address mode (4BAM) command directly sets this bit into 4-byte address mode.

QPI CR2V[6]: This bit controls the expected instruction width for all commands. This volatile QPI configuration bit enables the device to enter and exit QPI mode during normal operation. When this bit is set to QPI mode, the QUAD bit is also set to Quad mode (CR1V[1] = 1). When this bit is cleared to legacy SPI mode, the QUAD bit is not affected.

IO3 Reset CR2V[5]: This bit controls the IO3, IO7 / RESET1#, RESET2# signal behavior. This volatile IO3, IO7 Reset configuration bit enables the use of IO3, IO7as a RESET# input during normal operation.

Read Latency CR2V[3:0]: This bit controls the read latency (dummy cycle) delay in variable latency read commands These volatile configuration bits enable the user to adjust the read latency during normal operation to optimize the latency for different commands or, at different operating frequencies, as needed.

9.6.5 Configuration Register 3

Configuration Register 3 controls certain command behaviors. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile register provides the POR, hardware reset, or software reset state of the controls. These configuration bits are OTP and may be programmed to their opposite state one time during system configuration if needed. The volatile version of Configuration Register 3 allows the configuration to be changed during system operation or testing.

9.6.5.1 Configuration Register 3 Non-volatile (CR3NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 29   Configuration Register 3 Non-volatile (CR3NV)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved		0	Reserved for Future Use
6	RFU	Reserved		0	Reserved for Future Use
5	BC_NV	Blank Check		0	1 = Blank Check during erase enabled 0 = Blank Check disabled
4	02h_NV	Page Buffer Wrap		0	1 = Wrap at 1024bytes 0 = Wrap at 512 bytes
3	20h_NV	8 KB Erase	OTP	0	1 = 8 KB Erase disabled (Uniform Sector Architecture) 0 = 8 KB Erase enabled (Hybrid Sector Architecture)
2	30h_NV	Clear Status / Resume Select		0	1 = 30h is Erase or Program Resume command 0 = 30h is clear status command
1	RFU	Reserved		1	Reserved for Future Use
0	F0h_NV	Legacy Software Reset Enable		0	1 = F0h Software Reset is enabled 0 = F0h Software Reset is disabled (ignored)

Blank Check Non-volatile CR3NV[5]: This bit controls the POR, hardware reset, or software reset state of the blank check during erase feature.

02h Non-volatile CR3NV[4]: This bit controls the POR, hardware reset, or software reset state of the page programming buffer address wrap point.

20h Non-volatile CR3NV[3]: This bit controls the POR, hardware reset, or software reset state of the availability of 8 KB parameter sectors in the main flash array address map.

30h Non-volatile CR3NV[2]: This bit controls the POR, hardware reset, or software reset state of the 30h instruction code is used.

F0h Non-volatile CR3NV[0]: This bit controls the POR, hardware reset, or software reset state of the availability of the Infineon FL-S family software reset instruction.

9.6.5.2 Configuration Register 3 Volatile (CR3V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 30   Configuration Register 3 Volatile (CR3V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Volatile	CR3NV	Reserved for Future Use
6	RFU	Reserved			Reserved for Future Use
5	BC_V	Blank Check			1 = Blank Check during erase enabled 0 = Blank Check disabled
4	02h_V	Page Buffer Wrap			1 = Wrap at 512 bytes 0 = Wrap at 256 bytes
3	20h_V	8 KB Erase	Volatile, Read Only		1 = 8 KB Erase disabled (Uniform Sector Architecture) 0 = 8 KB Erase enabled (Hybrid Sector Architecture)
2	30h_V	Clear Status / Resume Select	Volatile		1 = 30h is Erase or Program Resume command 0 = 30h is clear status command
1	RFU	Reserved			Reserved for Future Use
0	F0h_V	Legacy Software Reset Enable			1 = F0h Software Reset is enabled 0 = F0h Software Reset is disabled (ignored)

Blank Check Volatile CR3V[5]: This bit controls the blank check during erase feature. When this feature is enabled an erase command first evaluates the erase status of the sector. If the sector is found to have not completed its last erase successfully, the sector is unconditionally erased. If the last erase was successful, the sector is read to determine if the sector is still erased (blank). The erase operation is started immediately after finding any programmed zero. If the sector is already blank (no programmed zero bit found) the remainder of the erase operation is skipped. This can dramatically reduce erase time when sectors being erased do not need the erase operation. When enabled the blank check feature is used within the parameter erase, sector erase, and bulk erase commands. When blank check is disabled an erase command unconditionally starts the erase operation.

02h Volatile CR3V[4]: This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256-byte page programming buffer and defined that if data is loaded into the buffer beyond the 255-byte location, the address at which additional bytes are loaded would be wrapped to address zero of the buffer. The S79FS01GS provides a 512-byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256-byte boundary or to enable full use of the available 512-byte buffer by not wrapping the load address at the 256-byte boundary.

20h Volatile CR3V[3]: This bit controls the availability of 8 KB parameter sectors in the main flash array address map. The parameter sectors can overlay the highest or lowest 64 KB address range of the device or they can be removed from the address map so that all sectors are uniform size. This bit shall not be written to a value different than the value of CR3NV[3]. The value of CR3V[3] may only be changed by writing CR3NV[3].

30h Volatile CR3V[2]: This bit controls how the 30h instruction code is used. The instruction may be used as a clear status command or as an alternate program / erase resume command. This allows software compatibility with either Infineon legacy SPI devices or alternate vendor devices.

F0h Volatile CR3V[0]: This bit controls the availability of the Infineon FL-S family software reset instruction. The S79FS01GS supports the industry common 66h + 99h instruction sequence for software reset. This configuration bit allows the option to continue use of the legacy F0h single command for software reset.

9.6.6 Configuration Register 4

Configuration Register 4 controls the main flash array read commands burst wrap behavior. The burst wrap configuration does not affect commands reading from areas other than the main flash array e.g. read commands for registers or OTP array. The non-volatile version of the register provides the ability to set the start up (boot) state of the controls as the contents are copied to the volatile version of the register during the POR, hardware reset, or software reset. The volatile version of the register controls the feature behavior during normal operation. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The volatile version of the register can also be written by the Set Burst Length (C0h) command.

9.6.6.1 Configuration Register 4 Non-volatile (CR4NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 31   Configuration Register 4 Non-volatile (CR4NV)

Bits	Field name	Function	Type	Default state	Description
7				0	
6	OI_O	Output Impedance		0	See **Table 32**.
5				0	
4	WE_O	Wrap Enable	OTP	1	0 = Wrap Enabled 1 = Wrap Disabled
3	RFU	Reserved		0	Reserved for Future Use
2	RFU	Reserved		0	Reserved for Future Use
1				0	00 = 16-byte wrap
0	WL_O	Wrap Length		0	01 = 32-byte wrap 10 = 64-byte wrap 11 = 128-byte wrap

Output Impedance Non-volatile CR4NV[7:5]: These bits control the POR, hardware reset, or software reset state of the IO signal output impedance (drive strength). Multiple drive strength are available to help match the output impedance with the system PCB environment to minimize overshoot and ringing. These non-volatile output impedance configuration bits enable the device to start immediately (boot) with the appropriate drive strength.

Table 32   Output impedance control

CR4NV[7:5] Impedance selection	Typical impedance to V_{SS} (Ohms)	Typical impedance to V_{CC} (Ohms)	Notes
000	47	45	Factory default
001	124	105	–
010	71	64	–
011	47	45	–
100	34	35	–
101	26	28	–
110	22	24	–
111	18	21	–

Wrap Enable Non-volatile CR4NV[4]: This bit controls the POR, hardware reset, or software reset state of the wrap enable. The commands affected by Wrap Enable are: Quad I/O Read, and DDR Quad I/O Read. This configuration bit enables the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.

Wrap Length Non-volatile CR4NV[1:0]: These bits controls the POR, hardware reset, or software reset state of the wrapped read length and alignment. These non-volatile configuration bits enable the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.

9.6.6.2 Configuration Register 4 Volatile (CR4V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h), Set Burst Length (SBL C0h).

Table 33 **Configuration Register 4 Volatile (CR4V)**

Bits	Field name	Function	Type	Default state	Description
7	OI	Output impedance	Volatile	CR4NV	See **Table 32**
6					
5					
4	WE	Wrap Enable			0 = Wrap Enabled 1 = Wrap Disabled
3	RFU	Reserved			Reserved for Future Use
2	RFU	Reserved			Reserved for Future Use
1	WL	Wrap Length			00 = 16-byte wrap 01 = 32-byte wrap 10 = 64-byte wrap 11 = 128-byte wrap
0					

Output Impedance CR2V[7:5]: These bits control the IO signal output impedance (drive strength). This volatile output impedance configuration bit enables the user to adjust the drive strength during normal operation.

Wrap Enable CR4V[4]: This bit controls the burst wrap feature. This volatile configuration bit enables the device to enter and exit burst wrapped read mode during normal operation.

Wrap Length CR4V[1:0]: These bits controls the wrapped read length and alignment during normal operation. These volatile configuration bits enable the user to adjust the burst wrapped read length during normal operation.

9.6.7 ECC Status Register (ECCSR)

Related Commands: ECC Read (ECCRD 18h or 19h). ECCSR does not have user programmable non-volatile bits, all defined bits are volatile read only status. The default state of these bits are set by hardware.

The status of ECC in each ECC unit is provided by the 8-bit ECC Status Register (ECCSR). The ECC Register Read command is written followed by an ECC unit address. The contents of the status register then indicates, for the selected ECC unit, whether there is an error in the ECC, the ECC unit data, or that ECC is disabled for that ECC unit.

Table 34   ECC Status Register (ECCSR)

Bits	Field name	Function	Type	Default state	Description
7 to 3	RFU	Reserved		0	Reserved for Future Use
2	EECC	Error in ECC	Volatile, Read only	0	1 = Single Bit Error found in the ECC unit error correction code 0 = No error
1	EECCD	Error in ECC unit data	Volatile, Read only	0	1 = Single Bit Error corrected in ECC unit data 0 = No error
0	ECCDI	ECC Disabled	Volatile, Read only	0	1 = ECC is disabled in the selected ECC unit 0 = ECC is enabled in the selected ECC unit

ECCSR[2] = 1 indicates an error was corrected in the ECC. ECCSR[1] = 1 indicates an error was corrected in the ECC unit data. ECCSR[0] = 1 indicates the ECC is disabled. The default state of '0' for all these bits indicates no failures and ECC is enabled.

The ECCSR[7:3] are reserved. These have undefined high or low values that can change from one ECC status read to another. These bits should be treated as "don't care" and ignored by any software reading status.

9.6.8 ASP Register (ASPR)

Related Commands: ASP Read (ASPRD 2Bh) and ASP Program (ASPP 2Fh), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The ASP register is a 16-bit OTP memory location used to permanently configure the behavior of Advanced Sector Protection (ASP) features. ASPR does not have user programmable volatile bits, all defined bits are OTP.

The default state of the ASPR bits are programmed by Infineon.

Table 35   ASP Register (ASPR)

Bits	Field name	Function	Type	Default state	Description
15 to 9	RFU	Reserved	OTP	1	Reserved for Future Use
8	RFU	Reserved	OTP	1	Reserved for Future Use
7	RFU	Reserved	OTP	1	Reserved for Future Use
6	RFU	Reserved	OTP	1	Reserved for Future Use
5	RFU	Reserved	OTP	1	Reserved for Future Use
4	RFU	Reserved	OTP	1	Reserved for Future Use
3	RFU	Reserved	OTP	1	Reserved for Future Use
2	PWDMLB	Password Protection Mode Lock Bit	OTP	1	0 = Password Protection Mode permanently enabled. 1 = Password Protection Mode not permanently enabled.
1	PSTMLB	Persistent Protection Mode Lock Bit	OTP	1	0 = Persistent Protection Mode permanently enabled. 1 = Persistent Protection Mode not permanently enabled.
0	RFU	Reserved	RFU	1	Reserved for Future Use

Password Protection Mode Lock Bit (PWDMLB) ASPR[2]: When programmed to '0', the Password Protection Mode is permanently selected.

Persistent Protection Mode Lock Bit (PSTMLB) ASPR[1]: When programmed to '0', the Persistent Protection Mode is permanently selected.

PWDMLB (ASPR[2]) and PSTMLB (ASPR[1]) are mutually exclusive, only one may be programmed to zero.

ASPR bits may only be programmed while ASPR[2:1] = 11b. Attempting to program ASPR bits when ASPR[2:1] is not = 11b will result in a programming error with P_ERR (SR1V[6]) set to '1'. After the ASP protection mode is selected by programming ASPR[2:1] = 10b or 01b, the state of all ASPR bits are locked and permanently protected from further programming. Attempting to program ASPR[2:1] = 00b will result in a programming error with P_ERR (SR1V[6]) set to '1'.

Similarly, OTP configuration bits listed in the ASP Register description (see **"ASP Register"** on page 75), may only be programmed while ASPR[2:1] = 11b. The OTP configuration must be selected before selecting the ASP protection mode. The OTP configuration bits are permanently protected from further change when the ASP protection mode is selected. Attempting to program these OTP configuration bits when ASPR[2:1] is not = 11b will result in a programming error with P_ERR (SR1V[6]) set to '1'.

The ASP protection mode should be selected during system configuration to ensure that a malicious program does not select an undesired protection mode at a later time. By locking all the protection configuration via the ASP mode selection, later alteration of the protection methods by malicious programs is prevented.

9.6.9 Password Register (PASS)

Related Commands: Password Read (PASSRD E7h) and Password Program (PASSP E8h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). The PASS register is a 64-bit OTP memory location used to permanently define a password for the Advanced Sector Protection (ASP) feature. PASS does not have user programmable volatile bits, all defined bits are OTP. A volatile copy of PASS is used to satisfy read latency requirements but the volatile register is not user writable or further described.

Table 36   Password Register (PASS)

Bits	Field name	Function	Type	Default state	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFF–FFFFFFFFh	Non-volatile OTP storage of 64-bit password. The password is no longer readable after the password protection mode is selected by programming ASP register bit 2 to '0'.

9.6.10 PPB Lock Register (PPBL)

Related Commands: PPB Lock Read (PLBRD A7h, PLBWR A6h), Read Any Register (RDAR 65h).

PPBL does not have separate user programmable non-volatile bits, all defined bits are volatile read only status. The default state of the RFU bits is set by hardware. The default state of the PPBLOCK bit is defined by the ASP protection mode bits in ASPR[2:1]. There is no non-volatile version of the PPBL register.

The PPBLOCK bit is used to protect the PPB bits. When PPBL[0] = 0, the PPB bits can not be programmed.

Table 37   PPB Lock Register (PPBL)

Bits	Field name	Function	Type	Default state	Description
7 to 1	RFU	Reserved	Volatile	00h	Reserved for Future Use
0	PPBLOCK	Protect PPB Array	Volatile Read Only	ASPR[2:1] = 1xb = Persistent Protection Mode = 1 ASPR[2:1] = 01b = Password Protection Mode = 0	0 = PPB array protected 1 = PPB array may be programmed or erased.

9.6.11 PPB Access Register (PPBAR)

Related Commands: PPB Read (PPBRD FCh or 4PPBRD E2h), PPB Program (PPBP FDh or 4PPBP E3h), PPB Erase (PPBE E4h).

PPBAR does not have user writable volatile bits, all PPB array bits are non-volatile. The default state of the PPB array is erased to FFh by Infineon. There is no volatile version of the PPBAR register.

Table 38   PPB Access Register (PPBAR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	PPB	Read or Program per sector PPB	Non-volatile	FFh	00h = PPB for the sector addressed by the PPBRD or PPBP command is programmed to '0', protecting that sector from program or erase operations. FFh = PPB for the sector addressed by the PPBRD command is '1', not protecting that sector from program or erase operations.

9.6.12 DYB Access Register (DYBAR)

Related Commands: DYB Read (DYBRD FAh or 4DYBRD E0h) and DYB Write (DYBWR FBh or 4DYBWR E1h).

DYBAR does not have user programmable non-volatile bits, all bits are a representation of the volatile bits in the DYB array. The default state of the DYB array bits is set by hardware. There is no non-volatile version of the DYBAR register.

Table 39   DYB Access Register (DYBAR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	DYB	Read or Write per sector DYB	Volatile	FFh	00h = DYB for the sector addressed by the DYBRD or DYBWR command is cleared to '0', protecting that sector from program or erase operations. FFh = DYB for the sector addressed by the DYBRD or DYBWR command is set to '1', not protecting that sector from program or erase operations.

9.6.13 SPI DDR Data Learning Registers

Related Commands: Program NVDLR (PNVDLR 43h), Write VDLR (WVDLR 4Ah), Data Learning Pattern Read (DLPRD 41h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The Data Learning Pattern (DLP) resides in an 8-bit non-volatile Data Learning Register (NVDLR) as well as an 8-bit Volatile Data Learning Register (VDLR). When shipped from Infineon, the NVDLR value is 00h. Once programmed, the NVDLR cannot be reprogrammed or erased; a copy of the data pattern in the NVDLR will also be written to the VDLR. The VDLR can be written to at any time, but on power cycles the data pattern will revert back to what is in the NVDLR. During the learning phase described in the SPI DDR modes, the DLP will come from the VDLR. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100) then during the first clock edge all IO's will output '0'; subsequently, the 2nd clock edge all I/O's will output '0', the 3rd will output '1', and so on.

When the VDLR value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

Table 40   Non-volatile Data Learning Register (NVDLR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	NVDLP	Non-volatile Data Learning Pattern	OTP	00h	OTP value that may be transferred to the host during DDR read command latency (dummy) cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits.

Table 41   Volatile Data Learning Register (VDLR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	VDLP	Volatile Data Learning Pattern	Volatile	Takes the value of NVDLR during POR or Reset	Volatile copy of the NVDLP used to enable and deliver the Data Learning Pattern (DLP) to the outputs. The VDLP may be changed by the host during system operation.

10 Data protection

10.1 Secure silicon region (OTP)

The device has a 2048-byte OTP address space that is separate from the main flash array. The OTP area is divided into 32, individually lockable, 64-byte aligned and length regions.

The OTP memory space is intended for increased system security. OTP values can "mate" a flash component with the system CPU/ASIC to prevent device substitution. See **"OTP address space"** on page 45, **"OTP Program (OTPP 42h)"** on page 125, and **"OTP Read (OTPR 4Bh)"** on page 125.

10.1.1 Reading OTP memory space

The OTP Read command uses the same protocol as Fast Read. OTP Read operations outside the valid 2 KB OTP address range will yield indeterminate data.

10.1.2 Programming OTP memory space

The protocol of the OTP programming command is the same as Page Program. The OTP Program command can be issued multiple times to any given OTP address, but this address space can never be erased.

Automatic ECC is programmed on the first programming operation to each 16 byte region. Programming within a 16 byte region more than once disables the ECC. It is recommended to program each 16 byte portion of each 32 byte region once so that ECC remains enabled to provide the best data integrity.

The valid address range for OTP Program is depicted in **Figure 36**. OTP Program operations outside the valid OTP address range will be ignored, without P_ERR in SR1V set to '1'. OTP Program operations within the valid OTP address range, while FREEZE = 1, will fail with P_ERR in SR1V set to '1'. The OTP address space is not protected by the selection of an ASP protection mode. The Freeze bit (CR1V[0]) may be used to protect the OTP Address Space.

10.1.3 Infineon programmed random number

Infineon standard practice is to program the low order 16 bytes of the OTP memory space (locations 0x0 to 0xF) with a 128-bit random number using the Linear Congruential Random Number method. The seed value for the algorithm is a random number concatenated with the day and time of tester insertion.

10.1.4 Lock bytes

The LSb of each Lock byte protects the lowest address region related to the byte, the MSb protects the highest address region related to the byte. The next higher address byte similarly protects the next higher eight regions. The LSb bit of the lowest address Lock Byte protects the higher address 16 bytes of the lowest address region. In other words, the LSb of location 0x10 protects all the Lock Bytes and RFU bytes in the lowest address region from further programming. See **"OTP address space"** on page 45.

10.2   Write Enable command

The Write Enable (WREN) command must be written prior to any command that modifies non-volatile data. The WREN command sets the Write Enable Latch (WEL) bit.

The WEL bit is cleared to '0' (disables writes) during power-up, hardware reset, or after the device completes the following commands:

• Reset

• Page Program (PP or 4PP)

• Parameter 8 KB Erase (P4E or 4P4E)

• Sector Erase (SE or 4SE)

• Bulk Erase (BE)

• Write Disable (WRDI)

• Write Registers (WRR)

• Write Any Register (WRAR)

• OTP Byte Programming (OTPP)

• Advanced Sector Protection Register Program (ASPP)

• Persistent Protection Bit Program (PPBP)

• Persistent Protection Bit Erase (PPBE)

• Password Program (PASSP)

• Program Non-volatile Data Learning Register (PNVDLR)

10.3 Block Protection

The Block Protect bits (Status Register bits BP2, BP1, BP0) in combination with the Configuration Register TBPROT_O bit can be used to protect an address range of the main flash array from program and erase operations. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range is selected by the TBPROT_O bit of the Configuration Register (CR1NV[5]).

Table 42   Upper array start of protection (TBPROT_O = 0)

Status register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		S79FS01GS 1024 Mb
0	0	0	None	0
0	0	1	Upper 64th	2048
0	1	0	Upper 32nd	4096
0	1	1	Upper 16th	8192
1	0	0	Upper 8th	16384
1	0	1	Upper 4th	32768
1	1	0	Upper Half	65536
1	1	1	All Sectors	131072

Table 43   Lower array start of protection (TBPROT_O = 1)

Status register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		FS512S 512 Mb
0	0	0	None	0
0	0	1	Lower 64th	2048
0	1	0	Lower 32nd	4096
0	1	1	Lower 16th	8192
1	0	0	Lower 8th	16384
1	0	1	Lower 4th	32768
1	1	0	Lower Half	65536
1	1	1	All Sectors	131072

When Block Protection is enabled (i.e., any BP2–0 are set to '1'), Advanced Sector Protection (ASP) can still be used to protect sectors not protected by the Block Protection scheme. In the case that both ASP and Block Protection are used on the same sector the logical OR of ASP and Block Protection related to the sector is used.

10.3.1 Freeze bit

Bit 0 of Configuration Register 1 (CR1V[0]) is the FREEZE bit. The Freeze Bit, when set to '1', locks the current state of the Block Protection control bits and OTP area until the next power off-on cycle (additional details in **"Configuration Register 1 Volatile (CR1V)"** on page 55).

10.3.2 Write Protect signal

The Write Protect (WP#) input in combination with the Status Register Write Disable (SRWD) bit (SR1NV[7]) provide hardware input signal controlled protection. When WP# is LOW and SRWD is set to '1', Status Register-1 (SR1NV and SR1V) and Configuration Register 1 (CR1NV and CR1V) are protected from alteration. This prevents disabling or changing the protection defined by the Block Protect bits. See **Table 22**.

10.4 Advanced sector protection

Advanced sector protection (ASP) is the name used for a set of independent hardware and software methods used to disable or enable programming or erase operations, individually, in any or all sectors.

Every main flash array sector has a non-volatile Persistent Protection Bit (PPB) and a volatile Dynamic Protection Bit (DYB) associated with it. When either bit is '0', the sector is protected from program and erase operations. The PPB bits are protected from program and erase when the volatile PPB Lock bit is '0'. There are two methods for managing the state of the PPB Lock bit: Password Protection, and Persistent Protection. An overview of these methods is shown in **Figure 38**.

Block Protection and ASP protection settings for each sector are logically ORed to define the protection for each sector i.e. if either mechanism is protecting a sector the sector cannot be programmed or erased. Refer to **"Block Protection"** on page 72 for full details of the BP2–0 bits.
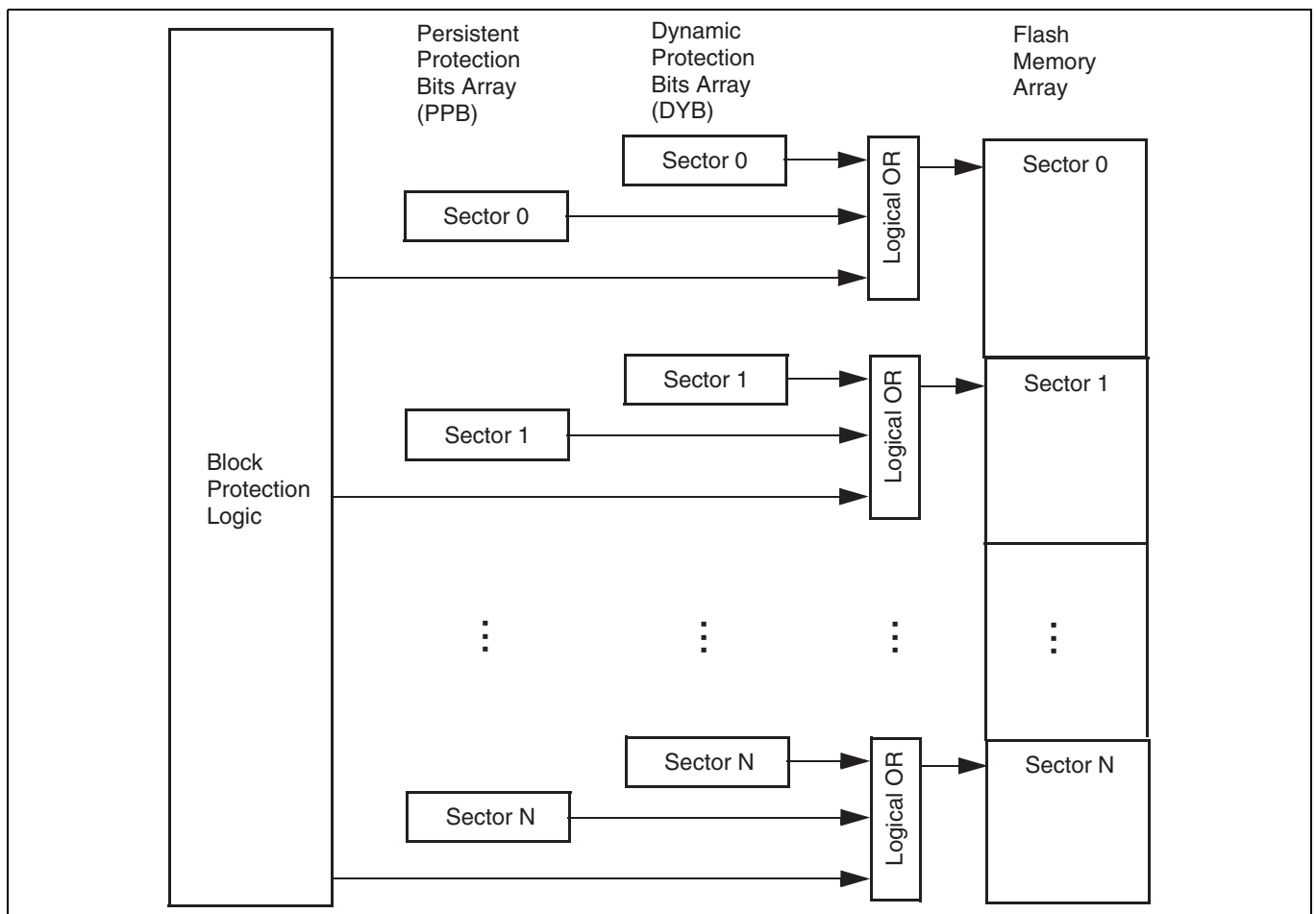
Figure 37   Sector protection control
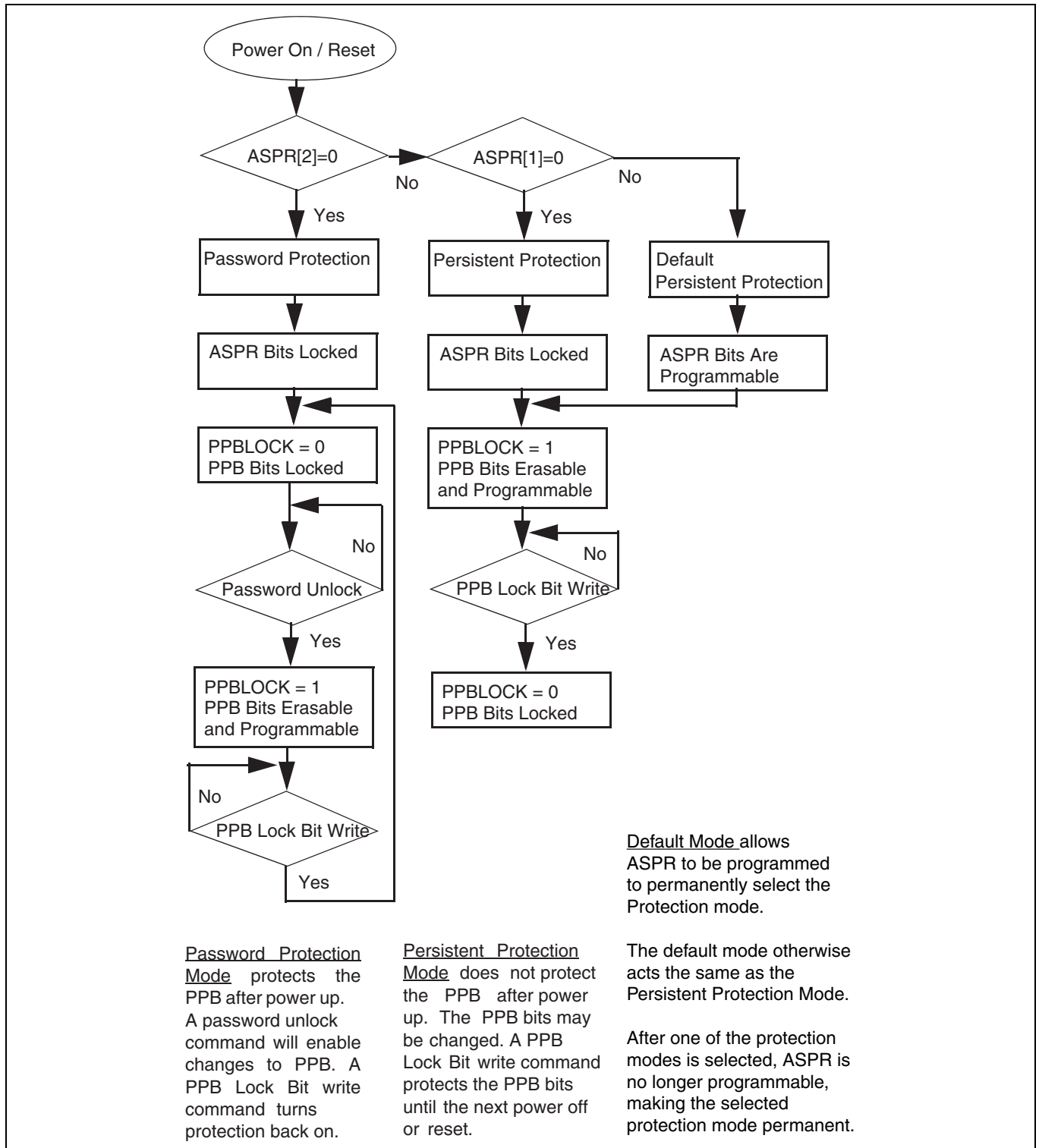
Figure 38   Advanced sector protection overview

The Persistent Protection method sets the PPB Lock bit to '1' during POR, or Hardware Reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB Lock bit to '0' to protect the PPB. There is no command in the Persistent Protection method to set the PPB Lock bit to '1', therefore the PPB Lock bit will remain at '0' until the next power-off or hardware reset. The Persistent Protection method allows boot code the option of changing sector protection by programming or erasing the PPB, then protecting the PPB from further change for the remainder of normal system operation by clearing the PPB Lock bit to '0'. This is sometimes called Boot-code controlled sector protection.

The Password method clears the PPB Lock bit to '0' during POR, or Hardware Reset to protect the PPB. A 64-bit password may be permanently programmed and hidden for the password method. A command can be used to provide a password for comparison with the hidden password. If the password matches, the PPB Lock bit is set to '1' to unprotect the PPB. A command can be used to clear the PPB Lock bit to '0'. This method requires use of a password to control PPB protection.

The selection of the PPB Lock bit management method is made by programming OTP bits in the ASP Register so as to permanently select the method used.

10.4.1   ASP Register

The ASP register is used to permanently configure the behavior of Advanced Sector Protection (ASP) features (see **Table 35**).

As shipped from the factory, all devices default ASP to the Persistent Protection mode, with all sectors unprotected, when power is applied. The device programmer or host system must then choose which sector protection method to use. Programming either of the, one-time programmable, Protection Mode Lock Bits, locks the part permanently in the selected mode:

- ASPR[2:1] = '11' = No ASP mode selected, Persistent Protection Mode is the default.

- ASPR[2:1] = '10' = Persistent Protection Mode permanently selected.

- ASPR[2:1] = '01' = Password Protection Mode permanently selected.

- ASPR[2:1] = '00' is an Illegal condition, attempting to program more than one bit to zero results in a programming failure.

ASP register programming rules:

- If the password mode is chosen, the password must be programmed prior to setting the Protection Mode Lock Bits.

- Once the Protection Mode is selected, the following OTP configuration register bits are permanently protected from programming and no further changes to the OTP register bits is allowed:
  - CR1NV[5:2]
  - CR2NV
  - CR3NV
  - CR4NV
  - ASPR
  - PASS
  - NVDLR
  - If an attempt to change any of the registers above, after the ASP mode is selected, the operation will fail and P_ERR (SR1V[6]) will be set to '1'.

The programming time of the ASP Register is the same as the typical page programming time. The system can determine the status of the ASP register programming operation by reading the WIP bit in the Status Register. See **"Status Register 1 Non-volatile (SR1NV)"** on page 48 for information on WIP. See **"Sector protection states summary"** on page 77.

10.4.2 Persistent protection bits

The persistent protection bits (PPB) are located in a separate non-volatile flash array. One of the PPB bits is related to each sector. When a PPB is '0', its related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire sector must be erased at the same time. The PPB have the same program and erase endurance as the main flash memory array. Pre-programming and verification prior to erasure are handled by the device.

Programming a PPB bit requires the typical page programming time. Erasing all the PPBs requires typical sector erase time. During PPB bit programming and PPB bit erasing, status is available by reading the Status register. Reading of a PPB bit requires the initial access time of the device.

Notes

- Each PPB is individually programmed to '0' and all are erased to '1' in parallel.

- If the PPB Lock bit is '0', the PPB Program or PPB Erase command does not execute and fails without programming or erasing the PPB.

- The state of the PPB for a given sector can be verified by using the PPB Read command.

10.4.3 Dynamic protection bits

Dynamic protection bits are volatile and unique for each sector and can be individually modified. DYB only control the protection for sectors that have their PPB set to '1'. By issuing the DYB Write command, a DYB is cleared to '0' or set to '1', thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The DYBs can be set or cleared as often as needed as they are volatile bits.

10.4.4 PPB Lock Bit (PPBL[0])

The PPB Lock Bit is a volatile bit for protecting all PPB bits. When cleared to '0', it locks all PPBs, when set to '1', it allows the PPBs to be changed. See **"PPB Lock Register (PPBL)"** on page 67 for more information.

The PLBWR command is used to clear the PPB Lock bit to '0'. The PPB Lock Bit must be cleared to '0' only after all the PPBs are configured to the desired settings.

In Persistent Protection mode, the PPB Lock is set to '1' during POR or a hardware reset. When cleared to '0', no software command sequence can set the PPB Lock bit to '1', only another hardware reset or power-up can set the PPB Lock bit.

In the Password Protection mode, the PPB Lock bit is cleared to '0' during POR or a hardware reset. The PPB Lock bit can only be set to '1' by the Password Unlock command.

10.4.5   Sector protection states summary

Each sector can be in one of the following protection states:

• Unlocked: The sector is unprotected and protection can be changed by a simple command. The protection state defaults to unprotected when the device is shipped from Infineon.

• Dynamically Locked: A sector is protected and protection can be changed by a simple command. The protection state is not saved across a power cycle or reset.

• Persistently Locked: A sector is protected and protection can only be changed if the PPB Lock Bit is set to '1'. The protection state is non-volatile and saved across a power cycle or reset. Changing the protection state requires programming and or erase of the PPB bits.

Table 44   Sector protection states

Protection bit values			Sector state
PPB lock	**PPB**	**DYB**	
1	1	1	Unprotected – PPB and DYB are changeable
1	1	0	Protected – PPB and DYB are changeable
1	0	1	Protected – PPB and DYB are changeable
1	0	0	Protected – PPB and DYB are changeable
0	1	1	Unprotected – PPB not changeable, DYB is changeable
0	1	0	Protected – PPB not changeable, DYB is changeable
0	0	1	Protected – PPB not changeable, DYB is changeable
0	0	0	Protected – PPB not changeable, DYB is changeable

10.4.6   Persistent Protection mode

The Persistent Protection method sets the PPB Lock bit to '1' during POR or Hardware Reset so that the PPB bits are unprotected by a device hardware reset. Software reset does not affect the PPB Lock bit. The PLBWR command can clear the PPB Lock bit to '0' to protect the PPB. There is no command to set the PPB Lock bit therefore the PPB Lock bit will remain at '0' until the next power-off or hardware reset.

10.4.7   Password Protection mode

Password Protection mode allows an even higher level of security than the Persistent Sector Protection mode, by requiring a 64-bit password for unlocking the PPB Lock bit. In addition to this password requirement, after power up and hardware reset, the PPB Lock bit is cleared to '0' to ensure protection at power-up. Successful execution of the Password Unlock command by entering the entire password sets the PPB Lock bit to '1', allowing for sector PPB modifications.

Password protection notes:

• Once the Password is programmed and verified, the Password Mode (ASPR[2] = 0) must be set in order to prevent reading the password.

• The Password Program Command is only capable of programming 0s. Programming '1' after a cell is programmed as '0' results in the cell left as '0' with no programming error set.

• The password is all 1s when shipped from Infineon. It is located in its own memory space and is accessible through the use of the Password Program, Password Read, RDAR, and WRAR commands.

• All 64-bit password combinations are valid as a password.

• The Password mode, once programmed, prevents reading the 64-bit password and further password programming. All further program and read commands to the password region are disabled and these commands are ignored or return undefined data. There is no means to verify what the password is after the Password Mode Lock Bit is selected. Password verification is only allowed before selecting the Password Protection mode.

• The Protection Mode Lock Bits are not erasable.

• The exact password must be entered in order for the unlocking function to occur. If the password unlock command provided password does not match the hidden internal password, the unlock operation fails in the same manner as a programming operation on a protected sector. The P_ERR bit is set to one, the WIP Bit remains set, and the PPB Lock bit remains cleared to '0'.

• The Password Unlock command cannot be accepted any faster than once every 100 μs ± 20 μs. This makes it take an unreasonably long time (58 million years) for a hacker to run through all the 64-bit combinations in an attempt to correctly match a password. The Read Status Register 1 command may be used to read the WIP bit to determine when the device has completed the password unlock command or is ready to accept a new password command. When a valid password is provided the password unlock command does not insert the 100 μs delay before returning the WIP bit to '0'.

• If the password is lost after selecting the Password mode, there is no way to set the PPB Lock bit.

10.5 Recommended protection process

During system manufacture, the flash device configuration should be defined by:

- Programming the OTP configuration bits in CR1NV[5, 3:2], CR2NV, CR3NV, and CR4NV as desired.

- Program the secure silicon region (OTP area) as desired.

- Program the PPB bits as desired via the PPBP command.

- Program the NVDLR if it will be used in DDR read commands.

- Program the Password register (PASS) if password protection will be used.

- Program the ASP Register as desired, including the selection of the persistent or password ASP protection mode in ASPR[2:1]. It is very important to explicitly select a protection mode so that later accidental or malicious programming of the ASP register and OTP configuration is prevented. This is to ensure that only the intended OTP protection and configuration features are enabled. During system power up and boot code execution:

- Trusted boot code can determine whether there is any need to program additional SSR (OTP area) information. If no SSR changes are needed the FREEZE bit (CR1V[0]) can be set to '1' to protect the SSR from changes during the remainder of normal system operation while power remains on.

- If the persistent protection mode is in use, trusted boot code can determine whether there is any need to modify the persistent (PPB) sector protection via the PPBP or PPBE commands. If no PPB changes are needed the PPBLOCK bit can be cleared to '0' via the PPBL to protect the PPB bits from changes during the remainder of normal system operation while power remains on.

- The dynamic (DYB) sector protection bits can be written as desired via the DYBAR.

11 Commands

All communication between the host system and S79FS01GS memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction

- address and instruction modifier (mode)

- data

Single bit wide commands start with an instruction and may provide an address or data, all sent only on the IO0 and IO4 signal. Data may be sent back to the host serially on the IO1 and IO5 signal. This is referenced as a 1-1-1 command protocol for single bit width instruction, single bit width address and modifier, single bit data.

Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO4 or, Data is returned to the host similarly as bit pairs on IO0 and IO4 or, four-bit (nibble) groups on IO0–IO3 and IO4–IO7. This is referenced as 1-4-4 for Quad I/O command protocols.

The S79FS01GS also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol for each Quad SPI die.

11.1 Command set summary

11.1.1 Extended addressing

To accommodate addressing above 128 Mb, there are two options:

1. Instructions that always require a 4-byte address, used to access up to 32 Gb of memory.

Table 45   Instructions and corresponding details

Command name	Function	Instruction (Hex)
4READ	Read	13
4FAST_READ	Read Fast	0C
4QIOR	Quad I/O Read	EC
4DDRQIOR	DDR Quad I/O Read	EE
4PP	Page Program	12
4P4E	Parameter 8 KB Erase	21
4SE	Erase 512 KB	DC
4ECCRD	ECC Status Read	18
4DYBRD	DYB Read	E0
4DYBWR	DYBWR	E1
4PPBRD	PPB Read	E2
4PPBP	PPB Program	E3

2. A 4-byte address mode for backward compatibility to the 3-byte address instructions. The standard 3-byte instructions can be used in conjunction with a 4-byte address mode controlled by the Address Length configuration bit (CR2V[7]). The default value of CR2V[7] is loaded from CR2NV[7] (following power up, hardware reset, or software reset), to enable default 3-byte (24-bit) or 4-byte (32 bit) addressing. When the address length (CR2V[7]) set to '1', the legacy commands are changed to require 4 bytes (32-bits) for the address field. The following instructions can be used in conjunction with the 4-byte address mode configuration to switch from 3 bytes to 4 bytes of address field.

Table 46   Instructions and corresponding details

Command name	Function	Instruction (Hex)
READ	Read	03
FAST_READ	Read Fast	0B
QIOR	Quad I/O Read	EB
DDRQIOR	DDR Quad I/O Read)	ED
PP	Page Program	02
P4E	Parameter 8 KB Erase	20
SE	Erase 512 KB	D8
RDAR	Read Any Register	65
WRAR	Write Any Register	71
EES	Evaluate Erase Status	D0
OTPP	OTP Program	42
OTPR	OTP Read	4B
ECCRD	ECC Status Read	19
DYBRD	DYB Read	FA
DYBWR	DYBWR	FB
PPBRD	PPB Read	FC
PPBP	PPB Program	FD

11.1.2   Dual-Quad SPI devices

The Dual-Quad SPI device contains two Quad SPI devices (Quad SPI-1 and Quad SPI-2)) stacked in a Dual Die Package (DDP). Both devices are selected to decode each command instruction and address when the CS# signal, shared by both devices, goes low. Quad SPI-1 device responds to commands, address, data in and data out on IO0–IO3. Quad SPI-2 device responds to commands, address, data in and data out on IO4–IO7. All commands are executed by both devices in parallel.

Both Quad SPI devices must be configured, by writing to the various status and configuration registers in parallel, to define the same overall sector map and behavior of both devices.

11.1.3 Command summary sorted by function

Table 47   S79FS01GS command set (sorted by function)[39]

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID and JEDEC CFI)	9F	133	0	Yes
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5A	50	3	Yes
	RDQID	Read Quad ID	AF	133	0	Yes
Register Access	RDSR1	Read Status Register 1	05	133	0	Yes
	RDSR2	Read Status Register 2	07	133	0	No
	RDCR	Read Configuration Register 1	35	133	0	No
	RDAR	Read Any Register	65	133	3 or 4	Yes
	WRR	Write Register (Status 1, Configuration 1)	01	133	0	Yes
	WRDI	Write Disable	04	133	0	Yes
	WREN	Write Enable	06	133	0	Yes
	WRAR	Write Any Register	71	133	3 or 4	Yes
	CLSR	Clear Status Register 1 — Erase / Program Fail Reset This command may be disabled and the instruction value instead used for a program / erase resume command - see **"Configuration Register 3"** on page 61.	30	133	0	Yes
	CLSR	Clear Status Register 1 (Alternate instruction) — Erase / Program Fail Reset	82	133	0	Yes
	4BAM	Enter 4-byte Address Mode	B7	133	0	No
	SBL	Set Burst Length	C0	133	0	No
	EES	Evaluate Erase Status	D0	133	3 or 4	Yes
	ECCRD	ECC Read	19	133	3 or 4	Yes
	4ECCRD	ECC Read	18	133	4	Yes
	DLPRD	Data Learning Pattern Read	41	133	0	No
	PNVDLR	Program NV Data Learning Register	43	133	0	No
	WVDLR	Write Volatile Data Learning Register	4A	133	0	No
Read Flash Array	READ	Read	03	50	3 or 4	No
	4READ	Read	13	50	4	No
	FAST_READ	Fast Read	0B	133	3 or 4	No
	4FAST_READ	Fast Read	0C	133	4	No
	QIOR	Quad I/O Read	EB	133	3 or 4	Yes
	4QIOR	Quad I/O Read	EC	133	4	Yes
	DDRQIOR	DDR Quad I/O Read	ED	80	3 or 4	Yes
	4DDRQIOR	DDR Quad I/O Read	EE	80	4	Yes

Note
39.Commands not supported In QPI mode, have undefined behavior if sent when the device is in QPI mode.

Table 47   S79FS01GS command set (sorted by function)[39] (Continued)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Program Flash Array	PP	Page Program	02	133	3 or 4	Yes
	4PP	Page Program	12	133	4	Yes
Erase Flash Array	P4E	Parameter 8 KB-sector Erase	20	133	3 or 4	Yes
	4P4E	Parameter 8KB-sector Erase	21	133	4	Yes
	SE	Erase 512 KB	D8	133	3 or 4	Yes
	4SE	Erase 512 KB	DC	133	4	Yes
	BE	Bulk Erase	60	133	0	Yes
	BE	Bulk Erase (alternate instruction)	C7	133	0	Yes
Erase /Program Suspend /Resume	EPS	Erase / Program Suspend	75	133	0	Yes
	EPS	Erase / Program Suspend (alternate instruction)	85	133	0	Yes
	EPS	Erase / Program Suspend (alternate instruction	B0	133	0	Yes
	EPR	Erase / Program Resume	7A	133	0	Yes
	EPR	Erase / Program Resume (alternate instruction)	8A	133	0	Yes
	EPR	Erase / Program Resume (alternate instruction This command may be disabled and the instruction value instead used for a clear status command — see **"Configuration Register 3"** on page 61.	30	133	0	Yes
OTP Array	OTPP	OTP Program	42	133	3 or 4	No
	OTPR	OTP Read	4B	133	3 or 4	No
Advanced Sector Protection	DYBRD	DYB Read	FA	133	3 or 4	Yes
	4DYBRD	DYB Read	E0	133	4	Yes
	DYBWR	DYB Write	FB	133	3 or 4	Yes
	4DYBWR	DYB Write	E1	133	4	Yes
	PPBRD	PPB Read	FC	133	3 or 4	No
	4PPBRD	PPB Read	E2	133	4	No
	PPBP	PPB Program	FD	133	3 or 4	No
	4PPBP	PPB Program	E3	133	4	No
	PPBE	PPB Erase	E4	133	0	No
	ASPRD	ASP Read	2B	133	0	No
	ASPP	ASP Program	2F	133	0	No
	PLBRD	PPB Lock Bit Read	A7	133	0	No
	PLBWR	PPB Lock Bit Write	A6	133	0	No
	PASSRD	Password Read	E7	133	0	No
	PASSP	Password Program	E8	133	0	No
	PASSU	Password Unlock	E9	133	0	No

Note

39.Commands not supported In QPI mode, have undefined behavior if sent when the device is in QPI mode.

Commands

Table 47   **S79FS01GS command set (sorted by function)**[39] (Continued)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Reset	RSTEN	Software Reset Enable	66	133	0	Yes
	RST	Software Reset	99	133	0	Yes
	RESET	Legacy Software Reset	F0	133	0	No
	MBR	Mode Bit Reset	FF	133	0	Yes
DPD	DPD	Enter Deep Power-Down Mode	B9	133	0	Yes
	RES	Release from Deep Power-Down Mode	AB	133	0	Yes

Note
39.Commands not supported In QPI mode, have undefined behavior if sent when the device is in QPI mode.

11.1.4 Read Device Identification

There are multiple commands to read information about the device manufacturer, device type, and device features. SPI memories from different vendors have used different commands and formats for reading information about the memories. The S79FS01GS supports the three device information commands.

11.1.5 Register read or write

There are multiple registers for reporting embedded operation status or controlling device configuration options. There are commands for reading or writing these registers. Registers contain both volatile and non-volatile bits. Non-volatile bits in registers are automatically erased and programmed as a single (write) operation.

11.1.5.1 Monitoring operation status

The host system can determine when a write, program, erase, suspend or other embedded operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register 1 command or Read Any Register command provides the state of the WIP bit. The program error (P_ERR) and erase error (E_ERR) bits in the status register indicate whether the most recent program or erase command has not completed successfully. When P_ERR or E_ERR bits are set to one, the WIP bit will remain set to one indicating the device remains busy and unable to receive most new operation commands. Only status read (RDSR1 05h), Read Any Register (RDAR 65h), status clear (CLSR 30h or 82h), and software reset (RSTEN 66h, RST 99h or RESET F0h) are valid commands when P_ERR or E_ERR is set to '1'. A Clear Status Register (CLSR) followed by a Write Disable (WRDI) command must be sent to return the device to standby state. Clear Status Register clears the WIP, P_ERR, and E_ERR bits. WRDI clears the WEL bit. Alternatively, Hardware Reset, or Software Reset (RST or RESET) may be used to return the device to standby state.

11.1.5.2 Configuration

There are commands to read, write, and protect registers that control interface path width, interface timing, interface address length, and some aspects of data protection.

11.1.6 Read flash array

Data may be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

There are several different read commands to specify different access latency and data path widths. DDR commands also define the address and data bit relationship to both SCK edges:

• The Read command provides a single address bit per SCK rising edge on the IO0 and IO4 signal with read data returning a single bit per SCK falling edge on the IO1 and IO5 signal. This command has zero latency between the address and the returning data but is limited to a maximum SCK rate of 50 MHz.

• Other read commands have a latency period between the address and returning data but can operate at higher SCK frequencies. The latency depends on a configuration register read latency value.

• The Fast Read command provides a single address bit per SCK rising edge on the IO0 and IO4 signal with read data returning a single bit per SCK falling edge on the IO1 and IO5 signal.

• Dual or Quad I/O Read commands provide address two bits or four bits per SCK rising edge with read data returning two bits, or four bits of data per SCK falling edge on the IO0–IO3 signals.

• Quad Double Data Rate read commands provide address four bits per every SCK edge with read data returning four bits of data per every SCK edge on the IO0–IO3 signals.

11.1.7 Program flash array

Programming data requires two commands: Write Enable (WREN), and Page Program (PP). The Page Program command accepts from 1 byte up to 256 or 512 consecutive bytes of data (page) to be programmed in one operation. Programming means that bits can either be left at '1', or programmed from '1' to '0'. Changing bits from '0' to '1' requires an erase operation.

11.1.8 Erase flash array

The Parameter Sector Erase, Sector Erase, or Bulk Erase commands set all the bits in a sector or the entire memory array to '1'. A bit needs to be first erased to '1' before programming can change it to '0'. While bits can be individually programmed from '1' to '0', erasing bits from '0' to '1' must be done on a sector-wide or array-wide (bulk) level. The Write Enable (WREN) command must precede an erase command.

11.1.9 OTP, block protection, and advanced sector protection

There are commands to read and program a separate OTP array for permanent data such as a serial number. There are commands to control a contiguous group (block) of flash memory array sectors that are protected from program and erase operations. There are commands to control which individual flash memory array sectors are protected from program and erase operations.

11.1.10 Reset

There are commands to reset to the default conditions present after power on to the device. However, the software reset commands do not affect the current state of the FREEZE or PPB Lock bits. In all other respects a software reset is the same as a hardware reset.

There is a command to reset (exit from) the Continuous Read mode.

11.1.11 DPD

A Deep Power-Down (DPD) mode is supported by the S79FS01GS devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being cleared to zero ($SR1V[0] = 0$). While in DPD mode the device ignores all commands except the Release from DPD (RES ABh) command, that will return the device to the Interface Standby state after a delay of t_{RES}.

11.1.12 Reserved

Some instructions are reserved for future use. In this generation of the S79FS01GS some of these command instructions may be unused and not affect device operation, some may have undefined results.

Some commands are reserved to ensure that a legacy or alternate source device command is allowed without effect. This allows legacy software to issue some commands that are not relevant for the current generation S79FS01GS with the assurance these commands do not cause some unexpected action.

Some commands are reserved for use in special versions of the FS-S not addressed by this document or for a future generation. This allows new host memory controller designs to plan the flexibility to issue these command instructions. The command format is defined if known at the time this document revision is published.

11.2 Identification commands

11.2.1 Read Identification (RDID 9Fh)

The Read Identification (RDID) command provides read access to manufacturer identification, device identification, and common flash interface (CFI) information. The manufacturer identification is assigned by JEDEC. The CFI structure is defined by JEDEC standard. The device identification and CFI values are assigned by Infineon.

The JEDEC common flash interface (CFI) specification defines a device information structure, which allows a vendor-specified software flash management program (driver) to be used for entire families of flash devices. Software support can then be device-independent, JEDEC manufacturer ID independent, forward and backward-compatible for the specified flash device families. System vendors can standardize their flash drivers for long-term software compatibility by using the CFI values to configure a family driver from the CFI information of the device in use.

Any RDID command issued while a program, erase, or write cycle is in progress is ignored and has no effect on execution of the program, erase, or write cycle that is in progress.

The RDID instruction is shifted on IO0 and IO4. After the last bit of the RDID instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, extended device identification, and CFI information will be shifted sequentially out on IO1 and IO5. As a whole this information is referred to as ID-CFI. See **"Device ID and common flash interface (ID-CFI) address map"** on page 144 for the detail description of the ID-CFI contents.

Continued shifting of output beyond the end of the defined ID-CFI address space will provide undefined data. The RDID command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

The maximum clock frequency for the RDID command is 133 MHz.

For the Dual-Quad SPI device the Read Identification (RDID) instruction and data read is only done on Quad SPI-1 using IO0 and IO1 and IO0–I03 when QPI mode is enabled.
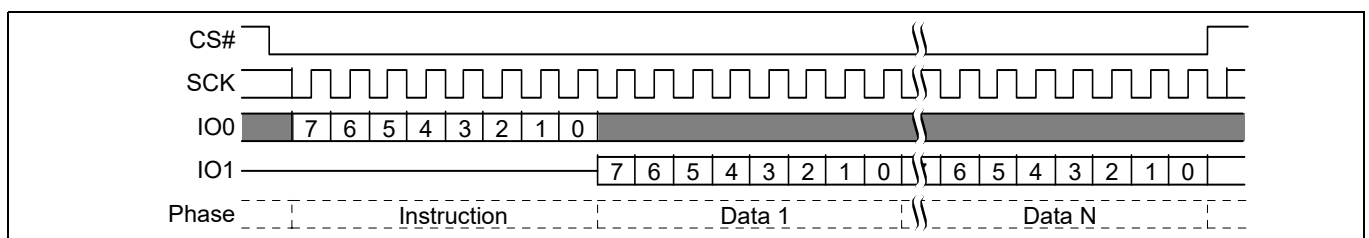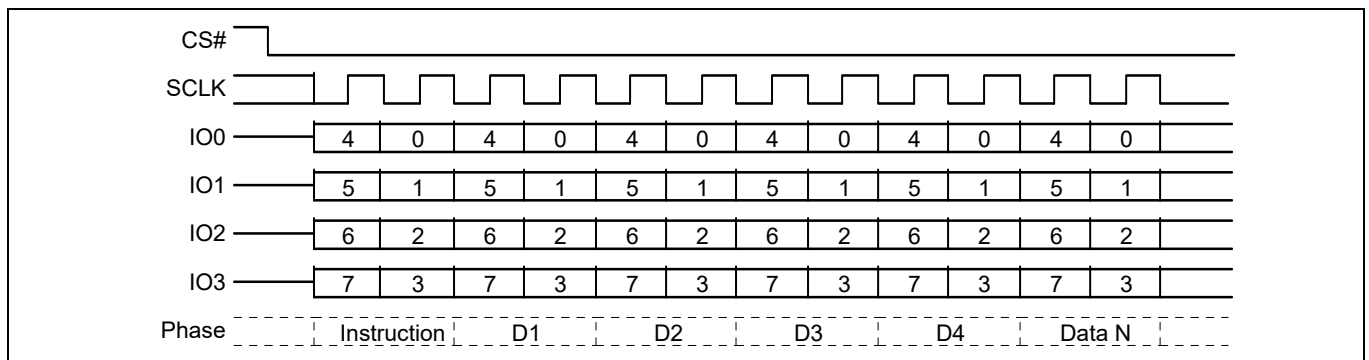

Figure 39   Read Identification (RDID) command sequence
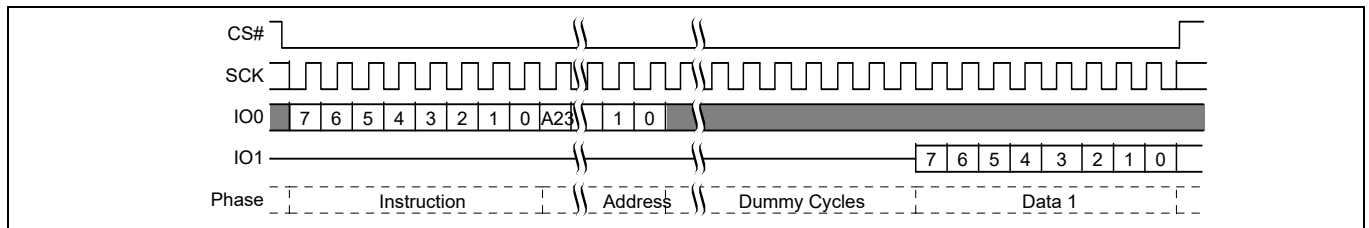
This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.
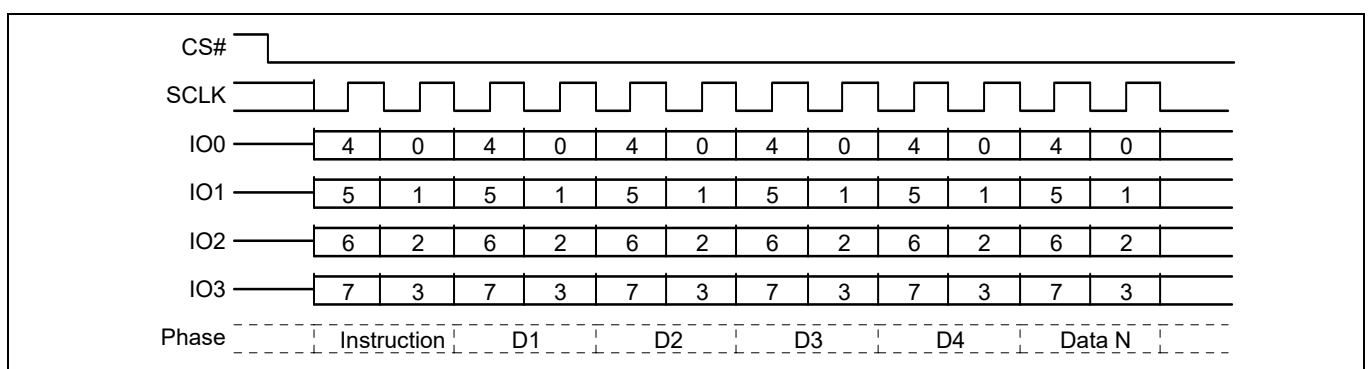

Figure 40   Read Identification (RDID) QPI Mode command

11.2.2 Read Quad Identification (RDQID AFh)

The Read Quad Identification (RDQID) command provides read access to manufacturer identification, device identification, and common flash interface (CFI) information. This command is an alternate way of reading the same information provided by the RDID command while in QPI mode. In all other respects the command behaves the same as the RDID command.

The command is recognized only when the device is In QPI mode, (CR2V[6] = 1). The instruction is shifted in on IO0–IO3. After the last bit of the instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, extended device identification, and CFI information will be shifted sequentially out on IO0–IO3. As a whole this information is referred to as ID-CFI. See **"Device ID and common flash interface (ID-CFI) address map"** on page 144 for the detail description of the ID-CFI contents.

Continued shifting of output beyond the end of the defined ID-CFI address space will provide undefined data. The command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

The maximum clock frequency for the command is 133 MHz.

For the Dual-Quad SPI device the Read Quad Identification (RDQID) instruction and data read is only done on Quad SPI-1 using IO0 and IO1 and IO0–I03 when QPI mode is enabled.

Figure 41   Read Quad Identification (RDQID) command sequence

11.2.3 Read Serial Flash Discoverable Parameters (RSFDP 5Ah)

The command is initiated by shifting on IO0 the instruction code '5Ah', followed by a 24-bit address of 000000h, followed by 8 dummy cycles. The SFDP bytes are then shifted out on IO1 starting at the falling edge of SCK after the dummy cycles. The SFDP bytes are always shifted out with the MSb first. If the 24-bit address is set to any other value, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. The RSFDP command is supported up to 50 MHz.

For the Dual-Quad SPI device the Read Serial Flash Discoverable Parameters (RSFDP) instruction and data read is only done on Quad SPI-1 using IO0 and IO1 and IO0–I03 when QPI mode is enabled.

Figure 42   RSFDP command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.
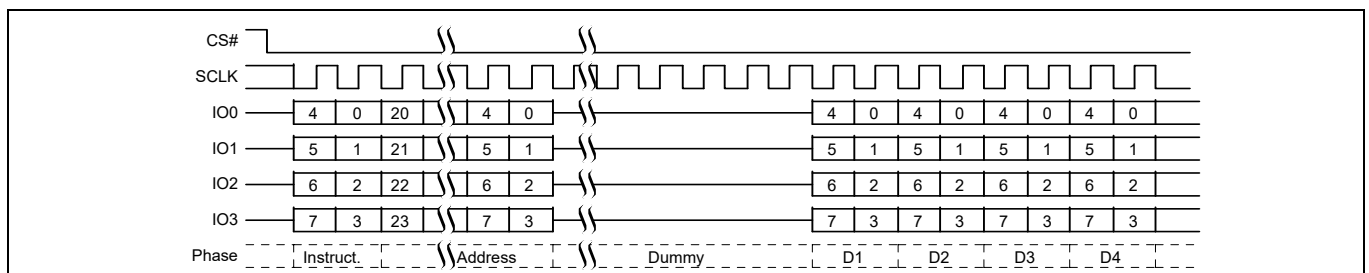
Figure 43   RSFDP QPI Mode command sequence

11.3 Register Access commands

11.3.1 Read Status Register 1 (RDSR1 05h)

The Read Status Register-1 (RDSR1) command allows the Status Register-1 contents of Quad SPI-1 to be read from IO1 and Quad SPI-2 to be read from IO5. In QPI mode, the Status Register-1 contents of Quad SPI-1 to be read from IO0–IO3 and Quad SPI-2 to be read from IO4–IO7.

The volatile version of Status Register 1 (SR1V) contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR1 (05h) command is 133 MHz.
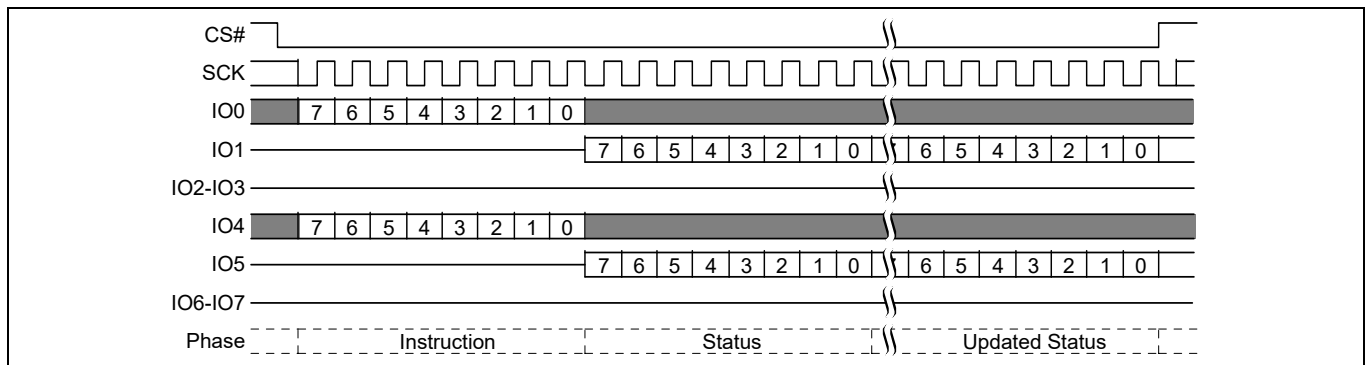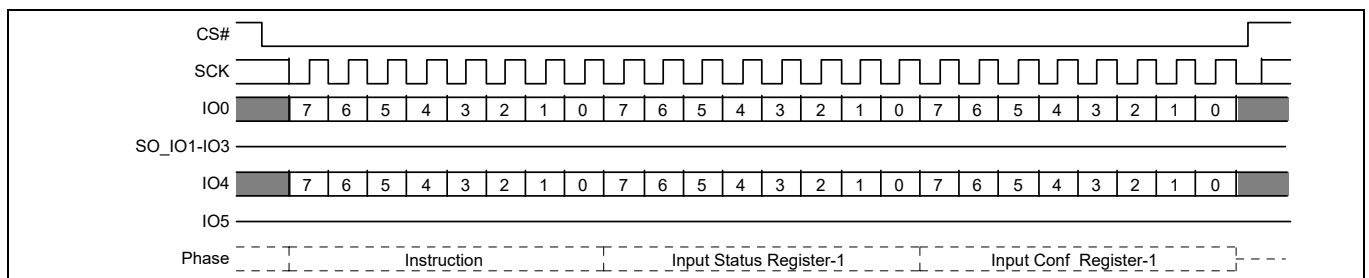

Figure 44   Read Status Register 1 (RDSR1) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2. The returning data is shifted out on IO0–IO3 for Quad SPI-1 and IO3–IO7 for Quad SPI-2.
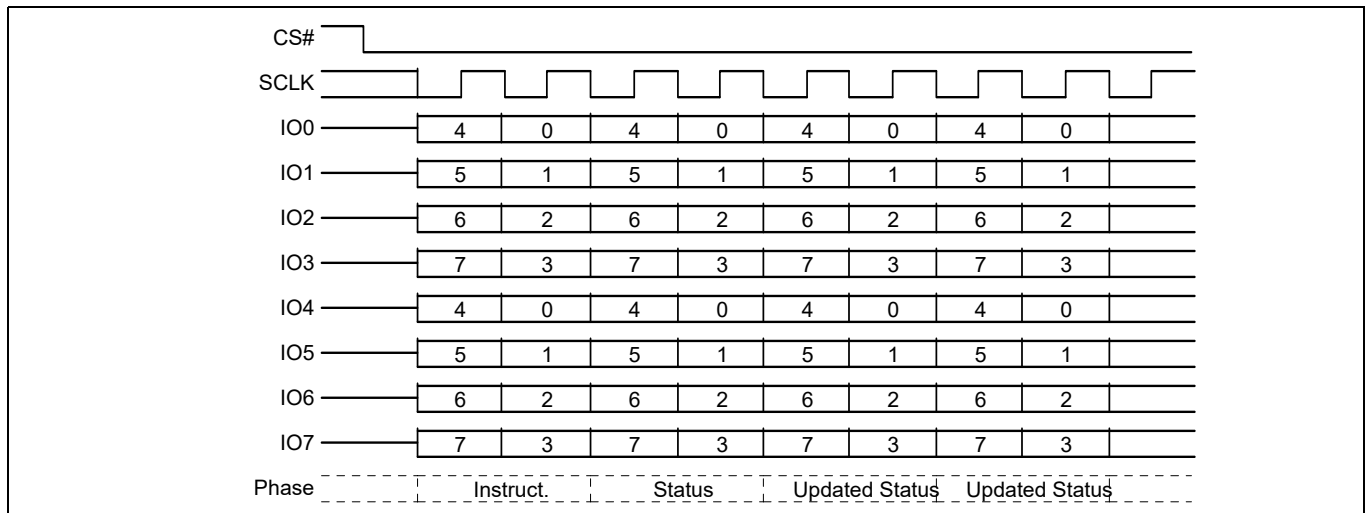
Figure 45   Read Status Register 1 (RDSR1) QPI Mode command

11.3.2 Read Status Register 2 (RDSR2 07h)

The Read Status Register-2 (RDSR2) command allows the Status Register-2 contents of Quad SPI-1 to be read from IO1 and Quad SPI-2 to be read from IO5.

The Status Register 2 contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read the Status Register 2 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR2 command is 133 MHz.
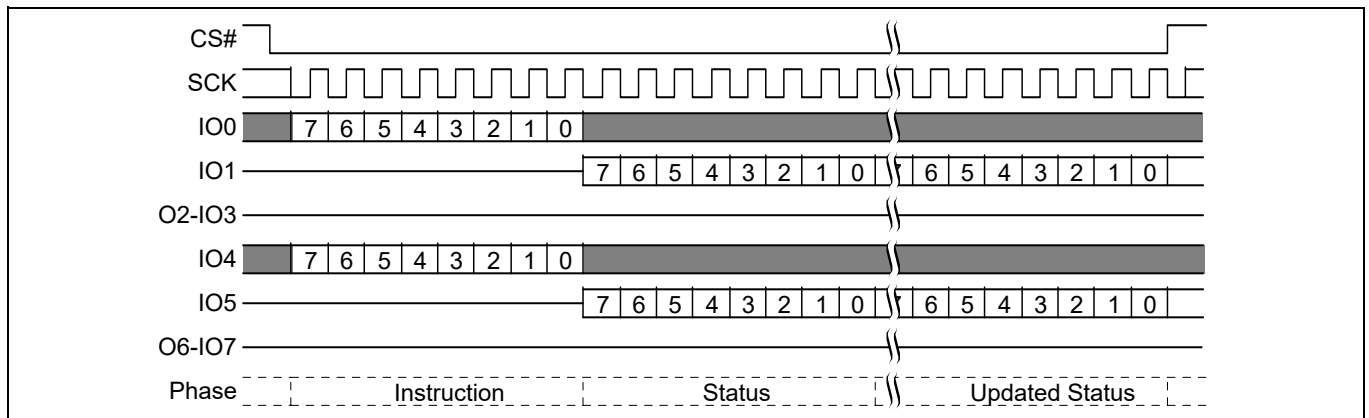
Figure 46   Read Status Register 2 (RDSR2) command

In QPI mode, Status Register 2 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 99.

11.3.3 Read Configuration Register (RDCR 35h)

The Read Configuration Register (RDCR) commands allows the volatile Configuration Registers (CR1V) contents of Quad SPI-1 to be read from IO1 and Quad SPI-2 to be read from IO5.

It is possible to read CR1V continuously by providing multiples of eight clock cycles. The Configuration Register contents may be read at any time, even while a program, erase, or write operation is in progress.
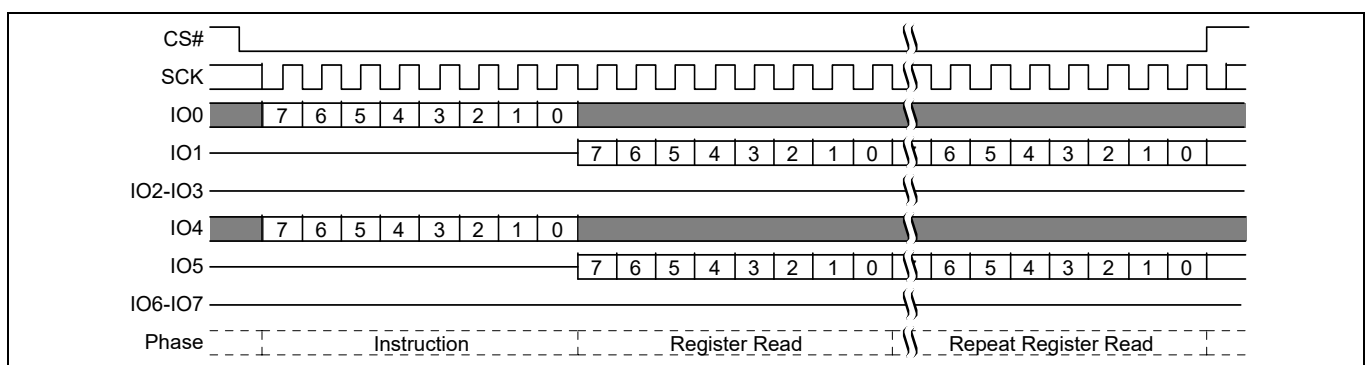
Figure 47   Read Configuration Register (RDCR) command sequence

In QPI mode, Configuration Register 1 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 99.

11.3.4 Write Registers (WRR 01h)

The Write Registers (WRR) command allows new values to be written to both the Status Register 1 and Configuration Register 1. Before the Write Registers (WRR) command can be accepted by the device, a Write Enable (WREN) command must be received. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The Write Registers (WRR) command is entered by shifting the instruction and the data bytes for Quad SPI-1 on IO0 and for Quad SPI-2 on IO4. The Status Register is one data byte in length.

The WRR operation first erases the register then programs the new value as a single operation. The Write Registers (WRR) command will set the P_ERR or E_ERR bits if there is a failure in the WRR operation. See **"Status Register 1 Volatile (SR1V)"** on page 50 for a description of the error bits. Any status or configuration register bit reserved for the future must be written as '0'.

CS# must be driven to the logic HIGH state after the eighth or sixteenth bit of data has been latched. If not, the Write Registers (WRR) command is not executed. If CS# is driven HIGH after the eighth cycle then only the Status Register 1 is written; otherwise, after the sixteenth cycle both the Status and Configuration Registers are written.

As soon as CS# is driven to the logic HIGH state, the self-timed Write Registers (WRR) operation is initiated. While the Write Registers (WRR) operation is in progress, the Status Register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed Write Registers (WRR) operation, and is '0' when it is completed. When the Write Registers (WRR) operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the WRR command is 133 MHz.

Figure 48   **Write Registers (WRR) command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
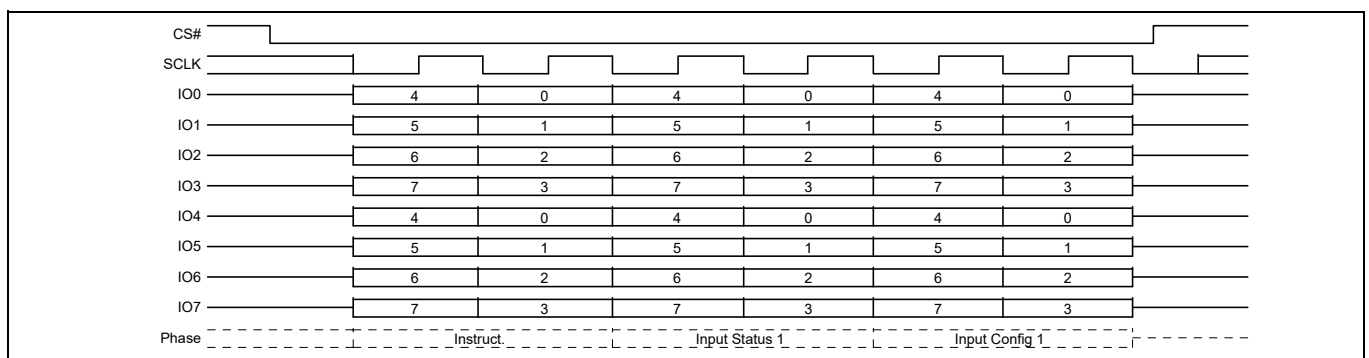

Figure 49   **Write Registers (WRR) command sequence QPI Mode**

The Write Register (WRR) command writes the non-volatile version of the Quad bit (CR1NV[1]), which also causes an update to the volatile version CR1V[1]. The WRR command can not write the volatile version CR1V[1] without first affecting the non-volatile version CR1NV[1]. The WRAR command must be used when it is desired to write the volatile Quad bit CR1V[1] without affecting the non-volatile version CR1NV[1].

Commands

The Write Registers (WRR) command allows the user to change the values of the Block Protect (BP2, BP1, and BP0) bits in either the non-volatile Status Register 1 or in the volatile Status Register 1, to define the size of the area that is to be treated as read-only. The BPNV_O bit (CR1NV[3]) controls whether WRR writes the non-volatile or volatile version of Status Register 1. When CR1NV[3] = 0 WRR writes SR1NV[4:2]. When CR1NV[3] = 1 WRR writes SR1V[4:2].

The Write Registers (WRR) command also allows the user to set the Status Register Write Disable (SRWD) bit to '1' or '0'. The Status Register Write Disable (SRWD) bit and Write Protect (WP#) signal allow the BP bits to be hardware protected.

When the Status Register Write Disable (SRWD) bit of the Status Register is '0' (its initial delivery state), it is possible to write to the status register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) command, regardless of the whether Write Protect (WP#) signal is driven to the logic HIGH or logic LOW state.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to '1', two cases need to be considered, depending on the state of Write Protect (WP#):

- If Write Protect (WP#) signal is driven to the logic HIGH state, it is possible to write to the Status and Configuration Registers provided that the Write Enable Latch (WEL) bit has previously been set to '1' by initiating a Write Enable (WREN) command.

- If Write Protect (WP#) signal is driven to the logic LOW state, it is not possible to write to the Status and Configuration Registers even if the Write Enable Latch (WEL) bit has previously been set to '1' by a Write Enable (WREN) command. Attempts to write to the Status and Configuration Registers are rejected, not accepted for execution, and no error indication is provided. As a consequence, all the data bytes in the memory area that are protected by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected by WP#.

The WP# hardware protection can be provided:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (WP#) signal to the logic LOW state;

- or by driving Write Protect (WP#) signal to the logic LOW state after setting the Status Register Write Disable (SRWD) bit to '1'.

The only way to release the hardware protection is to pull the Write Protect (WP#) signal to the logic HIGH state. If WP# is permanently tied HIGH, hardware protection of the BP bits can never be activated.

Table 48   Block Protection modes[40, 41]

WP#	SRWD bit	Mode	Write protection of registers	Memory content	
				Protected area	**Unprotected area**
1	1	Software Protected	Status and Configuration Registers are Writable (if WREN command has set the WEL bit). The values in the SRWD, BP2, BP1, and BP0 bits and those in the Configuration Register can be changed	Protected against Page Program, Sector Erase, and Bulk Erase	Ready to accept Page Program, and Sector Erase commands
1	0				
0	0				
0	1	Hardware Protected	Status and Configuration Registers are Hardware Write Protected. The values in the SRWD, BP2, BP1, and BP0 bits and those in the Configuration Register cannot be changed	Protected against Page Program, Sector Erase, and Bulk Erase	Ready to accept Page Program or Erase commands

Notes
40. The Status Register originally shows 00h when the device is first shipped from Infineon to the customer.
41. Hardware protection is disabled when Quad Mode is enabled (CR1V[1] = 1). WP# becomes IO2; therefore, it cannot be utilized.

11.3.5 Write Enable (WREN 06h)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to '1'. The Write Enable Latch (WEL) bit must be set to '1' by issuing the Write Enable (WREN) command to enable write, program and erase commands.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 for Quad SPI-1 and IO4 for Quad SPI-2. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 for Quad SPI-1 and IO4 for Quad SPI-2, the write enable operation will not be executed.
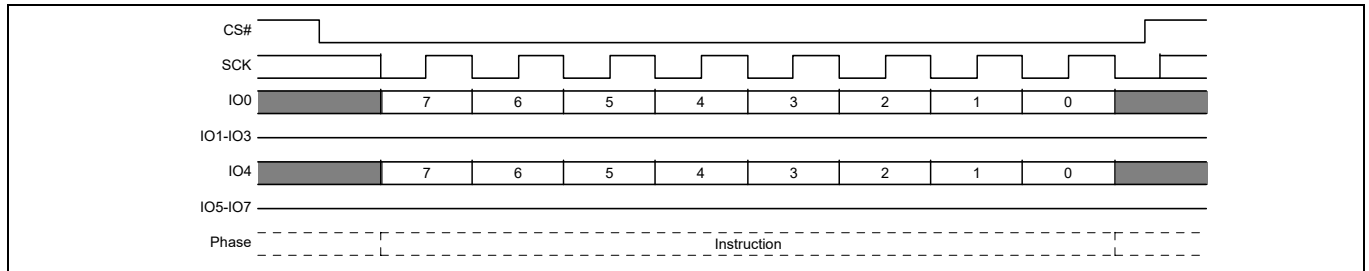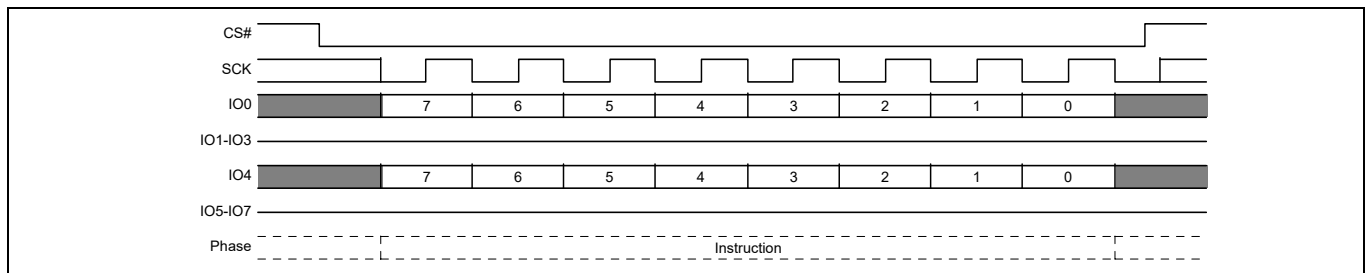

Figure 50   **Write Enable (WREN) command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
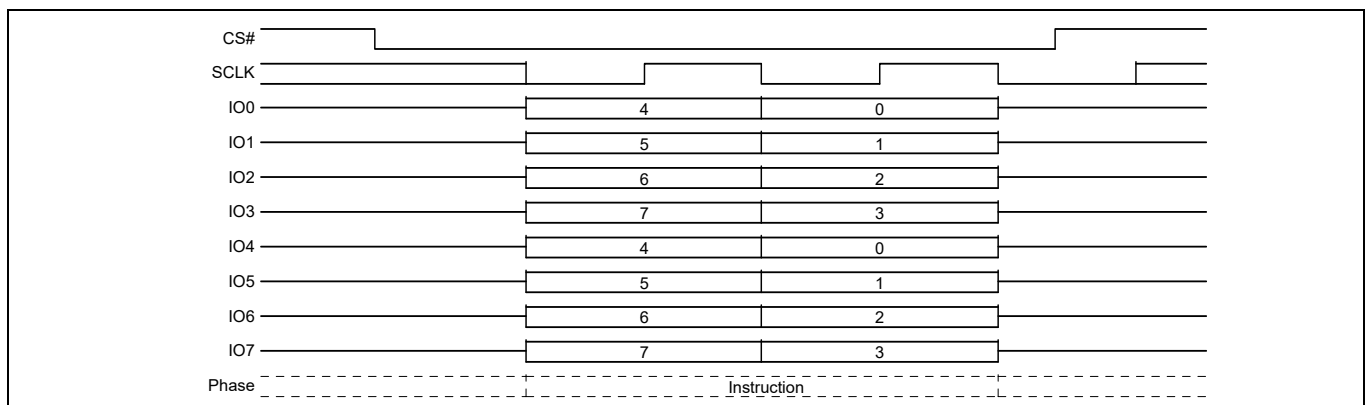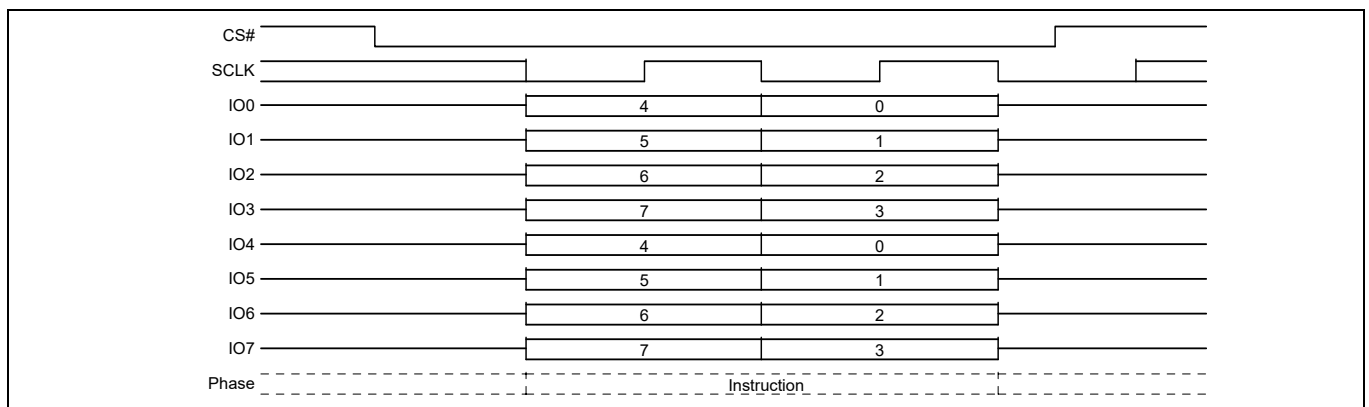

Figure 51   **Write Enable (WREN) command sequence QPI mode**

11.3.6 Write Disable (WRDI 04h)

The Write Disable (WRDI) command clears the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to '0'.

The Write Enable Latch (WEL) bit may be cleared to '0' by issuing the Write Disable (WRDI) command to disable Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Registers (WRR or WRAR), OTP Program (OTPP), and other commands, that require WEL be set to '1' for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit = 1.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 for Quad SPI-1 and IO4 for Quad SPI-2. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 for Quad SPI-1 and IO4 for Quad SPI-2, the write disable operation will not be executed.
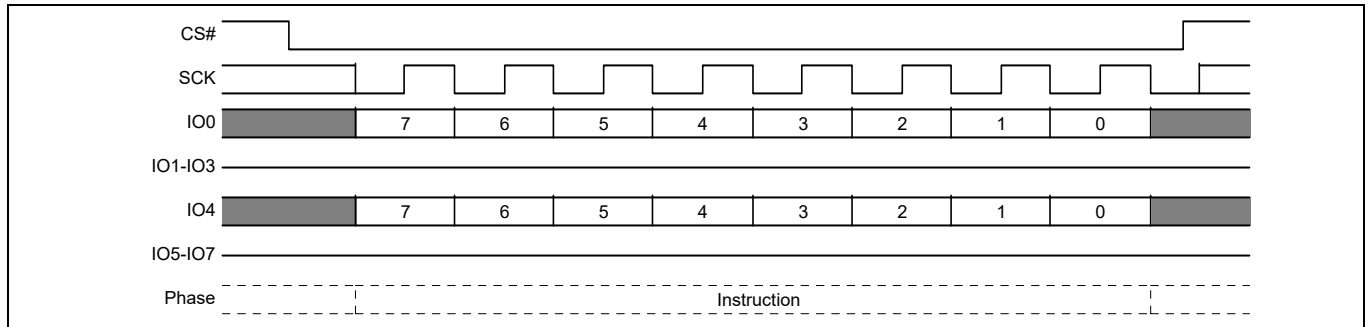

Figure 52   Write Disable (WRDI) command sequence

This command is also supported in QPI mode.In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.


Figure 53   Write Disable (WRDI) command sequence QPI mode

11.3.7 Clear Status Register (CLSR 30h or 82h)

The Clear Status Register command resets bit SR1V[5] (Erase Fail Flag) and bit SR1V[6] (Program Fail Flag). It is not necessary to set the WEL bit before a Clear Status Register command is executed. The Clear Status Register command will be accepted even when the device remains busy with WIP set to '1', as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

The legacy Clear Status Register (CLSR 30h) instruction may be disabled and the 30h instruction value instead used for a program / erase resume command, see **"Configuration Register 3"** on page 61. The Clear Status Register alternate instruction (CLSR 82h) is always available to clear the status register.

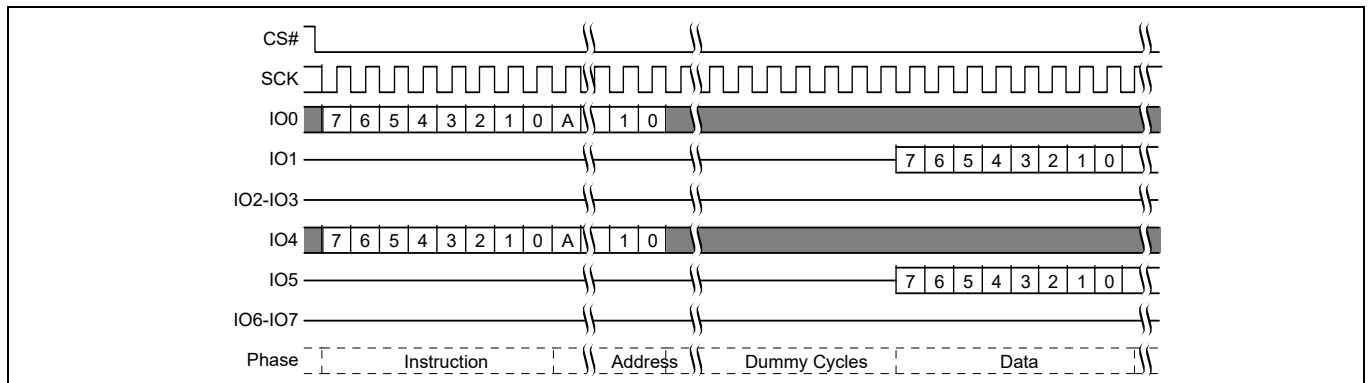**Figure 54   Clear Status Register (CLSR) command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
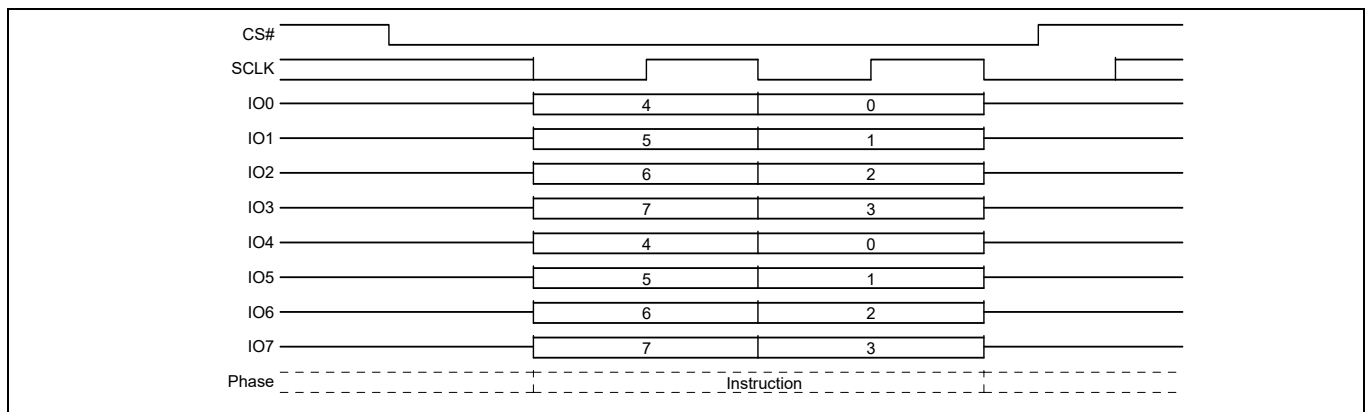
Figure 55   Clear Status Register (CLSR) command sequence QPI mode

11.3.8 ECC Status Register Read (ECCRD 19h or 4EECRD 18h)

To read the ECC Status Register, the command is followed by the ECC unit address, the four least significant bits (LSb) of address must be set to '0'. This is followed by the number of dummy cycles selected by the read latency value in CR2V[3:0]. Then the 8-bit contents of the ECC Register, for the ECC unit selected, are shifted out on IO1 and IO5 16 times, once for each byte in the ECC Unit. If CS# remains LOW the next ECC unit status is sent through IO1 and IO5 16 times, once for each byte in the ECC Unit. The maximum operating clock frequency for the ECC READ command is 133 MHz.

Figure 56   ECC Status Register Read command sequence[42, 43]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2. The returning data is shifted out on IO0–IO3 for Quad SPI-1 and IO3–IO7 for Quad SPI-2.
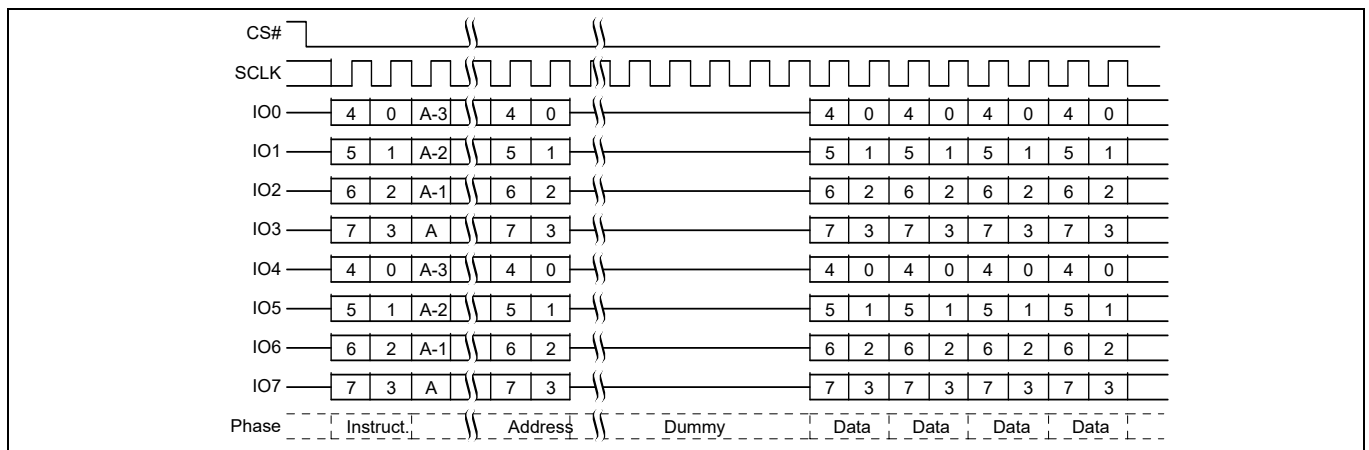

Figure 57   ECCRD (19h), QPI Mode, CR2[7] = 0 command sequence[42, 43]

Notes
42. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command 19h.
43. A = MSb of address = 31 with command 18h.

11.3.9 Program NVDLR (PNVDLR 43h)

Before the Program NVDLR (PNVDLR) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable the PNVDLR operation.

The PNVDLR command is entered by shifting the instruction and the data byte on IO0 for Quad SPI-1 and IO4 for Quad SPI-2.

CS# must be driven to the logic HIGH state after the eighth (8th) bit of data has been latched. If not, the PNVDLR command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PNVDLR operation is initiated. While the PNVDLR operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed PNVDLR cycle, and is '0' when it is completed. The PNVDLR operation can report a program error in the P_ERR bit of the status register. When the PNVDLR operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PNVDLR command is 133 MHz.
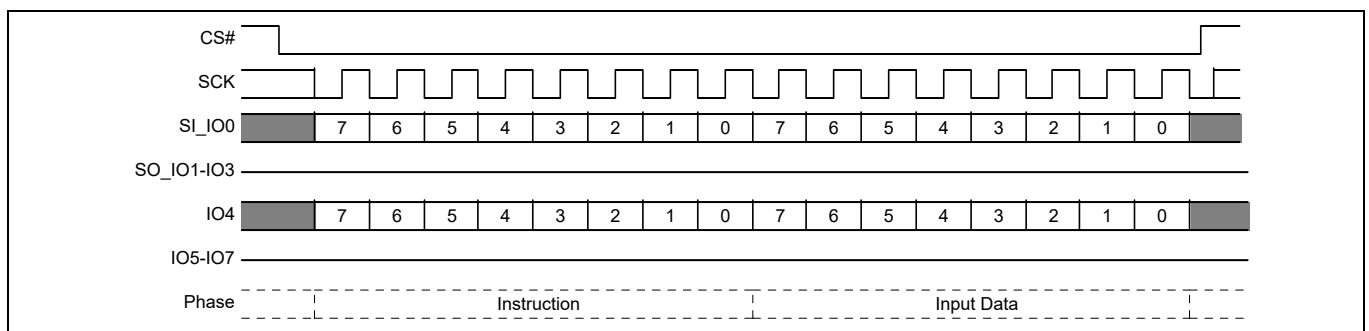

Figure 58   Program NVDLR (PNVDLR) command sequence

11.3.10 Write VDLR (WVDLR 4Ah)

Before the Write VDLR (WVDLR) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable WVDLR operation.

The WVDLR command is entered by shifting the instruction and the data byte on IO0 for Quad SPI-1 and IO4 for Quad SPI-2.

CS# must be driven to the logic HIGH state after the eighth (8th) bit of data has been latched. If not, the WVDLR command is not executed. As soon as CS# is driven to the logic HIGH state, the WVDLR operation is initiated with no delays. The maximum clock frequency for the PNVDLR command is 133 MHz.
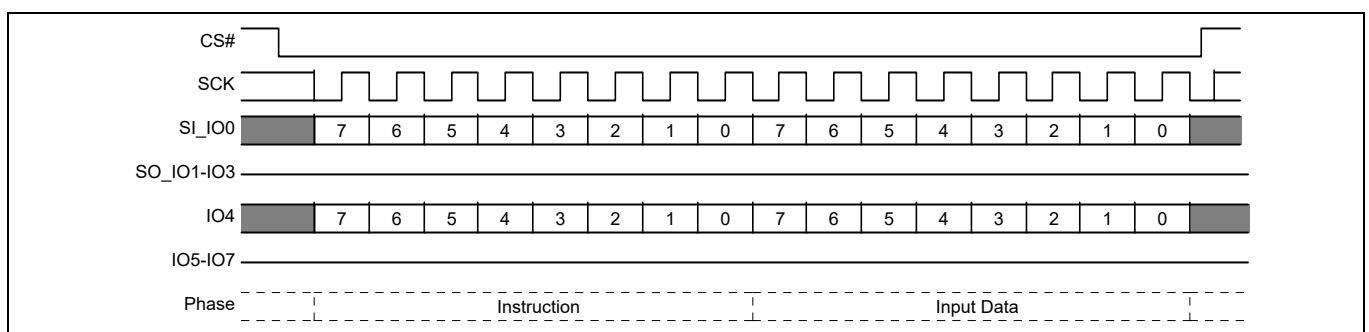

Figure 59   Write VDLR (WVDLR) command sequence

11.3.11 Data Learning Pattern Read (DLPRD 41h)

The instruction is shifted on IO0 and IO4, then the 8-bit DLP is shifted out on IO1 and IO5. It is possible to read the DLP continuously by providing multiples of eight clock cycles. The maximum operating clock frequency for the DLPRD command is 133 MHz.
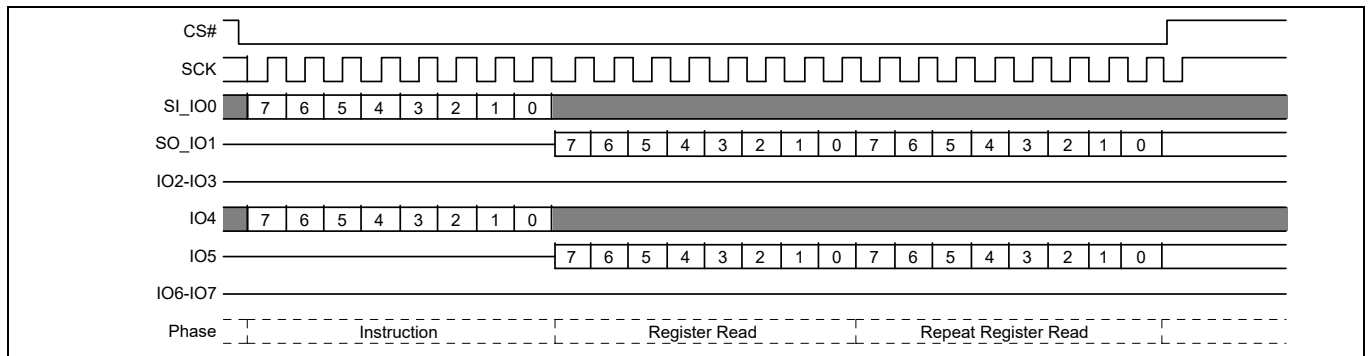

Figure 60   DLP Read (DLPRD) command sequence

11.3.12 Enter 4-Byte Address Mode (4BAM B7h)

The enter 4-byte Address Mode (4BAM) command sets the volatile Address Length bit (CR2V[7]) to '1' to change most 3-byte address commands to require 4 bytes of address. The Read SFDP (RSFDP) command is the only 3-byte command that is not affected by the Address Length bit. RSFDP is required by the JEDEC JESD216 standard to always have only 3 bytes of address.

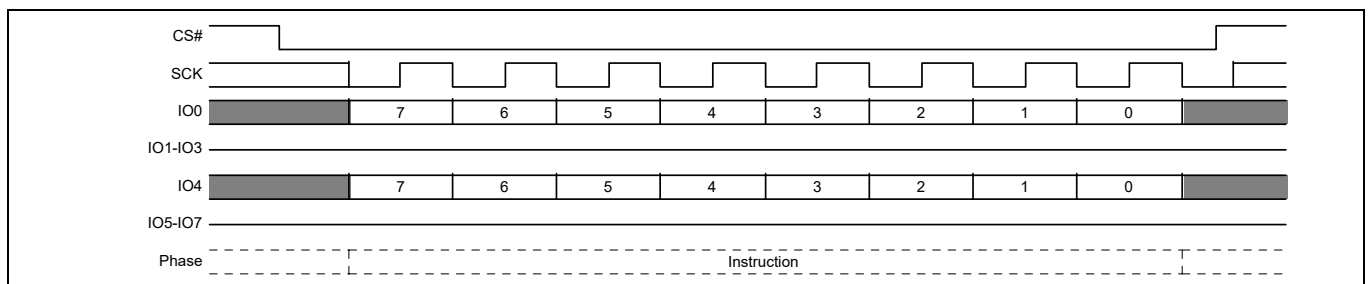A hardware or software reset is required to exit the 4-byte address mode.

Figure 61   Enter 4-Byte Address Mode (4BAM B7h) command sequence

11.3.13 Read Any Register (RDAR 65h)

The Read Any Register (RDAR) command provides a way to read all device registers - non-volatile and volatile. The instruction is followed by a 3- or 4-byte address (depending on the address length configuration CR2V[7], followed by a number of latency (dummy) cycles set by CR2V[3:0]. Then the selected register contents are returned. If the read access is continued the same addressed register contents are returned until the command is terminated – only one register is read by each RDAR command.

Reading undefined locations provides undefined data.

The RDAR command may be used during embedded operations to read Status Register 1 (SR1V).

The RDAR command is not used for reading registers that act as a window into a larger array: PPBAR, and DYBAR. There are separate commands required to select and read the location in the array accessed.

The RDAR command will read invalid data from the PASS register locations if the ASP Password protection mode is selected by programming ASPR[2] to '0'.

Table 49   Register address map

| Byte address (Hex)	Register name	Description
00000000	SR1NV	Non-volatile Status and Configuration Registers
00000001	N/A	
00000002	CR1NV	
00000003	CR2NV	
00000004	CR3NV	
00000005	CR4NV	
...	N/A	
00000010	NVDLR	Non-volatile Data Learning Register
...	N/A	
00000020	PASS[7:0]	Non-volatile Password Register
00000021	PASS[15:8]	
00000022	PASS[23:16]	
00000023	PASS[31:24]	
00000024	PASS[39:32]	
00000025	PASS[47:40]	
00000026	PASS[55:48]	
00000027	PASS[63:56]	
...	N/A	
00000030	ASPR[7:0]	Non-volatile
00000031	ASPR[15:8]	
...	N/A	
00800000	SR1V	Volatile Status and Configuration Registers
00800001	SR2V	
00800002	CR1V	
00800003	CR2V	
00800004	CR3V	
00800005	CR4V	
...	N/A	
00800010	VDLR	Volatile Data Learning Register
...	N/A	
00800040	PPBL	Volatile PPB Lock Register
...	N/A	

Commands
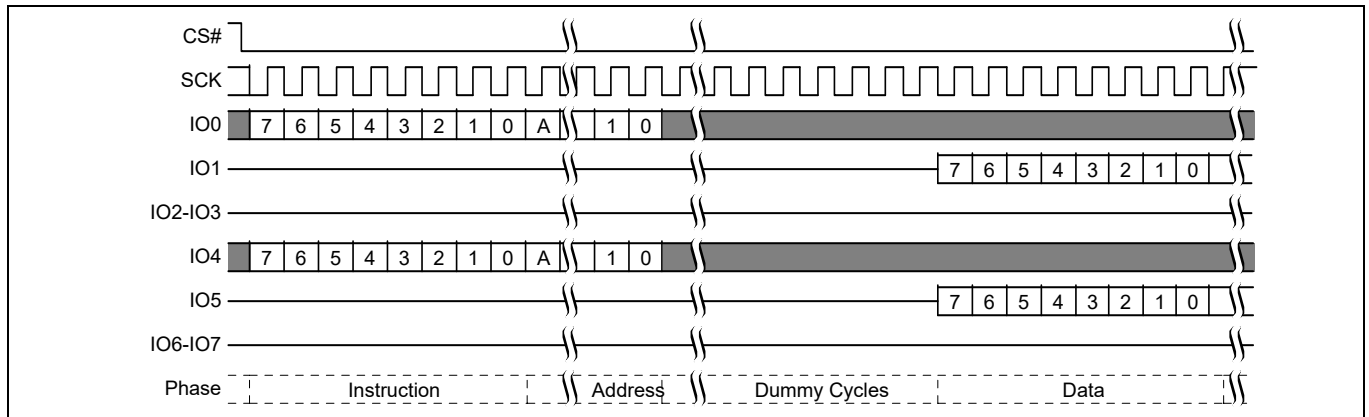
Figure 62   Read Any Register Read command sequence[44]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2. The returning data is shifted out on IO0–IO3 for Quad SPI-1 and IO3–IO7 for Quad SPI-2.
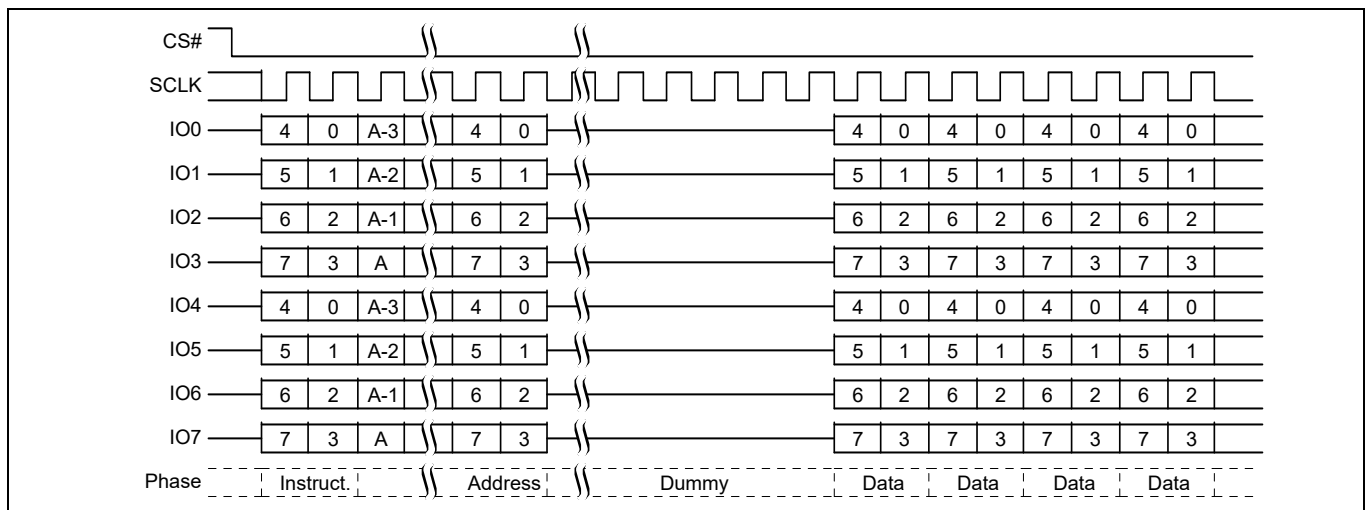

Figure 63   Read Any Register, QPI Mode command sequence[44]

Note
 44.A = MSb of address = 23 for Address length CR2V[7] = 0, or 31 for CR2V[7] = 1.

11.3.14   Write Any Register (WRAR 71h)

The Write Any Register (WRAR) command provides a way to write any device register - non-volatile/volatile. The instruction is followed by a 3 or 4-byte address (depending on the address length configuration CR2V[7], followed by one byte of data to write in the address selected register.

Before the WRAR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR and E_ERR bits in SR1V may be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits may be modified. Some bits are read only, some are OTP.

Read only bits are never modified and the related bits in the WRAR command data byte are ignored without setting a program or erase error indication (P_ERR or E_ERR in SR1V). Hence, the value of these bits in the WRAR data byte do not matter.

OTP bits may only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Non-volatile bits which are changed by the WRAR data, require non-volatile register write time (t_W) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails the related error bit and WIP in SR1V will be set to '1'.

Volatile bits which are changed by the WRAR data, require the volatile register write time (t_{CS}) to be updated.

Status Register 1 may be repeatedly read (polled) to monitor the Write-In-Progress (WIP) bit (SR1V[0]) and the error bits (SR1V[6,5]) to determine when the register write is completed or failed. If there is a write failure, the clear status command is used to clear the error status and enable the device to return to standby state.

However, the PPBL register can not be written by the WRAR command. Only the PPB Lock Bit Write (PLBWR) command can write the PPBL register.

The command sequence and behavior is the same as the PP or 4PP command with only a single byte of data provided. See **"Page Program (PP 02h or 4PP 12h)"** on page 113.

The address map of the registers is the same as shown for **"Read Any Register (RDAR 65h)"** on page 99.

11.3.15   Set Burst Length (SBL C0h)

The Set Burst Length (SBL) command is used to configure the Burst Wrap feature. Burst Wrap is used in conjunction with Quad I/O Read and DDR Quad I/O Read, in legacy SPI or QPI mode, to access a fixed length and alignment of data. Certain applications can benefit from this feature by improving the overall system code execution performance. The Burst Wrap feature allows applications that use cache, to start filling a cache line with instruction or data from a critical address first, then fill the remainder of the cache line afterwards within a fixed length (8/16/32/64 bytes) of data, without issuing multiple read commands.

The Set Burst Length (SBL) command writes the CR4V register bits 4, 1, and 0 to enable or disable the wrapped read feature and set the wrap boundary. Other bits of the CR4V register are not affected by the SBL command. When enabled the wrapped read feature changes the related read commands from sequentially reading until the command ends, to reading sequentially wrapped within a group of bytes.

When CR4V[4] = 1, the wrap mode is not enabled and unlimited length sequential read is performed.

When CR4V[4] = 0, the wrap mode is enabled and a fixed length and aligned group of 8, 16, 32, or 64 bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.

The group of bytes is of length and aligned on an 8, 16, 32, or 64 byte boundary. CR4V[1:0] selects the boundary. See **"Configuration Register 4 Volatile (CR4V)"** on page 64.

The starting address of the read command selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If the read continues the address wraps to the beginning of the group and continues to read sequentially. This wrapped read sequence continues until the command is ended by CS# returning HIGH.

Table 50   Example burst wrap sequences

CR4V[4,1:0] value (Hex)	Wrap boundary (Bytes)	Start address (Hex)	Address sequence (Hex)
1X	Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...
00	16	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02, ...
00	16	XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, ...
01	32	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, ...
01	32	XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, ...
02	64	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, ...
02	64	XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, ...
03	128	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 ...
03	128	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, ...

The POR, hardware reset, or software reset default burst length can be changed by programming CR4NV with the desired value using the WRAR command.
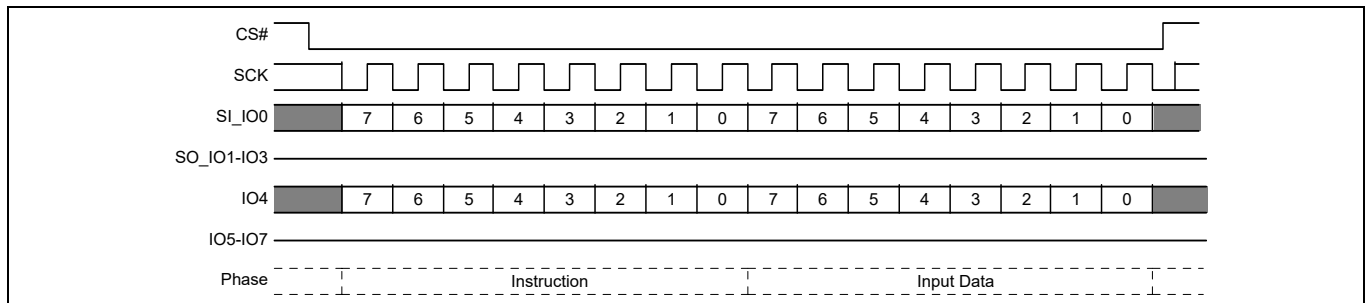

Figure 64   Set Burst Length command sequence

11.4　　　Read Memory Array commands

Read commands for the main flash array provide many options for prior generation SPI compatibility or enhanced performance SPI:

- Some commands transfer address or data on each rising edge of SCK. These are called Single Data Rate commands (SDR).

- Some SDR commands transfer address one bit per rising edge of SCK and return data 2 bit of data per rising edge of SCK. These are called Single Width commands.

- Some SDR commands transfer both address and data 2 or 4 bits per rising edge of SCK. These are called Quad I/O, and QPI for 8 bit. QPI also transfers instructions 4 bits per rising edge.

- Some commands transfer address and data on both the rising edge and falling edge of SCK. These are called DDR commands.

- There are DDR commands for 4 bits of address per each die or 8 bits data per SCK edge. These are called Quad I/O DDR and QPI DDR for 8 bit per edge transfer.

All of these commands, except QPI Read, begin with an instruction code that is transferred one bit per SCK rising edge. QPI Read transfers the instruction 4 bits per SCK rising edge per die.The instruction is followed by either a 3- or 4-byte address transferred at SDR or DDR. Commands transferring address or data 4 bits per die and clock edge are called Multiple I/O (MIO) commands. For S79FS01GS devices, the traditional SPI 3-byte addresses are unable to directly address all locations in the memory array. Separate 4-byte address read commands are provided for access to the entire address space. These devices may be configured to take a 4-byte address from the host system with the traditional 3-byte address commands. The 4-byte address mode for traditional commands is activated by setting the Address Length bit in Configuration Register 2 to '0'.

The Quad I/O and QPI commands provide a performance improvement option controlled by mode bits that are sent following the address bits. The mode bits indicate whether the command following the end of the current read will be another read of the same type, without an instruction at the beginning of the read. These mode bits give the option to eliminate the instruction cycles when doing a series of Quad read accesses.

Some commands require delay cycles following the address or mode bits to allow time to access the memory array - read latency. The delay or read latency cycles are traditionally called dummy cycles. The dummy cycles are ignored by the memory thus any data provided by the host during these cycles is 'don't care' and the host may also leave the IO0 and IO4 signal at high impedance during the dummy cycles. When MIO commands are used the host must stop driving the IO signals (outputs are high impedance) before the end of last dummy cycle. When DDR commands are used the host must not drive the I/O signals during any dummy cycle. The number of dummy cycles varies with the SCK frequency or performance option selected via the Configuration Register 2 (CR2V[3:0]) Latency Code. Dummy cycles are measured from SCK falling edge to next SCK falling edge. SPI outputs are traditionally driven to a new value on the falling edge of each SCK. Zero dummy cycles means the returning data is driven by the memory on the same falling edge of SCK that the host stops driving address or mode bits.

The DDR commands may optionally have an 8-edge Data Learning Pattern (DLP) driven by the memory, on all data outputs, in the dummy cycles immediately before the start of data. The DLP can help the host memory controller determine the phase shift from SCK to data edges so that the memory controller can capture data at the center of the data eye.

When using SDR I/O commands at higher SCK frequencies (>50 MHz), an LC that provides one or more dummy cycles should be selected to allow additional time for the host to stop driving before the memory starts driving data, to minimize I/O driver conflict. When using DDR I/O commands with the DLP enabled, an LC that provides five or more dummy cycles should be selected to allow one cycle of additional time for the host to stop driving before the memory starts driving the four-cycle DLP.

Each read command ends when CS# is returned HIGH at any point during data return. CS# must not be returned HIGH during the mode or dummy cycles before data returns as this may cause mode bits to be captured incorrectly; making it indeterminate as to whether the device remains in continuous read mode.

11.4.1 Read (Read 03h or 4READ 13h)

The instruction

- 03h (CR2V[7] = 0) is followed by a 3-byte address (A23–A0) or

- 03h (CR2V[7] = 1) is followed by a 4-byte address (A31–A0) or

- 13h is followed by a 4-byte address (A31–A0)

Then the memory contents, at the address given, are shifted out on IO1 and IO5. The maximum operating clock frequency for the READ command is 50 MHz.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.
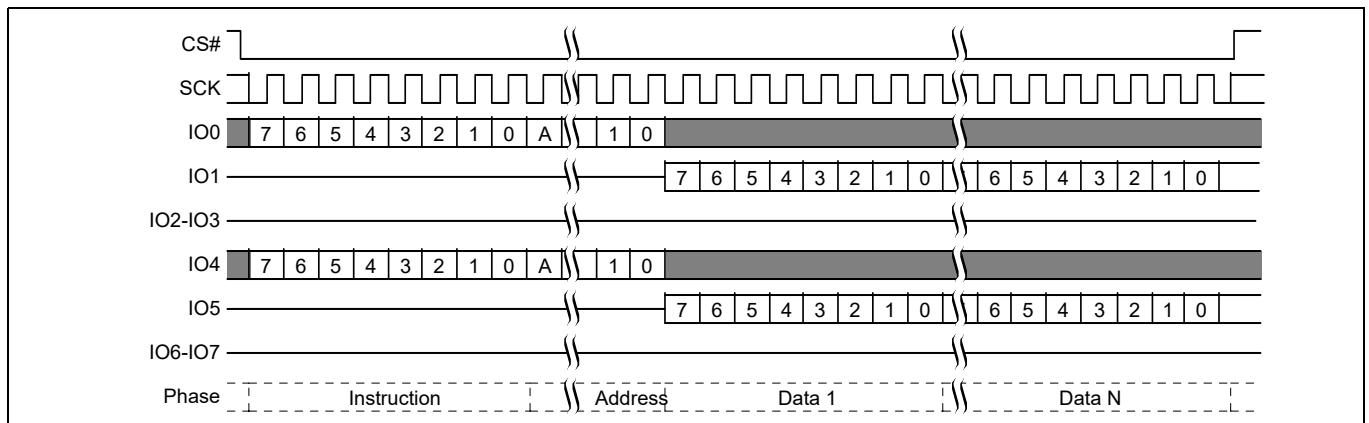

Figure 65   Read command sequence[45]

Note
 45.A = MSb of address = 23 for CR2V[7] = 0, or 31 for CR2V[7] = 1 or command 13h.

Commands

11.4.2 Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)

The instruction

- 0Bh (CR2V[7] = 0) is followed by a 3-byte address (A23–A0) or

- 0Bh (CR2V[7] = 1) is followed by a 4-byte address (A31–A0) or

- 0Ch is followed by a 4-byte address (A31–A0)

The address is followed by dummy cycles depending on the latency code set in the Configuration Register CR2V[3:0]. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on IO1 and IO5 is 'don't care' and may be high impedance. Then the memory contents, at the address given, are shifted out on IO1 and IO5.

The maximum operating clock frequency for FAST READ command is 133 MHz.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.
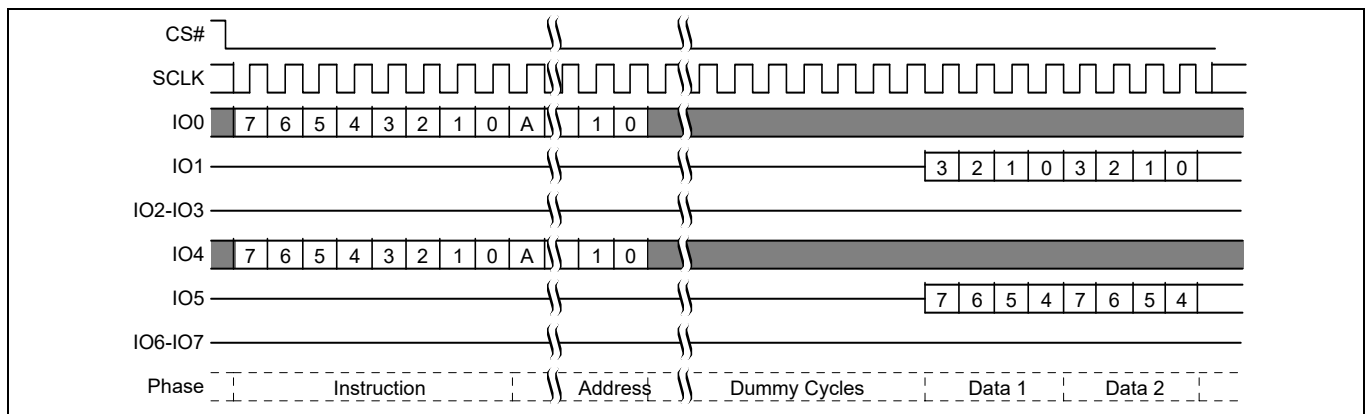

Figure 66   Fast Read (FAST_READ) command sequence[46]

Note
 46.A = MSb of address = 23 for CR2V[7] = 0, or 31 for CR2V[7] = 1 or command 0Ch.

11.4.3　Quad I/O Read (QIOR EBh or 4QIOR ECh)

The instruction

- EBh (CR2V[7] = 0) is followed by a 3-byte address (A23–A0) or

- EBh (CR2V[7] = 1) is followed by a 4-byte address (A31–A0) or

- ECh is followed by a 4-byte address (A31–A0)

The QUAD bit of the Configuration Register must be set (CR1V[1] = 1) to enable the Quad capability of S79FS01GS devices.

The maximum operating clock frequency for Quad I/O Read is 133 MHz.

For the Quad I/O Read command, there is a latency required after the mode bits (described below) before data begins shifting out of IO0–IO7. This latency period (i.e., dummy cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO7 are 'don't care' and may be high impedance. The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR2V[3:0].

Following the latency period, the memory contents at the address given, is shifted out eight bits at a time through IO0–IO7. Each byte is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

Address jumps can be done without the need for additional Quad I/O Read instructions. This is controlled through the setting of the Mode bits (after the address sequence, as shown in **Figure 67**). This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7–4) of the Mode bits control the length of the next Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3–0) of the Mode bits are 'don't care' (x). If the Mode bits equal Axh, then the device remains in Quad I/O High Performance Read Mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the EBh or ECh instruction, as shown in **Figure 69**; thus, eliminating eight cycles for the command sequence.

The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI commands:

1. During the Quad I/O Read Command Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised HIGH the device will be released from Quad I/O High Performance Read mode.

2. Send the Mode Reset command.

Note that the two mode bit clock cycles and additional wait states (i.e., dummy cycles) allow the device's internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0–IO3.

It is important that the IO0–IO7 signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing IO0–IO7 signal contention, for the host system to turn off the IO0–IO7 signal outputs (make them high impedance) during the last 'don't care' mode cycle or during any dummy cycles.

CS# should not be driven HIGH during mode or dummy bits as this may make the mode bits indeterminate. In QPI mode, (CR2V[6] = 1) the Quad I/O instructions are sent 4 bits per SCK rising edge. The remainder of the command protocol is identical to the Quad I/O commands.
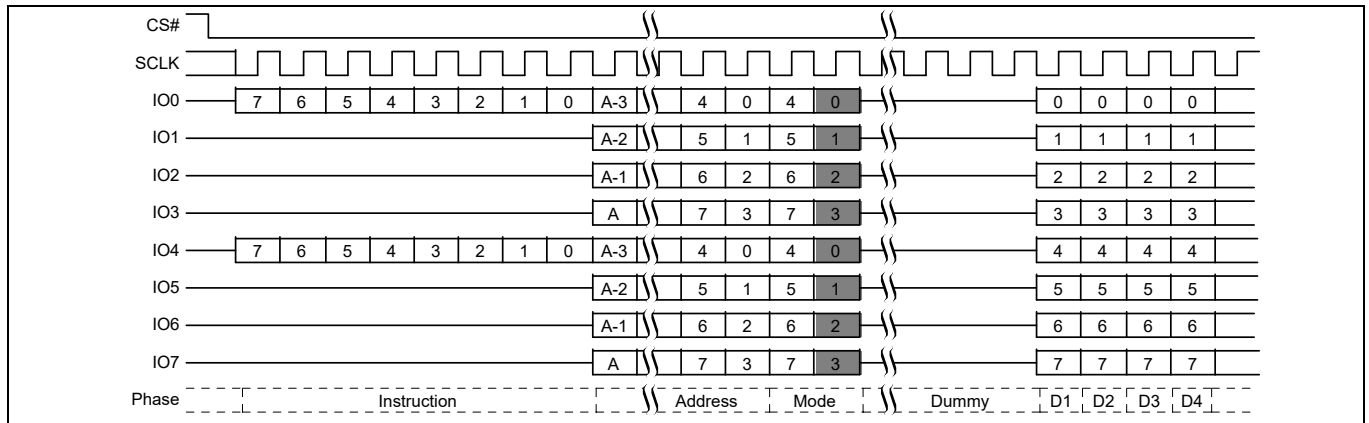
Commands

Figure 67 **Quad I/O Read command sequence (EBh or ECh)**[47, 48]
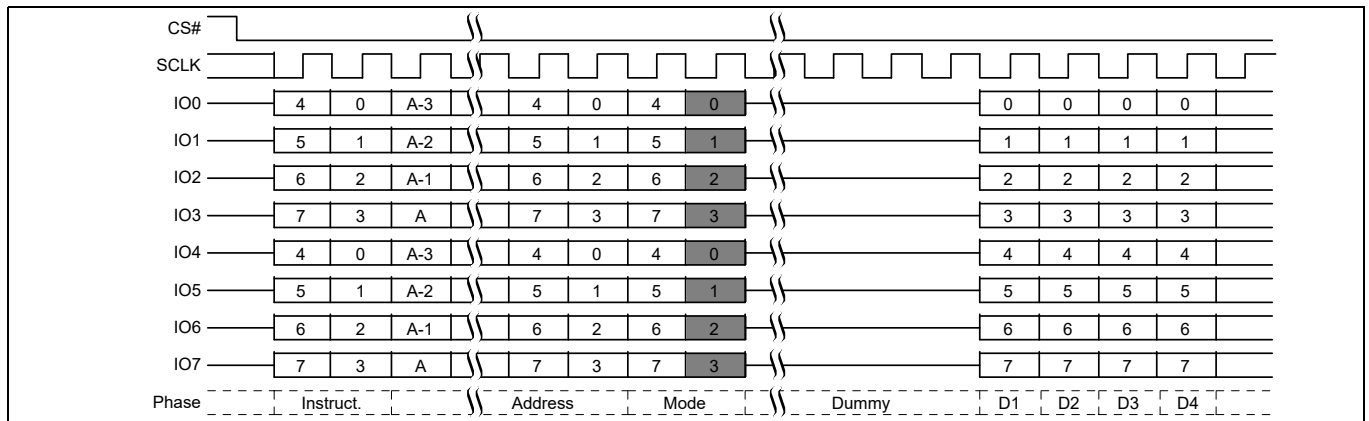

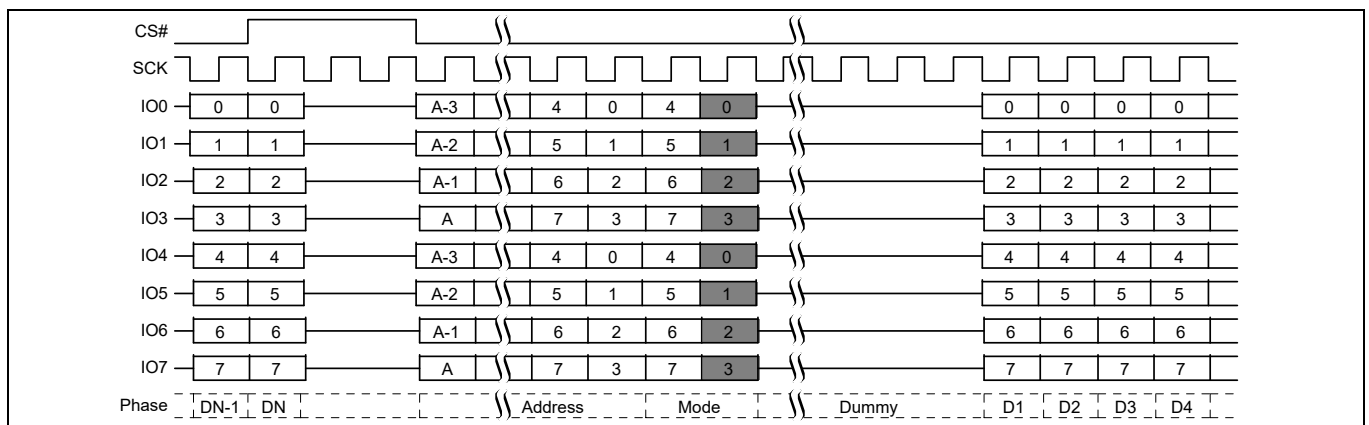**Figure 68** **Quad I/O Read command sequence (EBh or ECh), QPI Mode**[47, 48]

Figure 69 **Continuous Quad I/O Read command sequence (EBh or ECh)**[47, 48]

Notes

47. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EBh.
48. A = MSb of address = 31 with command ECh.

11.4.4 DDR Quad I/O Read (EDh, EEh)

The DDR Quad I/O Read command improves throughput with four I/O signals: IO0–IO3. It is similar to the Quad I/O Read command but allows input of the address four bits on every edge of the clock. In some applications, the reduced instruction overhead might allow for code execution (XIP) directly from S79FS01GS devices. The QUAD bit of the Configuration Register must be set (CR1V[1] = 1) to enable the Quad capability.

The instruction

- EDh (CR2V[7] = 0) is followed by a 3-byte address (A23–A0) or

- EDh (CR2V[7] = 1) is followed by a 4-byte address (A31–A0) or

- EEh is followed by a 4-byte address (A31–A0)

The address is followed by mode bits. Then the memory contents, at the address given, is shifted out, in a DDR fashion, with four bits at a time on each clock edge through IO0–IO7.

The maximum operating clock frequency for DDR Quad I/O Read command is 102 MHz.

For DDR Quad I/O Read, there is a latency required after the last address and mode bits are shifted into the IO0–IO7 signals before data begins shifting out of IO0–IO7. This latency period (dummy cycles) allows the device's internal circuitry enough time to access the initial address. During these latency cycles, the data value on IO0–IO3 are 'don't care' and may be high impedance. When the Data Learning Pattern (DLP) is enabled the host system must not drive the IO signals during the dummy cycles. The IO signals must be left high impedance by the host so that the memory device can drive the DLP during the dummy cycles.

The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR2V[3:0].

Mode bits allow a series of Quad I/O DDR commands to eliminate the 8-bit instruction after the first command sends a complementary mode bit pattern, as shown in **Figure 70**. This feature removes the need for the eight bit SDR instruction sequence and dramatically reduces initial access times (improves XIP performance). The Mode bits control the length of the next DDR Quad I/O Read operation through the inclusion or exclusion of the first byte instruction code. If the upper nibble (IO[7:4]) and lower nibble (IO[3:0]) of the Mode bits are complementary (i.e. 5h and Ah) the device transitions to Continuous DDR Quad I/O Read Mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the EDh or EEh instruction, as shown in **Figure 71**, thus eliminating eight cycles from the command sequence. The following sequences will release the device from Continuous DDR Quad I/O Read mode; after which, the device can accept standard SPI commands:

1. During the DDR Quad I/O Read command sequence, if the Mode bits are not complementary the next time CS# is raised HIGH and then asserted LOW the device will be released from DDR Quad I/O Read mode.
2. Send the Mode Reset command.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

CS# should not be driven HIGH during mode or dummy bits as this may make the mode bits indeterminate. Note that the memory devices may drive the IOs with a preamble prior to the first data value. The preamble is a Data Learning Pattern (DLP) that is used by the host controller to optimize data capture at higher frequencies. The preamble drives the IO bus for the four clock cycles immediately before data is output. The host must be sure to stop driving the IO bus prior to the time that the memory starts outputting the preamble.

The preamble is intended to give the host controller an indication about the round trip time from when the host drives a clock edge to when the corresponding data value returns from the memory device. The host controller will skew the data capture point during the preamble period to optimize timing margins and then use the same skew time to capture the data during the rest of the read operation. The optimized capture point will be determined during the preamble period of every read operation. This optimization strategy is intended to compensate for both the PVT (process, voltage, temperature) of both the memory device and the host controller as well as any system level delays caused by flight time on the PCB.

Commands

Although the data learning pattern (DLP) is programmable, the following example shows example of the DLP of 34h. The DLP 34h (or 00110100) will be driven on each of the active outputs (i.e. all IOs). This pattern was chosen to cover both 'DC' and 'AC' data transition scenarios. The two DC transition scenarios include data low for a long period of time (two half clocks) followed by a high going transition (001) and the complementary low going transition (110). The two AC transition scenarios include data low for a short period of time (one half clock) followed by a high going transition (101) and the complementary low going transition (010). The DC transitions will typically occur with a starting point closer to the supply rail than the AC transitions that may not have fully settled to their steady state (DC) levels. In many cases the DC transitions will bound the beginning of the data valid period and the AC transitions will bound the ending of the data valid period. These transitions will allow the host controller to identify the beginning and ending of the valid data eye. Once the data eye has been characterized the optimal data capture point can be chosen. See **"SPI DDR Data Learning Registers"** on page 69 for more details.

In QPI mode, (CR2V[6] = 1) the DDR Quad I/O instructions are sent 4 bits per die at the SCK rising edge. The remainder of the command protocol is identical to the DDR Quad I/O commands.

Figure 70   DDR Quad I/O Read Initial Access (EDh or EEh)[49, 50]

Notes
49. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EDh.
50. A = MSb of address = 31 with command EEh.

Commands

Figure 71   DDR Quad I/O Read Initial Access (EDh or EEh), QPI mode[51, 52]
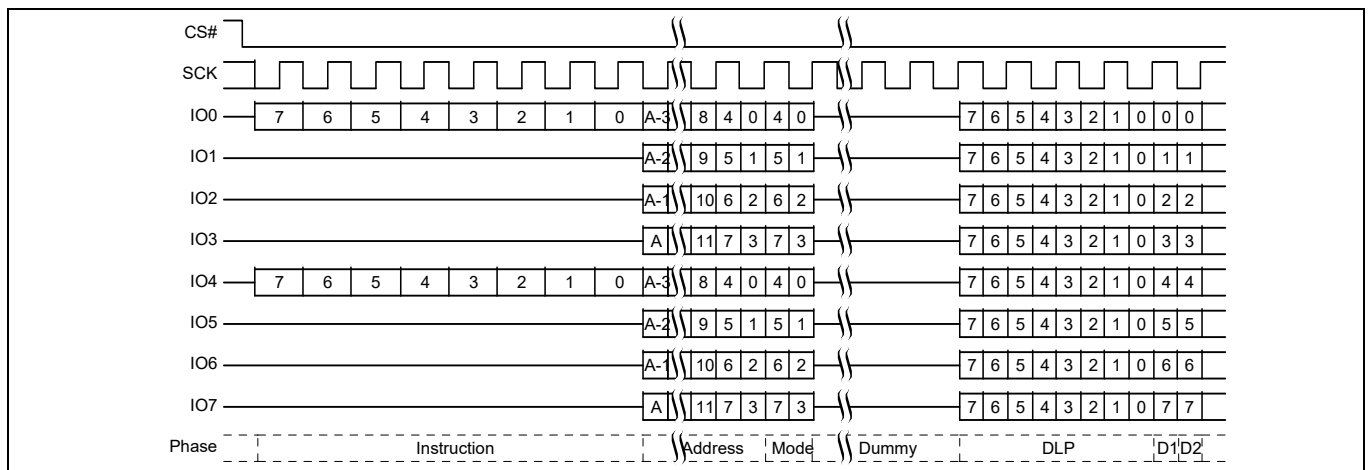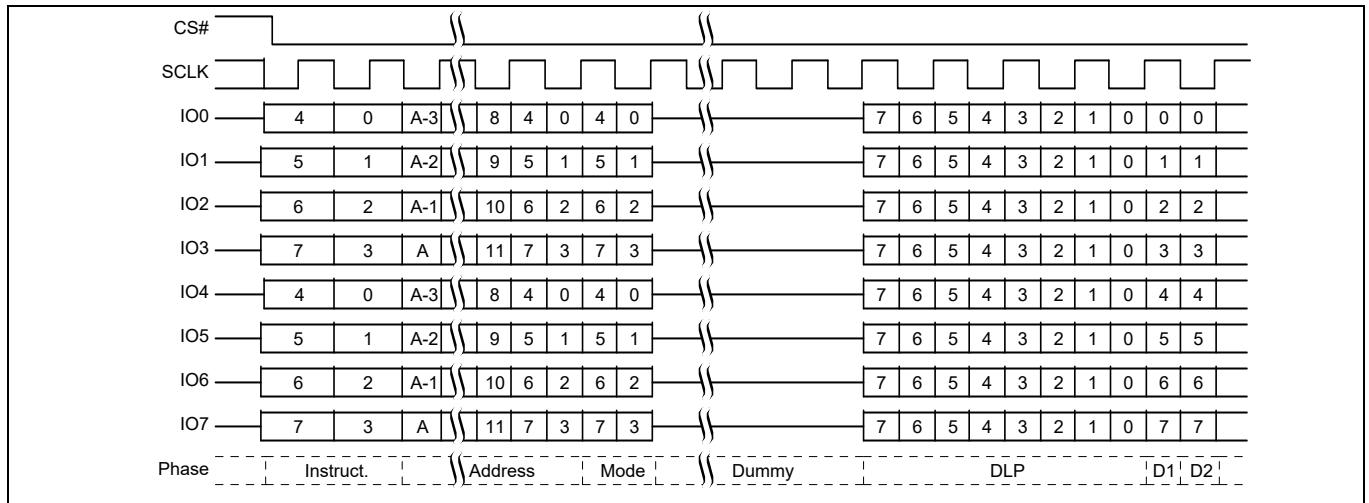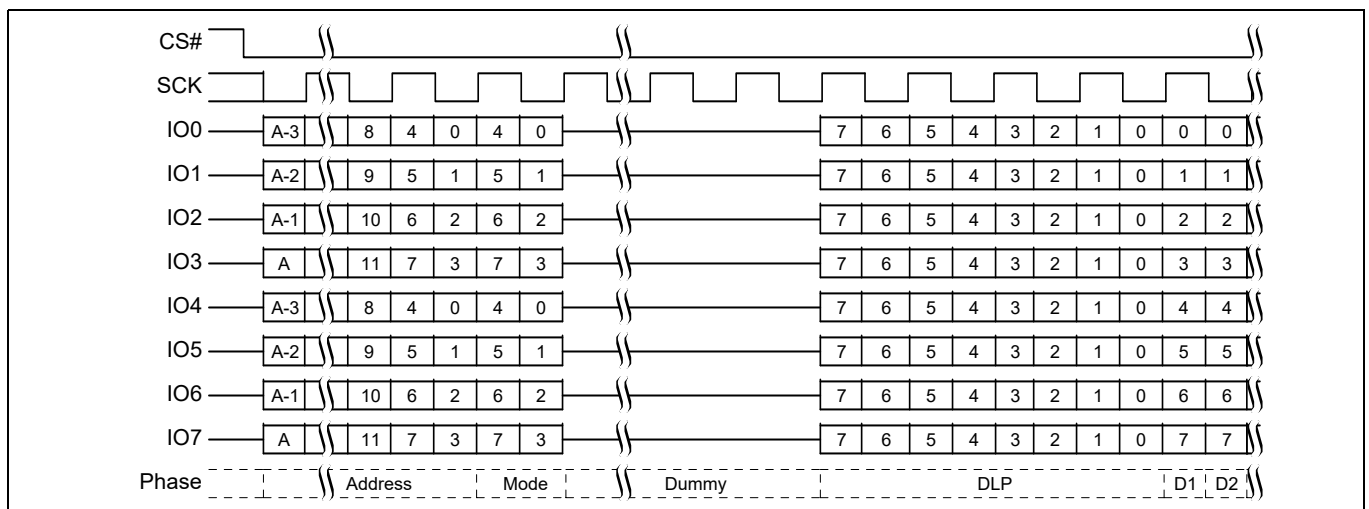

Figure 72   Continuous DDR Quad I/O Read Subsequent Access (EDh or EEh)[51, 52]

Notes
51. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EDh.
52. A = MSb of address = 31 with command EEh.

11.5 Program Flash Array commands

11.5.1 Program granularity

11.5.1.1 Automatic ECC

Each 16 byte aligned and 16 byte length Programming Block has an automatic error correction code (ECC) value. The data block plus ECC form an ECC unit. In combination with error detection and correction (EDC) logic the ECC is used to detect and correct any single bit error found during a read access. When data is first programmed within an ECC unit the ECC value is set for the entire ECC unit. If the same ECC unit is programmed more than once the ECC value is changed to disable the EDC function. A sector erase is needed to again enable Automatic ECC on that Programming Block. The 16 byte Program Block is the smallest program granularity on which Automatic ECC is enabled.

These are automatic operations transparent to the user. The transparency of the Automatic ECC feature enhances data accuracy for typical programming operations which write data once to each ECC unit but, facilitates software compatibility to previous generations of FL family of products by still allowing for single byte programming and bit walking in which the same ECC unit is programmed more than once. When an ECC unit has Automatic ECC disabled, EDC is not done on data read from the ECC unit location.

An ECC status register is provided for determining if ECC is enabled on an ECC unit and whether any errors have been detected and corrected in the ECC unit data or the ECC. The ECC Status Register Read (ECCRD) command is used to read the ECC status on any ECC unit.

EDC is applied to all parts of the Flash address spaces other than registers. An ECC is calculated for each group of bytes protected and the ECC is stored in a hidden area related to the group of bytes. The group of protected bytes and the related ECC are together called an ECC unit.

- ECC is calculated for each 16 byte aligned and length ECC unit

- Single Bit EDC is supported with 8 ECC bits per ECC unit, plus 1 bit for an ECC disable Flag

- Sector erase resets all ECC disable flags in a sector to the default state (enabled)

- ECC is programmed as part of the standard Program commands operation

- ECC is disabled automatically if multiple programming operations are done on the same ECC unit.

- Single byte programming or bit walking is allowed but disables ECC on the second program to the same 16 byte ECC unit.

- The ECC disable flag is programmed when ECC is disabled

- To re-enable ECC for an ECC unit that has been disabled, the Sector that includes the ECC unit must be erased

- To ensure the best data integrity provided by EDC, each ECC unit should be programmed only once so that ECC is stored for that unit and not disabled.

- The calculation, programming, and disabling of ECC is done automatically as part of programming operations. The detection and correction if needed is done automatically as part of read operations. The host system sees only corrected data from a read operation.

- ECC protects the OTP region — however a second program operation on the same ECC unit will disable ECC permanently on that ECC unit (OTP is one time programmable, hence an erase operation to re-enable the ECC enable/indicator bit is prohibited).

11.5.1.2 Page programming

Page programming is done by loading a Page Buffer with data to be programmed and issuing a programming command to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming command. Page programming allows up to a page size (either 512 or 1024 bytes) to be programmed in one operation. The page size is determined by the configuration register bit CR3V[4]. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each Page programming operation. It is recommended that a multiple of 16-byte length and aligned Program Blocks be written. This insures that Automatic ECC is not disabled. For the very best performance, programming should be done in full pages of 1024 bytes aligned on 2014 byte boundaries with each Page being programmed only once.

11.5.1.3 Single byte programming

Single byte programming allows full backward compatibility to the legacy standard SPI page programming (PP) command by allowing a single byte to be programmed anywhere in the memory array. While single byte programming is supported, this will disable Automatic ECC on the 16 byte ECC unit where the byte is located.

11.5.2 Page Program (PP 02h or 4PP 12h)

The Page Program (PP) command allows bytes to be programmed in the memory (changing bits from '1' to '0'). Before the Page Program (PP) commands can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 02h (CR2V[7] = 0) is followed by a 3-byte address (A23–A0), or

- 02h (CR2V[7] = 1) is followed by a 4-byte address (A31–A0), or

- 12h is followed by a 4-byte address (A31–A0)

and at least one data byte on IO0 and IO4. Depending on CR3V[4], the page size can either be 256 or 512 bytes. Up to a page can be provided on IO0 and IO4 after the 3-byte address with instruction 02h or 4-byte address with instruction 12h has been provided.

If more data is sent to the device than the space between the starting address and the page aligned end boundary, the data loading sequence will wrap from the last byte in the page to the zero byte location of the same page and begin overwriting any data previously loaded in the page. The last page worth of data is programmed in the page. This is a result of the device being equipped with a page program buffer that is only page size in length. If less than a page of data is sent to the device, these data bytes will be programmed in sequence, starting at the provided address within the page, without having any affect on the other bytes of the same page.

Using the Page Program (PP) command to load an entire page, within the page boundary, will save overall programming time versus loading less than a page into the program buffer.

The programming process is managed by the flash memory device internal control logic. After a programming command is issued, the programming operation status can be checked using the Read Status Register 1 command. The WIP bit (SR1V[0]) will indicate when the programming operation is completed. The P_ERR bit (SR1V[6]) will indicate if an error occurs in the programming operation that prevents successful completion of programming. This includes attempted programming of a protected area.
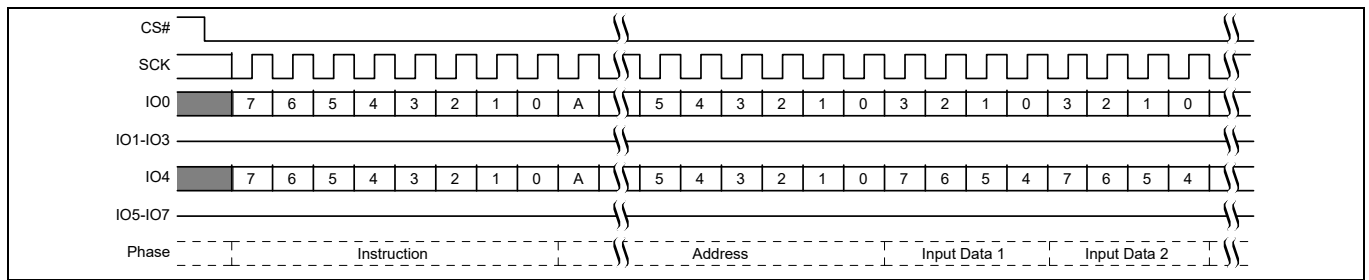
Commands

Figure 73   **Page Program (PP 02h or 4PP 12h) command sequence**[53]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
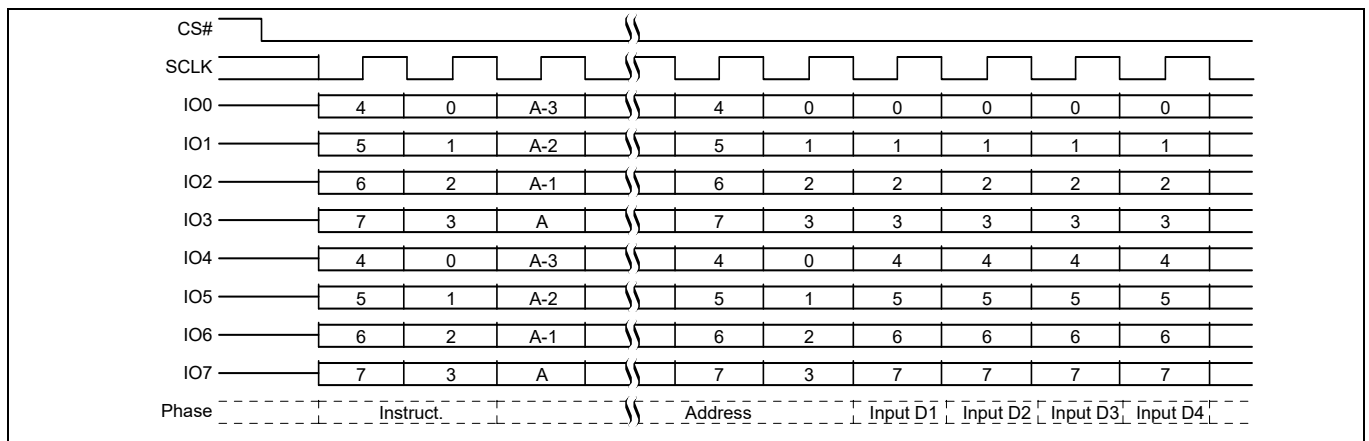

Figure 74   **Page Program (PP 02h or 4PP 12h) QPI mode command sequence**[53]

Note
  53. A = MSb of address = A23 for PP 02h, or A31 for 4PP 12h.

11.6 Erase Flash Array commands

11.6.1 Parameter 8 KB Sector Erase (P4E 20h or 4P4E 21h)

The main flash array address map may be configured to overlay 8 KB parameter sectors over the lowest address portion of the lowest address uniform sector (bottom parameter sectors) or over the highest address portion of the highest address uniform sector (top parameter sectors). The main flash array address map may also be configured to have only uniform size sectors. The parameter sector configuration is controlled by the configuration bit CR3V[3]. The P4E and 4P4E commands are ignored when the device is configured for uniform sectors only (CR3V[3] = 1).

The Parameter 8 KB Sector Erase commands set all the bits of a 8-KB parameter sector to '1' (all bytes are FFh). Before the P4E or 4P4E command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 20h [CR2V[7] = 0] is followed by a 3-byte address (A23–A0), or

- 20h [CR2V[7] = 1] is followed by a 4-byte address (A31–A0), or

- 21h is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of the address has been latched in on IO0 and IO4. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the chosen sector of the flash memory array. If CS# is not driven HIGH after the last bit of address, the sector erase operation will not be executed.

As soon as CS# is driven HIGH, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate '1', when the erase cycle is in progress and '0', when the erase cycle has been completed.

A P4E or 4P4E command applied to a sector that has been write protected through the Block Protection bits or ASP, will not be executed and will set the E_ERR status. A P4E command applied to a sector that is larger than 8 KB will not be executed and will not set the E_ERR status.

Commands

Figure 75   Parameter Sector Erase (P4E 20h or 4P4E 21h) command sequence[54]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.

Figure 76   Parameter Sector Erase (P4E 20h or 4P4E 21h) QPI mode command sequence[54]

Note
54. A = MSb of address = A23 for P4E 20h with CR2V[7] = 0, or A31 for P4E 20h with CR2V[7] = 1 or 4P4E 21h.

11.6.2   Sector Erase (SE D8h or 4SE DCh)

The Sector Erase (SE) command sets all bits in the addressed sector to '1' (all bytes are FFh). Before the Sector Erase (SE) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- D8h [CR2V[7] = 0] is followed by a 3-byte address (A23–A0), or

- D8h [CR2V[7] = 1] is followed by a 4-byte address (A31–A0), or

- DCh is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of address has been latched in on IO0 and IO4. This will initiate the erase cycle, which involves the pre-programming and erase of the chosen sector. If CS# is not driven HIGH after the last bit of address, the sector erase operation will not be executed.

As soon as CS# is driven into the logic HIGH state, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate '1', when the erase cycle is in progress and '0', when the erase cycle has been completed.

A Sector Erase (SE) command applied to a sector that has been Write Protected through the Block Protection bits or ASP, will not be executed and will set the E_ERR status.

A device configuration option (CR3V[3]) determines whether 8 KB parameter sectors are in use. When CR3V[3] = 0, 8 KB parameter sectors overlay a portion of the highest or lowest address 64 KB of the device address space. If a sector erase command is applied to a 512 KB range that is overlaid by 8 KB sectors, the overlaid 8 KB sectors are not affected by the erase. When CR3V[3] = 1, there are no 8 KB parameter sectors in the device address space and the Sector Erase command always operates on fully visible 512 KB sectors. ASP has a PPB and a DYB protection bit for each physical sector, including any 8 KB sectors.
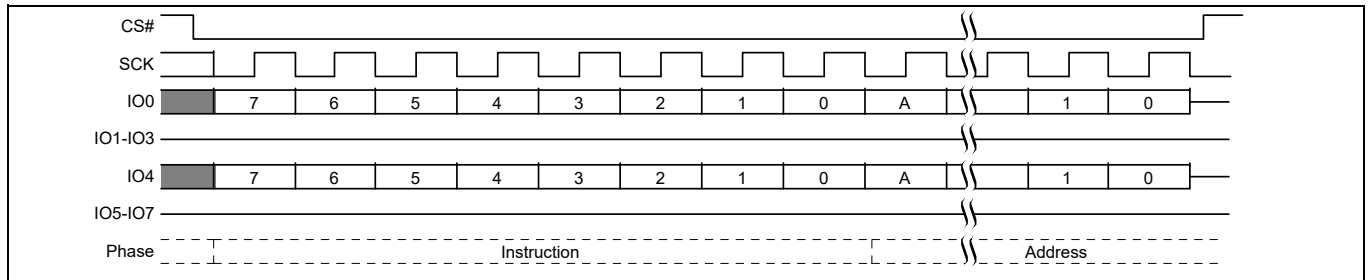
Commands

Figure 77 **Sector Erase (SE D8h or 4SE DCh) command sequence**[55]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
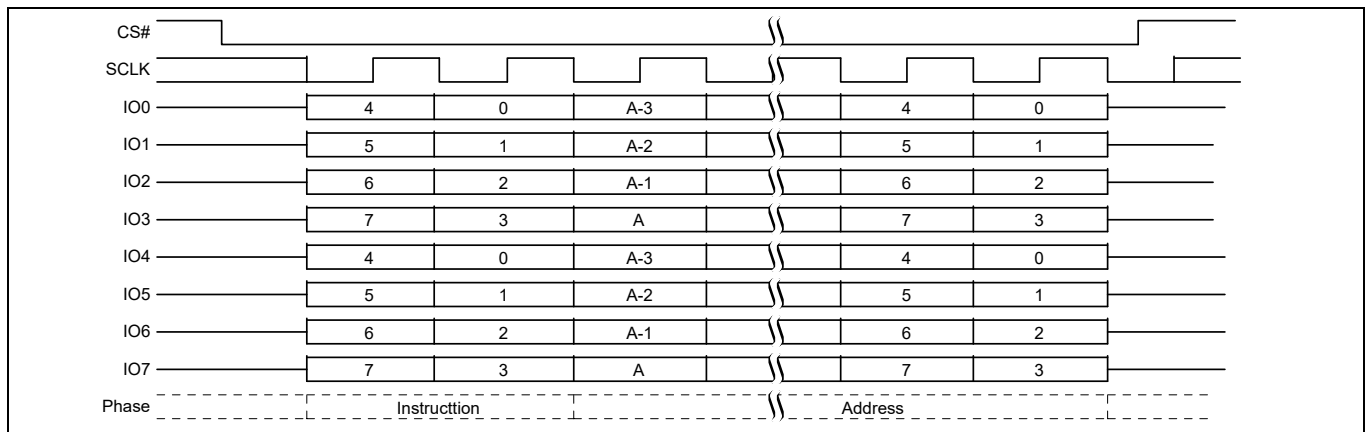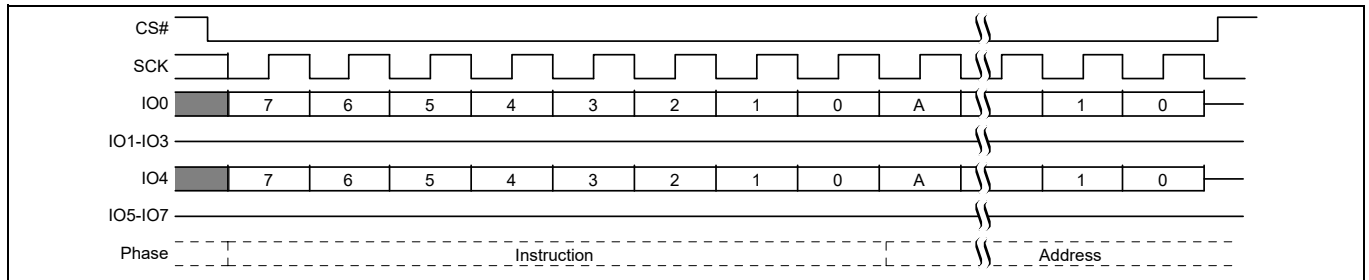

Figure 78 **Sector Erase (SE D8h or 4SE DCh) QPI mode command sequence**[55]

Note
 55. A = MSb of address = A23 for SE D8h with CR2V[7] = 0, or A31 for SE D8h with CR2V[7] = 1 or 4P4E DCh.

11.6.3   Bulk Erase (BE 60h or C7h)

The Bulk Erase (BE) command sets all bits to '1' (all bytes are FFh) inside the entire flash memory array. Before the BE command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 and IO7. This will initiate the erase cycle, which involves the pre-programming and erase of the entire flash memory array. If CS# is not driven HIGH after the last bit of instruction, the BE operation will not be executed.

As soon as CS# is driven into the logic HIGH state, the erase cycle will be initiated. With the erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate '1', when the erase cycle is in progress and '0', when the erase cycle has been completed.

A BE command can be executed only when the Block Protection (BP2, BP1, BP0) bits are set to 0s. If the BP bits are not '0', the BE command is not executed and E_ERR is not set. The BE command will skip any sectors protected by the DYB or PPB and the E_ERR status will not be set.

Figure 79   Bulk Erase command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.

Figure 80   Bulk Erase command sequence QPI mode

11.6.4   Evaluate Erase Status (EES D0h)

The Evaluate Erase Status (EES) command verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased, the erase status bit (SR2V[2]) is set to '1'. If the selected sector was not completely erased, SR2V[2] is '0'.

The EES command can be used to detect erase operations failed due to loss of power, reset, or failure during the erase operation.

The EES instruction is followed by a 3- or 4-byte address, depending on the address length configuration (CR2V[7]). The EES command requires tEES to complete and update the erase status in SR2V. The WIP bit (SR1V[0]) may be read using the RDSR1 (05h) command, to determine when the EES command is finished. Then the RDSR2 (07h) or the RDAR (65h) command can be used to read SR2V[2]. If a sector is found not erased with SR2V[2] = 0, the sector must be erased again to ensure reliable storage of data in the sector.

The Write Enable command (to set the WEL bit) is not required before the EES command. However, the WEL bit is set by the device itself and cleared at the end of the operation, as visible in SR1V[1] when reading status.

Figure 81   EES command sequence[56]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
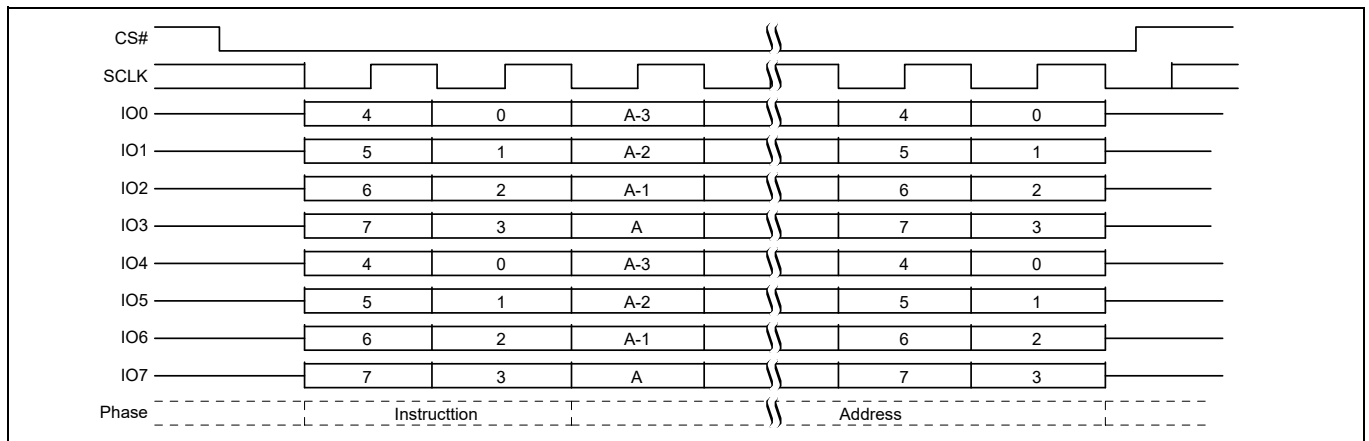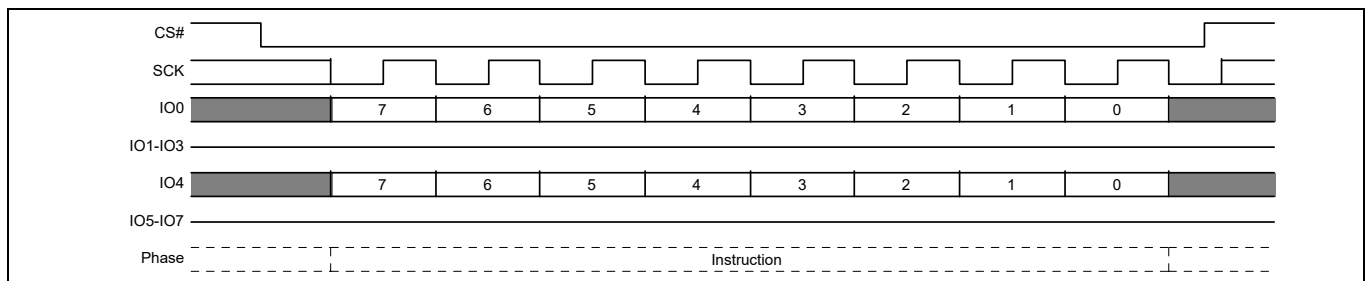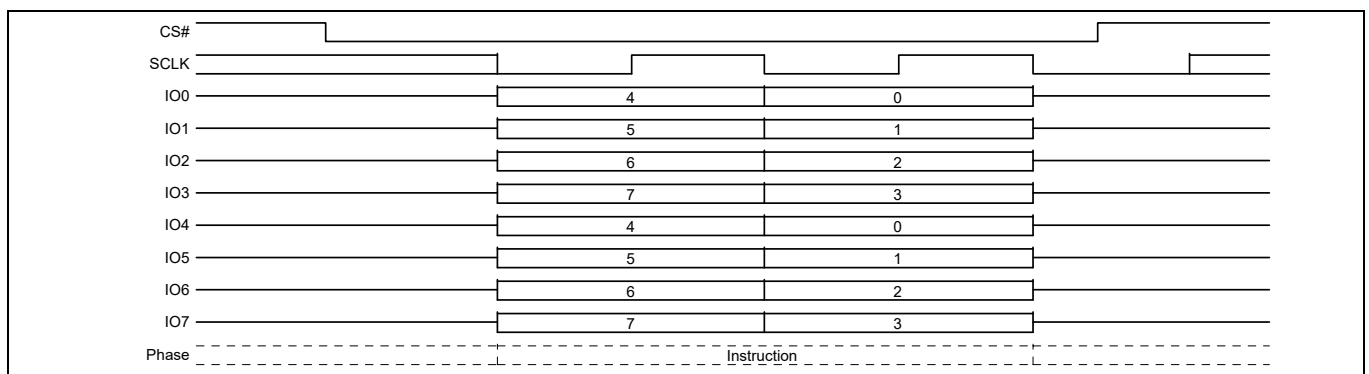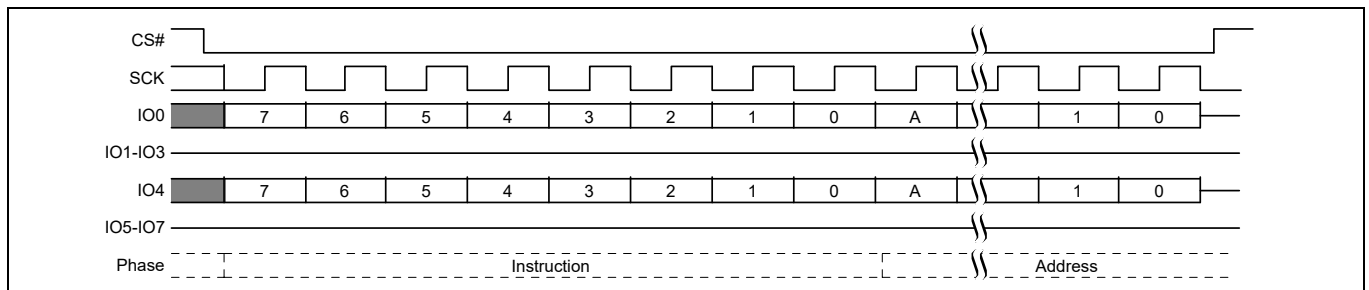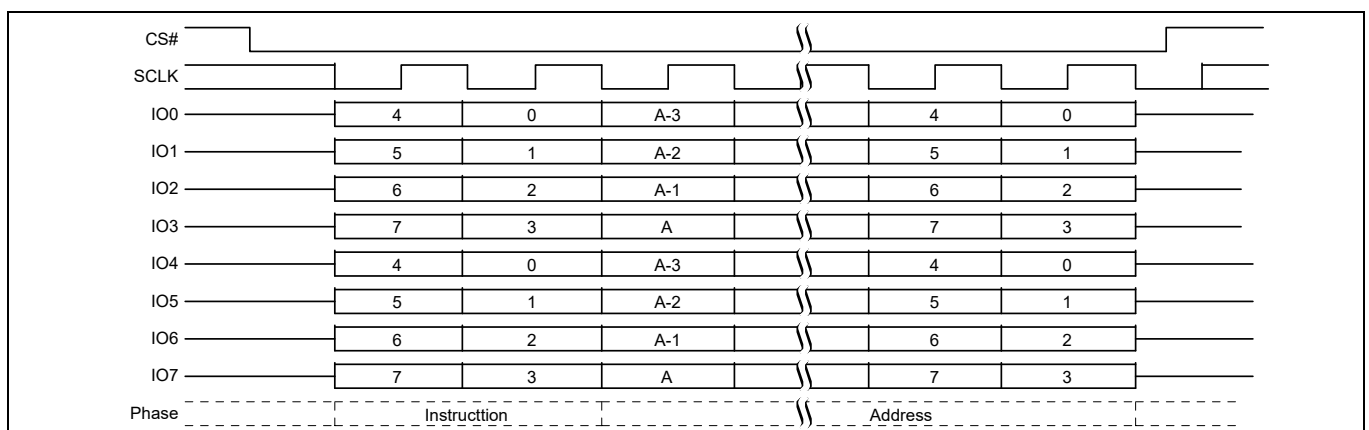

Figure 82   EES QPI mode command sequence[56]

Note
56. A = MSb of address = A23 for CR2V[7] = 0, or A31 for CR2V[7] = 1.

11.6.5 Erase or Program Suspend (EPS 85h, 75h, B0h)

There are three instruction codes for Program or Erase Suspend (EPS) to enable legacy and alternate source software compatibility.

The EPS command allows the system to interrupt a programming or erase operation and then read from any other non-erase-suspended sector or non-program-suspended-page. Program or Erase Suspend is valid only during a programming or sector erase operation. A Bulk Erase operation cannot be suspended.

The Write in Progress (WIP) bit in Status Register 1 (SR1V[0]) must be checked to know when the programming or erase operation has stopped. The Program Suspend Status bit in the Status Register 2 (SR2[0]) can be used to determine if a programming operation has been suspended or was completed at the time WIP changes to '0'. The Erase Suspend Status bit in the Status Register 2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to '0'. The time required for the suspend operation to complete is t_{SL}, see **Table 53**.

An Erase can be suspended to allow a program operation or a read operation. During an erase suspend, the DYB array may be read to examine sector protection and written to remove or restore protection on a sector to be programmed.

A program operation may be suspended to allow a read operation.

A new erase operation is not allowed with an already suspended erase or program operation. An erase command is ignored in this situation.

Table 51   Commands allowed during Program or Erase Suspend

Instruction name	Instruction code (Hex)	Allowed during Erase Suspend	Allowed during Program Suspend	Comment
PP	02	X	–	Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
READ	03	X	X	All array reads allowed in suspend.
RDSR1	05	X	X	Needed to read WIP to determine end of suspend process.
RDAR	65	X	X	Alternate way to read WIP to determine end of suspend process.
WREN	06	X		Required for program command within erase suspend.
RDSR2	07	X	X	Needed to read suspend status to determine whether the operation is suspended or complete.
4PP	12	X	–	Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
4READ	13	X	X	All array reads allowed in suspend.
CLSR	30	X	–	Clear status may be used if a program operation fails during erase suspend. Note the instruction is only valid if enabled for clear status by CR4NV[2 = 1].
CLSR	82	X	–	Clear status may be used if a program operation fails during erase suspend.
EPR	30	X	X	Required to resume from erase or program suspend. Note the command must be enabled for use as a resume command by CR3NV[2] = 1.
EPR	7A	X	X	Required to resume from erase or program suspend.
EPR	8A	X	X	Required to resume from erase or program suspend.

Commands

Table 51   Commands allowed during Program or Erase Suspend (Continued)

Instruction name	Instruction code (Hex)	Allowed during Erase Suspend	Allowed during Program Suspend	Comment
RSTEN	66	X	X	Reset allowed anytime.
RST	99	X	X	Reset allowed anytime.
FAST_READ	0B	X	X	All array reads allowed in suspend.
4FAST_READ	0C	X	X	All array reads allowed in suspend.
EPR	7A	X	–	Required to resume from erase suspend.
EPR	8A	X	–	Required to resume from erase suspend.
DIOR	BB	X	X	All array reads allowed in suspend.
4DIOR	BC	X	X	All array reads allowed in suspend.
DYBRD	FA	X	–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
DYBWR	FB	X	–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
PPBRD	FC	X	–	Allowed for checking persistent protection before attempting a program command during erase suspend.
4DYBRD	E0	X	–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
4DYBWR	E1	X	–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
4PPBRD	E2	X	–	Allowed for checking persistent protection before attempting a program command during erase suspend.
QIOR	EB	X	X	All array reads allowed in suspend.
4QIOR	EC	X	X	All array reads allowed in suspend.
DDRQIOR	ED	X	X	All array reads allowed in suspend.
4DDRQIOR	EE	X	X	All array reads allowed in suspend.
RESET	F0	X	X	Reset allowed anytime.
MBR	FF	X	X	May need to reset a read operation during suspend.

Commands

Reading at any address within an erase-suspended sector or program-suspended page produces undetermined data.

The WRR, WRAR, or PPB Erase commands are not allowed during Erase or Program Suspend, it is therefore not possible to alter the Block Protection or PPB bits during Erase Suspend. If there are sectors that may need programming during Erase suspend, these sectors should be protected only by DYB bits that can be turned off during Erase Suspend.

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the WIP bit in the Status Register, just as in the standard program operation.

Figure 83   **Erase or Program Suspend command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.

Figure 84   **Erase or Program Suspend command sequence QPI mode**

Figure 85   **Program or Erase Suspend command with continuing instruction commands sequence**

11.6.6 Erase or Program Resume (EPR 7Ah, 8Ah, 30h)

An Erase or Program Resume command must be written to resume a suspended operation. There are three instruction codes for Erase or Program Resume (EPR) to enable legacy and alternate source software compatibility.

After program or read operations are completed during a program or erase suspend the Erase or Program Resume command is sent to continue the suspended operation.

After an Erase or Program Resume command is issued, the WIP bit in the Status Register 1 will be set to '1' and the programming operation will resume if one is suspended. If no program operation is suspended the suspended erase operation will resume. If there is no suspended program or erase operation the resume command is ignored.

Program or erase operations may be interrupted as often as necessary, e.g. a program suspend command could immediately follow a program resume command but, in order for a program or erase operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{RS}. See **Table 53**.
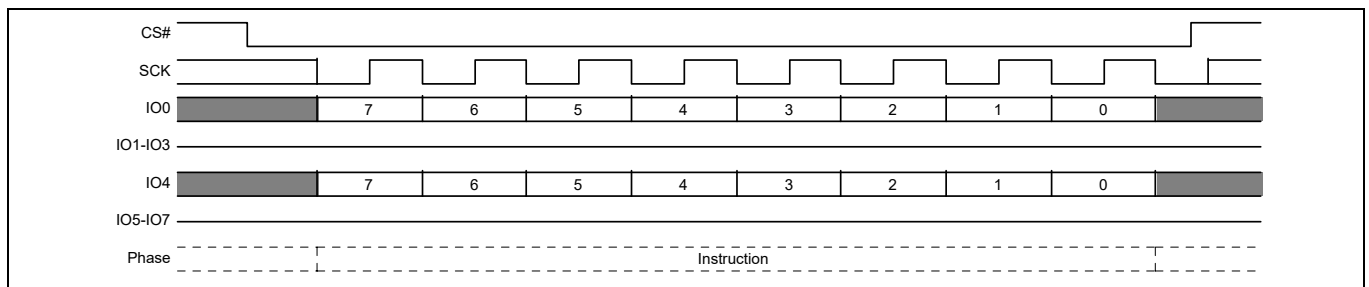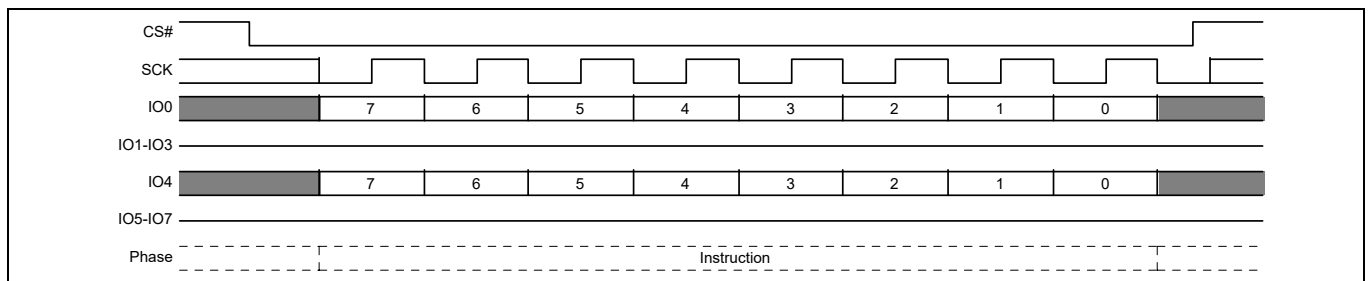

Figure 86   **Erase or Program Resume command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
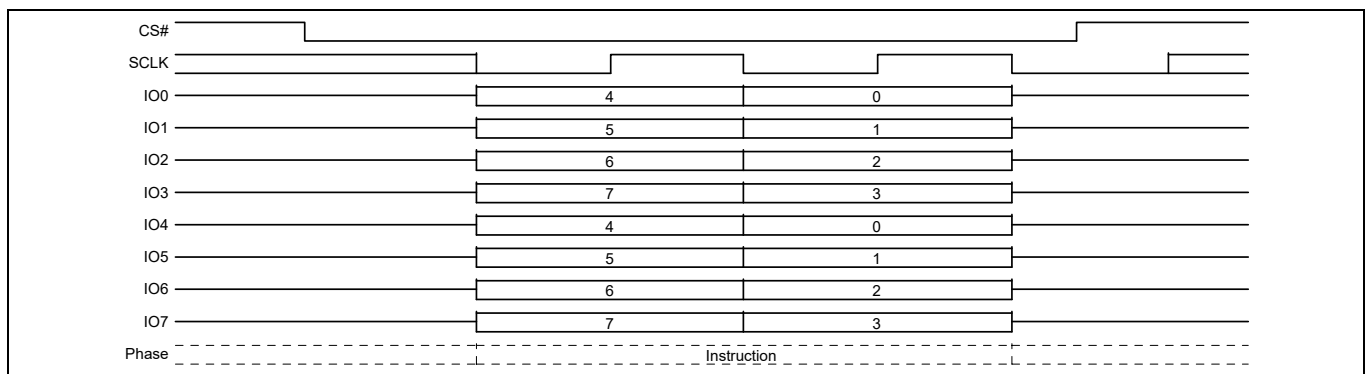

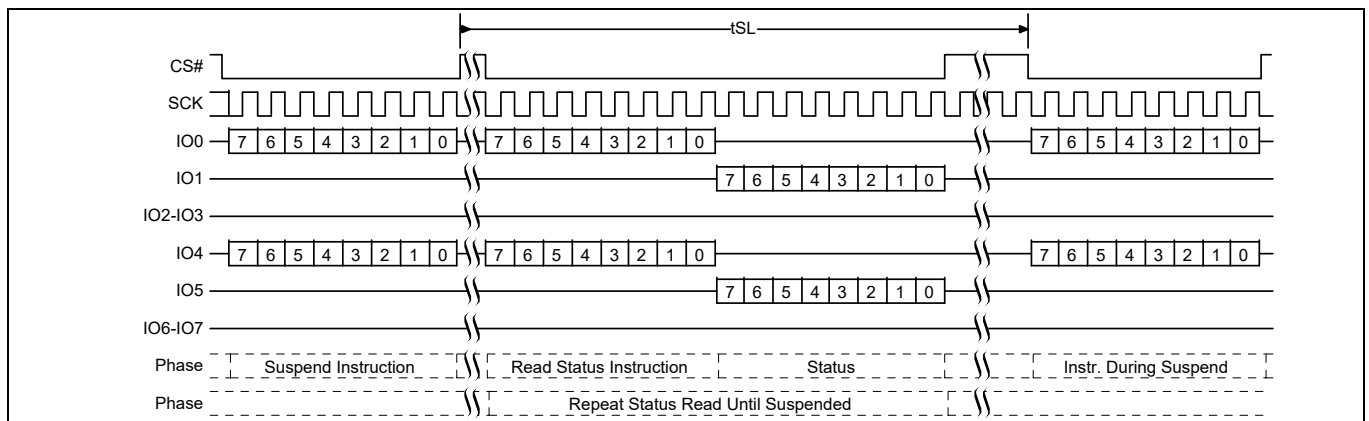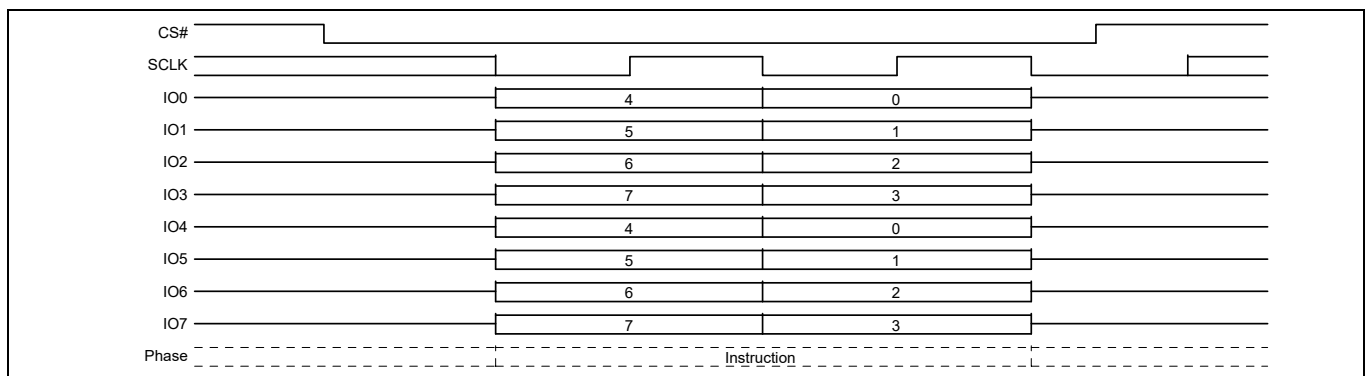**Figure 87**   **Erase or Program Resume command sequence QPI mode**

11.7 OTP Array commands

11.7.1 OTP Program (OTPP 42h)

The OTP Program command programs data in the OTP region, which is in a different address space from the main array data. The OTP region is 2048 bytes so, the address bits from A31 to A10 must be '0' for this command. Refer to **"OTP address space"** on page 45 for details on the OTP region.

Before the OTP Program command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the status register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR bit in SR1V may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to '1'.

Each region in the OTP memory space can be programmed one or more times, provided that the region is not locked. Attempting to program zeros in a region that is locked will fail with the P_ERR bit in SR1V set to '1'. Programming ones, even in a protected area does not cause an error and does not set P_ERR. Subsequent OTP programming can be performed only on the un-programmed bits (that is, one data). Programming more than once within an ECC unit will disable ECC on that unit.

The protocol of the OTP Program command is the same as the Page Program command. See **"Page Program (PP 02h or 4PP 12h)"** on page 113 for the command sequence.

11.7.2 OTP Read (OTPR 4Bh)

The OTP Read command reads data from the OTP region. The OTP region is 1024 bytes so, the address bits from A31 to A10 must be '0' for this command. Refer to **"OTP address space"** on page 45 for details on the OTP region. The protocol of the OTP Read command is similar to the Fast Read command except that it will not wrap to the starting address after the OTP address is at its maximum; instead, the data beyond the maximum OTP address will be undefined. The OTP Read command read latency is set by the latency value in CR2V[3:0].

See **"Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)"** on page 106 for the command sequence.

11.8 Advanced Sector Protection commands

11.8.1 ASP Read (ASPRD 2Bh)

The ASP Read instruction 2Bh is shifted into IO0 and IO4 by the rising edge of the SCK signal. Then the 16-bit ASP register contents are shifted out on the serial output IO1 and IO5, least significant byte first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the ASP register continuously by providing multiples of 16 clock cycles. The maximum operating clock frequency for the ASP Read (ASPRD) command is 133 MHz.
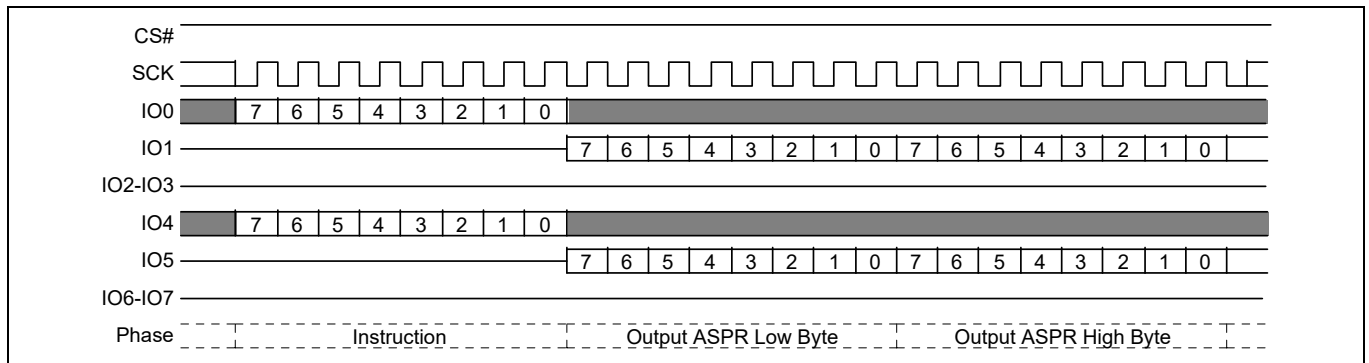
Figure 88   **ASPRD command**

11.8.2 ASP Program (ASPP 2Fh)

Before the ASP Program (ASPP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The ASPP command is entered by driving CS# to the logic LOW state, followed by the instruction and two data bytes on IO0 and IO4, least significant byte first. The ASP Register is two data bytes in length.

The ASPP command affects the P_ERR and WIP bits of the status and configuration registers in the same manner as any other programming operation.

CS# input must be driven to the logic HIGH state after the sixteenth bit of data has been latched in. If not, the ASPP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed ASPP operation is initiated. While the ASPP operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed ASPP operation, and is '0' when it is completed. When the ASPP operation is completed, the Write Enable Latch (WEL) is set to '0'.
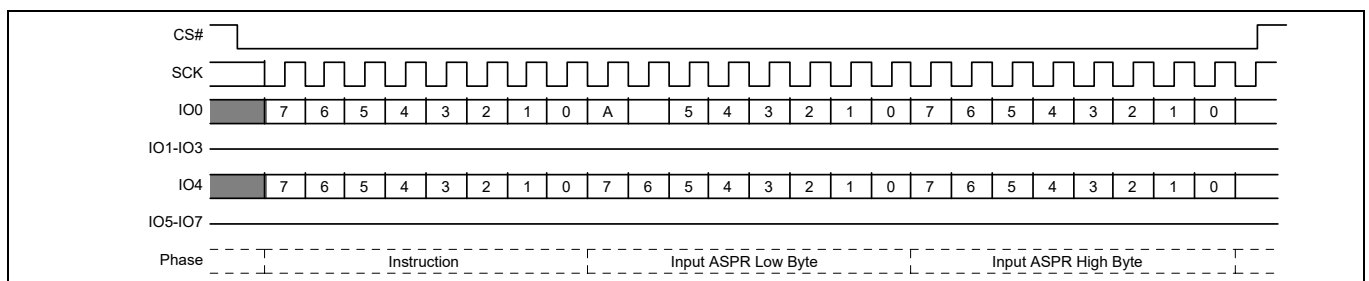
Figure 89   **ASPP command**

11.8.3 DYB Read (DYBRD FAh or 4DYBRD E0h)

The instruction is latched into IO0 and IO4 by the rising edge of the SCK signal. The instruction is followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector. Note, the high order address bits not used by a particular density device must be '0'. Then the 8-bit DYB access register contents are shifted out on the serial output IO1 and IO5. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the same DYB access register continuously by providing multiples of eight clock cycles. The address of the DYB register does not increment so this is not a means to read the entire DYB array. Each location must be read with a separate DYB Read command. The maximum operating clock frequency for READ command is 133 MHz.

Figure 90   DYBRD command sequence[57, 58]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2. The returning data is shifted out on IO0–IO3 for Quad SPI-1 and IO3–IO7 for Quad SPI-2.

Figure 91   DYBRD QPI mode command sequence[57, 58]

Notes

57. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FAh.
58. A = MSb of address = 31 with command E0h.

11.8.4 DYB Write (DYBWR FBh or 4DYBWR E1h)

Before the DYB Write (DYBWR) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the status register to enable any write operations.

The DYBWR command is entered by driving CS# to the logic LOW state, followed by the instruction, followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be '0'), then the data byte on IO0 and IO4. The DYB Access Register is one data byte in length. The data value must be 00h to protect or FFh to unprotect the selected sector.

The DYBWR command affects the P_ERR and WIP bits of the Status and Configuration Registers in the same manner as any other programming operation. CS# must be driven to the logic HIGH state after the eighth bit of data has been latched in. As soon as CS# is driven to the logic HIGH state, the self-timed DYBWR operation is initiated. While the DYBWR operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed DYBWR operation, and is '0' when it is completed. When the DYBWR operation is completed, the Write Enable Latch (WEL) is set to '0'.


Figure 92   DYBWR command sequence[59, 60]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2. The returning data is shifted out on IO0–IO3 for Quad SPI-1 and IO3–IO7 for Quad SPI-2.

Figure 93   DYBWR QPI mode command sequence[59, 60]

Notes
59. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FBh.
60. A = MSb of address = 31 with command E1h.

11.8.5   PPB Read (PPBRD FCh or 4PPBRD E2h)

The instruction E2h is shifted into IO0 and IO4 by the rising edges of the SCK signal, followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be '0'). Then the 8-bit PPB access register contents are shifted out on IO1 and IO5.

It is possible to read the same PPB access register continuously by providing multiples of eight clock cycles. The address of the PPB register does not increment so this is not a means to read the entire PPB array. Each location must be read with a separate PPB Read command. The maximum operating clock frequency for the PPB Read command is 133 MHz.
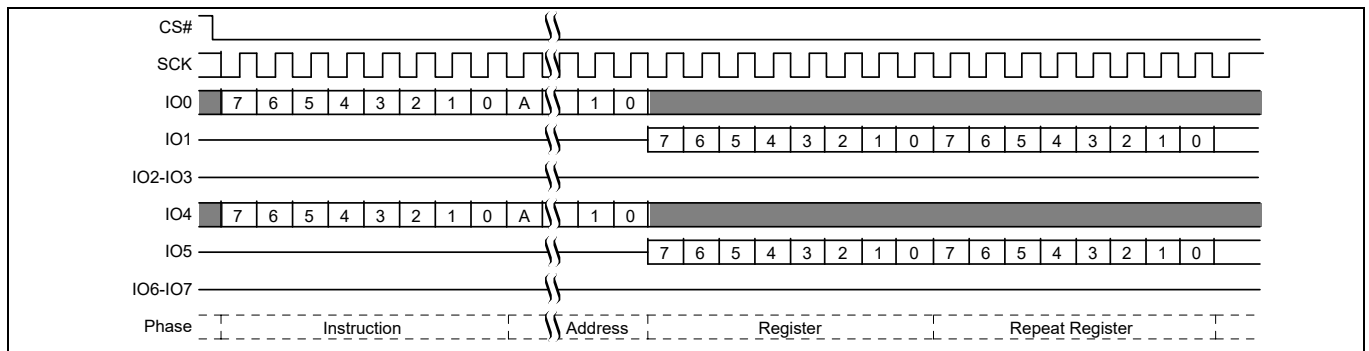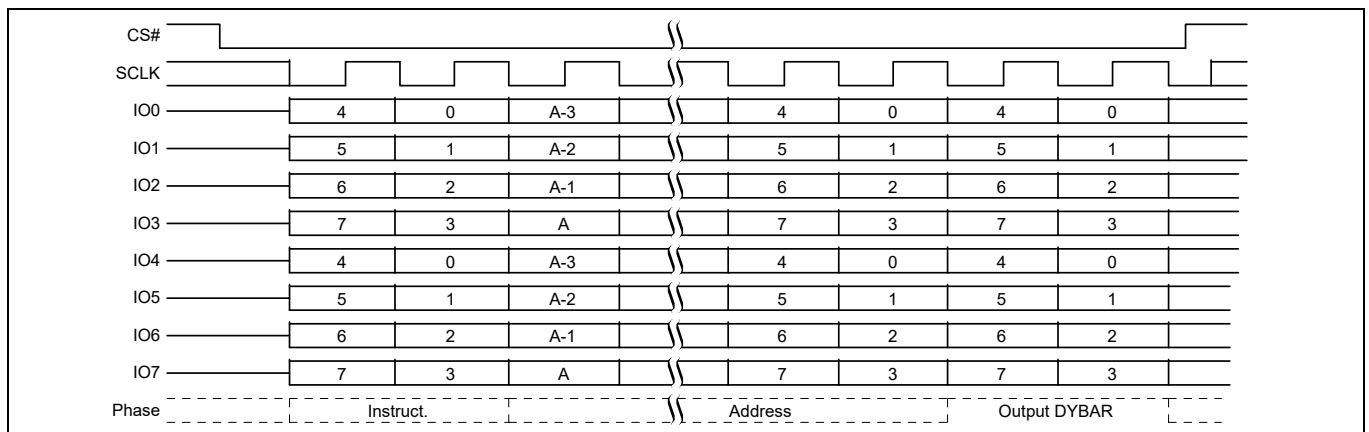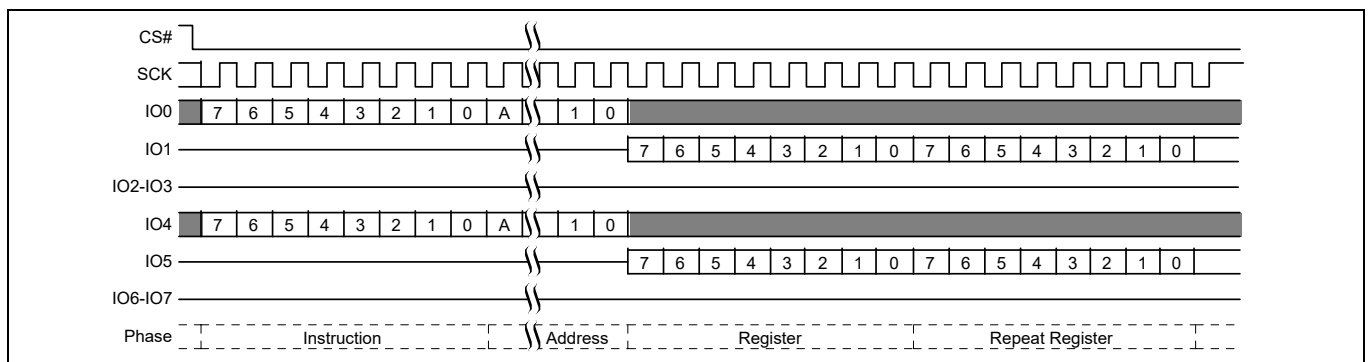

Figure 94   PPBRD command sequence[61, 62]

Notes
 61.A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FCh.
 62.A = MSb of address = 31 with command E2h.

11.8.6 PPB Program (PPBP FDh or 4PPBP E3h)

Before the PPB Program (PPBP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The PPBP command is entered by driving CS# to the logic LOW state, followed by the instruction, followed by the 24 or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be '0').

The PPBP command affects the P_ERR and WIP bits of the status and configuration registers in the same manner as any other programming operation.

CS# must be driven to the logic HIGH state after the last bit of address has been latched in. If not, the PPBP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PPBP operation is initiated. While the PPBP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed PPBP operation, and is '0' when it is completed. When the PPBP operation is completed, the Write Enable Latch (WEL) is set to '0'.
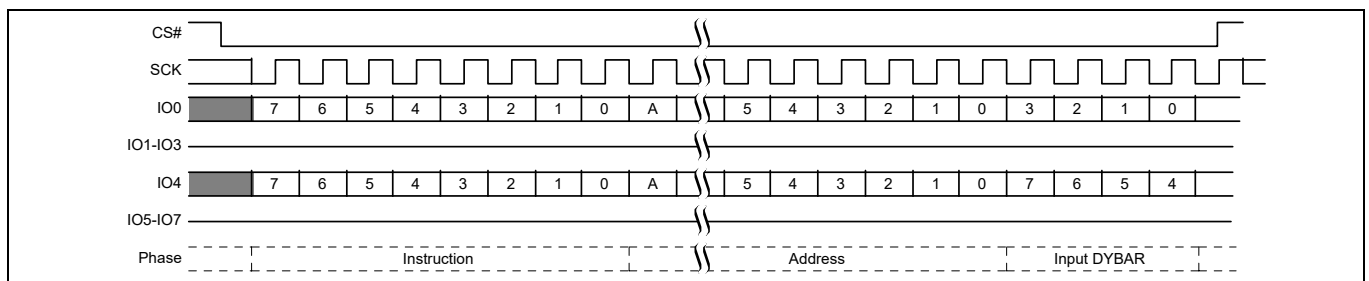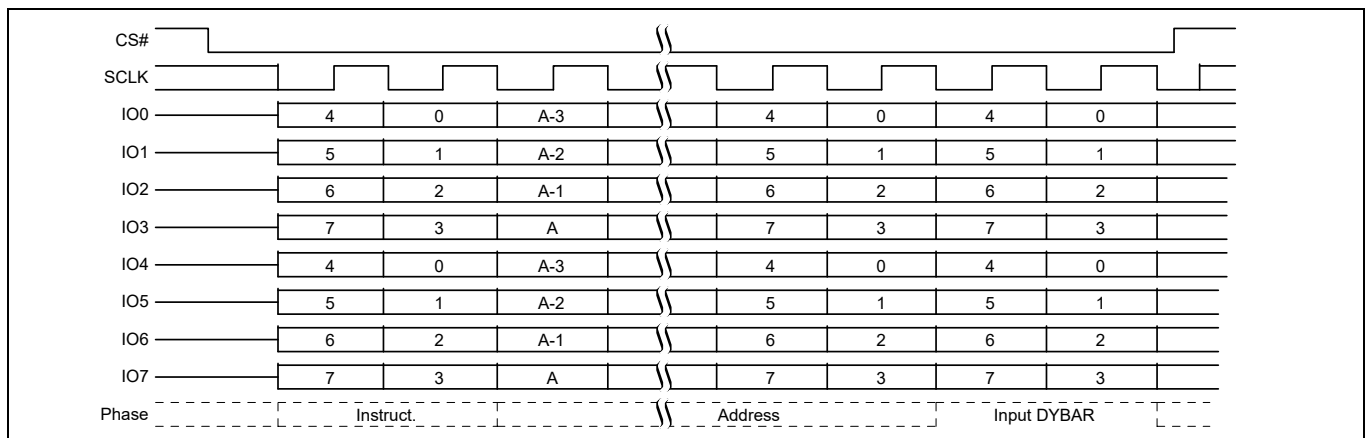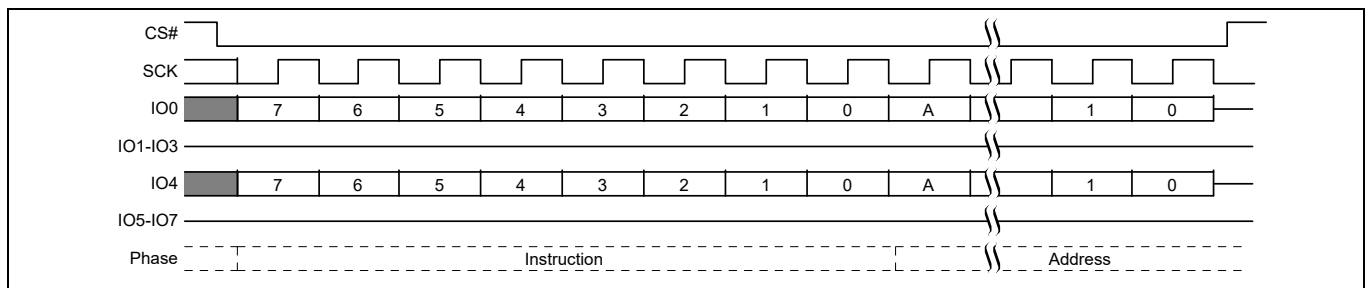

Figure 95   PPBP command sequence[63, 64]

Notes
 63. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FDh.
 64. A = MSb of address = 31 with command E3h.

11.8.7 PPB Erase (PPBE E4h)

The PPB Erase (PPBE) command sets all PPB bits to '1'. Before the PPB Erase command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction E4h is shifted into IO0 and IO4 by the rising edges of the SCK signal.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on IO0 and IO4. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the entire PPB memory array. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction, the PPB erase operation will not be executed.

With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate '1', when the erase cycle is in progress and '0', when the erase cycle has been completed. Erase suspend is not allowed during PPB Erase.
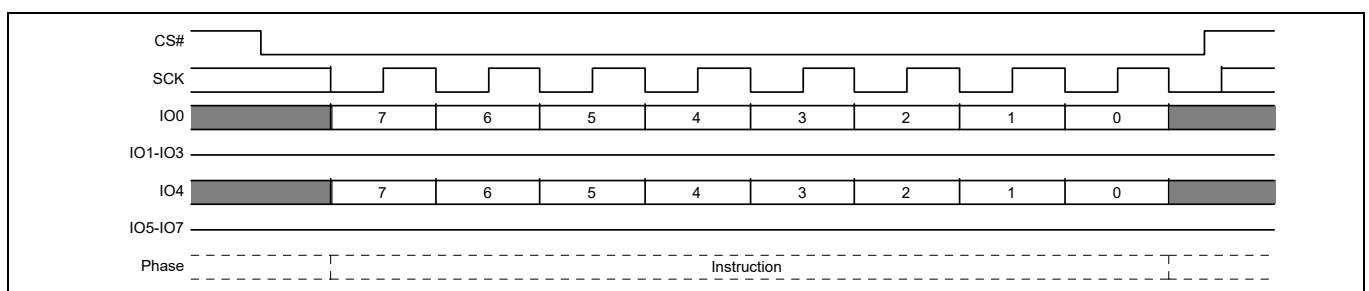
Figure 96   PPB Erase command sequence

11.8.8 PPB Lock Bit Read (PLBRD A7h)

The PPB Lock Bit Read (PLBRD) command allows the PPB lock register contents to be read out of IO1 and IO5. It is possible to read the PPB lock register continuously by providing multiples of eight clock cycles. The PPB Lock Register contents may only be read when the device is in standby state with no other operation in progress. It is recommended to check the Write-In Progress (WIP) bit of the status register before issuing a new command to the device.
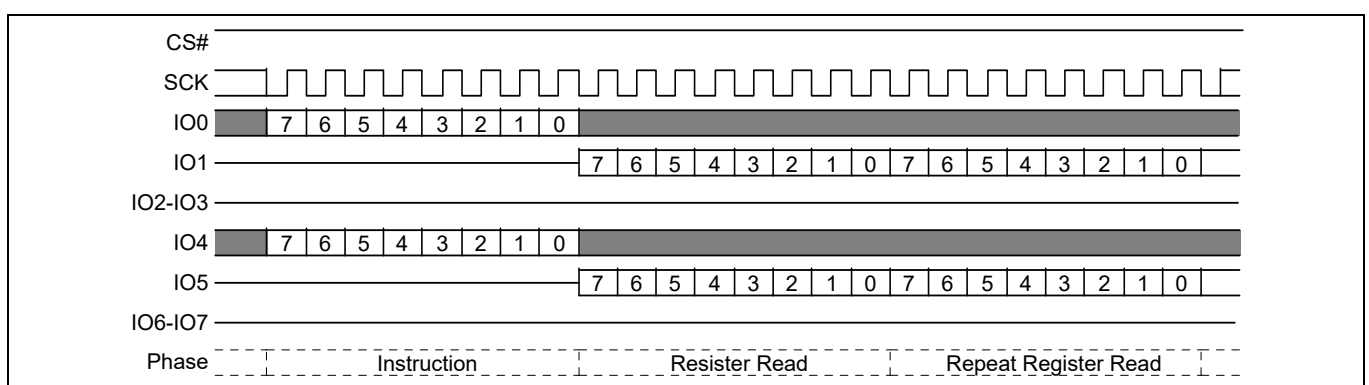
Figure 97   PPB Lock Register Read command sequence

11.8.9 PPB Lock Bit Write (PLBWR A6h)

The PPB Lock Bit Write (PLBWR) command clears the PPB Lock Register to zero. Before the PLBWR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The PLBWR command is entered by driving CS# to the logic LOW state, followed by the instruction.

CS# must be driven to the logic HIGH state after the eighth bit of instruction has been latched in. If not, the PLBWR command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PLBWR operation is initiated. While the PLBWR operation is in progress, the status register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed PLBWR operation, and is '0' when it is completed. When the PLBWR operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PLBWR command is 133 MHz.
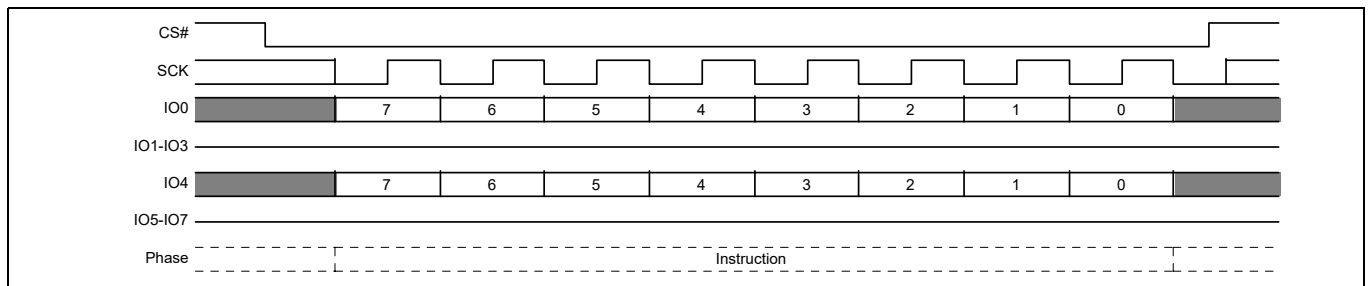
Figure 98   PPB Lock Bit Write command sequence

11.8.10 Password Read (PASSRD E7h)

The correct password value may be read only after it is programmed and before the Password Mode has been selected by programming the Password Protection Mode bit to '0' in the ASP Register (ASP[2]). After the Password Protection Mode is selected the password is no longer readable, the PASSRD command will output undefined data.

The PASSRD command is shifted into IO0 and IO4. Then the 64-bit password is shifted out on the serial output IO1 and IO5, least significant byte first, most significant bit of each byte first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the password continuously by providing multiples of 64 clock cycles. The maximum operating clock frequency for the PASSRD command is 133 MHz.
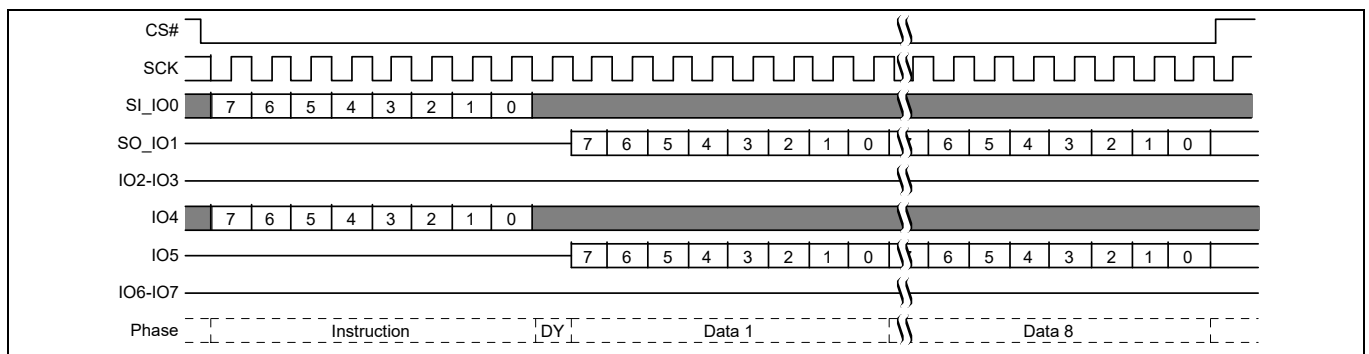
Figure 99   Password Read command sequence

11.8.11   Password Program (PASSP E8h)

Before the Password Program (PASSP) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded, the device sets the Write Enable Latch (WEL) to enable the PASSP operation.

The password can only be programmed before the Password Mode is selected by programming the Password Protection Mode bit to '0' in the ASP Register (ASP[2]). After the Password Protection Mode is selected the PASSP command is ignored.

The PASSP command is entered by driving CS# to the logic LOW state, followed by the instruction and the password data bytes on IO0 and IO4, least significant byte first, most significant bit of each byte first. The password is 64 bits in length.

CS# must be driven to the logic HIGH state after the 64th bit of data has been latched. If not, the PASSP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PASSP operation is initiated. While the PASSP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed PASSP cycle, and is '0' when it is completed. The PASSP command can report a program error in the P_ERR bit of the status register. When the PASSP operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PASSP command is 133 MHz.
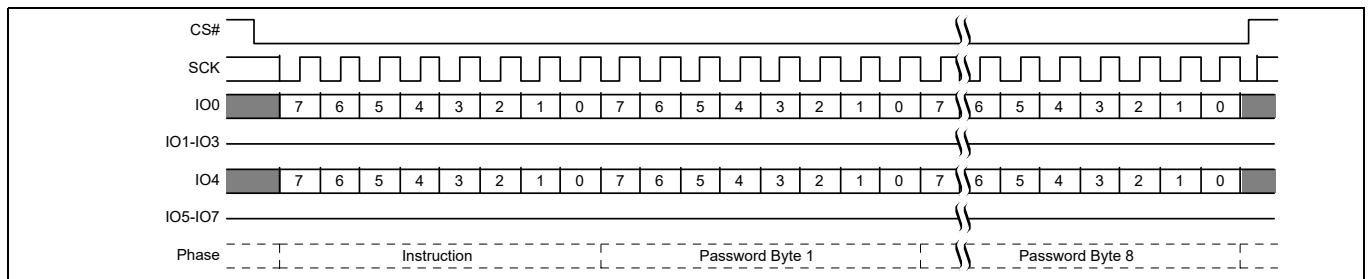
Figure 100   Password Program command sequence

11.8.12   Password Unlock (PASSU E9h)

The PASSU command is entered by driving CS# to the logic LOW state, followed by the instruction and the password data bytes on IO0 and IO4, least significant byte first, most significant bit of each byte first. The password is 64 bits in length.

CS# must be driven to the logic HIGH state after the 64th bit of data has been latched. If not, the PASSU command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PASSU operation is initiated. While the PASSU operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is '1' during the self-timed PASSU cycle, and is '0' when it is completed.

If the PASSU command supplied password does not match the hidden password in the Password Register, an error is reported by setting the P_ERR bit to '1'. The WIP bit of the Status Register also remains set to '1'. It is necessary to use the CLSR command to clear the Status Register, the RESET command to software reset the device, or drive the RESET# input LOW to initiate a hardware reset, in order to return the P_ERR and WIP bits to '0'. This returns the device to standby state, ready for new commands such as a retry of the PASSU command.

If the password does match, the PPB Lock bit is set to '1'. The maximum clock frequency for the PASSU command is 133 MHz.
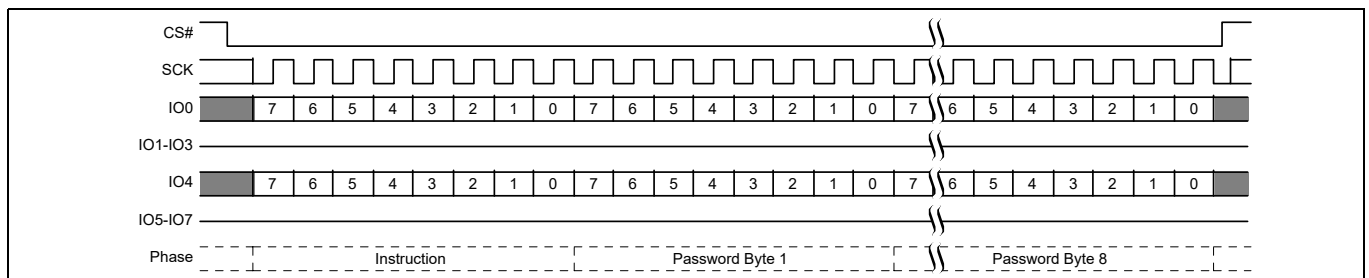
Figure 101   Password Unlock command sequence

11.9 Reset commands

Software controlled Reset commands restore the device to its initial power up state, by reloading volatile registers from non-volatile default values. However, the volatile FREEZE bit in the Configuration Register CR1V[0] and the volatile PPB Lock bit in the PPB Lock Register are not changed by a software reset. The software reset cannot be used to circumvent the FREEZE or PPB Lock bit protection mechanisms for the other security configuration bits.

The Freeze bit and the PPB Lock bit will remain set at their last value prior to the software reset. To clear the FREEZE bit and set the PPB Lock bit to its protection mode selected power on state, a full POR sequence or hardware reset must be done.

The non-volatile bits in the Configuration Register (CR1NV), TBPROT_O, TBPARM, and BPNV_O, retain their previous state after a Software Reset.

The Block Protection bits BP2, BP1, and BP0, in the status register (SR1V) will only be reset to their default value if FREEZE = 0.

A reset command (RST or RESET) is executed when CS# is brought HIGH at the end of the instruction and requires t_{RPH} time to execute.

In the case of a previous Power-up Reset (POR) failure to complete, a reset command triggers a full power-up sequence requiring t_{PU} to complete.

Figure 102   Software Reset command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.

Figure 103   Software Reset command sequence QPI mode

11.9.1 Software Reset Enable (RSTEN 66h)

The Reset Enable (RSTEN) command is required immediately before a Reset command (RST) such that a software reset is a sequence of the two commands. Any command other than RST following the RSTEN command, will clear the reset enable condition and prevent a later RST command from being recognized.

11.9.2 Software Reset (RST 99h)

The Reset (RST) command immediately following a RSTEN command, initiates the software reset process.

11.9.3 Legacy Software Reset (RESET F0h)

The Legacy Software Reset (RESET) is a single command that initiates the software reset process. This command is disabled by default but can be enabled by programming CR3V[0] = 1, for software compatibility with Infineon legacy FL-S devices.

11.9.4 Mode Bit Reset (MBR FFh)

The Mode Bit Reset (MBR) command is used to return the device from continuous high performance read mode back to normal standby awaiting any new command. Because some device packages lack a hardware RESET# input and a device that is in a continuous high performance read mode may not recognize any normal SPI command, a system hardware reset or software reset command may not be recognized by the device. It is recommended to use the MBR command after a system reset when the RESET# signal is not available or, before sending a software reset, to ensure the device is released from continuous high performance read mode.

The MBR command sends Ones on SI/IO0 IO0 and IO4 for 8 SCK cycles. IO1–IO3 and IO5–IO7 are "don't care" during these cycles.

The MBR command sends Ones on IO0 and IO4 for 8 SCK cycles. IO1–IO3 and IO5–IO7 are "don't care" during these cycles.
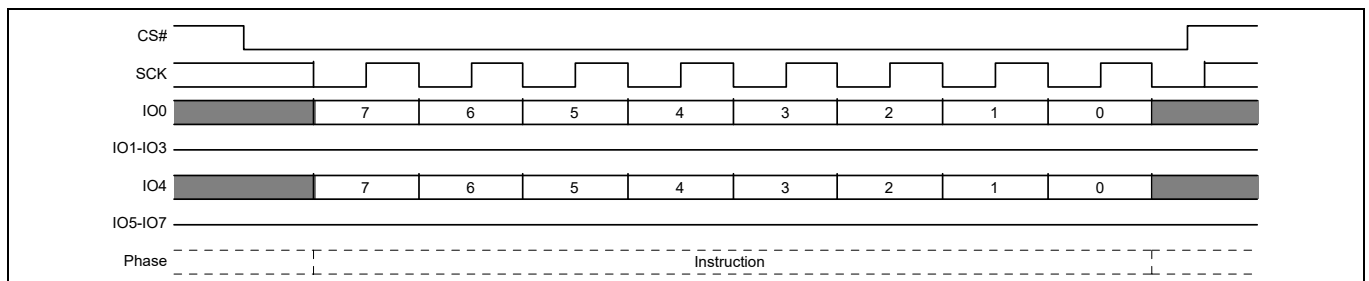
Figure 104   Mode Bit Reset command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
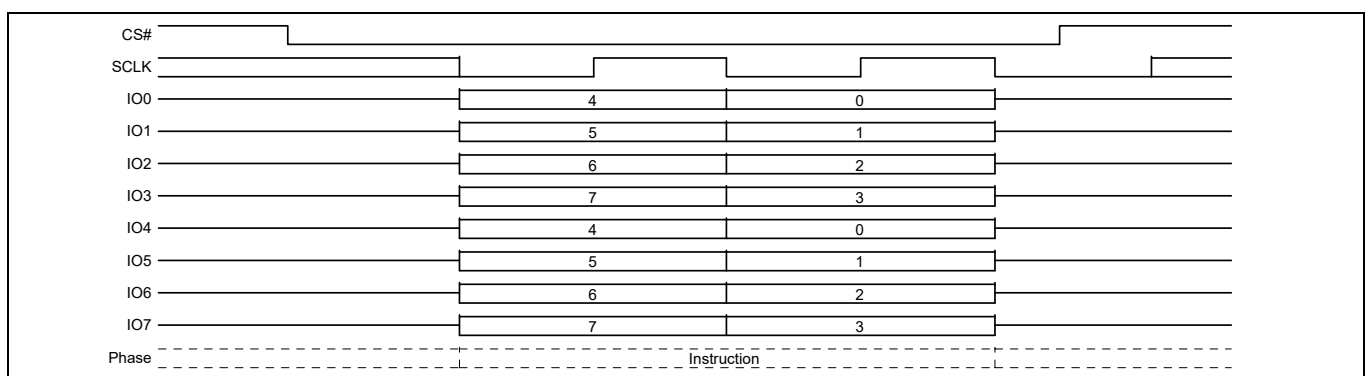
Figure 105   Mode Bit Reset command sequence QPI mode

11.10 DPD commands

11.10.1 Enter Deep Power-Down (DPD B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-Down command. The lower power consumption makes the Deep Power-Down (DPD) command especially useful for battery powered applications (see I_{DPD} in **"DC characteristics"** on page 28).

The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register 1 volatile Write In Progress (WIP) bit being cleared to '0' (SR1V[0] = 0).

The command is initiated by driving the CS# pin LOW and shifting the instruction code 'B9h' as shown in **Figure 106**. The CS# pin must be driven HIGH after the eighth bit has been latched. If this is not done the Deep Power-Down command will not be executed. After CS# is driven HIGH, the power-down state will be entered within the time duration of t_{DPD} (refer to **"Timing specifications"** on page 30).

While in the power-down state only the Release from Deep Power-Down command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power Down state useful for write protection. The device always powers-up in the interface standby state with the standby current of I_{CC1}.
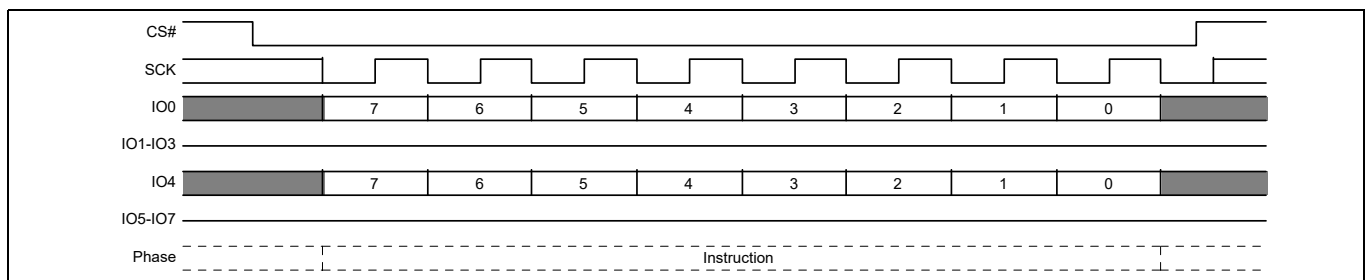
Figure 106 **Deep Power-Down command sequence**

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
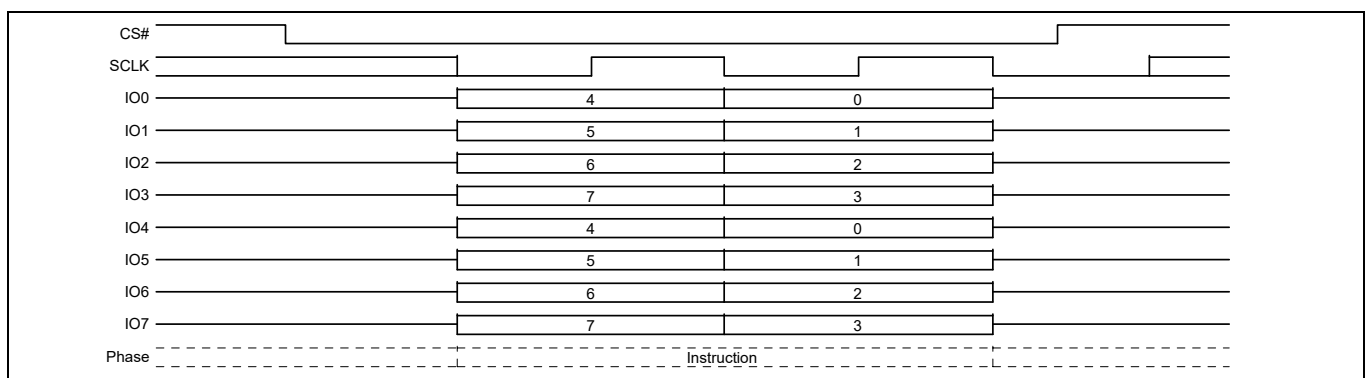
Figure 107 **DPD command sequence QPI mode**

11.10.2 Release from Deep Power-Down (RES ABh)

The Release from Deep Power-Down command is used to release the device from the deep power-down state. In some legacy SPI devices the RES command could also be used to obtain the device electronic identification (ID) number. However, the device ID function is not supported by the RES command.

To release the device from the deep power-down state, the command is issued by driving the CS# pin LOW, shifting the instruction code 'ABh' and driving CS# HIGH as shown in **Figure 108**. Release from deep power-down will take the time duration of t_{RES} (**"Timing specifications"** on page 30) before the device will resume normal operation and other commands are accepted. The CS# pin must remain HIGH during the t_{RES} time duration.

Hardware Reset will also release the device from the DPD state as part of the hardware reset process.
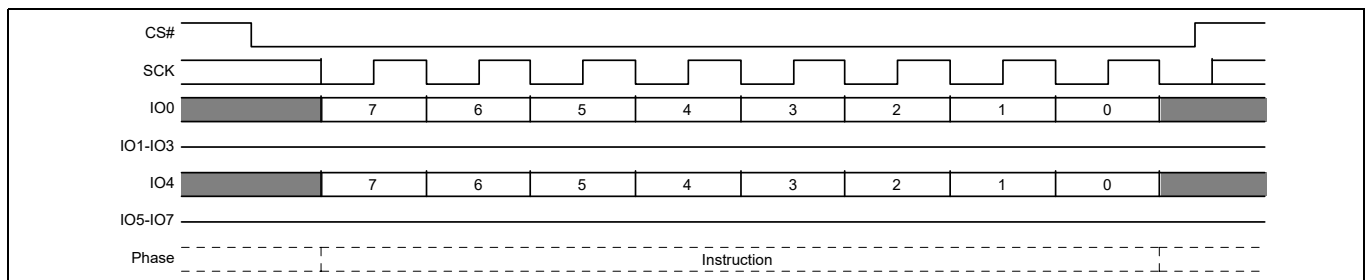
Figure 108   Release from Deep Power-Down command sequence
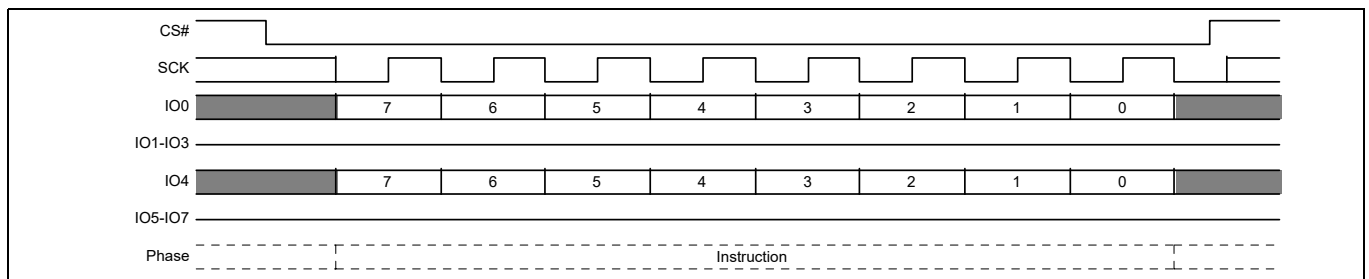
This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 for Quad SPI-1 and IO4–IO7 for Quad SPI-2.
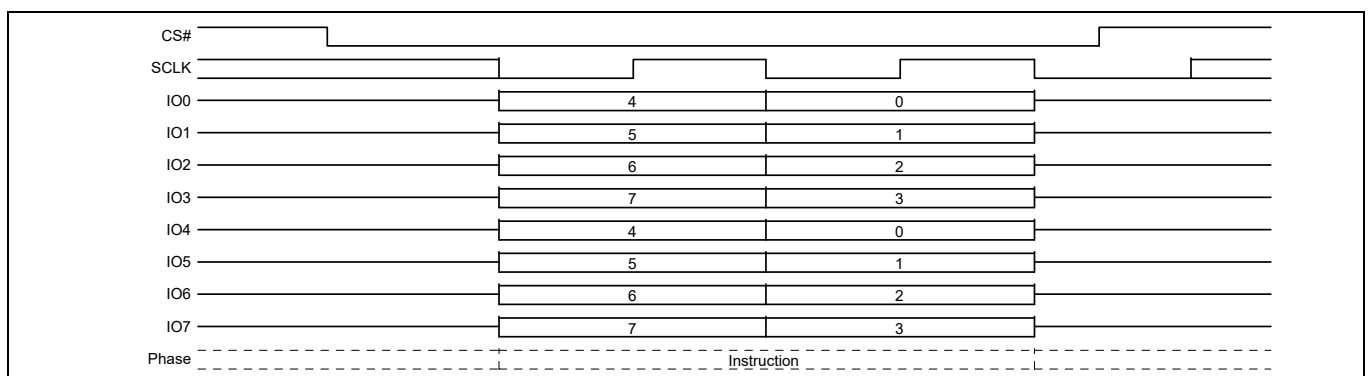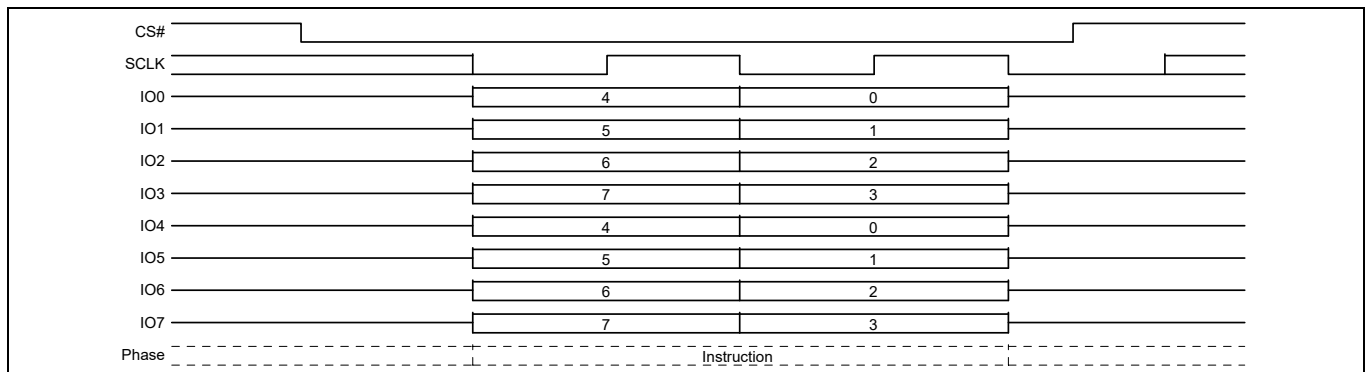

Figure 109   RES command sequence QPI mode

12 Embedded Algorithm Performance tables

Table 52 **Program and erase performance**

Symbol	Parameter	Min	Typ[66]	Max	Unit
t_W	Non-volatile Register Write Time	–	240	750	ms
t_{PP}	Page Programming (1024bytes) Page Programming (512 bytes)	–	475 360	2000 2000	μs
t_{SE}	Sector Erase Time (512 KB physical sectors)	–	930	2900	ms
	Sector Erase Time (8 KB sectors)	–	240	725	
t_{BE}[65]	Bulk Erase Time (S25FS01GS)	–	220	720	sec
tEES	Evaluate Erase Status Time (8 KB physical sectors)	–	20	25	μs
	Evaluate Erase Status Time (512 KB physical or logical sectors)	–	80	100	

Table 53 **Program or erase suspend AC parameters**

Parameter	Typical	Max	Unit	Comments
Suspend Latency (t_{SL})	–	50	μs	The time from Suspend command until the WIP bit is '0'.
Resume to next Program Suspend (t_{RS})	100	–	μs	Minimum is the time needed to issue the next Suspend command but ≥ typical periods are needed for Program or Erase to progress to completion.

Notes

65.Not 100% tested.

66.Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8 V; random data pattern.

67.The programming time for any OTP programming command is the same as t_{PP}. This includes OTPP 42h, PNVDLR 43h, ASPP 2Fh, and PASSP E8h.

68.The programming time for the PPBP E3h command is the same as t_{PP}. The erase time for PPBE E4h command is the same as t_{SE}.

69.Data retention of 20 years is based on 1k erase cycles or less.

13   Data integrity

13.1   Erase endurance

Table 54   Erase endurance

Parameter	Minimum	Unit
Program/erase cycles per main Flash array sectors	100K	P/E cycle
Program/erase cycles per PPB array or Non-volatile register array[70]		

13.2   Data retention

Table 55   Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	10K program/erase cycles	20	Years
	100K program/erase cycles	2	Years

Note

70. Each write command to a non-volatile register causes a P/E cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not P/E cycled.

13.3 Serial flash discoverable parameters (SFDP) address map

The SFDP tables are programmed for the S25FS512S individual Die, not referenced to the Dual-Quad S79FS01GS device.

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One parameter is mandated by the JEDEC JESD216 standard. Infineon provides an additional parameter by pointing to the ID-CFI address space, i.e. the ID-CFI address space is a sub-set of the SFDP address space. The JEDEC parameter is located within the ID-CFI address space and is thus both a CFI parameter and an SFDP parameter. In this way both SFDP and ID-CFI information can be accessed by either the RSFDP or RDID commands.

Table 56   SFDP overview map

Byte address	Description
0000h	Location zero within JEDEC JESD216B SFDP space – start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
1000h	Location zero within ID-CFI space – start of ID-CFI parameter tables
...	ID-CFI parameters
1090h	Start of SFDP parameter tables which are also grouped as one of the CFI parameter tables (the CFI parameter itself starts at 108Eh, the SFDP parameter table data is double word aligned starting at 1090h)
...	Remainder of SFDP parameter tables followed by either more CFI parameters or undefined space

13.3.1 Field definitions

Table 57   SFDP header

SFDP byte address	SFDP Dword name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space ASCII "S"
01h		46h	ASCII "F"
02h		44h	ASCII "D"
03h		50h	ASCII "P"
04h	SFDP Header 2nd DWORD	06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B) This revision is backward compatible with all prior minor revisions. Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields. Increments of the minor revision value indicate that previously reserved parameter fields may have been assigned a new definition or entire Dwords may have been added to the parameter table. However, the definition of previously existing fields is unchanged and therefore remain backward compatible with earlier SFDP parameter table revisions. Software can safely ignore increments of the minor revision number, as long as only those parameters the software was designed to support are used i.e. previously reserved fields and additional Dwords must be masked or ignored. Do not do a simple compare on the minor revision number, looking only for a match with the revision number that the software is designed to handle. There is no problem with using a higher number minor revision.
05h		01h	SFDP Major Revision This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		05h	Number of Parameter Headers (zero based, 05h = 6 parameters)
07h		FFh	Unused

Table 57   **SFDP header** (Continued)

SFDP byte address	SFDP Dword name	Data	Description
08h	Parameter Header 0 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		00h	Parameter Minor Revision (00h = JESD216) - This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 0 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a higher numbered minor revision that contains additional parameters for that software revision.
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		09h	Parameter Table Length (in double words = Dwords = 4 byte units) 09h = 9 Dwords
0Ch	Parameter Header 0 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h
0Dh		10h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)
10h	Parameter Header 1 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
11h		05h	Parameter Minor Revision (05h = JESD216 Revision A) - This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 5 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a later minor revision that contains additional parameters.
12h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.)
13h		10h	Parameter Table Length (in double words = Dwords = 4 byte units) 10h = 16 Dwords
14h	Parameter Header 1 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h address
15h		10h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18h	Parameter Header 2 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
19h		06h	Parameter Minor Revision (06h = JESD216 Revision B)
1Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
1Bh		10h	Parameter Table Length (in double words = Dwords = 4 byte units) 10h = 16 Dwords
1Ch	Parameter Header 2 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h address
1Dh		10h	Parameter Table Pointer Byte 1
1Eh		00h	Parameter Table Pointer Byte 2
1Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
20h	Parameter Header 3 1st DWORD	81h	Parameter ID LSB (81h = SFDP Sector Map Parameter)
21h		00h	Parameter Minor Revision (00h = Initial version as defined in JESD216 Revision B)
22h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
23h		10h (512 Mb)	Parameter Table Length (in double words = Dwords = 4 byte units) OPN Dependent 16 = 10h (512 Mb)

Table 57 **SFDP header** (Continued)

SFDP byte address	SFDP Dword name	Data	Description
24h	Parameter Header 3 2nd DWORD	D8h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC parameter byte offset = 10D8h
25h		10h	Parameter Table Pointer Byte 1
26h		00h	Parameter Table Pointer Byte 2
27h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
28h	Parameter Header 4 1st DWORD	84h	Parameter ID LSB (00h = SFDP 4 Byte Address Instructions Parameter)
29h		00h	Parameter Minor Revision (00h = Initial version as defined in JESD216 Revision B)
2Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
2Bh		02h	Parameter Table Length (in double words = Dwords = 4 byte units) (2h = 2 Dwords)
2Ch	Parameter Header 4 2nd DWORD	D0h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC parameter byte offset = 10D0h
2Dh		10h	Parameter Table Pointer Byte 1
2Eh		00h	Parameter Table Pointer Byte 2
2Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
30h	Parameter Header 5 1st DWORD	01h	Parameter ID LSB (Infineon Vendor Specific ID-CFI parameter) Legacy Manufacturer ID 01h = AMD / Infineon
31h		01h	Parameter Minor Revision (01h = ID-CFI updated with SFDP Rev B table)
32h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
33h		47h (512 Mb)	Parameter Table Length (in double words = Dwords = 4 byte units) Parameter Table Length (in double words = Dwords = 4 byte units)
34h	Parameter Header 5 2nd DWORD	00h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) Entry point for ID-CFI parameter is byte offset = 1000h relative to SFDP location zero.
35h		10h	Parameter Table Pointer Byte 1
36h		00h	Parameter Table Pointer Byte 2
37h		01h	Parameter ID MSB (01h = JEDEC JEP106 Bank Number 1)

13.4 Device ID and common flash interface (ID-CFI) address map

13.4.1 Field definitions

Table 58 **Manufacturer and Device ID**

Byte address	Data	Description
00h	01h	Manufacturer ID for Infineon
01h	02h	Device ID Most Significant Byte — Memory Interface Type
02h	20h (512 Mb in x8 Dual-Quad SPI)	Device ID Least Significant Byte — Density
03h	4Dh	ID-CFI Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID-CFI legacy address map. The legacy CFI address map ends with the Primary Vendor-Specific Extended Query. The original legacy length is maintained for backward software compatibility. However, the CFI Query Identification String also includes a pointer to the Alternate Vendor-Specific Extended Query that contains additional information related to the FS-S family.
04h	00h (Uniform 512 KB physical sectors)	Physical Sector Architecture The S79FS01GS may be configured with or without parameter sectors in addition to the uniform sectors.
05h	81h (FS-S Family)	Family ID
06h	xxh	ASCII characters for Model. Refer to **"Ordering part number"** on page 166 for the model number definitions.
07h	xxh	
08h	xxh	Reserved
09h	xxh	Reserved
0Ah	xxh	Reserved
0Bh	xxh	Reserved
0Ch	xxh	Reserved
0Dh	xxh	Reserved
0Eh	xxh	Reserved
0Fh	xxh	Reserved

Data integrity

Table 59   CFI query identification string

Byte address	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string "QRY"
13h 14h	02h 00h	Primary OEM Command Set FL-P backward compatible command set ID
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	53h 46h	Alternate OEM Command Set ASCII characters "FS" for SPI (F) interface, S Technology
19h 1Ah	51h 00h	Address for Alternate OEM Extended Table

Table 60   CFI system interface string

Byte address	Data	Description
1Bh	17h	V_{CC} Min. (erase / program): 100 mV BCD)
1Ch	19h	V_{CC} Max. (erase / program): 100 mV BCD)
1Dh	00h	V_{PP} Min. voltage (00h = no V_{PP} present)
1Eh	00h	V_{PP} Max. voltage (00h = no V_{PP} present)
1Fh	09h	Typical timeout per single byte program 2^N µs
20h	09h	Typical timeout for Min. size Page program 2^N µs (00h = not supported)
21h	0Ah (256 KB)	Typical timeout per individual sector erase 2^N ms
22h	11h (512 Mb)	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	02h	Max. timeout for byte program 2^N times typical
24h	02h	Max. timeout for page program 2^N times typical
25h	03h	Max. timeout per individual sector erase 2^N times typical
26h	03h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Data integrity

Table 61   Device geometry definition for bottom boot initial delivery state[71]

Byte address	Data	Description
27h	1Ah (512 Mb)	Device Size = 2^N bytes
28h	02h	Flash Device Interface Description: 0000h = x8 only
29h	01h	0001h = x16 only 0002h = x8/x16 capable 0003h = x32 only 0004h = Single I/O SPI, 3-byte address 0005h = Multi I/O SPI, 3-byte address 0102h = Multi I/O SPI, 3- or 4-byte address
2Ah	08h	Max. number of bytes in multi-byte write = 2^N
2Bh	00h	0000h = not supported 0008h = 256B page 0009h = 512B page
2Ch	03h	Number of Erase Block Regions within device 1 = Uniform Device, >1 = Boot Device
2Dh	07h	Erase Block Region 1 Information (refer to JEDEC JEP137) 8 sectors = 8-1 = 0007h 4 KB sectors = 256 bytes x 0010h
2Eh	00h	
2Fh	10h	
30h	00h	
31h	00h	Erase Block Region 2 Information (refer to JEDEC JEP137) 512 Mb: 1 sectors = 1-1 = 0000h 224 KB sector = 256 bytes x 0380h
32h	00h	
33h	80h	
34h	00h (128 Mb) 00h (256 Mb) 03h (512 Mb)	
35h	FEh	Erase Block Region 3 Information 512 Mb: 255 sectors = 255-1 = 00FEh 256 KB sectors = 0400h x 256 bytes
36h	00h (128 Mb) 01h (256 Mb) 00h (512 Mb) 01h (1 Gb	
37h	00h	
38h	01h (128 Mb) 01h (256 Mb) 04h (512 Mb) 04h (1 Gb)	
39h thru 3Fh	FFh	RFU

Note

71. FS512S die are user configurable to have either a hybrid sector architecture (with eight 4 KB sectors / one 224 KB sector and all remaining sectors are uniform 256 KB) or a uniform sector architecture with all sectors uniform 256 KB. FS-S devices are also user configurable to have the 4 KB parameter sectors at the top of memory address space. The CFI geometry information of the above table is relevant only to the initial delivery state. All devices are initially shipped from Infineon with the hybrid sector architecture with the 4 KB sectors located at the bottom of the array address map. However, the device configuration TBPARM bit CR1NV[2] may be programed to invert the sector map to place the 4 KB sectors at the top of the array address map. The 20h_NV bit (CR3NV[3} may be programmed to remove the 4 KB sectors from the address map. The flash device driver software must examine the TBPARM and 20h_NV bits to determine if the sector map was inverted or hybrid sectors removed at a later time.

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Table 62   **CFI primary vendor-specific extended query**

Byte address	Data	Description
40h	50h	Query-unique ASCII string "PRI"
41h	52h	
42h	49h	
43h	31h	Major version number = 1, ASCII
44h	33h	Minor version number = 3, ASCII
45h	21h	Address Sensitive Unlock (Bits 1–0) 00b = Required, 01b = Not Required Process Technology (Bits 5–2) 0000b = 0.23 µm Floating Gate 0001b = 0.17 µm Floating Gate 0010b = 0.23 µm MIRRORBIT™ 0011b = 0.11 µm Floating Gate 0100b = 0.11 µm MIRRORBIT™ 0101b = 0.09 µm MIRRORBIT™ 1000b = 0.065 µm MIRRORBIT™
46h	02h	Erase Suspend 0 = Not Supported, 1 = Read Only, 2 = Read and Program
47h	01h	Sector Protect 00 = Not Supported, X = Number of sectors in group
48h	00h	Temporary Sector Unprotect 00 = Not Supported, 01 = Supported
49h	08h	Sector Protect/Unprotect Scheme 04 = High Voltage Method 05 = Software Command Locking Method 08 = Advanced Sector Protection Method
4Ah	00h	Simultaneous Operation 00 = Not supported, X = Number of sectors
4Bh	01h	Burst Mode (Synchronous sequential read) support 00 = Not supported, 01 = Supported
4Ch	03h	Page Mode Type, initial delivery configuration, user configurable for 512B page 00 = Not Supported, 01 = 4 Word Read Page, 02 = 8 Read Word Page, 03 = 256 Byte Program Page, 04 = 512 Byte Program Page
4Dh	00h	ACC (Acceleration) Supply Minimum 00 = Not supported, 100 mV
4Eh	00h	ACC (Acceleration) Supply Maximum 00 = Not supported, 100 mV
4Fh	07h	WP# Protection 01 = Whole Chip 04 = Uniform Device with Bottom WP Protect 05 = Uniform Device with Top WP Protect 07 = Uniform Device with Top or Bottom Write Protect (user configurable)
50h	01h	Program Suspend 00 = Not supported, 01 = Supported

The alternate vendor-specific extended query provides information related to the expanded command set provided by the FS-S family. The alternate query parameters use a format in which each parameter begins with an identifier byte and a parameter length byte. Driver software can check each parameter ID and can use the length value to skip to the next parameter if the parameter is not needed or not recognized by the software.

Table 63   CFI alternate vendor-specific extended query header

Byte address	Data	Description
51h	41h	Query-unique ASCII string "ALT"
52h	4Ch	
53h	54h	
54h	32h	Major version number = 2, ASCII
55h	30h	Minor version number = 0, ASCII

Table 64   CFI alternate vendor-specific extended query parameter 0

Parameter relative byte address offset	Data	Description
00h	00h	Parameter ID (ordering part number)
01h	10h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	53h	ASCII "S" for manufacturer (Infineon)
03h	32h	ASCII "25" for Product Characters (Single Die SPI)
04h	35h	
05h	46h	ASCII "FS" for Interface Characters (SPI 1.8Volt)
06h	53h	
07h	35h (512 Mb)	ASCII characters for density
08h	31h (512 Mb)	
09h	32h (512 Mb)	
0Ah	53h	ASCII "S" for Technology (65-nm MIRRORBIT™)
0Bh	FFh	Reserved for Future Use
0Ch	FFh	
0Dh	FFh	Reserved for Future Use
0Eh	FFh	
0Fh	FFh	Reserved for Future Use
10h	xxh	ASCII characters for Model. Refer to **"Ordering part number"** on page 166 for the model number definitions.
11h	xxh	

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Table 65 **CFI alternate vendor-specific extended query parameter 80h address options**

Parameter relative byte address offset	Data	Description
00h	80h	Parameter ID (ordering part number)
01h	01h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	EBh	Bits 7:5 – Reserved = 111b Bit 4 – Address Length Bit in CR2V[7] – Yes= 0b Bit 3 – AutoBoot support – No = 1b Bit 2 – 4 byte address instructions supported – Yes= 0b Bit 1 – Bank address + 3 byte address instructions supported –No = 1b Bit 0 - 3 byte address instructions supported – No = 1b

Table 66 **CFI alternate vendor-specific extended query parameter 84h Suspend commands**

Parameter relative byte address offset	Data	Description
00h	84h	Parameter ID (Suspend Commands
01h	08h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	75h	Program suspend instruction code
03h	32h	Program suspend latency maximum (µs)
04h	7Ah	Program resume instruction code
05h	64h	Program resume to next suspend typical (µs)
06h	75h	Erase suspend instruction code
07h	32h	Erase suspend latency maximum (µs)
08h	7Ah	Erase resume instruction code
09h	64h	Erase resume to next suspend typical (µs)

Table 67   CFI alternate vendor-specific extended query parameter 88h Data Protection

Parameter relative byte address offset	Data	Description
00h	88h	Parameter ID (Data Protection)
01h	04h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	0Ah	OTP size 2^N bytes, FFh = not supported
03h	01h	OTP address map format, 01h = FL-S and FS-S format, FFh = not supported
04h	xxh	Block Protect Type, model dependent 00h = FL-P, FL-S, FS-S FFh = not supported
05h	xxh	Advanced Sector Protection type, model dependent 01h = FL-S and FS-S ASP

Table 68   CFI alternate vendor-specific extended query parameter 8Ch Reset Timing

Parameter relative byte address offset	Data	Description
00h	8Ch	Parameter ID (Reset Timing)
01h	06h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	96h	POR maximum value
03h	01h	POR maximum exponent 2^N µs
04h	23h	Hardware Reset maximum value, FFh = not supported (the initial delivery state has hardware reset disabled but it may be enabled by the user at a later time)
05h	00h	Hardware Reset maximum exponent 2^N µs
06h	23h	Software Reset maximum value, FFh = not supported
07h	00h	Software Reset maximum exponent 2^N µs

Table 69   CFI alternate vendor-specific extended query parameter 94h ECC

Parameter relative byte address offset	Data	Description
00h	94h	Parameter ID (ECC)
01h	01h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	10h	ECC unit size byte, FFh = ECC disabled

Table 70   CFI alternate vendor-specific extended query parameter F0h RFU

Parameter relative byte address offset	Data	Description
00h	F0h	Parameter ID (RFU)
01h	09h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter)
02h	FFh	RFU
...	FFh	RFU
0Ah	FFh	RFU

This parameter type (Parameter ID F0h) may appear multiple times and have a different length each time. The parameter is used to reserve space in the ID-CFI map or to force space (pad) to align a following parameter to a required boundary.

13.4.1.1   JEDEC SFDP Rev B Parameter tables

The SFDP Table are programmed for the S25FS512S individual Die, not referenced to the Dual-Quad S79FS01GS device.

From the view point of the CFI data structure, all of the SFDP parameter tables are combined into a single CFI Parameter as a contiguous byte sequence.

From the viewpoint of the SFDP data structure, there are three independent parameter tables. Two of the tables have a fixed length and one table has a variable structure and length depending on the device density Ordering Part Number (OPN). The Basic Flash Parameter table and the 4-byte Address Instructions Parameter table have a fixed length and are presented below as a single table. This table is Section 1 of the overall CFI parameter.

The JEDEC Sector Map Parameter table structure and length depends on the density OPN and is presented as a set of tables, one for each device density. The appropriate table for the OPN is Section 2 of the overall CFI parameter and is appended to Section 1.

Table 71   **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter**

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
00h	--	N/A	A5h	CFI Parameter ID (JEDEC SFDP)
01h	--	N/A	88h (512 Mb)	CFI Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value + 1 = the first byte of the next parameter). OPN dependent: 18Dw + 16Dw = 34Dw * 4B = 136B = 88h B (512 Mb)
02h	00h	JEDEC Basic Flash Parameter Dword-1	E7h	Start of SFDP JEDEC parameter, located at 1090h in the overall SFDP address space. Bits 7:5 = unused = 111b Bit 4:3 = 06h is status register write instruction and status register is default non-volatile = 00b Bit 2 = Program Buffer > 64 bytes = 1 Bits 1:0 = Uniform 4 KB erase unavailable = 11b
03h	01h		FFh	Bits 15:8 = Uniform 4 KB erase opcode = not supported = FFh
04h	02h		B2h (FSxxxSAG) BAh (FSxxxSDS)	Bit 23 = Unused = 1b Bit 22 = Supports Quad Out Read = No = 0b Bit 21 = Supports Quad I/O Read = Yes = 1b Bit 20 = Supports Dual I/O Read = Yes = 1b Bit19 = Supports DDR 0= No, 1 = Yes; FS-SAG = 0b, FS-SDS = 1b Bit 18:17 = Number of Address Bytes, 3 or 4 = 01b Bit 16 = Supports Dual Out Read = No = 0b
05h	03h		FFh	Bits 31:24 = Unused = FFh
06h	04h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 512 Mb = 1FFFFFFFh
07h	05h		FFh	
08h	06h		FFh	
09h	07h		1Fh (512 Mb)	

Table 71   **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
0Ah	08h	JEDEC Basic Flash Parameter Dword-3	48h	Bits 7:5 = number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = number of Quad I/O Dummy cycles = 01000b (Initial Delivery State)
0Bh	09h		EBh	Quad I/O instruction code
0Ch	0Ah		FFh	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 111b Bits 20:16 = number of Quad Out Dummy cycles = 11111b
0Dh	0Bh		FFh	Quad Out instruction code
0Eh	0Ch	JEDEC Basic Flash Parameter Dword-4	FFh	Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = 111b Bits 4:0 = number of Dual Out Dummy cycles = 11111b
0Fh	0Dh		FFh	Dual Out instruction code
10h	0Eh		88h	Bits 23:21 = number of Dual I/O (1-2-2) Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 01000b (Initial Delivery State)
11h	0Fh		BBh	Dual I/O instruction code
12h	10h	JEDEC Basic Flash Parameter Dword-5	FEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = Yes = 1b Bits 3:1 RFU = 111b Bit 0 = Dual All not supported = 0b
13h	11h		FFh	Bits 15:8 = RFU = FFh
14h	12h		FFh	Bits 23:16 = RFU = FFh
15h	13h		FFh	Bits 31:24 = RFU = FFh
16h	14h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
17h	15h		FFh	Bits 15:8 = RFU = FFh
18h	16h		FFh	Bits 23:21 = number of Dual All Mode cycles = 111b Bits 20:16 = number of Dual All Dummy cycles = 11111b
19h	17h		FFh	Dual All instruction code
1Ah	18h	JEDEC Basic Flash Parameter Dword-7	FFh	Bits 7:0 = RFU = FFh
1Bh	19h		FFh	Bits 15:8 = RFU = FFh
1Ch	1Ah		48h	Bits 23:21 = number of QPI Mode cycles = 010b Bits 20:16 = number of QPI Dummy cycles = 01000b
1Dh	1Bh		EBh	QPI mode Quad I/O (4-4-4) instruction code
1Eh	1Ch	JEDEC Basic Flash Parameter Dword-8	0Ch	Erase type 1 size 2^N bytes = 4 KB = 0Ch for Hybrid (Initial Delivery State)
1Fh	1Dh		20h	Erase type 1 instruction
20h	1Eh		10h	Erase type 2 size 2^N bytes = 64 KB = 10h
21h	1Fh		D8h	Erase type 2 instruction
22h	20h	JEDEC Basic Flash Parameter Dword-9	12h	Erase type 3 size 2^N bytes = 256 KB = 12h
23h	21h		D8h	Erase type 3 instruction
24h	22h		00h	Erase type 4 size 2^N bytes = not supported = 00h
25h	23h		FFh	Erase type 4 instruction = not supported = FFh

Table 71   **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
26h	24h		82h	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU)
27h	25h		42h	
28h	26h		11h	Bits 29:25 = Erase type 4 Erase, Typical time count = 11111b (RFU)
29h	27h	JEDEC Basic Flash Parameter Dword-10	FFh	Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128ms = 10b Bits 22:18 = Erase type 3 Erase, Typical time count = 00100b (typ erase time = count + 1 * units = 5 * 128 ms = 640 ms) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b Bits 15:11 = Erase type 2 Erase, Typical time count = 01000b (typ erase time = count + 1 * units = 9 * 16 ms = 144 ms) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16 ms = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 01000b (typ erase time = count + 1 * units = 9 * 16 ms = 144 ms) Bits 3:0 = Multiplier from typical erase time to maximum erase time = 2 * (N + 1), N = 2h = 6x multiplier Binary Fields: 11-11111-10-00100-01-01000-01-01000-0010 Nibble Format: 1111_1111_0001_0001_0100_0010_1000_0010 Hex Format: FF_11_42_82

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Table 71 **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
2Ah	28h		91h	Bit 31 Reserved = 1b
2Bh	29h		26h	Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s,
2Ch	2Ah		07h	11b: 64 s) = 512 Mb = 64 s = 11b
2Dh	2Bh	JEDEC Basic Flash Parameter Dword-11	E2h (512 Mb)	Bits 28:24 = Chip Erase, Typical time count, (count + 1)*units, 512 Mb = 00010b = 2 + 1 * 64 µs = 192 s Bits 23 = Byte Program Typical time, additional byte units (0b:1 µs, 1b:8 µs) = 1 µs = 0b Bits 22:19 = Byte Program Typical time, additional byte count, (count + 1)*units, count = 0000b, (typ Program time = count +1 * units = 1 * 1 µs = 1 µs Bits 18 = Byte Program Typical time, first byte units (0b:1 µs, 1b:8 µs) = 8 µs = 1b Bits 17:14 = Byte Program Typical time, first byte count, (count + 1) * units, count = 1100b, (typ Program time = count +1 * units = 13 * 8 µs = 104 µs) Bits 13 = Page Program Typical time units (0b:8 µs, 1b:64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical time count, (count + 1) * units, count = 00110b, (typ Program time = count + 1 * units = 7 * 64 µs = 448 µs) Bits 7:4 = Page size 2^N, N = 9h, = 512B page Bits 3:0 = Multiplier from typical time to maximum for Page or Byte program = 2 * (N + 1), N = 1h = 4x multiplier 128 Mb Binary Fields: 1-10-01000-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1100_1000_0000_0111_0010_0110_1001_0001 Hex Format: C8_07_26_91 256 Mb Binary Fields: 1-10-10001-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1101_0001_0000_0111_0010_0110_1001_0001 Hex Format: D1_07_26_91 512 Mb Binary Fields: 1-11-00010-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1110_0010_0000_0111_0010_0110_1001_0001 Hex Format: E2_07_26_91

Data integrity

Table 71   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
2Eh	2Ch		ECh	Bit 31 = Suspend and Resume supported = 0b
2Fh	2Dh		83h	Bits 30:29 = Suspend in-progress erase max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8µs= 10b
30h	2Eh		18h	Bits 28:24 = Suspend in-progress erase max latency count = 00100b, max erase suspend latency = count + 1 * units = 5 * 8 µs = 40 µs
31h	2Fh	JEDEC Basic Flash Parameter Dword-12	44h	Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count + 1 * 64 µs = 2 * 64 µs = 128 µs
				Bits 19:18 = Suspend in-progress program max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs= 10b
				Bits 17:13 = Suspend in-progress program max latency count = 00100b, max erase suspend latency = count + 1 * units = 5 * 8 µs = 40 µs
				Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count + 1 * 64 µs = 2 * 64 µs = 128 µs
				Bit 8 = RFU = 1b
				Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b
				Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b
				Binary Fields: 0-10-00100-0001-10-00100-0001-1-1110-1100 Nibble Format: 0100_0100_0001_1000_1000_0011_1110_1100 Hex Format: 44_18_83_EC
32h	30h	JEDEC Basic Flash Parameter Dword-13	8Ah	Bits 31:24 = Erase Suspend Instruction = 75h
33h	31h		85h	Bits 23:16 = Erase Resume Instruction = 7Ah
34h	32h		7Ah	Bits 15:8 = Program Suspend Instruction = 85h
35h	33h		75h	Bits 7:0 = Program Resume Instruction = 8Ah

Data integrity

Table 71   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B,
Section 1, basic flash parameter and 4-byte address instructions parameter (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
36h	34h		F7h	Bit 31 = Deep Power Down Supported = supported = 0
37h	35h		BDh	Bits 30:23 = Enter Deep Power Down Instruction = B9h
38h	36h		D5h	Bits 22:15 = Exit Deep Power Down Instruction = ABh
39h	37h	JEDEC Basic Flash Parameter Dword-14	5Ch	Bits 14:13 = Exit Deep Power Down to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 1 µs = 01b Bits 12:8 = Exit Deep Power Down to next operation delay count = 11101b, Exit Deep Power Down to next operation delay = (count + 1) * units = 29 + 1 * 1 µs = 30 µs Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). = 01b Bits 1:0 = RFU = 11b Binary Fields: 0-10111001-10101011-01-11101-1111-01-11 Nibble Format: 0101_1100_1101_0101_1011_1101_1111_0111 Hex Format: 5C_D5_BD_F7

Data integrity

Table 71 **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
3Ah	38h		8Ch	Bits 31:24 = RFU = FFh
3Bh	39h		F6h	Bit 23 = Hold and WP Disable = not supported = 0b Bits 22:20 = Quad Enable Requirements
3Ch	3Ah		5Dh	= 101b: QE is bit 1 of the Status Register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is '0'.
3Dh	3Bh	JEDEC Basic Flash Parameter Dword-15	FFh	Bits 19:16 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0] = Axh + 1xxxb: RFU = 1101b Bits 15:10 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxxb: Mode Bit[7:0] != Axh + 1x_x1xx: RFU = 11_1101 Bit 9 = 0-4-4 mode supported = 1 Bits 8:4 = 4-4-4 mode enable sequences = x_1xxxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 01000b Bits 3:0 = 4-4-4 mode disable sequences = x1xxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h.. This configuration is volatile. + 1xxxb: issue the Soft Reset 66/99 sequence = 1100b Binary Fields: 11111111-0-101-1101-111101-1-01000-1100 Nibble Format: 1111_1111_0101_1101_1111_0110_1000-1100 Hex Format: FF_5D_F6_8C

Table 71 **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
3Eh	3Ch		F0h	Bits 31:24 = Enter 4-Byte Addressing
3Fh	3Dh		30h	= xxxx_xxx1b: issue instruction B7h (preceding write enable not required)
40h	3Eh		F8h	+ xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition.
41h	3Fh	JEDEC Basic Flash Parameter Dword-16	A1h	+ 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing = xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_1110_0000b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. + 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 110000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-volatile Register and Write Enable Instruction for Status Register 1 = + xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1110000b Binary Fields: 10100001-1111100000-110000-1-1110000 Nibble Format: 1010_0001_1111_1000_0011_0000_1111_0000 Hex Format: A1_F8_30_F0

Data integrity

Table 71   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 1, basic flash parameter and 4-byte address instructions parameter (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
42h non-volatile	40h	JEDEC 4 Byte Address Instructions Parameter Dword-1	6Bh	Supported = 1, Not Supported = 0
43h	41h		8Eh	Bits 31:20 = RFU = FFFh
44h	42h		FFh	Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 1
45h	43h		FFh	Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 1 Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1 Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1 Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 1 Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0 Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0 Bit 12 = Support for Erase Command – Type 4 = 0 Bit 11 = Support for Erase Command – Type 3 = 1 Bit 10 = Support for Erase Command – Type 2 = 1 Bit 9 = Support for Erase Command – Type 1 = 1 Bit 8 = Support for (1-4-4) Page Program Command, Instruction=3Eh = 0 Bit 7 = Support for (1-1-4) Page Program Command, Instruction=34h = 0 Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1 Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction=ECh = 1 Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction=6Ch = 0 Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction=BCh = 1 Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction=3Ch = 0 Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 1 Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1
46h	44h	JEDEC 4 Byte Address Instructions Parameter Dword-2	21h	Bits 31:24 = FFh = Instruction for Erase Type 4: RFU Bits 23:16 = DCh = Instruction for Erase Type 3 Bits 15:8 = DCh = Instruction for Erase Type 2 Bits 7:0 = 21h = Instruction for Erase Type 1
47h	45h		DCh	
48h	46h		DCh	
49h	47h		FFh	

Sector map parameter table notes

The sector map parameter (see **Table 72**) provides a means to identify how the device address map is configured and provides a sector map for each supported configuration. This is done by defining a sequence of commands to read out the relevant configuration register bits that affect the selection of an address map. When more than one configuration bit must be read, all the bits are concatenated into an index value that is used to select the current address map.

To identify the sector map configuration in FS512S the following configuration bits are read in the following MSb to LSb order to form the configuration map index value:

• CR3NV[3] — 0 = Hybrid Architecture, 1 = Uniform Architecture

• CR1NV[2] — 0 = 4 KB parameter sectors at bottom, 1 = 4 KB sectors at top

The value of some configuration bits may make other configuration bit values not relevant (don't care), hence not all possible combinations of the index value define valid address maps. Only selected configuration bit combinations are supported by the SFDP Sector Map Parameter Table. Other combinations must not be used in configuring the sector address map when using this SFDP parameter table to determine the sector map. The following index value combinations are supported.

Table 72   **Sector map parameter**

Device	CR3NV[3]	CR1NV[2]	Index value	Description
FS512S	0	0	01h	4 KB sectors at bottom with remainder 256 KB sectors
	0	1	03h	4 KB sectors at top with remainder 256 KB sectors
	1	0	05h	Uniform 256 KB sectors

Table 73   **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 2, sector map parameter table, 512 Mb**

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
4Ah	48h	JEDEC Sector Map Parameter Dword-1 Config. Detect-1	FCh	Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for 20h_NV value
4Bh	49h		65h	
4Ch	4Ah		FFh	0 = Hybrid map with 4 KB parameter sectors
4Dh	4Bh		08h	1 = Uniform map Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = not the end descriptor = 0
4Eh	4Ch	JEDEC Sector Map Parameter Dword-2 Config. Detect-1	04h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_04h: address of CR3NV
4Fh	4Dh		00h	
50h	4Eh		00h	
51h	4Fh		00h	

Table 73 **CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 2, sector map parameter table, 512 Mb** (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
52h	50h	JEDEC Sector Map Parameter Dword-3 Config. Detect-2	FCh	Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TBPARM_O value
53h	51h		65h	
54h	52h		FFh	0 = 4 KB parameter sectors at bottom 1 = 4 KB parameter sectors at top
55h	53h		04h	Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = not the end descriptor = 0
56h	54h	JEDEC Sector Map Parameter Dword-4 Config. Detect-2	02h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_02h: address of CR1NV
57h	55h		00h	
58h	56h		00h	
59h	57h		00h	
5Ah	58h	JEDEC Sector Map Parameter Dword-5 Config. Detect-3	FDh	Bits 31:24 = Read data mask = 0000_0010b: Select bit 1 of the data byte for D8h_NV value
5Bh	59h		65h	
5Ch	5Ah		FFh	0 = 64 KB uniform sectors 1 = 256 KB uniform sectors
5Dh	5Bh		02h	Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = The end descriptor = 1
5Eh	5Ch	JEDEC Sector Map Parameter Dword-6 Config. Detect-3	04h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_04h: address of CR3NV
5Fh	5Dh		00h	
60h	5Eh		00h	
61h	5Fh		00h	
62h	60h	JEDEC Sector Map Parameter Dword-7 Config-1 Header	FEh	Bits 31:24 = RFU = FFh Bits 23:16 = Region count (Dwords -1) = 02h: Three regions Bits 15:8 = Configuration ID = 01h: 4 KB sectors at bottom with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = not the end descriptor = 0
63h	61h		01h	
64h	62h		02h	
65h	63h		FFh	

Table 73   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 2, sector map parameter table, 512 Mb (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
66h	64h	JEDEC Sector Map Parameter Dword-8 Config-1 Region-0	F1h	Bits 31:8 = Region size = 00007Fh: Region size as count – 1 of 256 Byte units = 8 x 4 KB sectors = 32 KB Count = 32 KB/256 = 128, value = count – 1 = 128 – 1 = 127 = 7Fh
67h	65h		7Fh	
68h	66h		00h	
69h	67h		00h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b --- Erase Type 3 is 256 KB erase and is supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 4 KB sector region Bit 0 = Erase Type 1 support = 1b --- Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
6Ah	68h	JEDEC Sector Map Parameter Dword-9 Config-1 Region-1	F4h	Bits 31:8 = Region size = 00037Fh: Region size as count – 1 of 256 Byte units = 1 x 224 KB sectors = 224 KB Count = 224 KB/256 = 896, value = count – 1 = 896 – 1 = 895 = 37Fh
6Bh	69h		7Fh	
6Ch	6Ah		03h	
6Dh	6Bh		00h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256 KB erase and is supported in the 32 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 32 KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 32 KB sector region
6Eh	6Ch	JEDEC Sector Map Parameter Dword-10 Config-1 Region-2	F4h	Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65280 KB Count = 65280 KB/256 = 261120, value = count – 1 = 261120 – 1 = 261119 = 3FBFFh
6Fh	6Dh		FFh	
70h	6Eh		FBh	
71h	6Fh		03h (512 Mb	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256 KB erase and is supported in the 64 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 64 KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 64 KB sector region

Table 73   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 2, sector map parameter table, 512 Mb (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
72h	70h	JEDEC Sector Map Parameter Dword-11 Config-3 Header	FEh	Bits 31:24 = RFU = FFh
73h	71h		03h	Bits 23:16 = Region count (Dwords – 1) = 02h: Three regions
74h	72h		02h	Bits 15:8 = Configuration ID = 03h: 4 KB sectors at top with remainder 256 KB sectors
75h	73h		FFh	Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = not the end descriptor = 0
76h	74h	JEDEC Sector Map Parameter Dword-12 Config-3 Region-0	F4h	Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65280 KB
77h	75h		FFh	
78h	76h		FBh	
79h	77h		03h (512 Mb	Count = 65280 KB/256 = 261120, value = count – 1 = 261120 – 1 = 261119 = 3FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256 KB erase and is supported in the 64 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 64 KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 64 KB sector region
7Ah	78h	JEDEC Sector Map Parameter Dword-13 Config-3 Region-1	F4h	Bits 31:8 = Region size = 00037Fh: Region size as count – 1 of 256 Byte units = 1 x 224 KB sectors = 224 KB
7Bh	79h		7Fh	
7Ch	7Ah		03h	Count = 224 KB/256 = 896, value = count – 1 = 896 – 1 = 895 = 37Fh
7Dh	7Bh		00h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256 KB erase and is supported in the 224 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 224 KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 224 KB sector region

Data integrity

Table 73   CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, Section 2, sector map parameter table, 512 Mb (Continued)

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
7Eh	7C		F1h	Bits 31:8 = Region size = 00007Fh: Region size as count – 1 of 256 Byte units = 8 x 4 KB sectors = 32 KB Count = 32 KB/256 = 128, value = count – 1 = 128 – 1 = 127 = 7Fh
7Fh	7D		7Fh	
80h	7E		00h	
81h	7F	JEDEC Sector Map Parameter Dword-14 Config-3 Region-2	00h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b --- Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 4 KB sector region Bit 0 = Erase Type 1 support = 1b --- Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region
82h	80h		FFh	Bits 31:24 = RFU = FFh Bits 23:16 = Region count (Dwords – 1) = 00h: One region Bits 15:8 = Configuration ID = 05h: Uniform 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = The end descriptor = 1
83h	81h	JEDEC Sector Map Parameter Dword-15 Config-4 Header	05h	
84h	82h		00h	
85h	83h		FFh	
86h	84h		F4h	Bits 31:8 = 512 Mb device Region size = 03FFFFh: Region size as count – 1 of 256 Byte units = 256 x 256 KB sectors = 65536 KB Count = 65536 KB/256 = 262144, value = count – 1 = 262144 – 1 = 262143 = 3FFFFh
87h	85h		FFh	
88h	86h		FFh	
89h	87h	JEDEC Sector Map Parameter Dword-16 Config-4 Region-0	03h	Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256 KB erase and is supported in the 256 KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64 KB erase and is not supported in the 256 KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region

13.5 Initial delivery state

The device is shipped from Infineon with non-volatile bits set as follows:

• The entire memory array is erased: i.e., all bits are set to '1' (each byte contains FFh).

• The OTP address space has the first 16 bytes programmed to a random number. All other bytes are erased to FFh.

• The SFDP address space contains the values as defined in the description of the SFDP address space.

• The ID-CFI address space contains the values as defined in the description of the ID-CFI address space.

• The Status Register 1 non-volatile contains 00h (all SR1NV bits are cleared to 0's).

• The Configuration Register 1 non-volatile contains 00h.

• The Configuration Register 2 non-volatile contains 08h.

• The Configuration Register 3 non-volatile contains 00h.

• The Configuration Register 4 non-volatile contains 10h.

• The Password Register contains FFFFFFFF–FFFFFFFFh.

• All PPB bits are '1'.

• The ASP Register bits are FFFFh.

14 Ordering information

14.1 Ordering part number

The ordering part number is formed by a valid combination of the following:

S79FS 512 S AG M F I 01 1

Packing type
0 = Tray
1 = Tube
3 = 13" Tape and reel

Model number (additional ordering options)
21 = 5 x 5 ball BGA footprint, 512 KB Physical Sector

Temperature range / grade
B = Automotive, AEC-Q100 grade 2 (-40°C to +105°C)

Package materials[72]
H = Halogen-free, Lead (Pb)-free

Package type
B = 24-ball BGA 6 x 8 mm package, 1.00 mm pitch

Speed
FA = 102 MHz DDR

Device technology
S = 65-nm MIRRORBIT™ Process Technology

Density
01G = 1 Gbit

Device family
S79FS
1.8 V-only, Dual-Quad Serial Peripheral Interface (SPI) Flash Memory

Note
72.Halogen free definition is in accordance with IE 61249-2-21 specification.

14.2 Valid combinations — automotive grade / AEC-Q100

Table 74 lists configurations that are automotive grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 74 **Valid combinations — automotive grade / AEC-Q100**

Base ordering part number	Speed option	Package and temperature	Model number	Packing type	Package marking
S79FS01GS	FA	BHB	21	0, 3	79FS01GSFBH21

Revision history

Document version	Date of release	Description of changes
**	2019-01-23	Initial release of full datasheet, created from 002-00488 specification. Replaces Supplemental Datasheet 002-19549.
*A	2019-05-30	Updated **Performance summary**: Updated **Typical current consumption**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz". Updated **DC characteristics**: Updated **Table 9**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz". Updated **Timing specifications**: Updated **DDR AC characteristics**: Updated **Table 15**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz". Updated **Address space maps**: Updated **Registers**: Updated **Configuration Register 2**: Updated **Configuration Register 2 Non-volatile (CR2NV)**: Updated Note 35 referred in **Table 27**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz". Updated **Commands**: Updated **Read Memory Array commands**: Updated **DDR Quad I/O Read (EDh, EEh)**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz". Updated **Ordering information**: Updated **Ordering part number**: Replaced "Quad DDR Read 80 MHz" with "Quad DDR Read 102 MHz".
*B	2019-11-25	Updated **Address space maps**: Updated **Registers**: Updated **Configuration Register 1**: Updated **Configuration Register 1 Volatile (CR1V)**: Updated **Table 25**. Updated **Commands**: Updated **Register Access commands**: Updated **Write Registers (WRR 01h)**: Updated description.
*C	2022-07-21	Updated **Features**: Updated description. Updated **Overview**: Removed "Glossary". Removed "Other resources". Updated **SPI with multiple input / output (SPI-MIO)**: Replaced "Hardware interface" with "SPI with multiple input / output (SPI-MIO)" in heading. Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 4**. Removed "Software interface". Updated **Package diagrams**: Replaced "Physical interface" with "Package diagrams" in heading. Updated **Data integrity**: Updated **Data retention**: Updated description. Updated **Ordering information**: Updated **Ordering part number**: Updated details under "Device family". Updated **Valid combinations — automotive grade / AEC-Q100**: Updated **Table 74**. Migrated to Infineon template.
*D	2023-04-22	Updated **Table 58**