SA111 • SA111A

Fully Integrated Half-Bridge Module

RoHS COMPLIANT

FEATURES

- 24 A continuous output current
  - •32 A for A-grade
- 1MHz switching frequency
- 650 V supply voltage
- Integrated gate drive with under-voltage lock-out and active Miller clamping
- Compact surface mount package (23.3 mm x 23.3 mm) with top-side heat sinking

APPLICATIONS

- DC/AC or DC/DC converters
- Motor Drive

DESCRIPTION

The SA111 • SA111A is a fully integrated half bridge module based on Silicon Carbide technology. The half bridge provides up to 32 A continuous output current with microcontroller or DSP control. Protection features include under-voltage lockout (UVLO) function and active Miller clamping.

Figure 1: Module Block Diagram

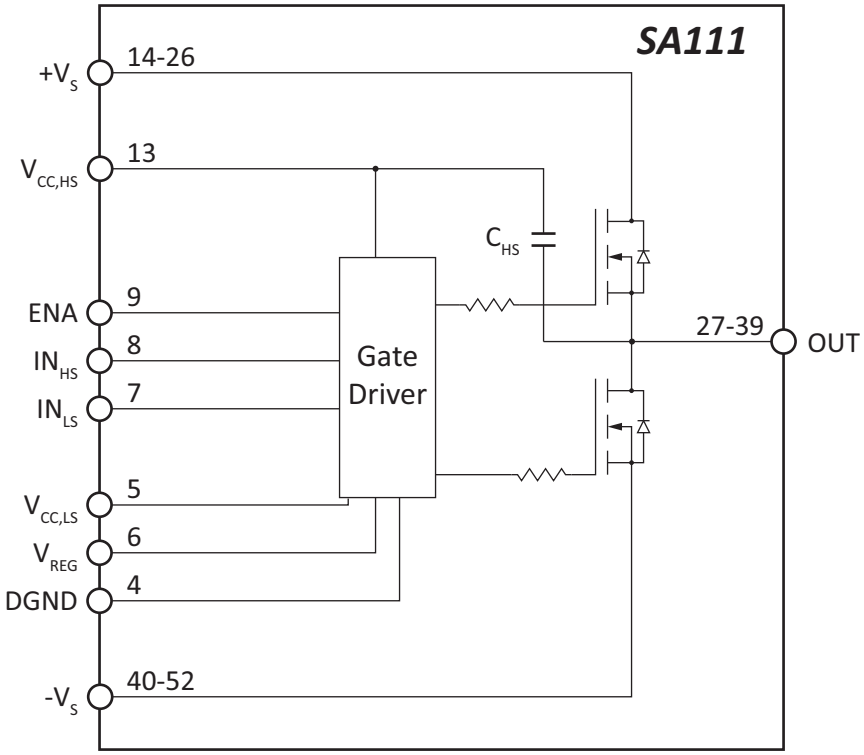
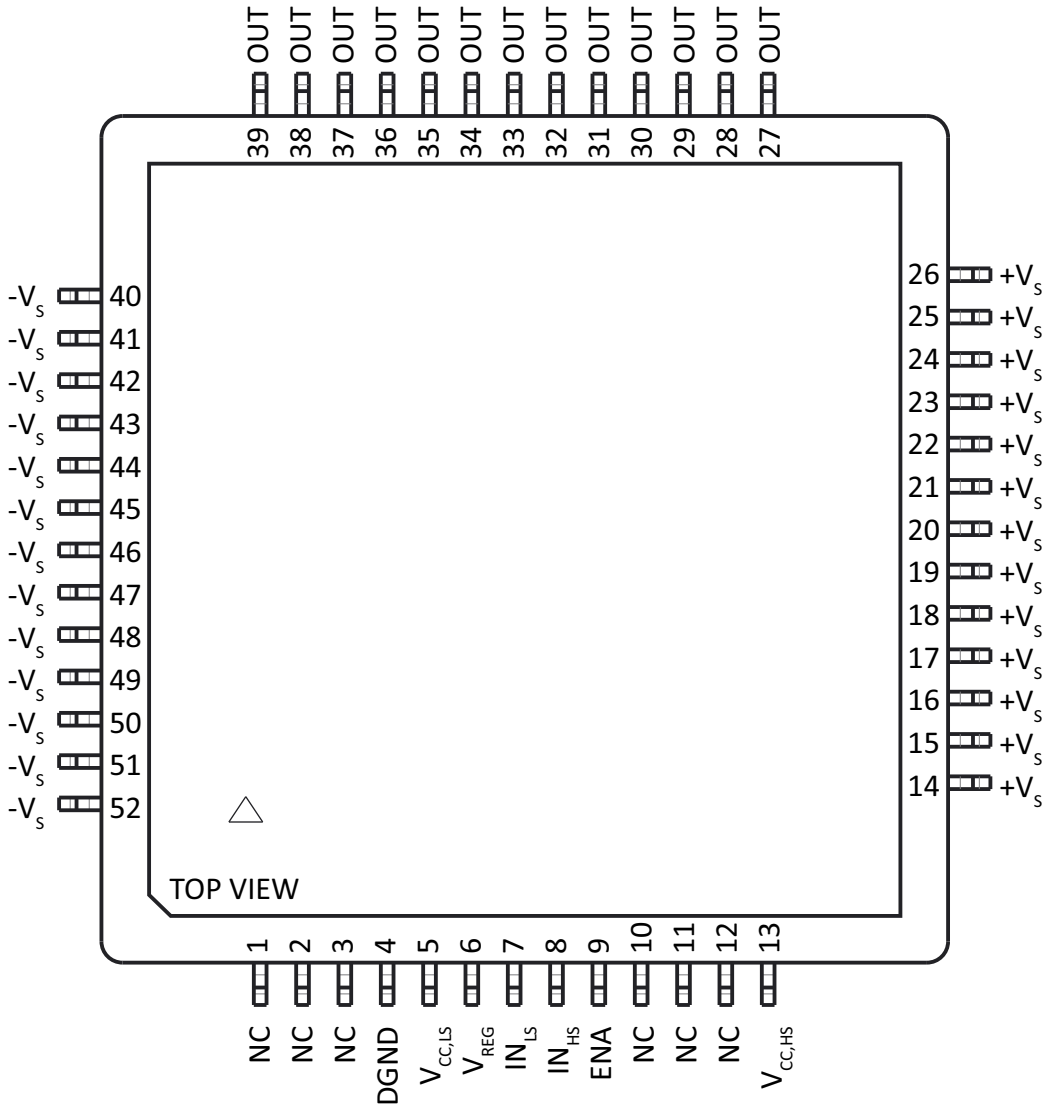


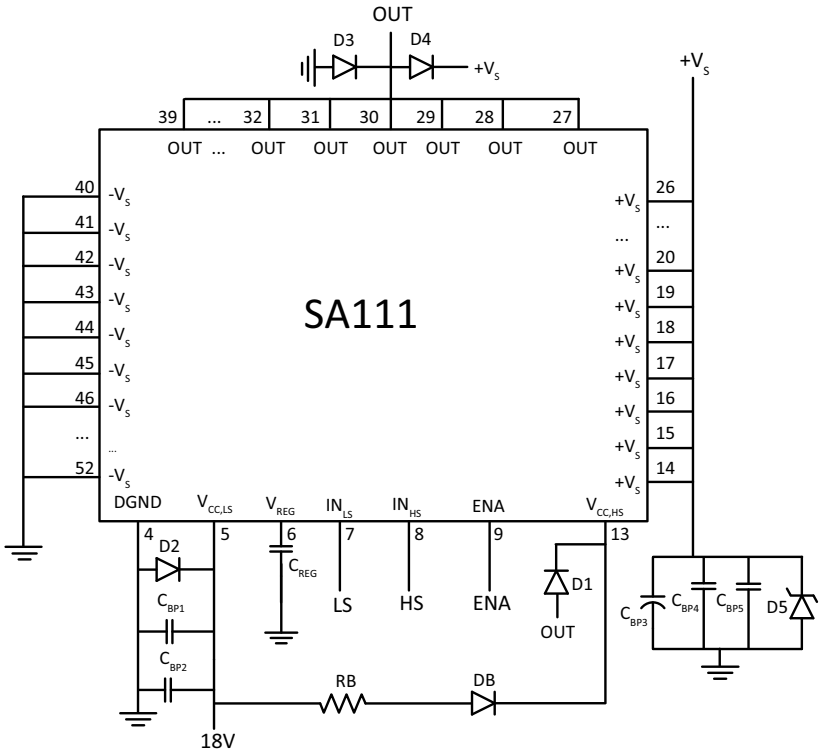
Figure 2: Device Pinout



PIN DESCRIPTION TABLE

Pin Number	Name	Description
1-3	NC	Not connected.
4	DGND	Input side ground pin. This pin needs to be connected externally to the negative supply rail or the power ground
5	$+V_{CC,LS}$	Low-side and input side power supply pin
6	V_{REG}	Internal power supply output pin. Pin must be connect to DGND with a 1 µF bypass capacitor.
7	IN_{LS}	Logic input for low-side SiC MOSFET control
8	IN_{HS}	Logic input for high-side SiC MOSFET control
9	ENA	Enable pin. A low level puts the high-side and low-side MOSFETs in high-impedance state. See logic table for details.
10-12	NC	Not connected.
13	$+V_{CC,HS}$	High-side gate drive power supply
14-26	$+V_S$	Positive supply rail
27-39	OUT	PWM output
40-52	$-V_S$	Negative supply rail or power ground.

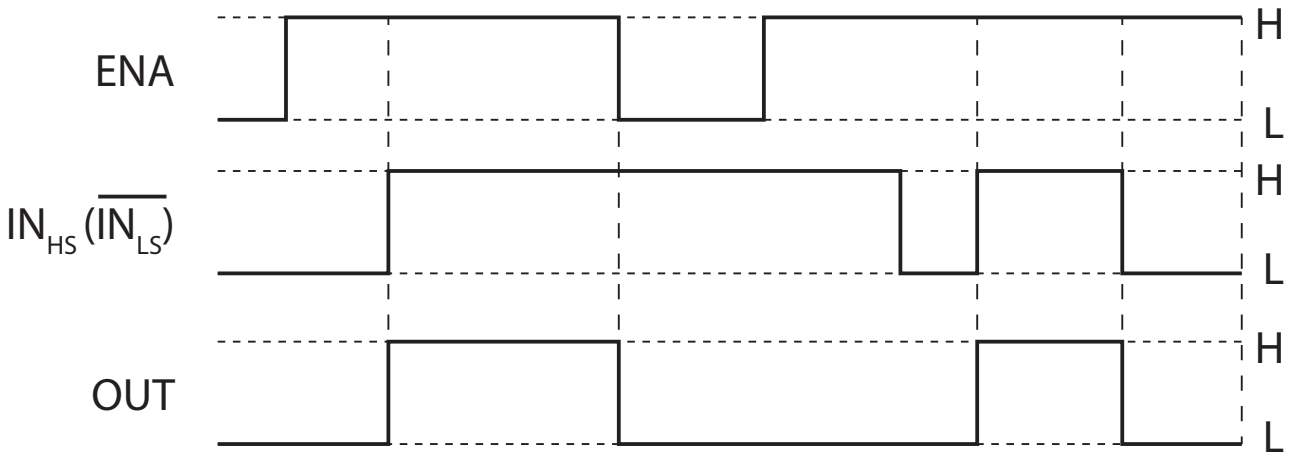
Figure 3: Typical Connection Diagram for Half Bridge Operation with Bootstrap



I/O CONDITION TABLE

ENA	IN_{HS}	IN_{LS}	OUT
L	X	X	High impedance
H	L	L	High impedance
H	H	L	$+V_S$
H	L	H	$-V_S$
H	H	H	High impedance

Figure 4: Input and Output Logic Timing Chart



DEVICE SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage, total	$+V_S$ to $-V_S$		650	V
Gate Driver Supply Voltage	$+V_{CC}$		22(rel.)	V
Output Current, continuous, SA111 • SA111A			24	A
Output Current, continuous, SA111 • SA111AA			32	A
Power Dissipation, internal, continuous, per MOSFET	P_D		56	W
Switching Frequency[1]			1000	kHz
Input Voltage, logic level		-0.3	$+V_{CC,LS}$	V
Temperature, pin solder, 10s max.			260	°C
Temperature, junction, MOSFET	T_J		175	°C
Temperature Range, storage		-55	+125	°C
Operating Temperature Range, case	T_C	-40	+125	°C

1. Within SOA. A high frequencies, the switching losses for hard switching might exceed the overall power dissipation of the device. Thus, soft switching is recommended for switching frequencies beyond 200 kHz

POWER SUPPLY (SINGLE RAIL SUPPLY)

Parameter	Test Conditions	Min	Typ	Max	Units
Low Side Supply Voltage, $+V_{CC,LS}$ [1]		12	18	20	V
Supply Voltage, $+V_S$				650	V
High Side Supply Voltage, $+V_{CC,HS}$ [2]		OUT+12	OUT+18	OUT+20	V
DGND			0		V

1. The maximum current might be limited at low temperatures around -25°C when operating the device at V_{CC}<14V.
2. The high-side supply should be realized either as a floating voltage supply relative to the device output or as a bootstrap circuit (resistor and diode in series between $+V_{CC,LS}$ and $+V_{CC,HS}$).

POWER SUPPLY (DUAL RAIL SUPPLY)

Parameter	Test Conditions	Min	Typ	Max	Units
Low Side Supply Voltage, $+V_{CC,LS}$ [1]		$-V_S$+12	$-V_S$+18	$-V_S$+20	V
Total Supply Voltage, $+V_S$-($-V_S$)				650	V
High Side Supply Voltage, $+V_{CC,HS}$ [2]		OUT+12	OUT+18	OUT+20	V
DGND			$-V_S$		V

1. The maximum current might be limited at low temperatures around -25°C when operating the device at V_{CC}<14V.
2. The high-side supply needs to be a floating supply relative to the device output (or a bootstrap circuit if suitable). The low-side supply voltage is relative to the negative supply rail.

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Logic High Level Input Voltage		DGND+2.0		$+V_{CC,LS}$	V
Logic Low Level Input Voltage		DGND		0.8	V
Logic Input Minimum Pulse Width [1]	IN_{HS}, IN_{LS}	60			ns
ENA Input Mask Time [1]	ENA	0.6	1.0	1.4	µs
Isolation			650	DGND + 0.8	V

1. Guaranteed by design.

OUTPUT

Parameter	Test Conditions	SA111 • SA111A			SA111 • SA111AA			Units
		Min	Typ	Max	Min	Typ	Max	
RDS(ON), per MOSFET[1]	I_D=27A, V_{CC}=18V, T_J=25°C		30			*		mΩ
RDS(ON), per MOSFET[1]	I_D=27A, V_{CC}=18V, T_J=125°C		39.6			*		mΩ
RDS(ON), (Including parasitics)	I_D=27A, V_{CC}=18V, T_J=25°C		36			*		mΩ
Rise Time, per MOSFET			45			*		ns
Fall Time, per MOSFET			30			*		ns
Switching Frequency[2 3]				1000			*	kHz
Current, continuous, source/sink		24			32			A
Current, peak, source/sink[3 4]				50			80	A
Current, continuous, body diode, per MOSFET[3]		24			32			A
Current, peak, body diode, per MOSFET[3 4]				50			80	A
Reverse Recovery Time, body diode, per MOSFET	V_S=300V, I_F=27A, di/dt=1100A/µs		26			*		ns

1. MOSFET only. Does not consider resistance due to layout/routing.
2. Carefully calculate the power dissipation of the device due to conduction and switching losses when operating SA111 • SA111A at higher switching frequencies and high output currents. It is recommended to use high switching frequencies only for soft switching (zero current switching) applications
3. Guaranteed by design.
4. Pulsed.

THERMAL SPECS

Parameter	Test Conditions	SA111 • SA111A			Units
		Min	Typ	Max	
Resistance, Junction to case	F < 60Hz			2.7	°C/W
Resistance, Junction to case	F ≥ 60Hz				°C/W
Resistance, Junction to air					°C/W
Temperature Range, Case		-40		125	°C

Figure 5: Power Derating

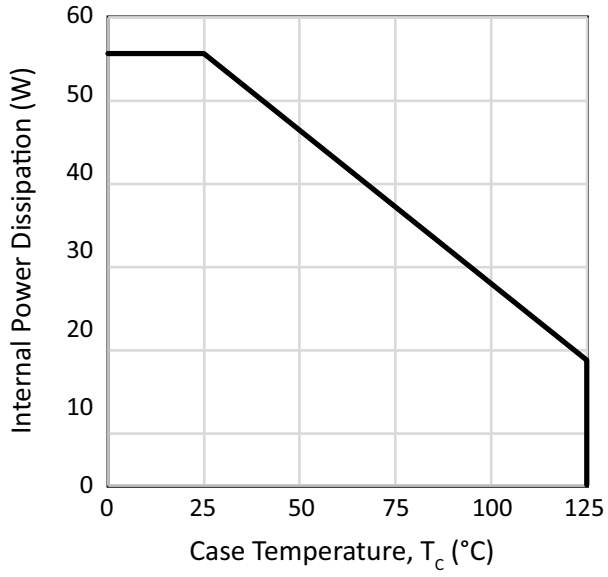


Figure 6: Output Current vs. Temperature

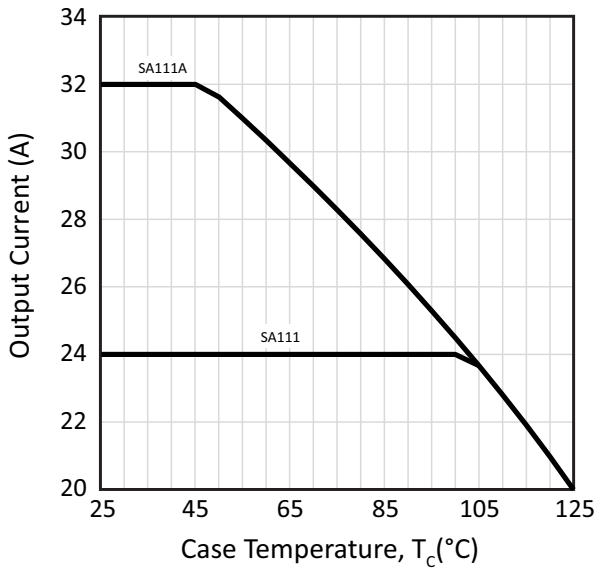


Figure 7: Flyback Current vs. Reverse Voltage

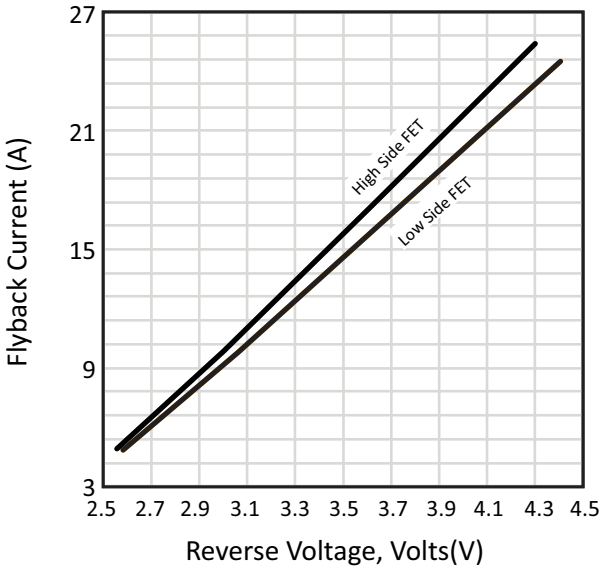


Figure 8: $R_{DS(ON)}$ vs. Temperature

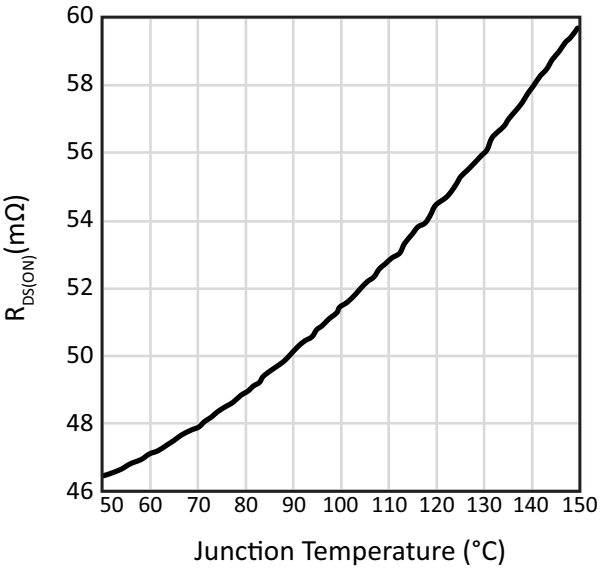


Figure 9: Output Voltage vs. Output Current (Low Side FET)

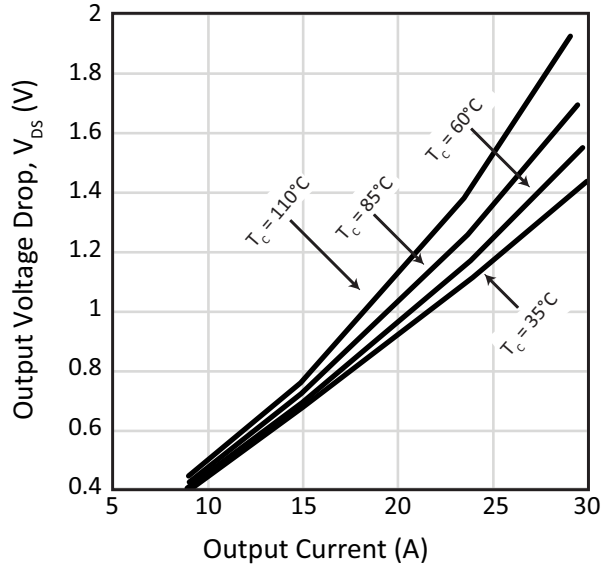


Figure 10: Output Voltage Drop vs. Output Current (High Side FET)

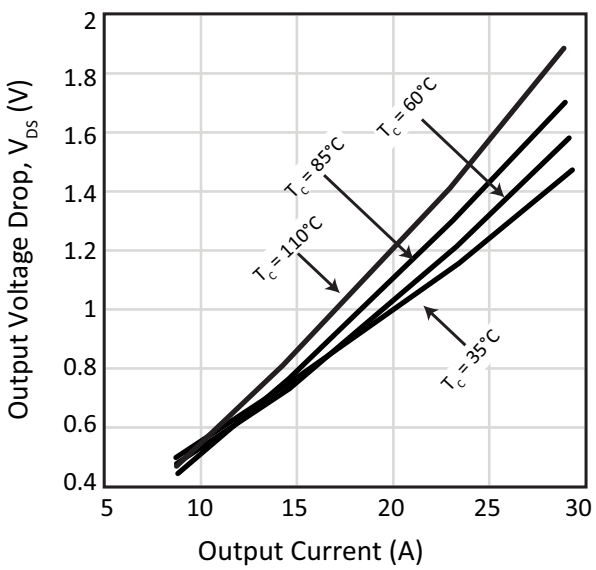


Figure 11: Switching Energy vs. Supply Voltage

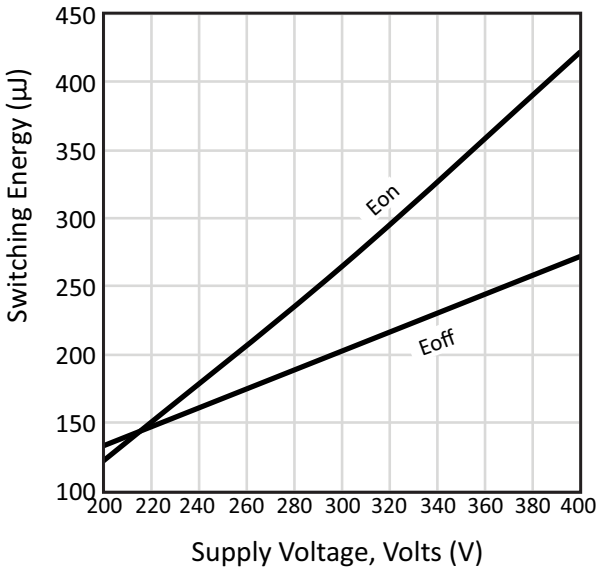
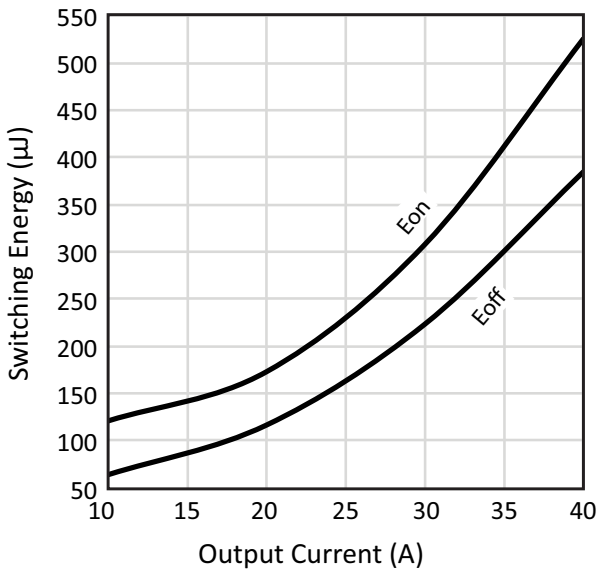


Figure 12: Switching Energy vs. Current



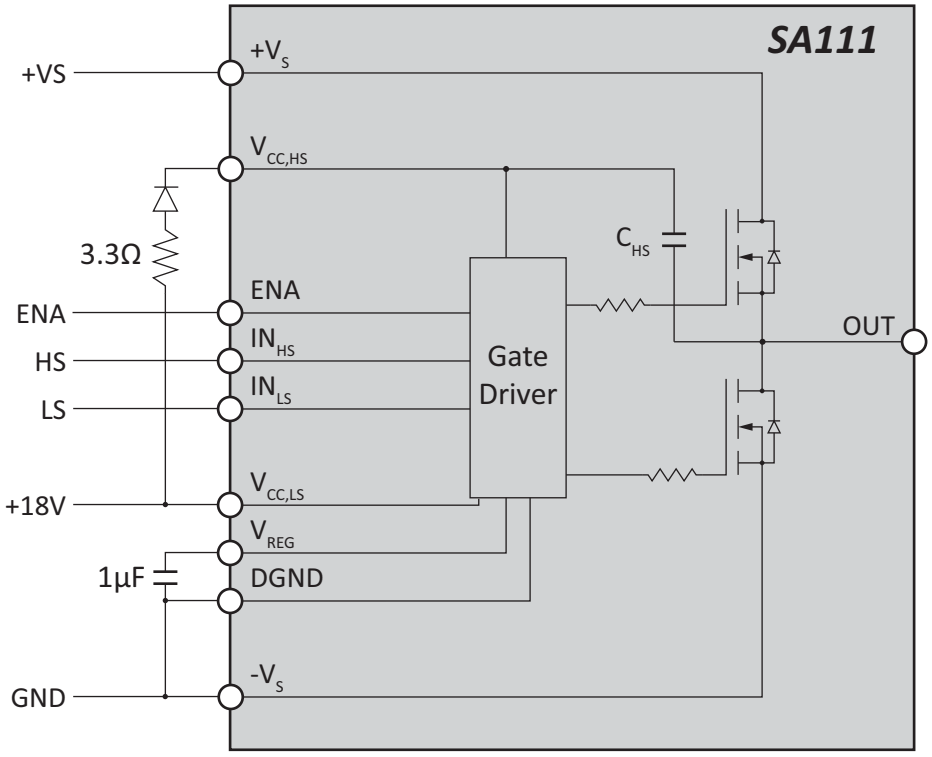
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

BOOTSTRAP CIRCUIT

When operating the device with Single Supply Rail, at the high-side supply voltage ($V_{CC,HS}$) can be realized through a bootstrap circuit if operating the device at 100% duty cycle is not required. Figure 13 illustrates the components required for the bootstrap circuit. The high-side supply voltage is connected to the low-side supply voltage through a resistor and a diode that are put in series.

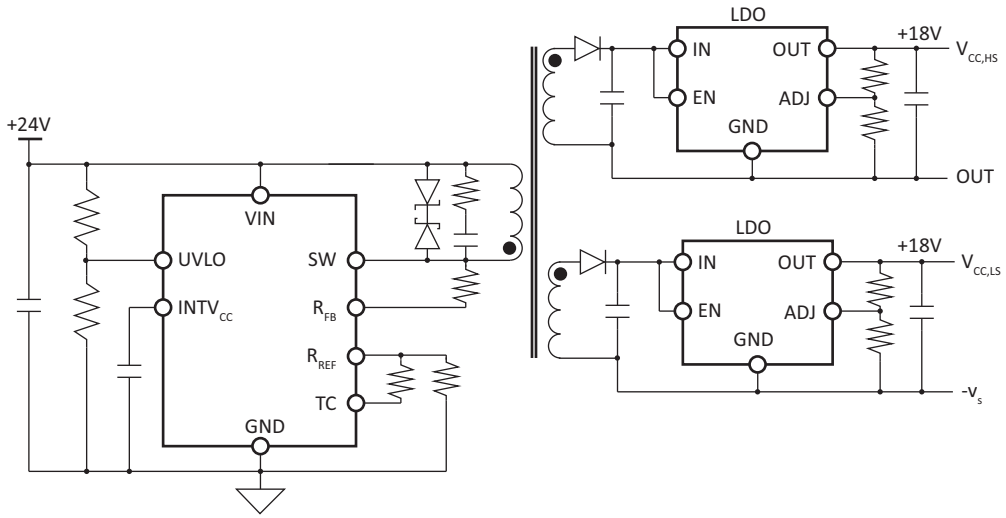
Figure 13: Bootstrap Circuit for Single Supply Rail Operation



POWER SUPPLY FOR DUAL RAIL MODE

In dual rail mode, the low-side gate driver is operating relative to the negative supply rail, which is not ground, but $-V_S$. Dual rail mode is typically used when you switch only one side (high side or low side) during each half period of an output sine wave, so a bootstrap circuit for the high-side is also not suitable. Figure 14 shows a simplified power supply for such condition. It is a fly-back converter circuit with two windings on the secondary side of the transformer.

Figure 14: Power Supply for Dual Rail Mode (Simplified)

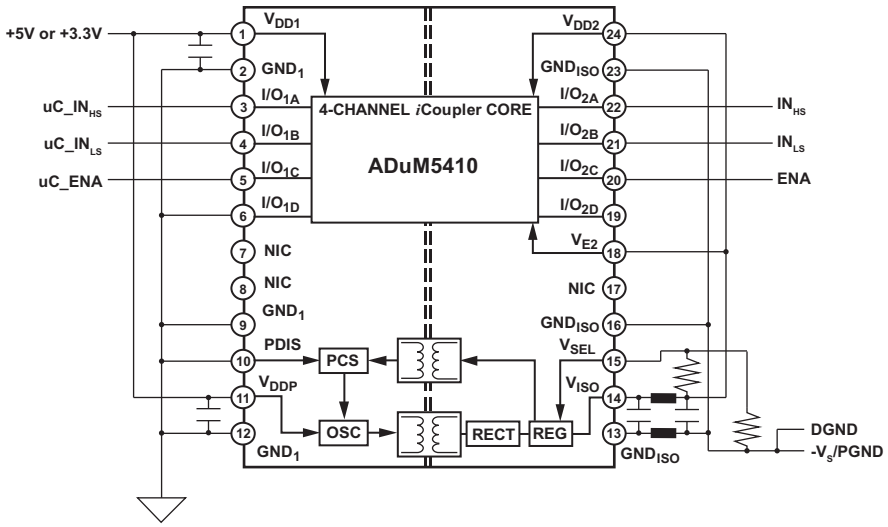


INPUT SIGNAL ISOLATION

When using dual rail mode, the input signals (which are referenced to the system ground) need to be level shifted relative to the $-V_S$ supply. The isoPower devices from Analog Devices are well suited to do that level shifting.

The same circuit also can be used when full isolation of the input signals to the SA111 • SA111A is desired.

Figure 15: Input Signal Isolation (Example using ADuM5410)



UNDER-VOLTAGE LOCKOUT FUNCTION

The SA111 • SA111A has a built-in under-voltage lockout function. When the $V_{CC,HS}$ or $V_{CC,LS}$ drops below approximately 9V, the output pin will be high impedance. When the supply voltages rise above approximately 10V, the output will return back to normal operating mode. In addition, to prevent malfunctions due to noise, a mask time of approximately 2.5µs is set on both high side supply voltages.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The V_S supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of a least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The 1µF ceramic capacitor must be physically connected directly to the +/-V_S and POWER GND pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the V_{CC} supply are less stringent, but still necessary. A 0.1µF to 0.47µF ceramic capacitor connected directly to the $V_{CC,LS}$ and $V_{CC,HS}$ pins will suffice.

POWER SUPPLY PROTECTION

Unidirectional transient Voltage suppressors are recommended as protection on the supply pins as shown in Figure 3. TVS diodes clamp transients to voltages within the power supply rating and clamp power supply reversals to ground. Whether the TVS diodes are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Unidirectional TVS diodes prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

OUTPUT PROTECTION

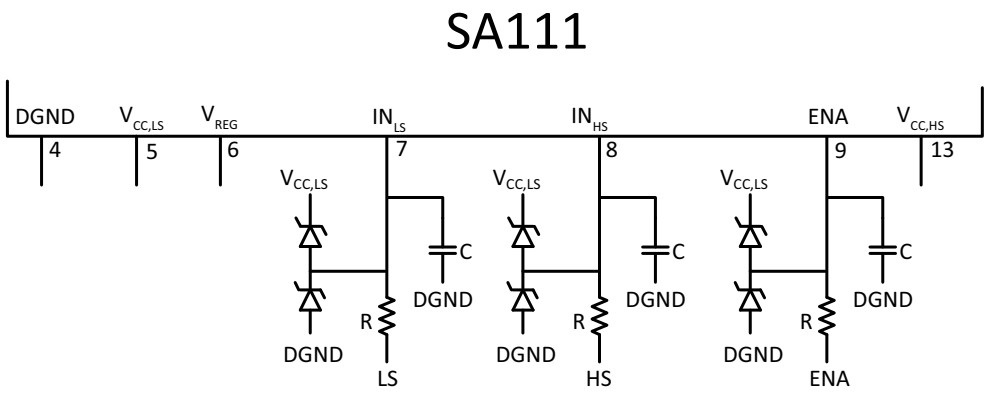
Two external diodes as shown in Figure 3, are required to protect these amplifiers from flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

INPUT PROTECTION

It is recommended to connect two Schottky diodes at the ENA, IN_{HS}, IN_{LS} pins to provide external protection for the SA111 • SA111A, as shown in Figure 16. A 100pF capacitor (capacitor C) can be connected to ground to provide ESD protection from coaxial cables and other ESD sources. A series resistor (approximately 200Ω) may be added in series with the input pins to limit excessive current going into pins.

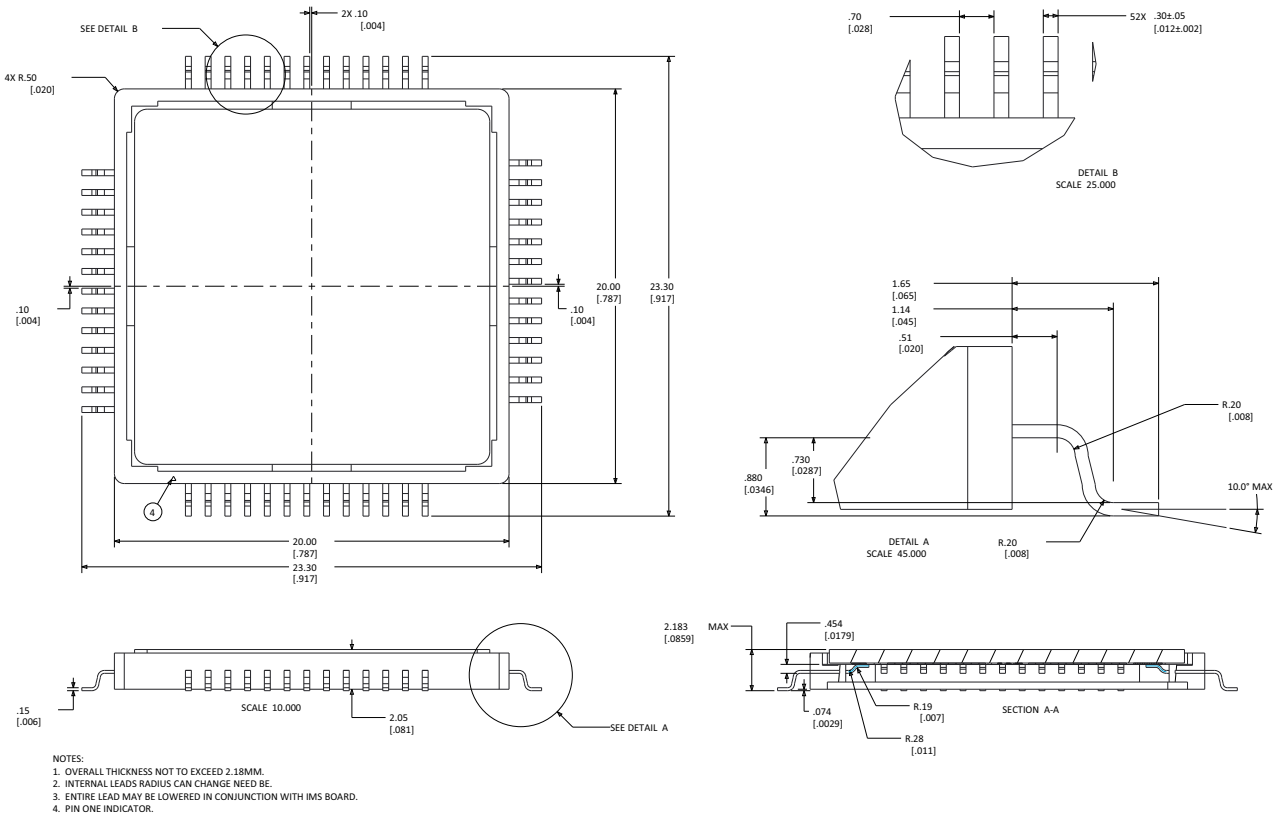
Figure 16: Input Protection



PACKAGE AND DEVICE OPTIONS

Part Number	Apex Package Style	Description	MSL[1]
SA111	PR	52-pin Surface-Mount Package, QFP Style	Level 6
SA111A	PR	52-pin Surface-Mount Package, QFP Style	Level 6

1. The Moisture Sensitivity Level rating according to the JEDEC industry standard classification.



NOTES:
1. OVERALL THICKNESS NOT TO EXCEED 2.18MM.
2. INTERNAL LEADS RADIUS CAN CHANGE NEED BE.
3. ENTIRE LEAD MAY BE LOWERED IN CONJUNCTION WITH IMS BOARD.
4. PIN ONE INDICATOR.