H-Bridge Motor Driver/Amplifiers

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/ HIGHSIDE DRIVE CIRCUITRY
- WIDE SUPPLY RANGE: UP TO 80V
- 10A CONTINUOUS OUTPUT
- ISOLATED CASE ALLOWS DIRECT HEATSINKING
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL/PROGRAMMABLE PWM FREQUENCY GENERATION

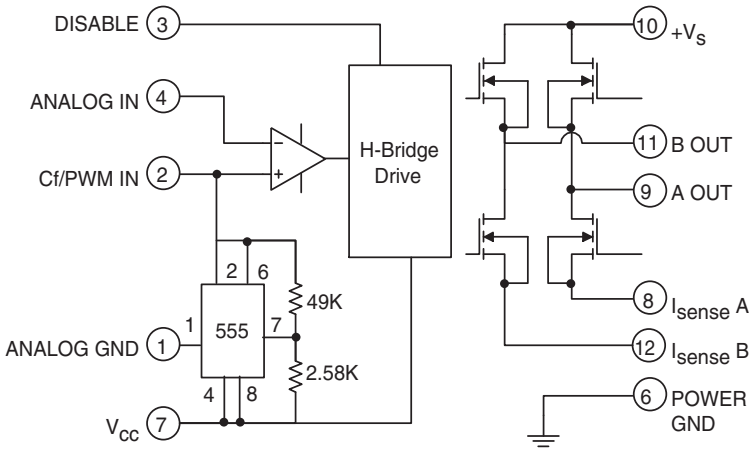
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

DESCRIPTION

The SA60 is a pulse width modulation amplifier that can supply 10A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed/direction, or audio signal for switchmode audio amplification. The internal PWM frequency can be programmed by an external integrator capacitor. Alternatively, the user may provide an external TTL-compatible PWM signal for simultaneous amplitude and direction control for four quadrant mode.

BLOCK DIAGRAM



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ (Note 4)			80	V
OUTPUT CURRENT, peak			15	A
LOGIC SUPPLY VOLTAGE, V_{CC}			16	V
POWER DISSIPATION, internal (Note 3)			156	W
TEMPERATURE, pin solder, 10s max.			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		−55	125	°C
OPERATING TEMPERATURE RANGE, case		−40	85	°C

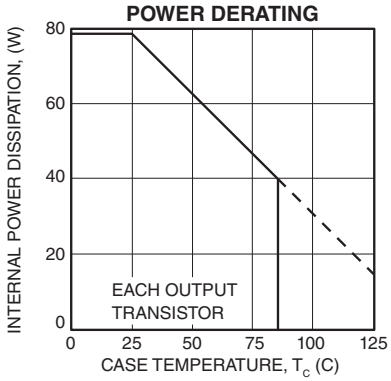
CAUTION The SA60 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

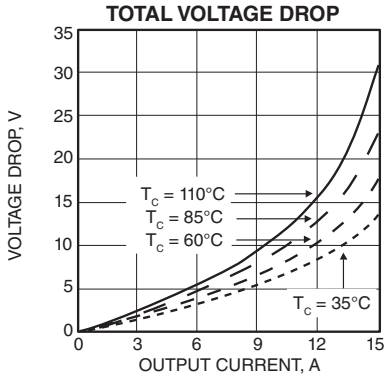
SPECIFICATIONS

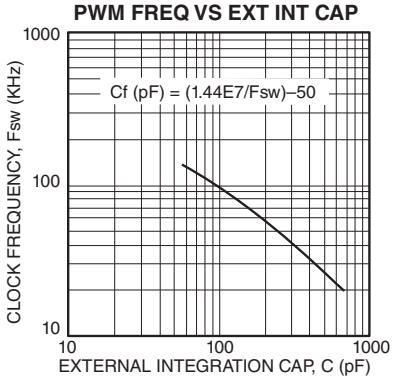
Parameter	Test Conditions[1]	Min	Typ	Max	Units
INPUT					
ANALOG INPUT VOLTAGES	V_{CC} = 12V				
A,B OUT = 50% Duty Cycle			1/2 V_{CC}		VDC
A OUT = 100% Duty Cycle High			1/3 V_{CC}		VDC
B OUT = 100% Duty Cycle High			2/3 V_{CC}		VDC
PWM INPUT					
PWM PULSE LOW VOLTAGE		0		0.8	VDC
PWM PULSE HIGH VOLTAGE		2.7		5.0	VDC
PWM FREQUENCY			45	250	KHz
DISABLE ON		2.7		V_{CC}	VDC
DISABLE OFF		0		0.8	VDC
OUTPUT					
V_{DS} (ON) VOLTAGE, each MOSFET	I_{DS} = 10A		1.7	2.5	VDC
TOTAL R_{ON}, both MOSFETs				0.45	Ω
EFFICIENCY, 10A OUTPUT	$+V_S$ = 80A		91		%
CURRENT, continuous		10			A
CURRENT, peak	t = 100 msec	15			A
SWITCHING FREQUENCY	C_F = 270pF		45		KHz
DEAD TIME			90		nS
POWER SUPPLY					
$+V_S$ VOLTAGE (Note 4)	$+V_S$ Current = Load Current			80	VDC
V_{CC} VOLTAGE		9.5	12	15	VDC
V_{CC} CURRENT	V_{CC} = 12VDC		28	36	mA
$+V_S$ CURRENT	Switching Freq. = 45kHz, no load, V_S = 50V		45		mA

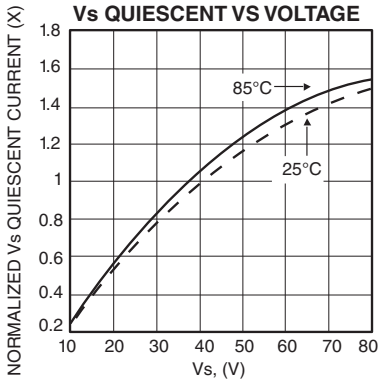
Parameter	Test Conditions[1]	Min	Typ	Max	Units
THERMAL (Note 3)					
RESISTANCE, junction to case	Full temperature range, for each transistor			1.6	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		-25		+85	°C

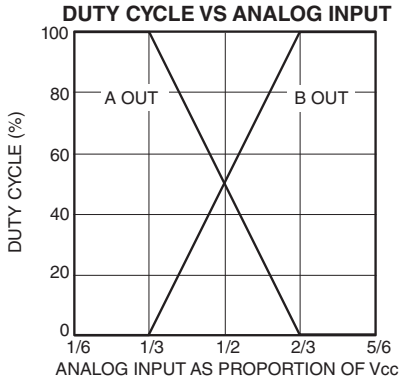
NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C, V_{CC} = 12VDC).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Each of the two active output transistors can dissipate 78W.
4. Derate to 70V below T_C = +25°C.

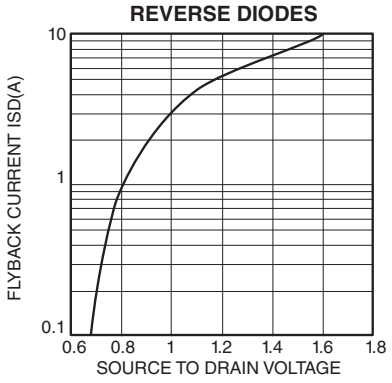


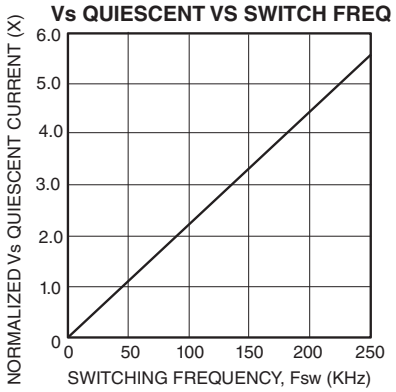


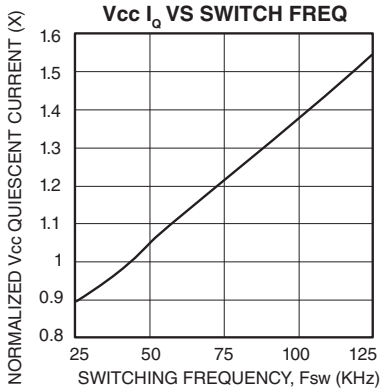


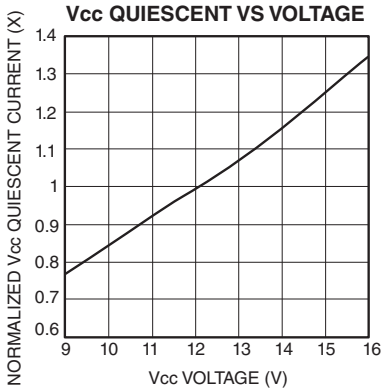




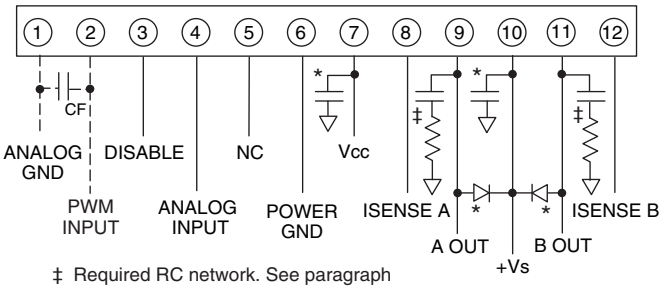








EXTERNAL CONNECTIONS



‡ Required RC network. See paragraph on transient shutdown.

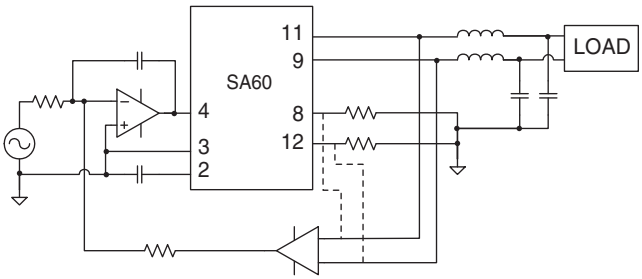
* Protection diodes are recommended for applications where +Vs exceeds 50V.

12-pin Power SIP
PACKAGE
STYLE DP

Formed Leads Available
See package style EE

TYPICAL APPLICATION

A wide variety of loads can be driven in either the voltage mode or the current mode. The most common applications use three external blocks: a low pass filter converting pulse width data to an analog output, a difference amplifier to monitor voltage or current and an error amplifier. Filter inductors must be suitable for square waves at the switching frequency (laminated steel is generally not acceptable). Filter capacitors must be low ESR and rated for the expected ripple current. A difference amplifier with gain of less than one translates the differential output voltage to a single feedback voltage. Dashed line connections and a higher gain difference amplifier would be used for current control. The error amplifier integrates the difference between the input and feedback voltages to close the loop.



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexanalog.com for design tools that help automate pwm filter design; heat sink selection; Apex Microtechnology's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

PWM OSCILLATOR – INTERNAL OR EXTERNAL

The SA60 contains an internal PWM oscillator whose frequency is determined by an external capacitor connected between pin 1 and pin 2. Maximum frequency is 125 kHz. The user may also disregard the internal PWM oscillator and supply the SA60 with an external TTL pulse generator up to 250KHZ.

PIN DESCRIPTION

V_{cc} - is the low voltage supply for poweri ng internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_s - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts.

ISENSE A & B - These are tied to power gnd directly or through sense resistors.

ANALOG GND - is the reference for the internal PWM oscillator. Connect this pin to pin 6. Connect low side of Vcc supply and any other supply used to generate analog input signals to ANALOG GND.

ANALOG INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than Vcc/2 will produce greater than 50% duty cycle pulses out of B OUT. A voltage lower than Vcc/2 will produce greater than 50% duty cycle pulses out of A OUT. If using in the digital mode, bias this point at 1/2 the logic high level.

DISABLE - Is the connection for disabling all 4 output switches. DISABLE high overrides all other inputs. When taken low, everything functions normally. An internal pullup to Vcc will keep DISABLE high if pin left open.

PWM INPUT - Is the TTL compatible digital input for controlling the PWM pulse width of the bridge. A duty cycle greater than 50% will produce greater than 50% duty cycle pulses out of the A out. A duty cycle less than 50% will produce greater than 50% duty cycle from the B out. For analog inputs, the integration capacitor for the internal clock must be connected between this pin and analog ground. The internal switching frequency is programmable up to 125 kHz by selection of the integration capacitor. The formula is:

$$C_F\,(pF) = \left(\frac{1.44 \times 10^7}{Fsw}\right) - 50$$

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The 1µF ceramic capacitor must be physically connected directly to the Vs and POWER GND pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc and ANALOG GND pins will suffice.

PCB LAYOUT

The designer needs to appreciate that the SA60 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA60:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Connect ANALOG GND to POWER GND with a conductor having no intermediate connections. Connect all Vs power supply, filter and load related ground connections to POWER GND keeping these conductors separate until reaching pin 6. Connect all Vcc power supply and input signal related ground connections to ANALOG GND keeping conductors separate until reaching pin 1. Do not allow ground loops to form by making additional ground connections at the low side of the physical power supplies. If ground plane is used do not allow more than 1mA to flow through it.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 8-12).

CURRENT SENSE

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted to POWER GND in the voltage mode connection but both must be used in the current mode connection. It is recommended that R SENSE resistors be non-inductive. Load current flows in the I SENSE pins. The SA60 has no internal current limit.

TRANSIENT SUPPRESSION

An RC network of a 100 pF Capacitor and a one ohm resistor is required as shown in the external connection diagram on page 1. This network assures proper operation under various loads. Minimal power is dissipated in the resistor.